



LC75421M

Electronic Volume Controller for Cars



Overview

The LC75421M is an electronic volume controller that enables control of volume, balance, fader, bass/treble + super bass, input switching, and input and output level control functions using only a small number of external components.

Functions

- Volume: 0 dB to -79 dB in 1-dB steps, and $-\infty$ (81 positions)
Balance function with separate L/R control
- Fader: rear output or front output can be attenuated across 16 positions (in 2-dB steps from 0 dB to -20 dB, 5-dB steps from -20 dB to -25 dB, 10-dB steps from -25 dB to -45 dB, and -60 dB, $-\infty$)
- Bass/treble: A tone control circuit can be configured using an external RC, with 15-position control from 0 dB to ± 11.9 dB in 1.7-dB steps possible for both bass and treble
- Input gain: 0 dB to +18.75 dB (1.25-dB steps)
amplification is possible for the input signal.
- Output gain: Fader output can be selected among 0 dB, +6.5 dB, and +8.5 dB.
- Input switching: Five input signals can be selected for Left and for Right
- Super bass: Step control with 11 positions is possible, with peaking characteristics (type T)

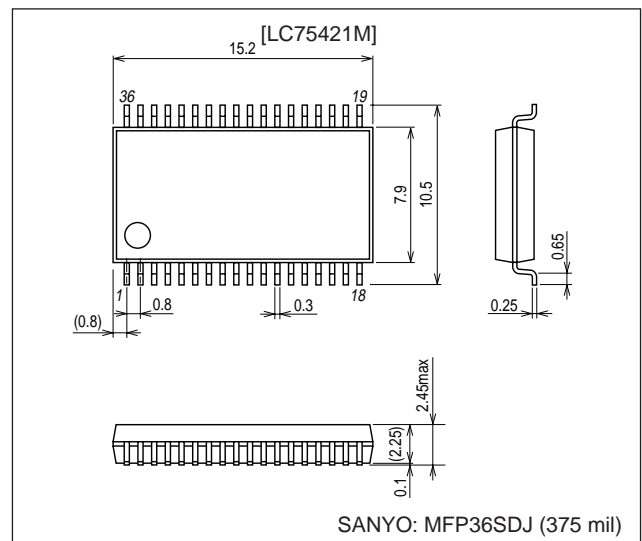
Features

- On-chip buffer amplifier cuts down number of external components
- Low switching noise generated by on-chip switch due to use of silicon gate CMOS process
- On-chip reference voltage circuit for analog ground
- Controls performed with serial input (CCB)

Package Dimensions

unit: mm

3263-MFP36SDJ (375 mil)



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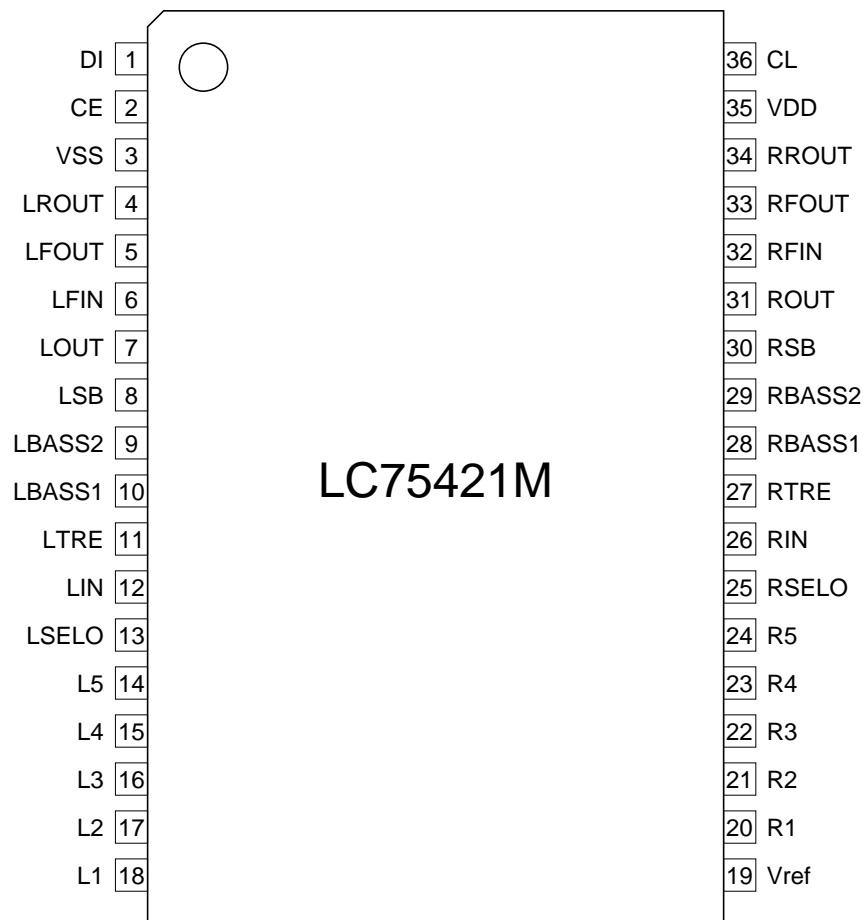
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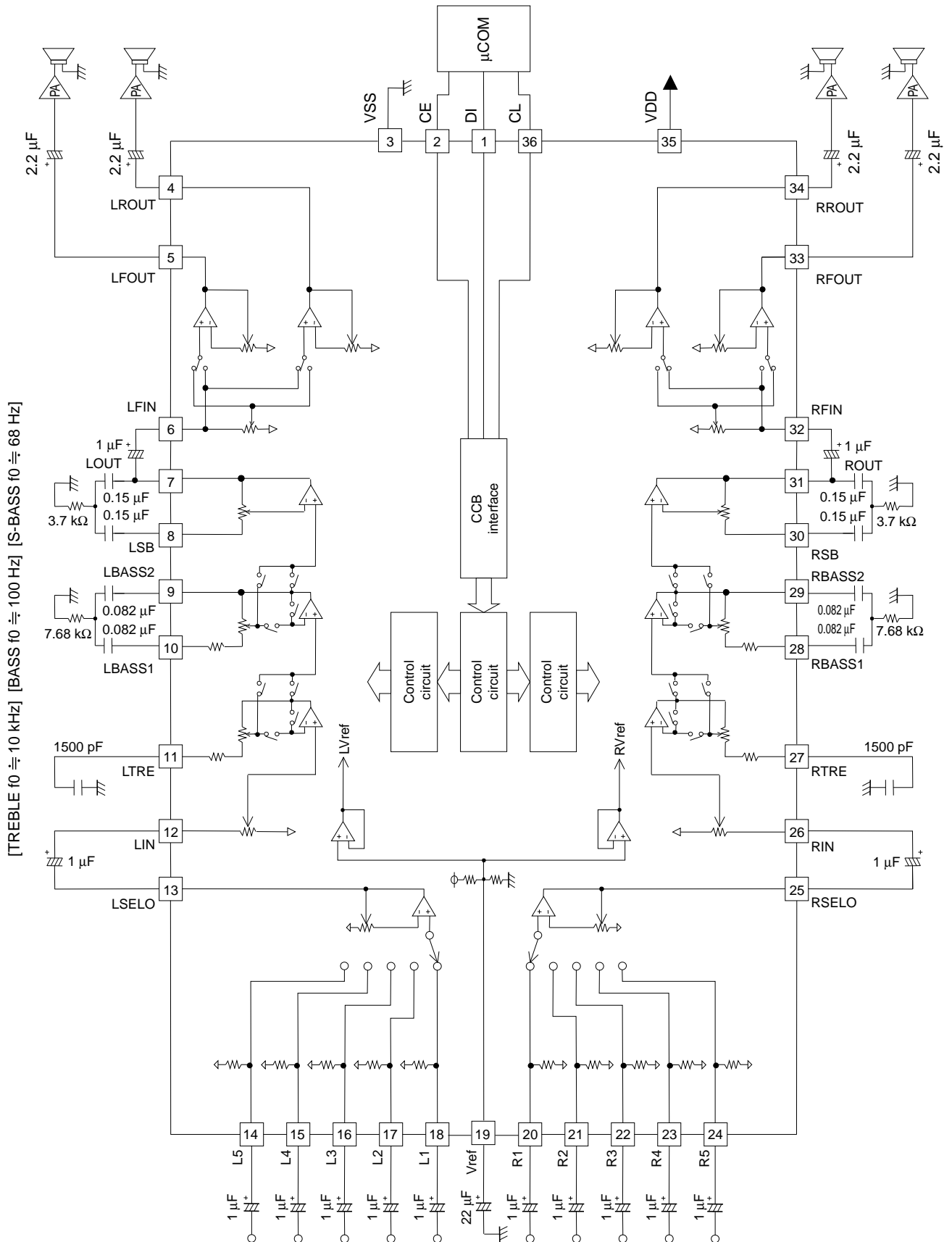
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Pin Assignment



Top view

Equivalent Circuit Block Diagram



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Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\text{ max}}$	V_{DD}	11	V
Maximum input voltage	$V_{IN\text{ max}}$	CE, DI, CL	-0.3 to 11	V
		Input pins other than CE, DI, CL	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	
Allowable power dissipation	P_{dmax}	$T_a \leq 85^\circ\text{C}$, when mounted on board	550	mW
Operating temperature	T_{opr}		-40 to +85	$^\circ\text{C}$
Storage temperature	T_{stg}		-50 to +125	$^\circ\text{C}$

Allowable Operating Ranges at $T_a = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Pin Name	Conditions	Ratings			Unit
				min	typ	max	
Supply voltage	V_{DD}	V_{DD}		7.5		10	V
Input high-level voltage	V_{IH}	CL, DI, CE		4.0		10	V
Input low-level voltage	V_{IL}	CL, DI, CE		V_{SS}		1.0	V
Input amplitude voltage	V_{IN}	CL, DI, CE, LIN, RIN, L1 to L5, R1 to R5, LFIN, RFIN		V_{SS}		V_{DD}	Vp-p
Input pulse width	$t_{\phi W}$	CL		1			μs
Setup time	t_{setup}	CL, DI, CE		1			μs
Hold time	t_{hold}	CL, DI, CE		1			μs
Operating frequency	f_{opg}	CL				500	kHz

Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{DD} = 8\text{ V}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Pin Name	Conditions	Ratings			Unit
				min	typ	max	
Maximum input gain	G_{inmax}				+18.75		dB
Step resolution	G_{step}				+1.25		dB
Input resistance	R_{in}	L1, L2, L3, L4, L5 R1, R2, R3, R4, R5			50		k Ω
Clipping level	V_{cl}	LSELO, RSELO	THD = 1.0%, $f = 1\text{ kHz}$		2.90		V _{rms}
Output load resistance	R_L	LSELO, RSELO		10			k Ω

Volume Block

Parameter	Symbol	Pin Name	Conditions	Ratings			Unit
				min	typ	max	
Input resistance	R_{in}	LIN, RIN			50		k Ω

Fader Volume Block

Parameter	Symbol	Pin Name	Conditions	Ratings			Unit
				min	typ	max	
Step resolution	AT_{step}		STEP = 0 dB to -20 dB		2		dB
			STEP = -20 dB to -25 dB		5		
			STEP = -25 dB to -45 dB		10		
Step error	AT_{err}		STEP = 0 dB to -45 dB	-2	0	+2	dB
			STEP = -45 dB to -60 dB	-3	0	+3	
Output load resistance	R_L			10			k Ω
Output impedance	R_O	LFOUT, LROUT RFOUT, RROUT	$R_L = 10\text{ k}\Omega$, $f = 1\text{ kHz}$ $V_{IN} = 1\text{ V}_{rms}$		46		Ω

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Bass Band Control Block

Parameter	Symbol	Pin Name	Conditions	Ratings			Unit
				min	typ	max	
Control range	Gbass		MAX. Boost/Cut	±10	±11.9	±14	dB
Step resolution	Estep			1	1.7	3	dB
Internal feedback resistance	Rfeed				45.084		kΩ

Treble Band Control Block

Parameter	Symbol	Pin Name	Conditions	Ratings			Unit
				min	typ	max	
Control range	Gtre		MAX. Boost/Cut	±10	±11.9	±14	dB
Step resolution	Estep			1	1.7	3	dB
Internal feedback resistance	Rfeed				56.084		kΩ

Super Bass Block (Type T)

Parameter	Symbol	Pin Name	Conditions	Ratings			Unit
				min	typ	max	
Control range	Crange		MAX. Boost		+20		dB
Step resolution	Estep				+2.0		dB
Internal feedback resistance	Rfeed				66.6		kΩ

General

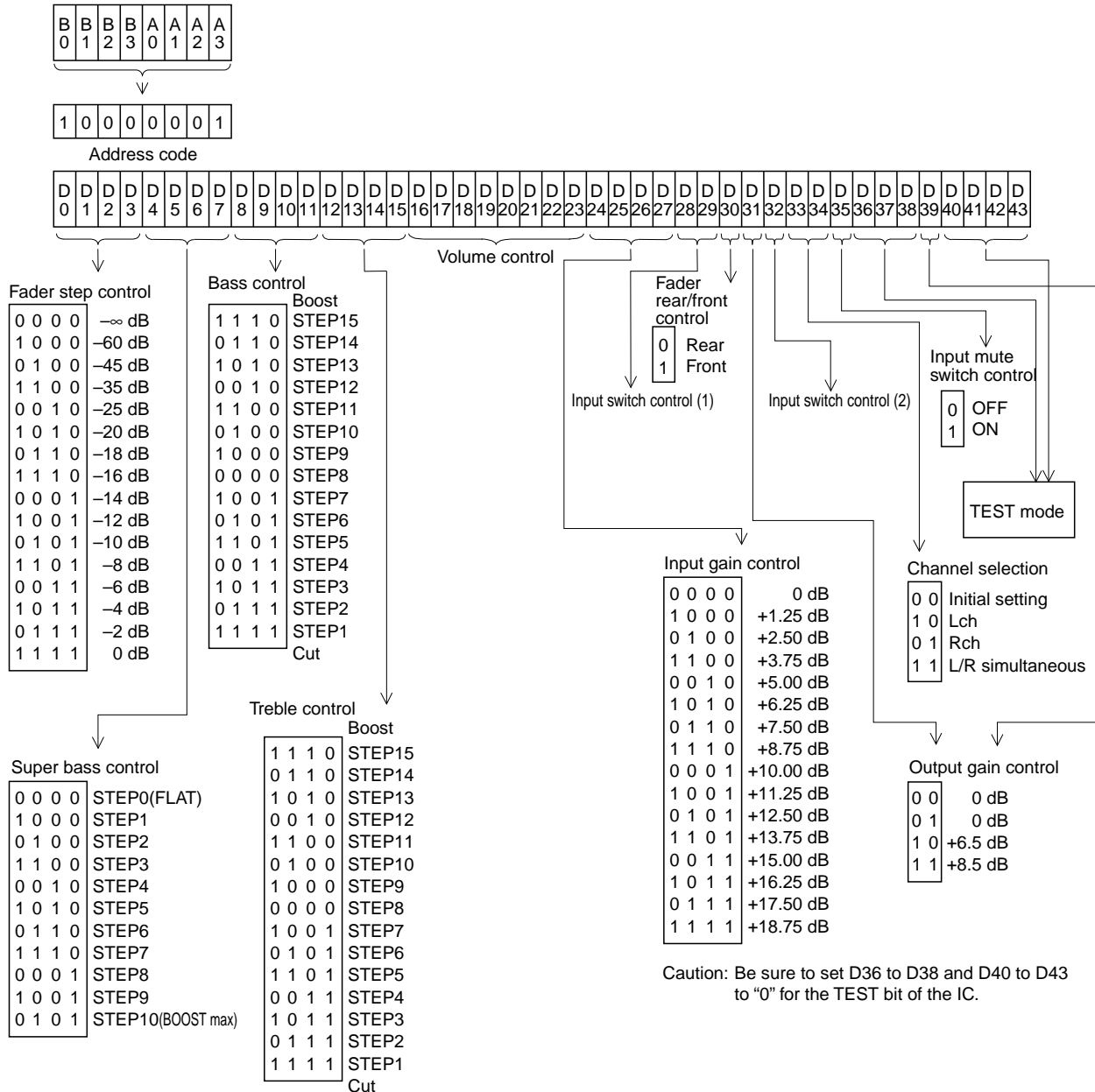
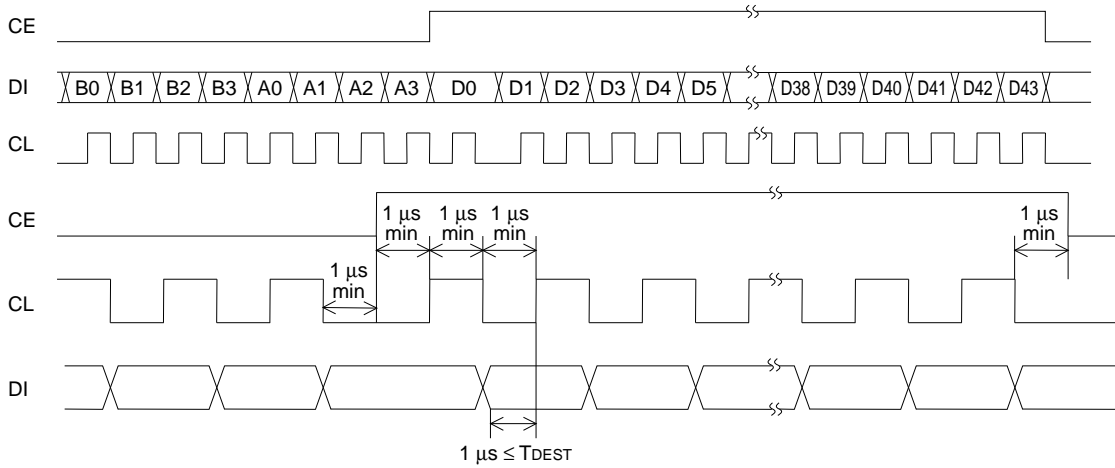
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Total harmonic distortion	THD	$V_{IN} = 1 \text{ Vrms}$, $f = 1 \text{ kHz}$, flat overall		0.003	0.01	%
Crosstalk	CT	$V_{IN} = 1 \text{ Vrms}$, $f = 1 \text{ kHz}$, flat overall, $R_g = 1 \text{ k}\Omega$		80.5		dB
Maximum attenuated output	Vomin	$V_{IN} = 1 \text{ Vrms}$, $f = 1 \text{ kHz}$, main volume $-\infty$		-80		dB
Output noise voltage	VN-1	Fflat overall, (IHF-A), $R_G = 1 \text{ k}\Omega$		8		μV
	VN-2	Fflat overall, (DIN-AUDIO), $R_G = 1 \text{ k}\Omega$		10		μV
Input high-level current	I_{IH}	CL, DI, CE $V_{IN} = 8 \text{ V}$			10	μA
Input low-level current	I_{IL}	CL, DI, CE $V_{IN} = 0 \text{ V}$	-10			μA

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Control Timing and Data Format

To control the LC75421M, input specified serial data to the CE, CL, and DI pins.

The data configuration consists of a total of 52 bits broken down into 8 address bits and 44 data bits.



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Volume Control

D16	D17	D18	D19	D20	D21	D22	D23	Operation
0	0	1	0	0	1	0	1	0dB
1	1	0	0	0	1	0	1	-1dB
0	1	0	0	0	1	0	1	-2dB
1	0	0	0	0	1	0	1	-3dB
0	0	1	1	1	0	0	1	-4dB
1	1	0	1	1	0	0	1	-5dB
0	1	0	1	1	0	0	1	-6dB
1	0	0	1	1	0	0	1	-7dB
0	0	1	0	1	0	0	1	-8dB
1	1	0	0	1	0	0	1	-9dB
0	1	0	0	1	0	0	1	-10dB
1	0	0	0	1	0	0	1	-11dB
0	0	1	1	0	0	0	1	-12dB
1	1	0	1	0	0	0	1	-13dB
0	1	0	1	0	0	0	1	-14dB
1	0	0	1	0	0	0	1	-15dB
0	0	1	0	0	0	0	1	-16dB
1	1	0	0	0	0	0	1	-17dB
0	1	0	0	0	0	0	1	-18dB
1	0	0	0	0	0	0	1	-19dB
0	0	1	1	1	1	1	0	-20dB
1	1	0	1	1	1	1	0	-21dB
0	1	0	1	1	1	1	0	-22dB
1	0	0	1	1	1	1	0	-23dB
0	0	1	0	1	1	1	0	-24dB
1	1	0	0	1	1	1	0	-25dB
0	1	0	0	1	1	1	0	-26dB
1	0	0	0	1	1	1	0	-27dB
0	0	1	1	0	1	1	0	-28dB
1	1	0	1	0	1	1	0	-29dB
0	1	0	1	0	1	1	0	-30dB
1	0	0	1	0	1	1	0	-31dB
0	0	1	0	0	1	1	0	-32dB
1	1	0	0	0	1	1	0	-33dB
0	1	0	0	0	1	1	0	-34dB
1	0	0	0	0	1	1	0	-35dB
0	0	1	1	1	0	1	0	-36dB
1	1	0	1	1	0	1	0	-37dB
0	1	0	1	1	0	1	0	-38dB
1	0	0	1	1	0	1	0	-39dB
0	0	1	0	1	0	1	0	-40dB
1	1	0	0	1	0	1	0	-41dB
0	1	0	0	1	0	1	0	-42dB
1	0	0	0	1	0	1	0	-43dB
0	0	1	1	0	0	1	0	-44dB
1	1	0	1	0	0	1	0	-45dB
0	1	0	1	0	0	1	0	-46dB
1	0	0	1	0	0	1	0	-47dB
0	0	1	0	0	0	1	0	-48dB
1	1	0	0	0	0	1	0	-49dB
0	1	0	0	0	0	1	0	-50dB

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D16	D17	D18	D19	D20	D21	D22	D23	Operation
1	0	0	0	0	0	1	0	-51dB
0	0	1	1	1	1	0	0	-52dB
1	1	0	1	1	1	0	0	-53dB
0	1	0	1	1	1	0	0	-54dB
1	0	0	1	1	1	0	0	-55dB
0	0	1	0	1	1	0	0	-56dB
1	1	0	0	1	1	0	0	-57dB
0	1	0	0	1	1	0	0	-58dB
1	0	0	0	1	1	0	0	-59dB
0	0	1	1	0	1	0	0	-60dB
1	1	0	1	0	1	0	0	-61dB
0	1	0	1	0	1	0	0	-62dB
1	0	0	1	0	1	0	0	-63dB
0	0	1	0	0	1	0	0	-64dB
1	1	0	0	0	1	0	0	-65dB
0	1	0	0	0	1	0	0	-66dB
1	0	0	0	0	1	0	0	-67dB
0	0	1	1	1	0	0	0	-68dB
1	1	0	1	1	0	0	0	-69dB
0	1	0	1	1	0	0	0	-70dB
1	0	0	1	1	0	0	0	-71dB
0	0	1	0	1	0	0	0	-72dB
1	1	0	0	1	0	0	0	-73dB
0	1	0	0	1	0	0	0	-74dB
1	0	0	0	1	0	0	0	-75dB
0	0	1	1	0	0	0	0	-76dB
1	1	0	1	0	0	0	0	-77dB
0	1	0	1	0	0	0	0	-78dB
1	0	0	1	0	0	0	0	-79dB
0	0	0	0	0	0	0	0	-∞dB

Input Switch Control (L1, L2, L3, L4, L5, R1, R2, R3, R4, R5)

D28	D29	D32	Operation
0	0	1	L1 (R1) ON
1	0	1	L2 (R2) ON
0	1	1	L3 (R3) ON
1	1	1	L4 (R4) ON
0	0	0	L5 (R5) ON

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Pin Functions

Pin No.	Pin Name	Function	Equivalent circuit
18 17 16 15 14 20 21 22 23 24	L1 L2 L3 L4 L5 R1 R2 R3 R4 R5	<ul style="list-style-type: none"> Input signal pins 	
13 25	LSELO RSELO	<ul style="list-style-type: none"> Input selector output pins 	
10 9 28 29	LBASS1 LBASS2 RBASS1 RBASS2	<ul style="list-style-type: none"> Bass band filter configuration capacitor and resistor connection pins 	
8 7 30 31	LSB LOUT RSB ROUT	<ul style="list-style-type: none"> Super bass band filter configuration capacitor and resistor connection pins 	
5 4 33 34	LFOUT LROUT RFOUT RROUT	<ul style="list-style-type: none"> Fader output pins. The front side and rear side can be attenuated separately. The attenuation is the same for both Left and Right. 	

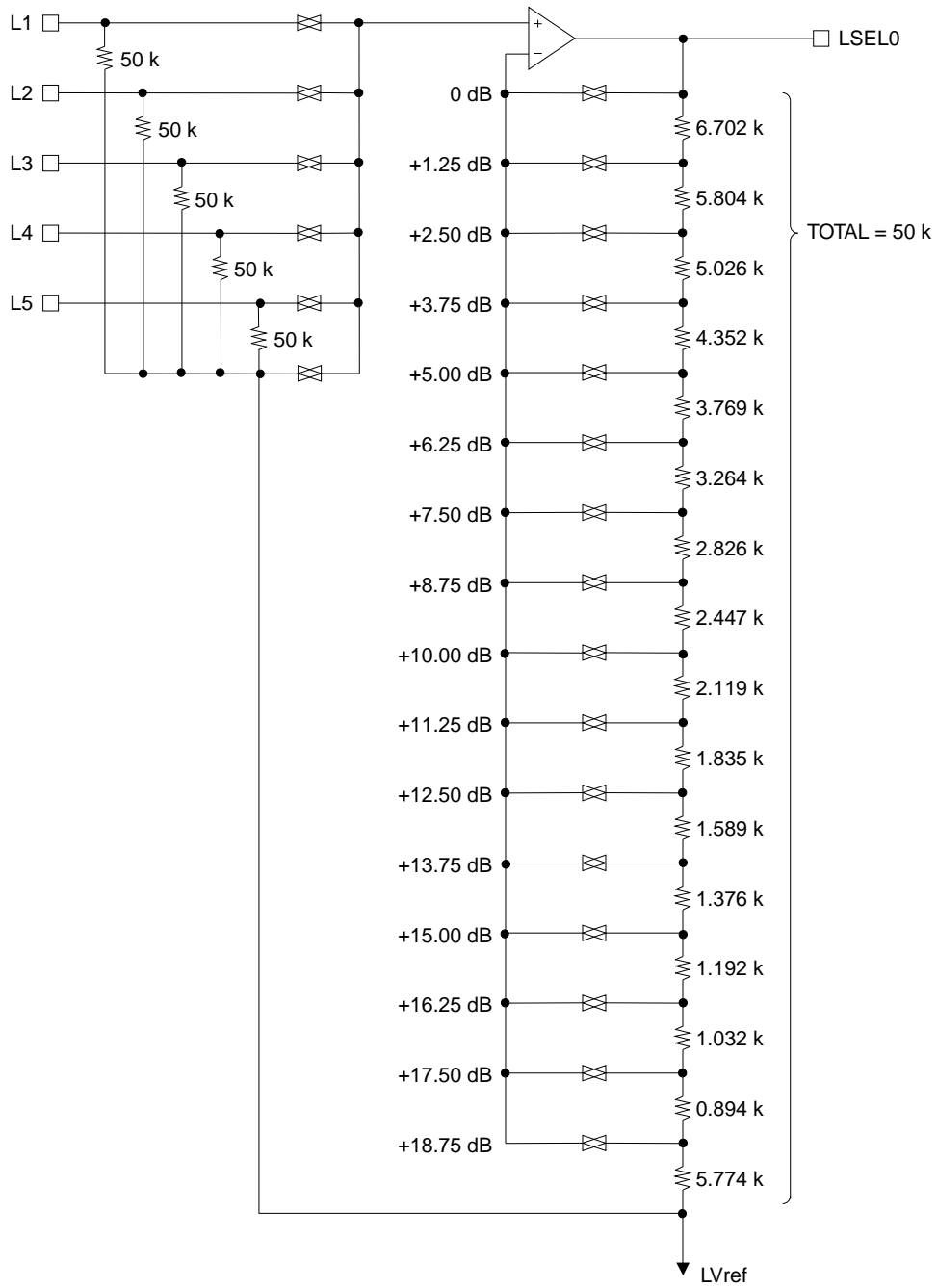
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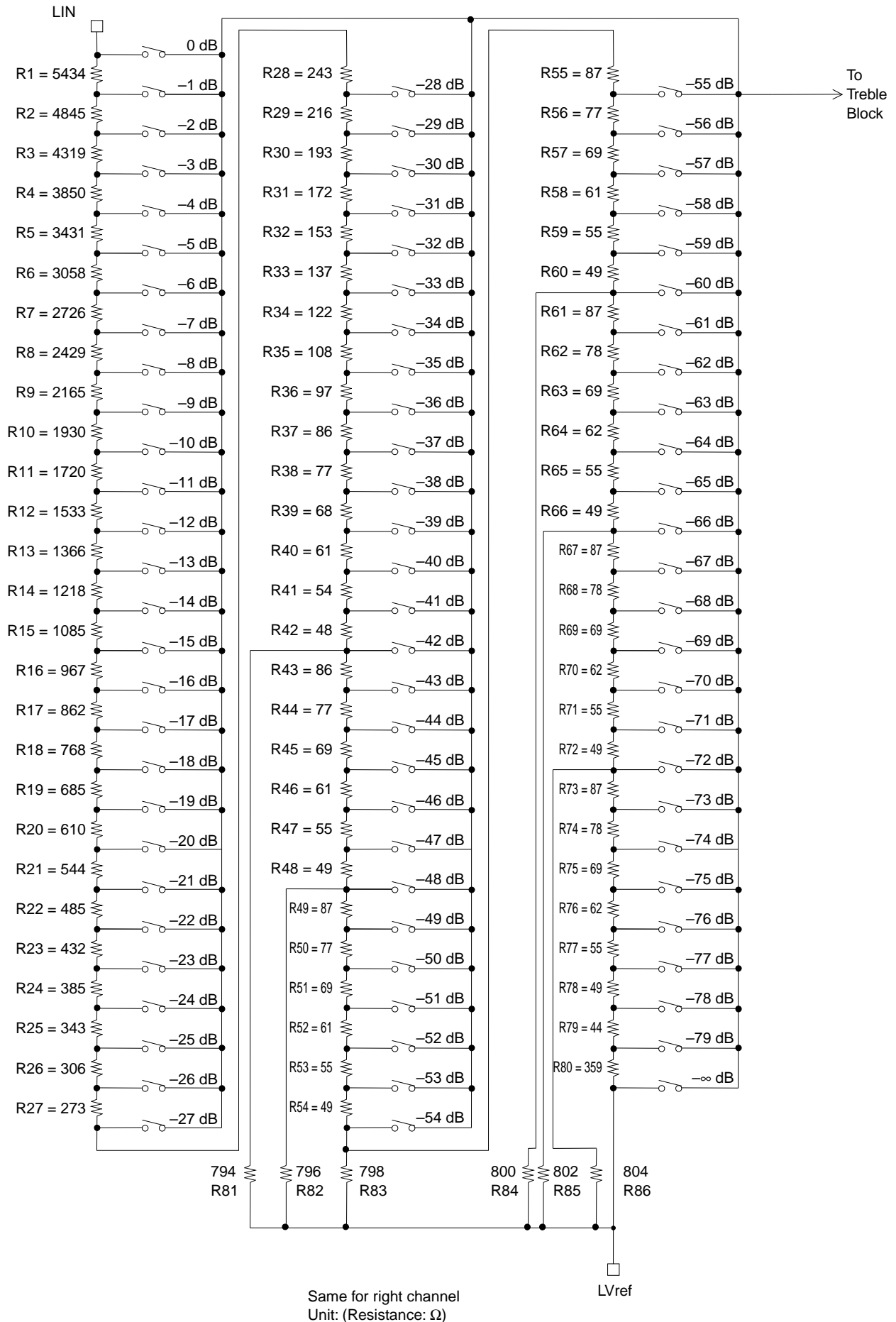
Pin No.	Pin Name	Function	Equivalent circuit
11 27	LTRE RTRE	<ul style="list-style-type: none"> Capacitor connection pin for configuring treble filter 	
19	Vref	<ul style="list-style-type: none"> Connect a capacitor of a few tens of μF between Vref and AV_{SS} (V_{SS}) as a analog ground $0.5 \times V_{\text{DD}}$ voltage generator, current ripple countermeasure. 	
3	V _{SS}	<ul style="list-style-type: none"> Ground pin 	
35	V _{DD}	<ul style="list-style-type: none"> Power supply pin 	
2	CE	<ul style="list-style-type: none"> Chip enable pin Data is written to the internal latch and the analog switches are operated when the level changes from High to Low. Data transfer is enabled when the level is High. 	
1 36	DI CL	<ul style="list-style-type: none"> Serial data pin and clock input pin for control 	

Equivalent Circuit Input Block Diagram

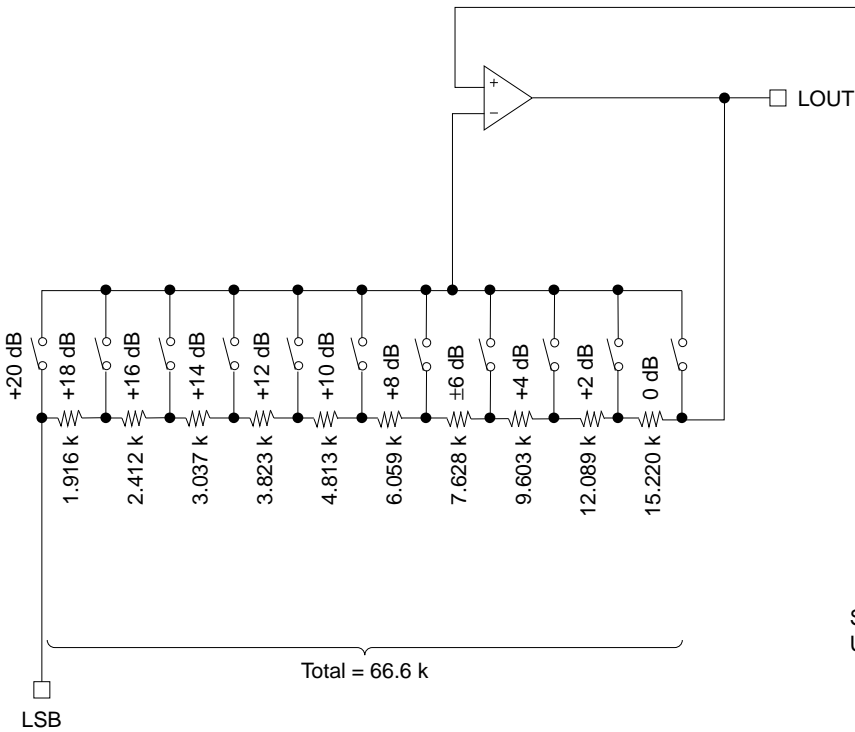
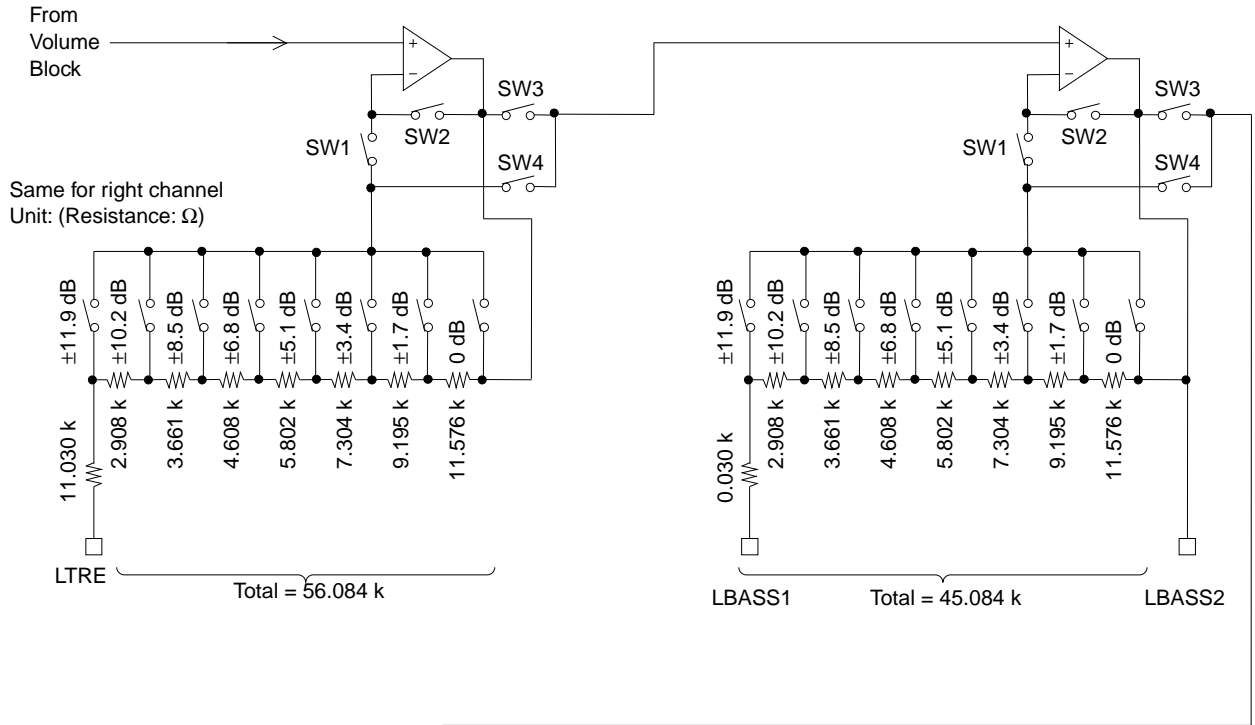


Same for right channel
Unit: (Resistance: Ω)

Volume Block Equivalent Circuit Diagram



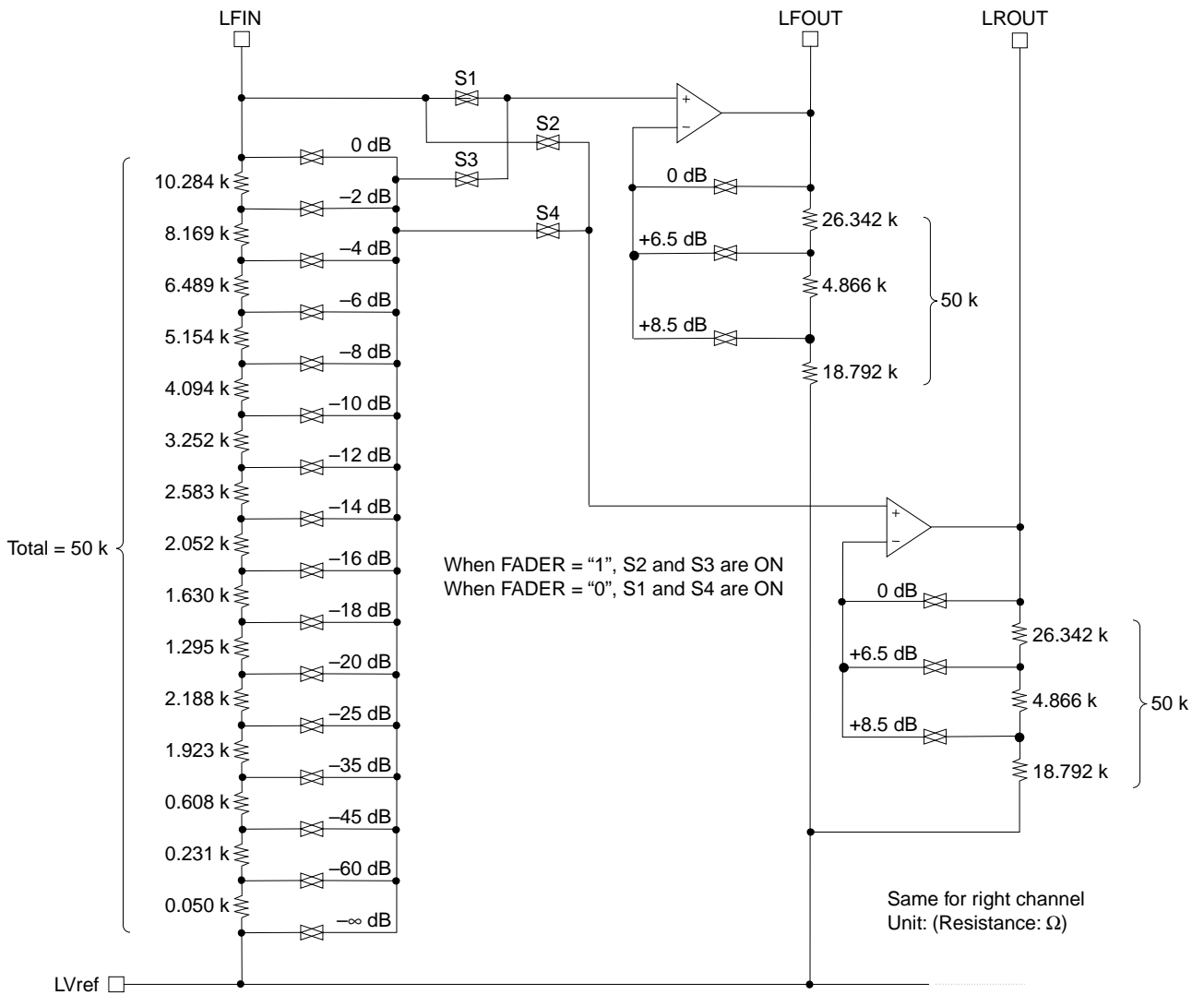
Treble/Bass/Super Bass Band Block Equivalent Circuit Diagram



Same for right channel
Units: (Resistance: Ω)

During boost, SW1 and SW3 are ON, during cut, SW2 and SW4 are ON,
when 0 dB, 0 dB SW and SW2 and SW3 are ON.

Fader Volume Block Equivalent Circuit Diagram



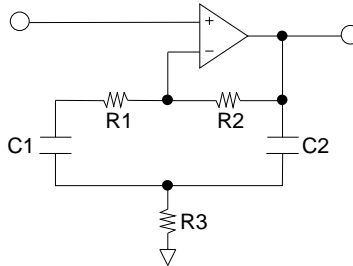
When $-\infty$ data is sent to the main volume, S1 and S2 become open, and S3 and S4 simultaneously become ON.

Tone Circuit Constant Calculation Examples

Super Bass Band Circuit

The equivalent circuit and the formula for calculating the external RC with a mean frequency of 68 Hz are shown below.

- Super bass band equivalent circuit block diagram



- Calculation example

Specification Mean frequency: $f_0 = 68 \text{ Hz}$

Gain during maximum boost: $G = 20 \text{ dB}$

Let us use $R_1 = 0$, $R_2 = 66.6 \text{ k}\Omega$, and $C_1 = C_2 = C$.

We obtain R_3 from $G = 20 \text{ dB}$.

$$G_{+20 \text{ dB}} = 20 \times \text{LOG}_{10} \left(1 + \frac{R_2}{2R_3} \right)$$

$$R_3 = \frac{R_2}{2(10^{G/20} - 1)} = \frac{66600}{2 \times (10 - 1)} \approx 3.7 \text{ K}\Omega$$

We obtain C from mean frequency $f_0 = 68 \text{ Hz}$.

$$f_0 = \frac{1}{2\pi\sqrt{R_3R_2C_1C_2}}$$

$$C = \frac{1}{2\pi f_0 \sqrt{R_3R_2}} = \frac{1}{2\pi \times 68 \sqrt{66600 \times 3700}} \approx 0.15 \mu\text{F}$$

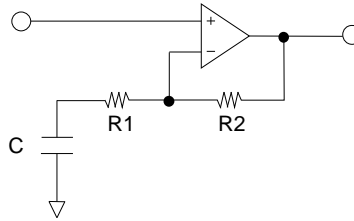
We obtain Q .

$$Q = \frac{R_3R_2}{2R_3} \frac{1}{\sqrt{R_3R_2}} \approx 2.1$$

Treble Band Circuit

The shelving characteristics can be obtained for the treble band.

The equivalent circuit and calculation formula during boost are indicated below.



• Calculation example 1

Specification Set frequency: $f = 10000 \text{ Hz}$

Gain during maximum boost: $G + 14 \text{ dB} = 14 \text{ dB}$

Let us use $R1 = 11.030 \text{ k}\Omega$ and $R2 = 45.054 \text{ k}\Omega$.

The above constants are inserted in the following formula.

$$G = 20 \times \text{LOG}_{10} \left(1 + \frac{R2}{\sqrt{R1^2 + (1 / \omega C)^2}} \right)$$

$$C = \frac{1}{2\pi f \sqrt{\left(\frac{R2}{10^{G/20} - 1}\right)^2 - R1^2}}$$

$$= \frac{1}{2\pi 10000 \sqrt{\left(\frac{45054}{5.01 - 1}\right)^2 - 11030^2}} \neq 6800(\text{pF})$$

Simulation Results

Setting	f = 10 kHz	f = 1 kHz
14 dB	13.95	7.42
12 dB	11.98	6.96
10 dB	10	6.34
8 dB	8	5.5
6 dB	6	4.43
4 dB	4	3.13
2 dB	2	1.64

• Calculation example 2

Specification Set frequency: $f = 10000 \text{ Hz}$

Gain during maximum boost: $G_{+11.9 \text{ dB}} = 11.9 \text{ dB}$

Let us use $R1 = 11.030 \text{ k}\Omega$ and $R2 = 45.054 \text{ k}\Omega$.

The above constants are inserted in the following formula.

$$G = 20 \times \text{LOG}_{10} \left(1 + \frac{R2}{\sqrt{R1^2 + (1 / \omega C)^2}} \right)$$

$$C = \frac{1}{2\pi f \sqrt{\left(\frac{R2}{10^{11.9/20} - 1}\right)^2 - R1^2}}$$

$$= \frac{1}{2\pi 10000 \sqrt{\left(\frac{45054}{3.94 - 1}\right)^2 - 11030^2}} \neq 1500(pF)$$

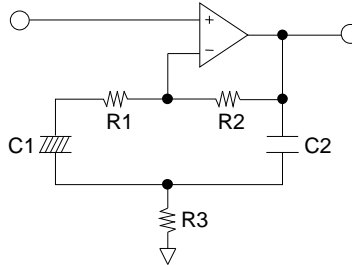
Simulation Results

Setting	f = 10 kHz	f = 1 kHz
11.9 dB	11.92	0.00
10.2 dB	10.64	0.00
8.5 dB	9.17	0.00
6.8 dB	7.52	0.00
5.1 dB	5.74	0.00
3.4 dB	3.88	0.00
1.7 dB	1.96	0.00

Bass Shelving Circuit

The equivalent circuit and calculation formula during boost are shown below.

- Bass band equivalent circuit diagram



- Calculation example 1

Specification Mean frequency: $f_0 = 40 \text{ Hz}$

Gain during maximum boost: $G_{+14 \text{ dB}} = 14 \text{ dB}$

Let us use $R_1 = 0 \text{ k}\Omega$, $R_2 = 45.054 \text{ k}\Omega$, $C_1 = 2.2 \text{ }\mu\text{F}$, and $C_1 \gg C_2$.

We obtain R_3 from $G = 14 \text{ dB}$.

$$G_{+14 \text{ dB}} = 20 \times \text{LOG}_{10} \left(\frac{R_2 + R_3}{R_3} \right)$$

$$R_3 = \frac{R_2}{10^{G/20} - 1} = \frac{45054}{5.01 - 1} \approx 11 \text{ K}\Omega$$

We obtain C_2 from mean frequency $f_0 = 40 \text{ Hz}$.

$$f_0 = \frac{1}{2\pi \sqrt{R_3 R_2 C_1 C_2}}$$

$$C_2 = \frac{1}{(2\pi f_0)^2 R_2 R_3 C_1} = \frac{1}{(2\pi \times 40)^2 \times 45054 \times 11000 \times (2.2 \times 10^{-6})} \approx 0.015 \text{ }\mu\text{F}$$

Simulation Results

Setting	f = 100 Hz	f = 1 kHz
14 dB	13.55	3.65
12 dB	11.73	3.51
10 dB	9.8	3.31
8 dB	7.89	3
6 dB	5.94	2.55
4 dB	3.97	1.92
2 dB	1.99	1.07

• Calculation example 2

Specification Mean frequency: $f_0 = 40 \text{ Hz}$

Gain during maximum boost: $G = 12 \text{ dB}$

Let us use $R_1 = 0 \text{ k}\Omega$, $R_2 = 45.054 \text{ k}\Omega$, $C_1 = 2.2 \text{ }\mu\text{F}$, and $C_1 \gg C_2$.

We obtain R_3 from $G = 12 \text{ dB}$.

$$G_{+12 \text{ dB}} = 20 \times \text{LOG}_{10} \left(\frac{R_2 + R_3}{R_3} \right)$$

$$R_3 = \frac{R_2}{10^{G/20} - 1} = \frac{45054}{3.98 - 1} \approx 15 \text{ K}\Omega$$

We obtain C_2 from mean frequency $f_0 = 40 \text{ Hz}$.

$$f_0 = \frac{1}{2\pi\sqrt{R_3 R_2 C_1 C_2}}$$

$$C_2 = \frac{1}{(2\pi f_0)^2 R_2 R_3 C_1} = \frac{1}{(2\pi \times 40)^2 \times 45054 \times 15000 \times (2.2 \times 10^{-6})} \approx 0.01 \text{ }\mu\text{F}$$

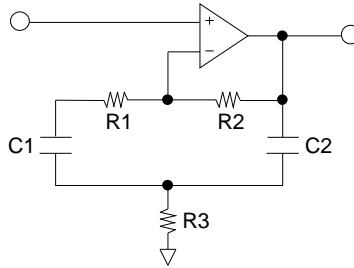
Simulation Results

Setting	f = 100 Hz	f = 1 kHz
14 dB	11.73	4.27
12 dB	10.29	4.07
10 dB	8.74	3.78
8 dB	7.11	3.38
6 dB	5.41	2.82
4 dB	3.65	2.09
2 dB	1.85	1.15

(4) Bass Peaking Circuit

The equivalent circuit and the formula for calculating the external RC with a mean frequency of 100 Hz are shown below.

- Bass band equivalent circuit diagram



- Calculation example

Specification Mean frequency: $f_0 = 100 \text{ Hz}$

Gain during maximum boost: $G = 11.9 \text{ dB}$

Let us use $R_1 = 0$, $R_2 = 45.084 \text{ k}\Omega$, and $C_1 = C_2 = C$.

We obtain R_3 from $G = 11.9 \text{ dB}$.

$$G_{+11.9 \text{ dB}} = 20 \times \text{LOG}_{10} \left(1 + \frac{R_2}{2R_3} \right)$$

$$R_3 = \frac{R_2}{2(10^{11.9 \text{ dB}/20} - 1)} = \frac{45084}{2 \times (3.936 - 1)} \approx 7.68 \text{ K}\Omega$$

We obtain C from mean frequency $f_0 = 100 \text{ Hz}$.

$$f_0 = \frac{1}{2\pi\sqrt{R_3R_2C_1C_2}}$$

$$C = \frac{1}{2\pi f_0 \sqrt{R_3R_2}} = \frac{1}{2\pi \times 100 \sqrt{45084 \times 7680}} \approx 0.082 \text{ }\mu\text{F}$$

We obtain Q .

$$Q = \frac{R_3R_2}{2R_3} \cdot \frac{1}{\sqrt{R_3R_2}} \approx 1.66$$

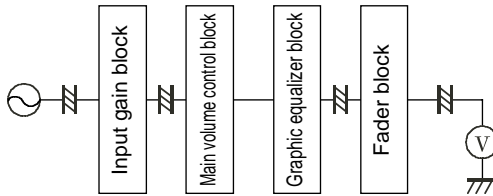
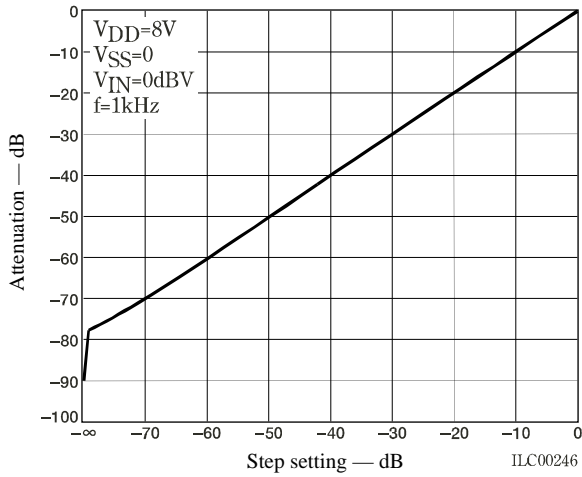
Simulation Results

Setting	f = 100 Hz	f = 1 kHz
11.9 dB	11.88	0.00
10.2 dB	10.38	0.00
8.5 dB	8.79	0.00
6.8 dB	7.14	0.00
5.1 dB	5.42	0.00
3.4 dB	3.66	0.00
1.7 dB	1.85	0.00

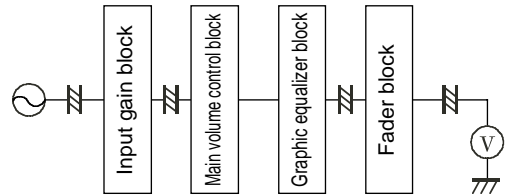
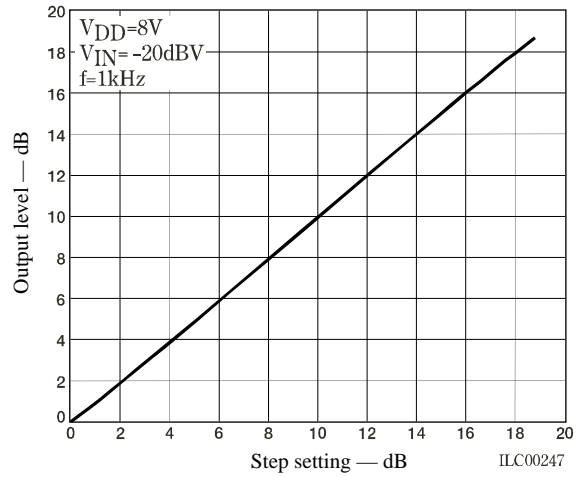
Usage Cautions

- (1) Upon power application, the internal analog switch status is undefined. Use an external countermeasure such as muting until data is set.
- (2) When performing initial data setting after applying power, send the initial data once, and then send the initial setting data.
- (3) To ensure that the digital frequency signal sent to the CL, DI, and CE pins do not spill over to the analog signal block, either guard these signal lines with a ground pattern, or perform transmission using shielded wires.

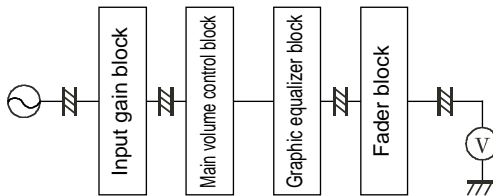
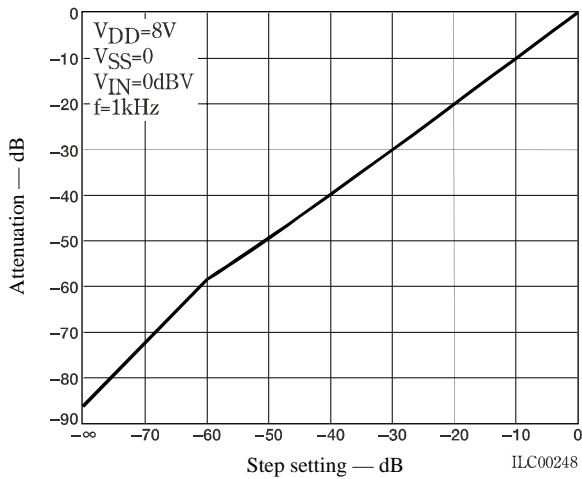
Main Volume Control Step Characteristics



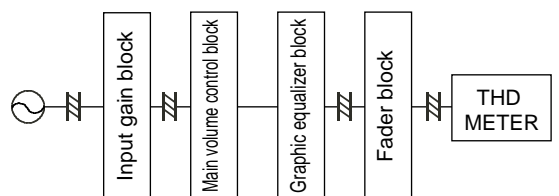
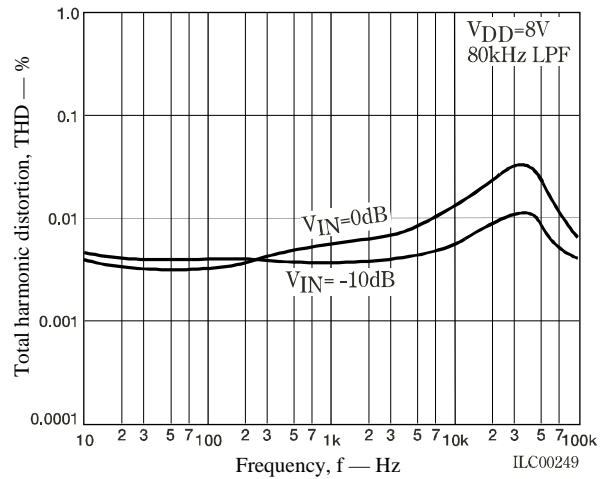
Input Gain Step Characteristics

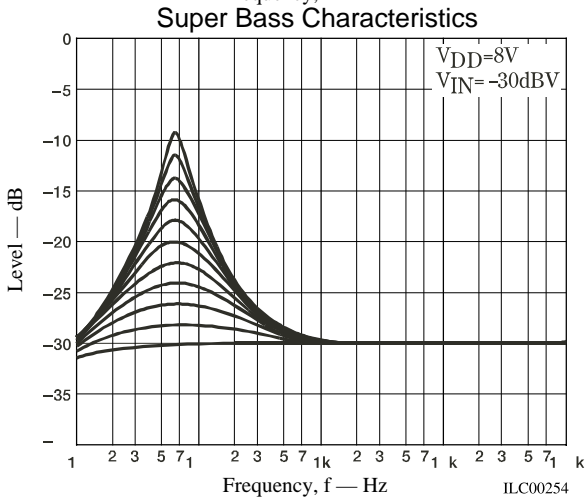
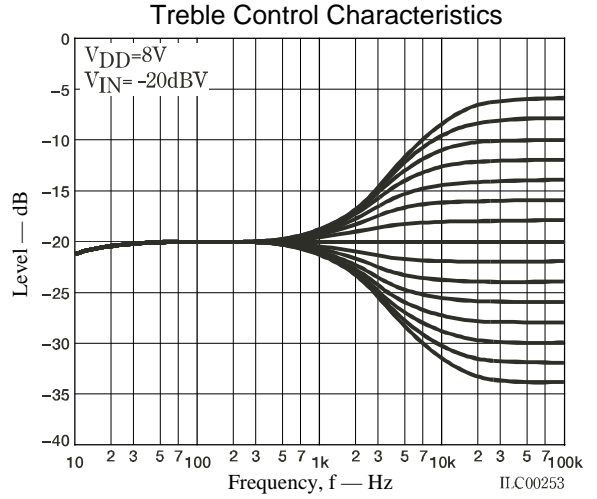
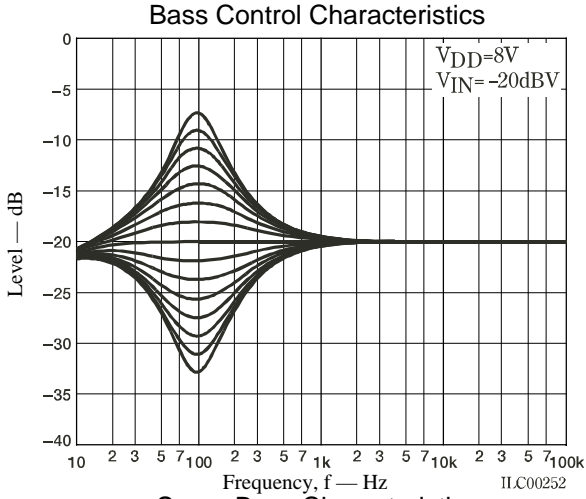
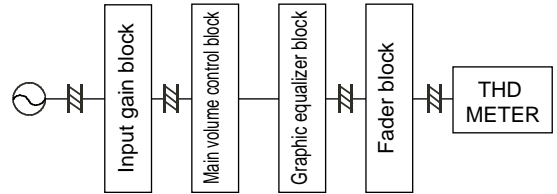
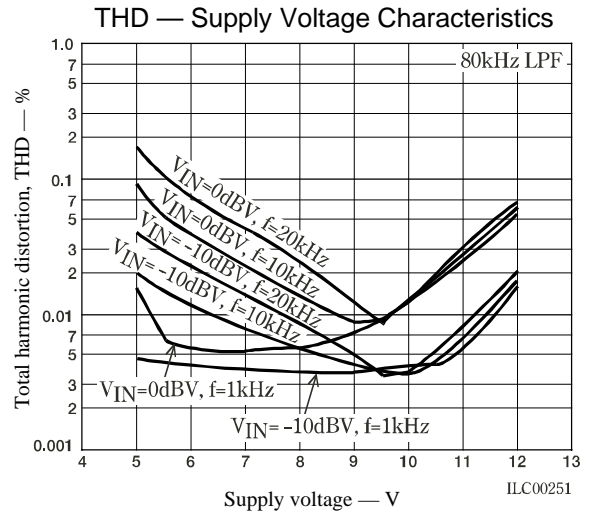
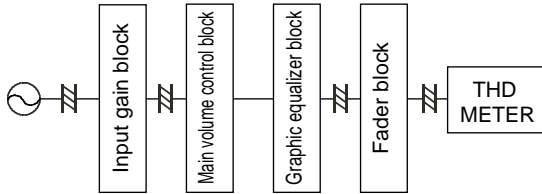
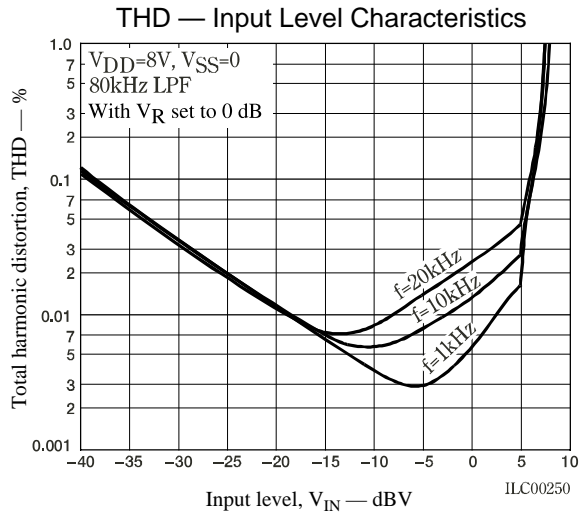


Fader Step Characteristics



THD — Frequency Characteristics





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