普誠科技股份有限公司
Princeton Technology Corp.
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DESCRIPTION

PT2318 is a sound fader controller IC utilizing CMOS Technology specially designed for car radio hi-fi audio applications. Four selectable stereo inputs, 1 mono input, bass, treble, volume, balance and fader controls, mute function and a special loudness feature which is automatically controlled in combination with the volume level setting are all built into a single I²C bus controlled stereo preamplifier chip having the highest performance and reliability. Pin assignments and application circuits are optimized for easy PCB layout and cost saving advantages.

FEATURES

- CMOS technology
- I²C bus control interface
- 4 selectable stereo inputs
- 1 mono input
- Volume, Balance and Fader controls
- Bass & Treble controls
- Noise reduction circuit interface provided
- External equalizer interface provided
- Mute control at audio signal zero crossing
- Internal power-on reset function
- Mute function controlled via the I²C bus or pin
- Special automatic loudness feature in combination with the volume setting

APPLICATIONS

- Car audio
- Hi-Fi audio applications

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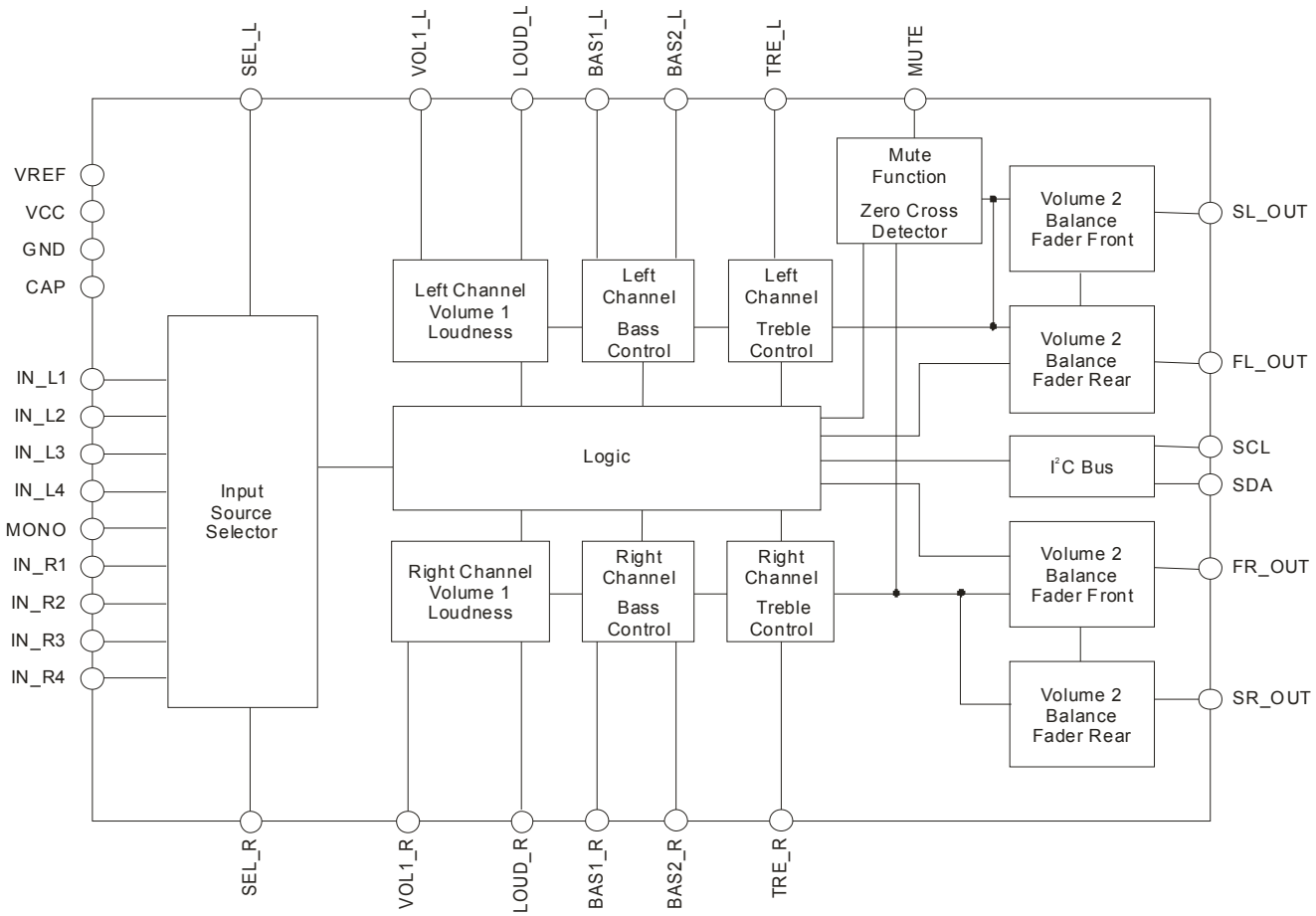
BLOCK DIAGRAM



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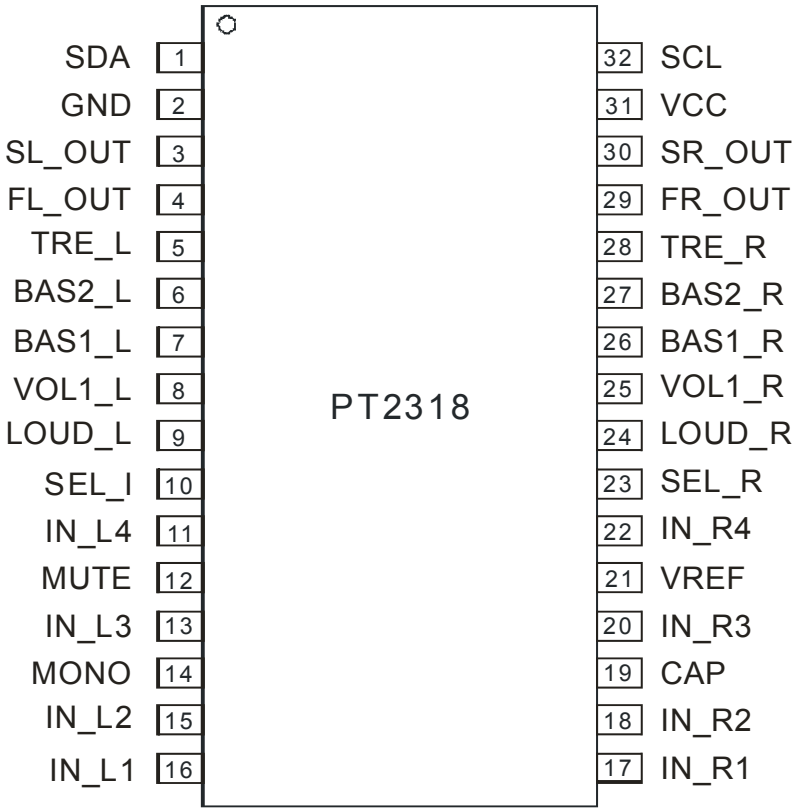
PIN CONFIGURATION



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PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
SDA	I	Serial Data Input Pin	1
GND	-	Ground	2
SL_OUT	O	Left Rear Channel Output Pin	3
FL_OUT	O	Left Front Channel Output Pin	4
TRE_L	I/O	Left Channel Treble Control Pin or may be used as External Equalizer Input Pin	5
BAS2_L	I/O	Left Channel Bass Control Pin or may be used as External Equalizer Output Pin	6
BAS1_L	I	Left Channel Bass Control Pin	7
VOL1_L	I	Left Control Section Volume Input Pin	8
LOUD_L	I	Left Control Section Loudness Input Pin	9
SEL_L	O	Left Channel Output Source Selector	10
IN_L4	I	Left Channel Source 4 Input Pin	11
MUTE	I	Mute Function Control Pin	12
IN_L3	I	Left Channel Source 3 Input Pin	13
MONO	I	Input “MONO” Source	14
IN_L2	I	Left Channel Source 2 Input Pin	15
IN_L1	I	Left Channel Source 1 Input Pin	16
IN_R1	I	Right Channel Source 1 Input Pin	17
IN_R2	I	Right Channel Source 2 Input Pin	18
CAP	-	Supply Electronic Filtering	19
IN_R3	I	Right Channel Source 3 Input Pin	20
VREF	-	Reference Voltage (0.5Vcc)	21
IN_R4	I	Right Channel Source 4 Input Pin	22
SEL_R	O	Right Channel Output Source Selector	23
LOUD_R	I	Right Control Section Loudness Input Pin	24
VOL1_R	I	Right Control Section Volume 1 Input Pin	25
BAS1_R	I	Right Channel Bass Control Pin	26
BAS2_R	I/O	Right Channel Bass Control Pin Or may be used as External Equalizer Output Pin	27
TRE_R	I/O	Right Channel Treble Control Pin Or may be used as External Equalizer Input Pin	28
FR_OUT	O	Right Front Output Pin	29
SR_OUT	O	Right Rear Output Pin	30
VCC	-	Supply Voltage	31
SCL	I	Serial Clock Input Pin	32

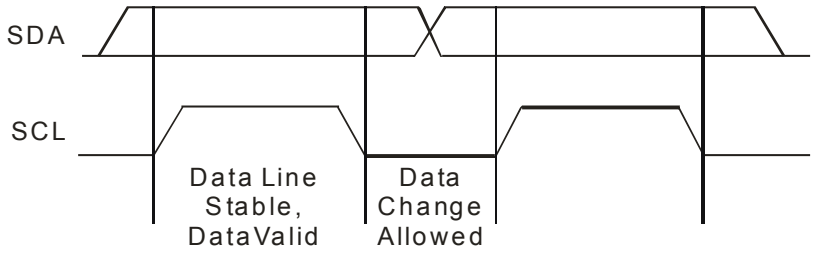
FUNCTION DESCRIPTION

BUS INTERFACE

Data are transmitted to and from the microprocessor to the PT2318 via the SDA and SCL. The SDA and SCL make up the BUS Interface. It should be noted that the pull-up resistors must be connected to the positive supply voltage.

DATA VALIDITY

A data on the SDA Line is considered valid and stable only when the SCL Signal is in HIGH State. The HIGH and LOW States of the SDA Line can only change when the SCL signal is LOW. Please refer to the figure below.



START AND STOP CONDITIONS

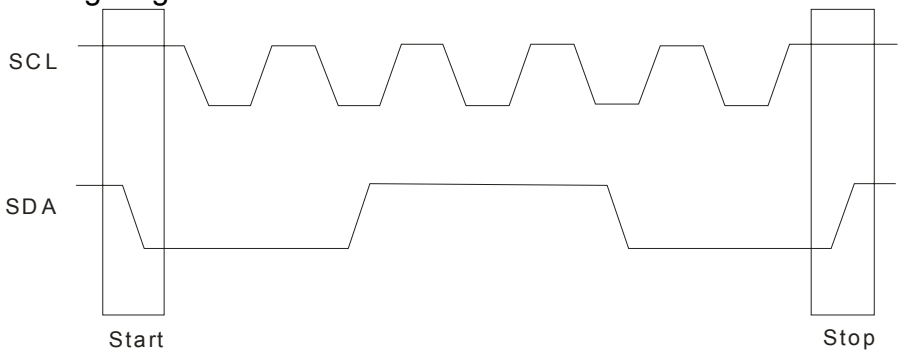
A Start Condition is activated when

1. the SCL is set to HIGH and
2. SDA shifts from HIGH to LOW State.

The Stop Condition is activated when

1. SCL is set to HIGH and
2. SDA shifts from LOW to HIGH State.

Please refer to the timing diagram below.

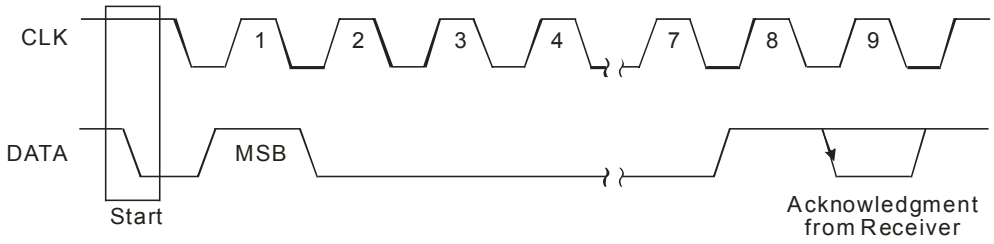


BYTE FORMAT

Every byte transmitted to the SDA Line consists of 8 bits. Each byte must be followed by an Acknowledge Bit. The MSB is transmitted first.

ACKNOWLEDGE

During the Acknowledge Clock Pulse, the master (μP) puts a resistive HIGH level on the SDA Line. The peripheral (audio processor) that acknowledges has to pull-down (LOW) the SDA line during the Acknowledge Clock Pulse so that the SDA Line is in a Stable Low State during this Clock Pulse. Please refer to the diagram below.



The audio processor that has been addressed has to generate an Acknowledge after receiving each byte, otherwise, the SDA Line will remain at the High Level during the ninth (9th) Clock Pulse. In this case, the master transmitter can generate the STOP Information in order to abort the transfer.

TRANSMISSION WITHOUT ACKNOWLEDGE

If you want to avoid the acknowledge detection of the audio processor, a simpler μP transmission may be used. Wait one clock and do not check the slave acknowledge of this same clock then send the new data. If you use this approach, there are greater chances of faulty operation as well as decrease in noise immunity.

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INTERFACE PROTOCOL

The interface protocol consists of the following:
1. START Condition
2. Chip Address Byte=80H
3. ACK=Acknowledge Bit
4. Data Byte
5. STOP Condition

Please refer to the diagram below:

	MSB			First Byte				LSB						
START	1	0	0	0	1	0	0	0	Subaddress	ACK	Data Byte	ACK	STOP
	Chip Address												

Notes:
1. ACK=ACKNOWLEDGE
2. Max. Clock Speed=100K Bits/S

The SUBADDRESS is the Second Byte transmitted following the CHIP ADDRESS Byte. Please refer to the table below.

MSB							**LSB**	**Function**
7	6	5	4	3	2*	1*	0*	
0	0	0	0	0	0	0	0	Volume/Loudness
0	0	0	0	0	0	0	1	Fader: Front, Right
0	0	0	0	0	0	1	0	Fader: Front, Left
0	0	0	0	0	0	1	1	Fader: Rear, Right
0	0	0	0	0	1	0	0	Fader: Rear, Left
0	0	0	0	0	1	0	1	Bass
0	0	0	0	0	1	1	0	Treble
0	0	0	0	0	1	1	1	Selector Switch

Note: These are Significant SUBADDRESS bits.

The last bits of SUBADDRESS are named “specific bit”. When more than one data bit send to PT2318, the SUBADDRESS will increase automatically depend on specific bit. It is unnecessary to send to SUBADDRESS, data bit will fill in SUBADDRESS bit. Please refer to following table.

START	Chip Address	ACK	Sub Address	ACK	Data Byte	ACK	Data Byte	ACK	Data Byte	ACK	Data Byte	ACK	STOP
Start	80H		00H		Corresponding Sub Address 00H		Corresponding Sub Address 01H		Corresponding Sub Address 02H		Corresponding Sub Address 03H		End

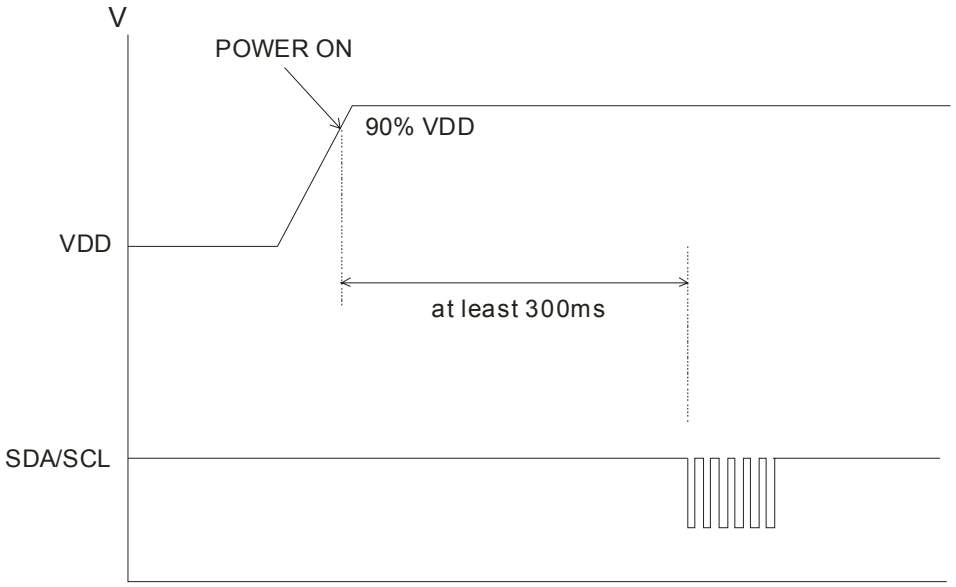
The Third Byte following the CIP ADDRESS & SUBADDRESS is defined in the table below.

MSB						LSB		Function
7	6	5	4	3	2	1	0	
ZCM	LOFF	V5	V4	V3	V2	V1	V0	Volume/Loudness
X	X	FFR5	FFR4	FFR3	FFR2	FFR1	FFR0	Fader: Front, Right
X	X	FFL5	FFL4	FFL3	FFL2	FFL1	FFL0	Fader: Front, Left
X	X	FSR5	FSR4	FSR3	FSR2	FSR1	FSR0	Fader: Rear, Right
X	X	FSL5	FSL4	FSL3	FSL2	FSL1	FSL0	Fader: Rear, Left
X	X	X	BAS4	BAS3	BAS2	BAS1	BAS0	Bass
X	X	X	TRE4	TRE3	TRE2	TRE1	TRE0	Treble
GMU	X	X	X	X	SC2	SC1	SC0	Selector Switch

X=Irrelevant (It should be noted that during testing, this bit is given the value of “1”)

I²C BUS START-UP TIMING

After Power is turned ON, PT2318 needs to wait for a short time in order to insure stability. This waiting period is relative to the value of Cref. When Cref=10 μF, the waiting time period for PT2318 to send I²C Bus Signal is at least 300ms. If the waiting time period is less than 300ms, I²C Control may fail. Please refer to the figure below.



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SOURCE SELECTOR

PT2318 provides 4 selectable stereo inputs and one mono input. The source selector is used to select any one of the mentioned source input options. Please refer to the table below.

Input Source	Source Selector Bits		
	SC2	SC1	SC0
Stereo Inputs: IN_L1 & IN_R1	1	1	1
Stereo Inputs: IN_L2 & IN_R2	1	1	0
Stereo Inputs: IN_L3 & IN_R3	1	0	1
Stereo Inputs: IN_L4 & IN_R4	1	0	0
Mono Input: MONO	0	X	X

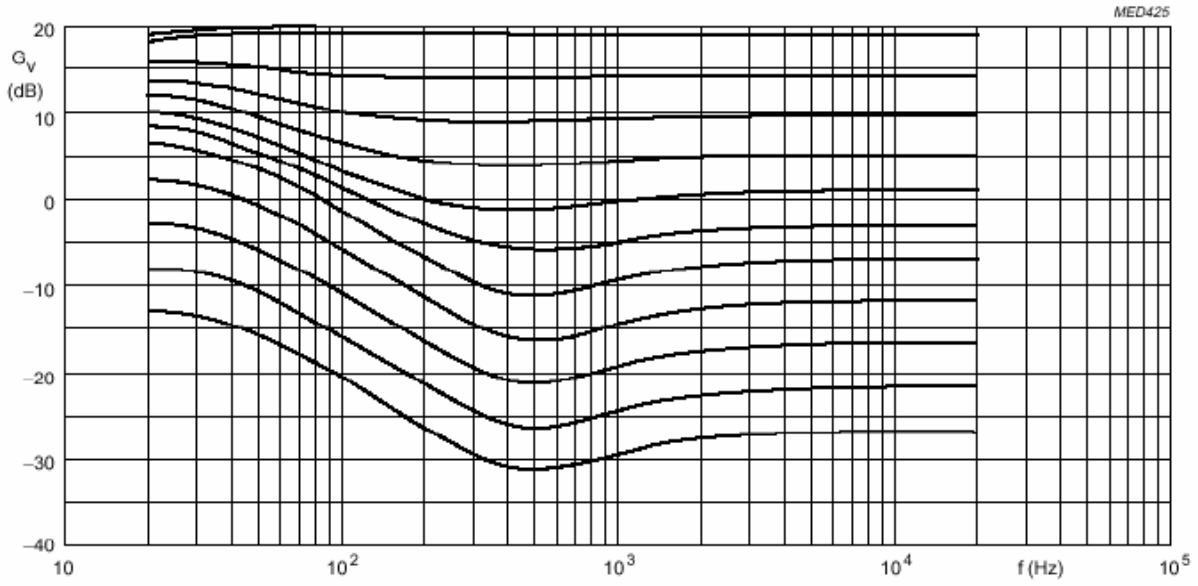
Notes:
1. SC0 to SC2=Source Selector Control Bits
2. X=Irrelevant

VOLUME CONTROL

The Volume Control Function consists of two blocks; namely, Volume 1 Control Block and Volume 2 Control Block.

VOLUME 1 CONTROL BLOCK

The Volume 1 Control Block has an attenuation range of +20dB to -31dB at 1dB/step. The left and right channels have the same gain/attenuation setting. This block operates in conjunction with the Loudness Control. When the Volume 1 Control maximum gain (=20dB) is selected, the filter characteristic is linear. The filter characteristic increases automatically over a range of 32dB down to a setting of -12dB. This means that the Volume 1 Control Block maximum filter characteristics is obtained at a -12dB setting. If the volume is further reduced, the filter characteristics are not in any way affected. The maximum selected filter characteristics is determined by the external components. Please refer to the diagram below.



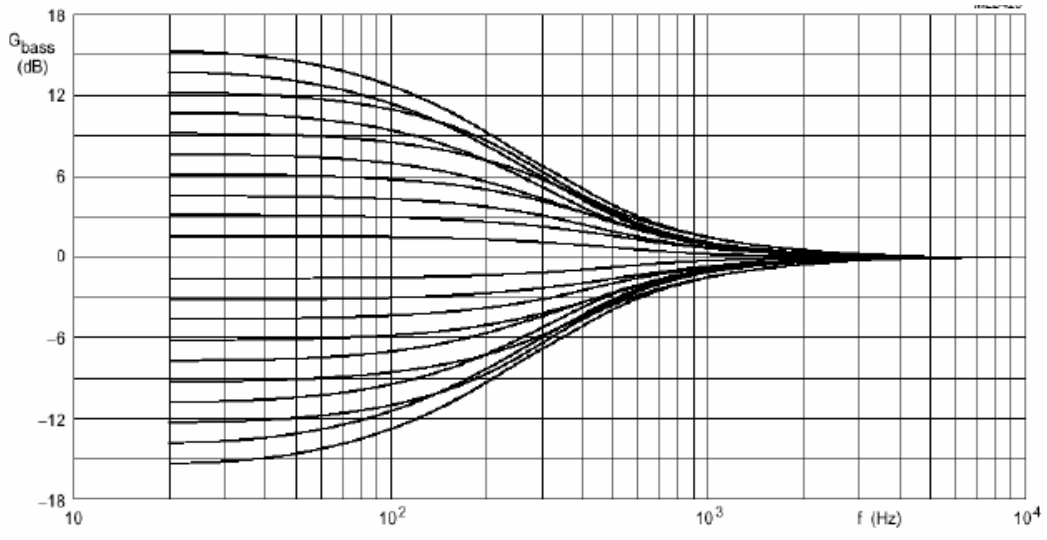
Volume control and Loudness (Low Roll-Off Frequency included)

VOLUME 2 CONTROL BLOCK

The Volume 2 Control Block operates in combination with the Balance and Fader Functions. Each output has one independent attenuator which has a control range of 0dB to -55dB at 1dB/step with an additional mute step.

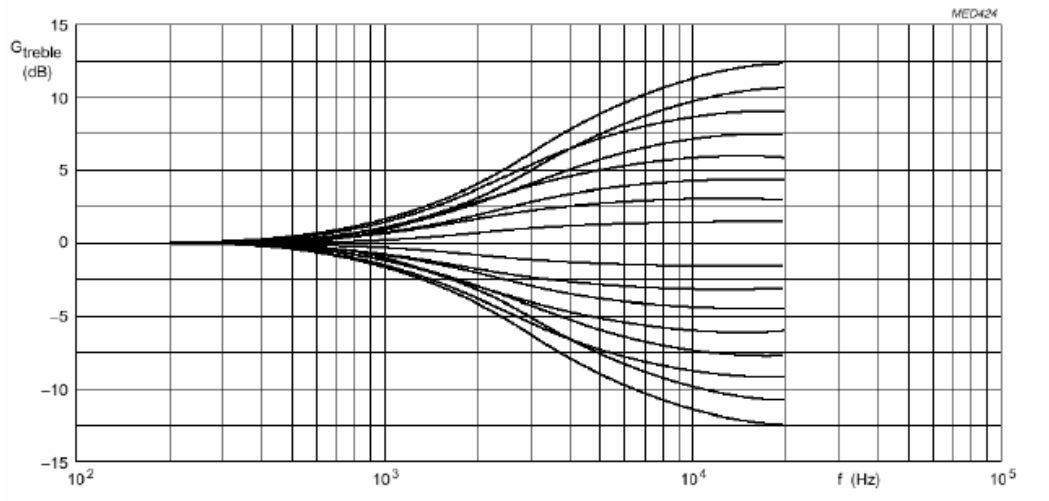
BASS FUNCTION

The bass function has a control range of -15dB to +15dB at 40Hz. The basic step width of the bass control is 3dB. The intermediate steps are obtained by switching 1.5dB boost and 1.5 dB attenuation steps. The bass control function can be disabled via the I^2C Bus. If the bass control function is disabled, the internal signal flow is discontinued, and the pins -- BAS2_L and BAS2-R are used as inputs for connecting an external equalizer. The Bass Function Frequency Response curve is shown below:



TREBLE FUNCTION

The Treble Function has a control range of -12dB to +12dB at 1.5dB / step at 15KHz. The basic step width of the treble control is 3dB and the intermediate steps are obtained by switching 1.5dB boost and 1.5 dB attenuation steps. The treble control function can be disabled via the I^2C Bus. If the treble control function is disabled, the internal signal flow is discontinued, and the treble pins -- TRE_L and TRE_R -- are used as inputs for connecting an external equalizer. The Treble Function Frequency Response Curve is given below.



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VOLUME SETTING

The volume setting table is given below. The loudness characteristic increases in a linear manner for every step in the volume whose range is from +20dB to -11dB.

GV (dB)	V5	V4	V3	V2	V1	V0
20	1	1	1	1	1	1
19	1	1	1	1	1	0
18	1	1	1	1	0	1
17	1	1	1	1	0	0
16	1	1	1	0	1	1
15	1	1	1	0	1	0
14	1	1	1	0	0	1
13	1	1	1	0	0	0
12	1	1	0	1	1	1
11	1	1	0	1	1	0
10	1	1	0	1	0	1
9	1	1	0	1	0	0
8	1	1	0	0	1	1
7	1	1	0	0	1	0
6	1	1	0	0	0	1
5	1	1	0	0	0	0
4	1	0	1	1	1	1
3	1	0	1	1	1	0
2	1	0	1	1	0	1
1	1	0	1	1	0	0
0	1	0	1	0	1	1
-1	1	0	1	0	1	0
-2	1	0	1	0	0	1
-3	1	0	1	0	0	0
-4	1	0	0	1	1	1
-5	1	0	0	1	1	0
-6	1	0	0	1	0	1
-7	1	0	0	1	0	0
-8	1	0	0	0	1	1
-9	1	0	0	0	1	0
-10	1	0	0	0	0	1
-11	1	0	0	0	0	0

The loudness characteristic is constant during the volume range from -12dB to -31 dB.

GV (dB)	V5	V4	V3	V2	V1	V0
-12	0	1	1	1	1	1
-13	0	1	1	1	1	0
-14	0	1	1	1	0	1
-15	0	1	1	1	0	0
-16	0	1	1	0	1	1
-17	0	1	1	0	1	0
-18	0	1	1	0	0	1
-19	0	1	1	0	0	0
-20	0	1	0	1	1	1
-21	0	1	0	1	1	0
-22	0	1	0	1	0	1
-23	0	1	0	1	0	0
-24	0	1	0	0	1	1
-25	0	1	0	0	1	0
-26	0	1	0	0	0	1
-27	0	1	0	0	0	0
-28	0	0	1	1	1	1
-29	0	0	1	1	1	0
-30	0	0	1	1	0	1
-31	0	0	1	1	0	0

The steps are repeated for range -28dB to -31dB.

GV(dB)	V5	V4	V3	V2	V1	V0
-28	0	0	1	0	1	1
-29	0	0	1	0	1	0
-30	0	0	1	0	0	1
-31	0	0	1	0	0	0
-28	0	0	0	1	1	1
-29	0	0	0	1	1	0
-30	0	0	0	1	0	1
-31	0	0	0	1	0	0
-28	0	0	0	0	1	1
-29	0	0	0	0	1	0
-30	0	0	0	0	0	1
-31	0	0	0	0	0	0

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The Volume 2 (Balance & Fader) Setting is shown below.

GV (dB)	FSR5 FSR5 FFL5 FFR5	FSR4 FSR4 FFL4 FFR4	FSR3 FSR3 FFL3 FFR3	FSR2 FSR2 FFL2 FFR2	FSR1 FSR1 FFL1 FFR1	FSR0 FSR0 FFL0 FFR0
0	1	1	1	1	1	1
-1	1	1	1	1	1	0
-2	1	1	1	1	0	1
-3	1	1	1	1	0	0
-4	1	1	1	0	1	1
-5	1	1	1	0	1	0
-6	1	1	1	0	0	1
-7	1	1	1	0	0	0
-8	1	1	0	1	1	1
-9	1	1	0	1	1	0
-10	1	1	0	1	0	1
-11	1	1	0	1	0	0
-12	1	1	0	0	1	1
-13	1	1	0	0	1	0
-14	1	1	0	0	0	1
-15	1	1	0	0	0	0
-16	1	0	1	1	1	1
-17	1	0	1	1	1	0
-18	1	0	1	1	0	1
-19	1	0	1	1	0	0
-20	1	0	1	0	1	1
-21	1	0	1	0	1	0
-22	1	0	1	0	0	1
-23	1	0	1	0	0	0
-24	1	0	0	1	1	1
-25	1	0	0	1	1	0
-26	1	0	0	1	0	1
-27	1	0	0	1	0	0
-28	1	0	0	0	1	1
-29	1	0	0	0	1	0
-30	1	0	0	0	0	1
-31	1	0	0	0	0	0
-32	0	1	1	1	1	1
-33	0	1	1	1	1	0
-34	0	1	1	1	0	1
-35	0	1	1	1	0	0

GV (dB)	FSR5 FSR5 FFL5 FFR5	FSR4 FSR4 FFL4 FFR4	FSR3 FSR3 FFL3 FFR3	FSR2 FSR2 FFL2 FFR2	FSR1 FSR1 FFL1 FFR1	FSR0 FSR0 FFL0 FFR0
-36	0	1	1	0	1	1
-37	0	1	1	0	1	0
-38	0	1	1	0	0	1
-39	0	1	1	0	0	0
-40	0	1	0	1	1	1
-41	0	1	0	1	1	0
-42	0	1	0	1	0	1
-43	0	1	0	1	0	0
-44	0	1	0	0	1	1
-45	0	1	0	0	1	0
-46	0	1	0	0	0	1
-47	0	1	0	0	0	0
-48	0	0	1	1	1	1
-49	0	0	1	1	1	0
-50	0	0	1	1	0	1
-51	0	0	1	1	0	0
-52	0	0	1	0	1	1
-53	0	0	1	0	1	0
-54	0	0	1	0	0	1
-55	0	0	1	0	0	0
MUTE	0	0	0	1	1	1
MUTE	0	0	0	1	1	0
MUTE	0	0	0	1	0	1
MUTE	0	0	0	1	0	0
MUTE	0	0	0	0	1	1
MUTE	0	0	0	0	1	0
MUTE	0	0	0	0	0	1
MUTE	0	0	0	0	0	0

Note: Only the subaddress changes, the data remains the same for a particular range.

Bass setting is shown below.

G_{BASS} (dB)	BAS4	BAS3	BAS2	BAS1	BAS0
+15.0	1	1	1	1	1
+13.5	1	1	1	1	0
+15.0	1	1	1	0	1
+13.5	1	1	1	0	0
+15.0	1	1	0	1	1
+13.5	1	1	0	1	0
+12.0	1	1	0	0	1
+10.5	1	1	0	0	0
+9.0	1	0	1	1	1
+7.5	1	0	1	1	0
+6.0	1	0	1	0	1
+4.5	1	0	1	0	0
+3.0	1	0	0	1	1
+1.5	1	0	0	1	0
0 (see note 1)	1	0	0	0	1
0 (see note 2)	1	0	0	0	0
-1.5	0	1	1	1	1
-3.0	0	1	1	1	0
-4.5	0	1	1	0	1
-6.0	0	1	1	0	0
-7.5	0	1	0	1	1
-9.0	0	1	0	1	0
-10.5	0	1	0	0	1
-12.0	0	1	0	0	0
-13.5	0	0	1	1	1
-15.0	0	0	1	1	0
-13.5	0	0	1	0	1
-15.0	0	0	1	0	0
(see note 3)	0	0	0	1	1
(see note 3)	0	0	0	1	0
(see note 3)	0	0	0	0	1
(see note 3 & 4)	0	0	0	0	0

Notes:
1. Recommended Data Word for step 0dB.
2. Result of 1.5dB boost and 1.5dB attenuation.
3. The last four bass control data words mute the bass response.
4. The last bass and treble control data words (00000) enable the external equalizer connection.

Treble setting is shown below.

G_{TREBLE} (dB)	TRE4	TRE3	TRE2	TRE1	TRE0
+12.0	1	1	1	1	1
+10.5	1	1	1	1	0
+12.0	1	1	1	0	1
+10.5	1	1	1	0	0
+12.0	1	1	0	1	1
+10.5	1	1	0	1	0
+12.0	1	1	0	0	1
+10.5	1	1	0	0	0
+9.0	1	0	1	1	1
+7.5	1	0	1	1	0
+6.0	1	0	1	0	1
+4.5	1	0	1	0	0
+3.0	1	0	0	1	1
+1.5	1	0	0	1	0
0 (see note 1)	1	0	0	0	1
0 (see note 2)	1	0	0	0	0
-1.5	0	1	1	1	1
-3.0	0	1	1	1	0
-4.5	0	1	1	0	1
-6.0	0	1	1	0	0
-7.5	0	1	0	1	1
-9.0	0	1	0	1	0
-10.5	0	1	0	0	1
-12.0	0	1	0	0	0
(see note 3)	0	0	1	1	1
(see note 3)	0	0	1	1	0
(see note 3)	0	0	1	0	1
(see note 3)	0	0	1	0	0
(see note 3)	0	0	0	1	1
(see note 3)	0	0	0	1	0
(see note 3)	0	0	0	0	1
(see note 3 & 4)	0	0	0	0	0

Notes:
1. Recommended Data Word for step 0dB.
2. Result of 1.5dB boost and 1.5dB attenuation.
3. The last eight treble control data words select the treble output.
4. The last bass and treble control data words (00000) enable the external equalizer connection.

MUTE

PT2318 provides three mute modes namely:
1. Zero Crossing Mode via the I^2C bus using 2 independent zero crossing detectors.
2. Fast Mute via Mute Pin
3. Fast Mute via I^2C Bus either by General Mute (GMU) or by Volume 2 Block Setting.

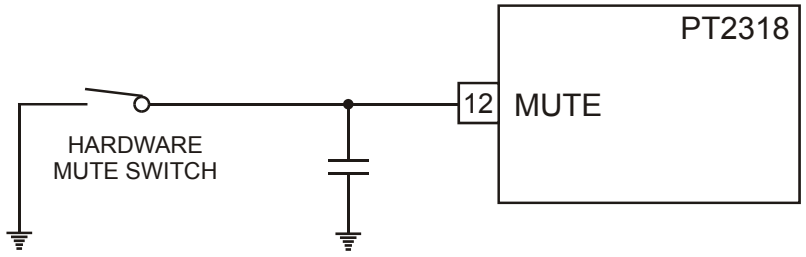
The following table shows the setting for the Zero Crossing Mode and the General Mute Mode

GMU	ZCM	Function
0	0	Direct MUTE off
0	1	MUTE off delayed until the next Zero Crossing
1	0	Direct MUTE
1	1	MUTE delayed until the next Zero Crossing

Notes:
1. GMU=General Mute Bit (Mute control for all outputs)
2. ZCM=Zero Crossing Mode Bit

The mute function is immediately performed if the ZCM="0". If ZCM="1", the mute is activated after changing the GMU bit. The actual mute switching is delayed until the next zero crossing of the audio frequency signal. The left and right audio channels are independent of each other, therefore, there are two built-in comparators controlling the independent mute switches. In order to avoid too much delay in mute switching when very low frequencies are processed, the maximum delay time is limited to a typical value of 100ms by an integrated timing circuit and an external capacitor. This timing circuit is triggered by the reception of a new data word for the switch function (including a GMU bit). After an external capacitor is discharged and charged, the muting switch follows the GMU bit if there was no zero crossing detected during that particular time.

Externally controlling the mute function is possible. If the mute pin is set to Ground, all outputs are muted immediately (this is the hardware mute.). Please refer to the diagram below.

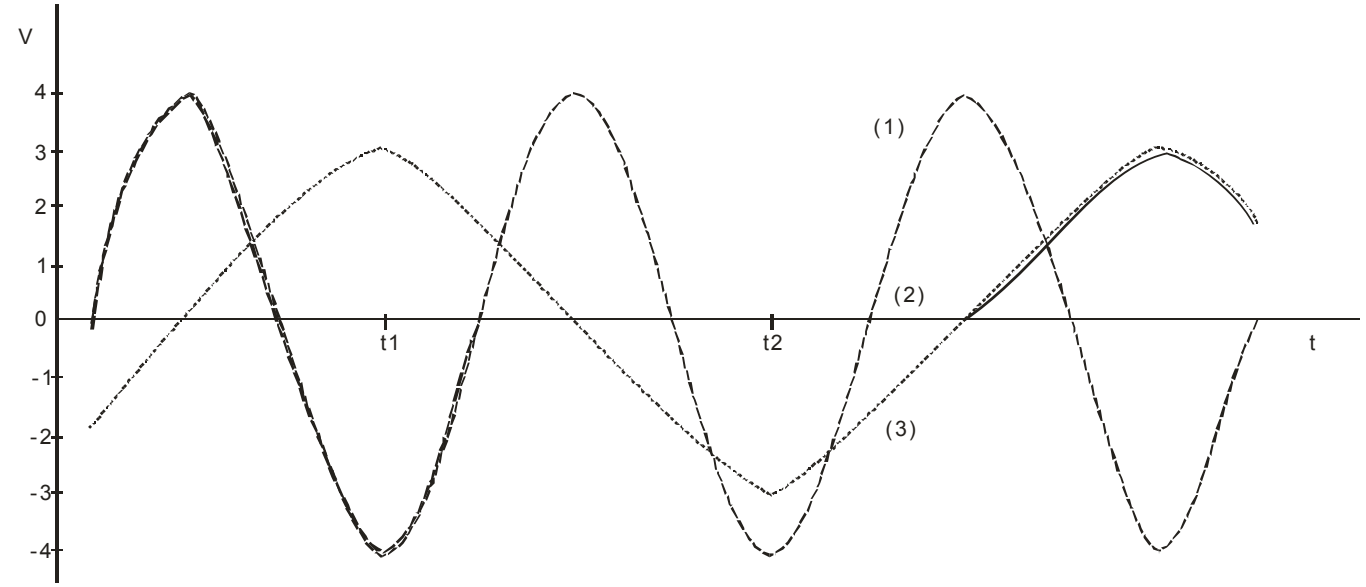


The mute request overwrites all mute controls via the I^2C bus for the time the pin is held at "LOW" level.

The hardware mute function is ideal for Radio Data System applications. The zero crossing mute avoids modulation plops. This feature is advantageous when the changing presets and/or sources.

INPUT SIGNAL SELECTION VIA ZERO CROSS MUTE MODE

A selection from the Input A (IN_L1) to Input B (IN_L2) Left Channels produces a modulation click at the time of the switching. This will depend on the difference between the signal values. Please refer to the diagram below for the zero cross function (L Channel Only)



Notes:
1. (1)=Output
2. (2)=Input 2 (IN_L2)
3. (3)=Input 1 (IN_L1)

At t1, the maximum different between signals is 7Vp-p. At this point, a loud click can be heard. Using the zero cross detector, no modulation click is audible.

LOUDNESS FUNCTION

The Loudness Function is used in combination with Volume 1 Control Block and may be enabled or disabled via the I²C Bus Control. Please refer to the table below for Loudness Function setting.

Loudness Function	LOFF
Loudness On	0
Loudness Off	1

Note: LOFF=Loudness Function Control Bit

ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Conditions	Min.	Max.	Unit
Supply voltage	Vcc		0	10	V
Operating temperature	Topr		-40	+85	℃
Storage temperature	Tstg		-65	+150	℃
Voltage at each pin (when Pin 2 as GND)	Vpin		0	Vcc	V

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, Vcc=8.5V, Rs=600Ω, RL=10kΩ, CL=2.5nF, AC Coupled, f=1KHz, Ta=25℃, Gain Control: Gv=0dB, Bass=Linear, Treble=Linear, Fader=Off, Balance in Mid Position Loudness Off)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	-	7.5	8.5	9.5	V
Supply current	Ic	-	-	26	32	mA
Internal DC voltage (Input & Output)	VDC	-	3.75	4.0	4.25	V
Max. voltage gain	GVmax	Rs=0Ω, RL=∞	19	20	21	dB
Input sensitivity	Vi (rms)	VO-2000mV, Gv=20dB	-	200	-	mV
Roll-off frequency	fro	CKIN=220nF, CKVL=220nF, Zi=Zi(min) Low frequency (-1dB)	60	-	-	Hz
		CKIN=220nF, CKVL=220nF, Zi=Zi(min) Low frequency (-3dB)	30	-	-	Hz
		CKIN=220nF, CKVL=220nF, Zi=Zi(min) High frequency (-1dB)	20000	-	-	Hz
		CKIN=470nF, CKVL=220nF, Zi=Zi(typ) Low frequency (-3dB)	17	-	-	Hz
Channel separation	αcs	Vi=2V, 250Hz to 10KHz	90	96	-	dB
Total harmonic distortion	THD	20Hz to 12.5KHz, Vi=100mV, Gv=20dB	-	0.07	-	%
		20Hz to 12.5KHz, Vi=1V, Gv=0dB	-	0.05	-	%
		20Hz to 12.5KHz, Vi=2V, Gv=0dB	-	0.2	-	%
		20Hz to 12.5KHz, Vi=2V, Gv=-10dB	-	0.03	-	%
Ripple rejection	RR	Vr(rms)<200mV, f=100Hz	-	62	-	dB
Signal to noise ratio	S/N	Vo=2.0V, Gv=0dB	-	99	-	dB
		Vo=2.0V, Gv=12dB	-	91	-	dB
		Vo=2.0V, Gv=12dB	-	83	-	dB
Crosstalk	αct	Between bus input & signal outputs	-	110	-	dB
Input impedance	Zi	-	22	30	40	KΩ

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input isolation (One selected source to any other input)	α s	f=1KHz	-	104	-	dB
		f=12.5KHz	-	95	-	dB
Max. input voltage (RMS value)	Vi (rms)	THD<0.5%, Vcc=8.5V	-	2.7	-	V
		THD<0.5%, Vcc=7.5V	-	2.3	-	V
Output impedance	Zo		-	130	220	Ω
Output load resistance	RL		10	-	-	KΩ
Voltage gain (Source selector)	Gv		-	0	-	dB
Control Section (Source Selector not connected, Source Resistance=600Ω)						
Input impedance	Zi	Volume input	70	150	200	KΩ
		Loudness input	20	30	40	KΩ
Output impedance	Zo		-	130	220	Ω
Output load resistance	RL		2	-	-	KΩ
Max. input voltage	Vi(rms)	THD<0.5%	-	2.4	-	V
Noise output voltage	Vno	Gv=20dB	-	120	220	μV
		Gv=0dB	-	25	50	μV
		Gv=-66dB	-	13	22	μV
		MUTE position	-	13	-	μV
Total continuous control range	CRtot		-	106	-	dB
Recommended control range			-	86	-	dB
Step resolution	Gstep	Step range	-	1	-	dB
		Step error between any adjoining step	-	-	1.0	dB
Attenuation set error	ΔGa	Gv=+20 to -50dB	-	-	2	dB
		Gv=-51 to -66dB	-	-	3	dB
Gain tracking error	ΔGt	Gv=+20 to -50dB	-	-	2	dB
Mute attenuation	MUTEatt		95	100	-	dB
Volume 1 Control + Loudness						
Continuous volume control range	CRvol		-	51	-	dB
Voltage gain	Gv		-31	-	+20	dB
Step resolution	Gstep		-	1	-	dB
Max. loudness	LBmax	f=40Hz	-	15	-	dB
		f=10KHz	-	4	-	dB

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Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Bass Control						
Max. boost (Bass control)	Gbass	f=40Hz	+14	+15	+16	dB
Max. attenuation		f=40Hz	-14	-15	-16	dB
Step resolution (Toggle switching)	Gstep	f=40Hz	-	1.5	-	dB
Step error between any adjoining step	Gstep	f=40Hz	-	-	1	dB
Treble Control						
Max. boost	Gtreble	f=15KHz	+11	+12	+13	dB
Max. attenuation	Gtreble	f=15KHz	-11	-12	-13	dB
Max. boost 2	Gtreble	f>15KHz	-	-	15	dB
Step resolution (Toggle switching)	Gstep	f=15KHz	-	1.5	-	dB
Step error between any adjoining step	Gstep	f=15KHz	-	-	1	dB
Volume 2 + Balance + Fader Controls						
Continuous attenuation (Fader & volume control)	CR		-	55	-	dB
Step resolution	Gstep		-	1	2	dB
Attenuation set error	Gstep		-	-	2	dB
Hardware Mute						
Mute: Active						
Input level	VSWLOW		-	0.8	-	V
Zero Crossing Mute						
Discharger current	Id		-	0.6	-	µA
Charge current	Ich		-300	-150	-	µA
Delay switch level	VSWDEL		-	1.5	-	V
Delay time	td	Cm=10nF	-	100	-	ms
Window for audio signal zero crossing detection	Vwind		-	50	-	mV
Muting at Power Supply Drop						
Supply drop for MUTE active	Vccdrop		6.9	7	-	V
I^2C Bus Control						
High level input voltage	VIH		3.4	-	9.5	V
Low level input voltage	VIL		-0.3	-	+1.5	V

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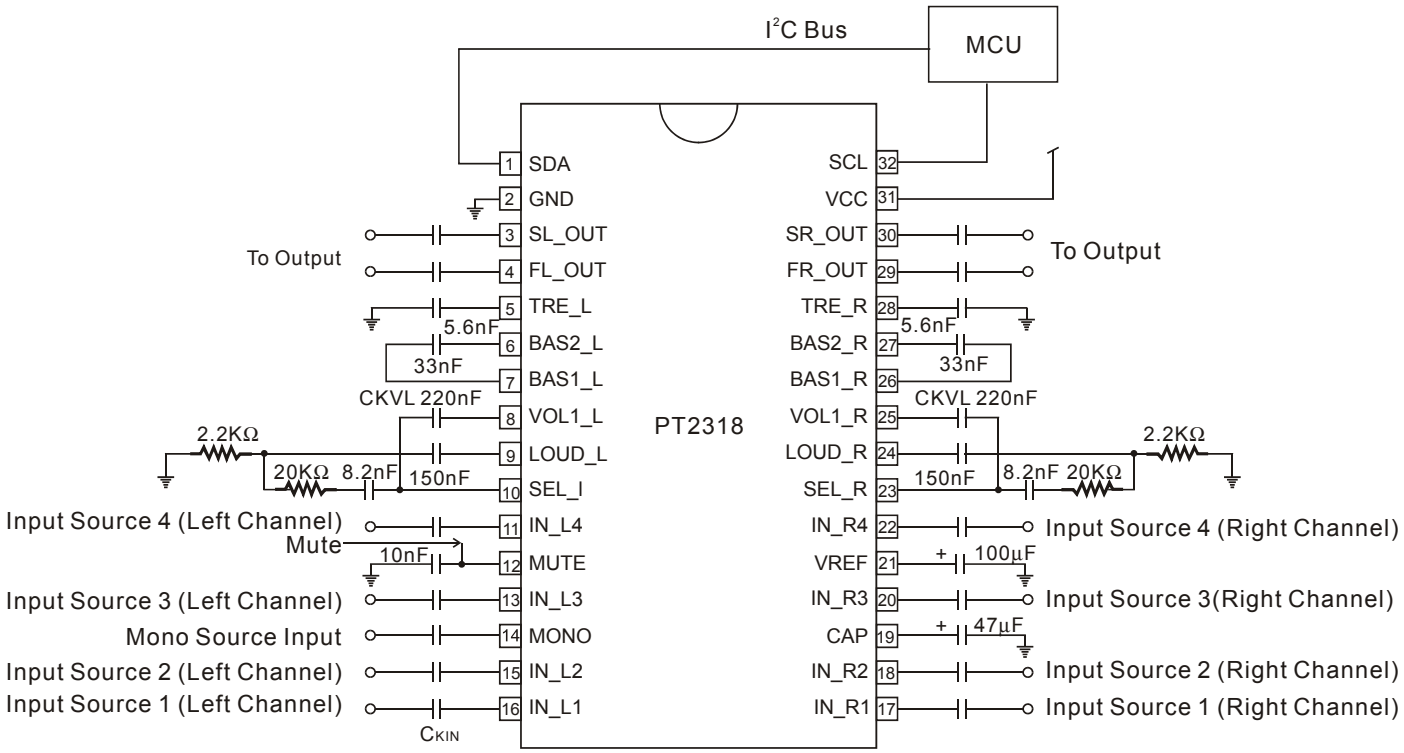
APPLICATION CIRCUIT



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ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT2318-S	32 Pins, SOP, 300mil	PT2318-S
PT2318	32 Pins, DIP, 600mil	PT2318

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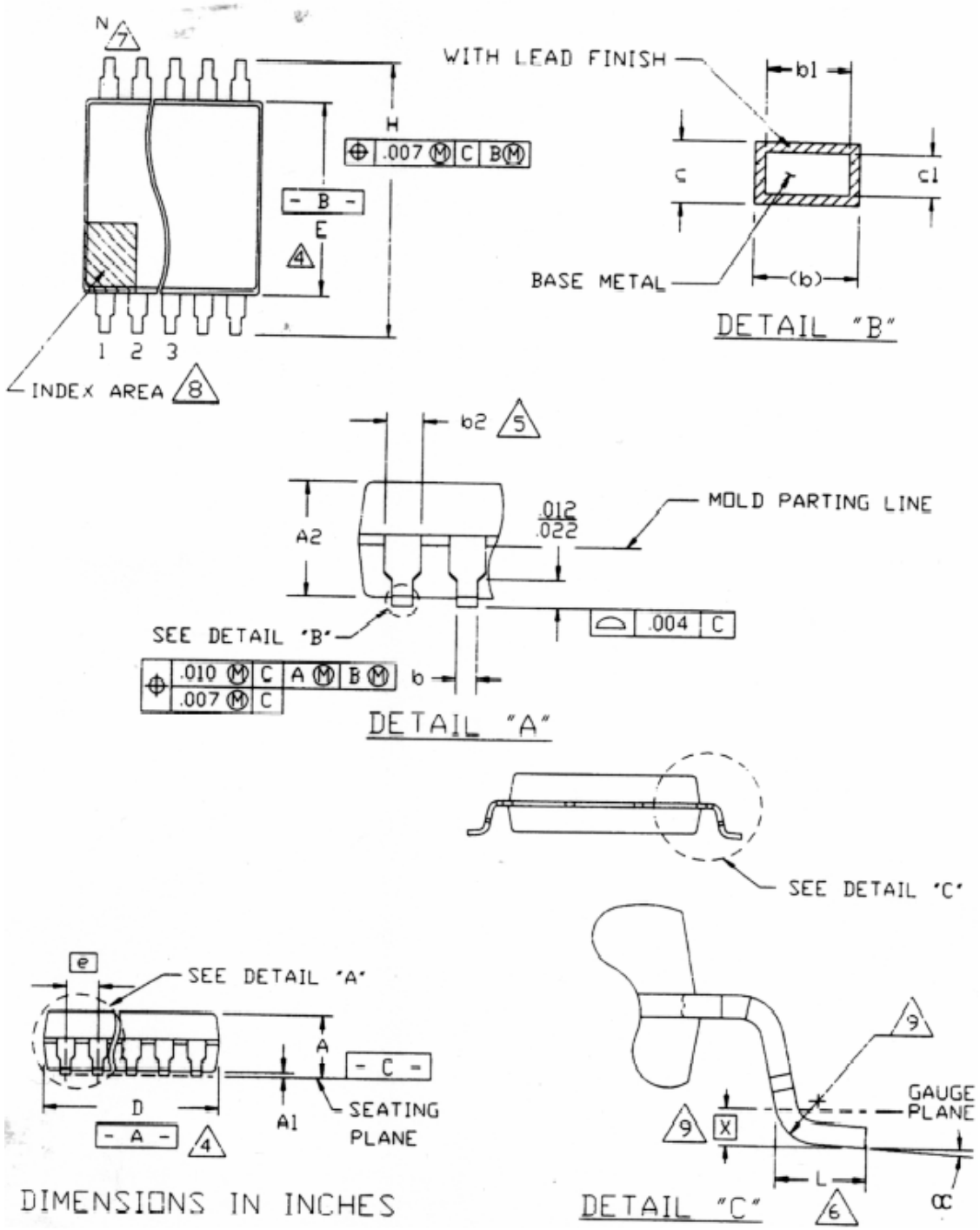
PACKAGE INFORMATION

32 PINS, SOP, 300MIL



Symbols	Min.	Nom.	Max.
A	-	-	0.104
A1	0.004		0.30
A2	0.082	0.088	0.094
b	0.014	0.016	0.020
b1	0.014	0.016	0.018
b2	0.026	0.028	0.032
c	0.007	0.008	0.0125
c1	0.007	0.008	0.010
D	0.812	0.818	0.824
E	0.292	0.296	0.299
e	0.050 BSC.		
H	0.405	0.412	0.419
L	0.021	0.031	0.041
α	0°	4°	8°

Notes:
1. Dimensioning and tolerancing per ANSI Y14.5-1982.
2. Dimension D does not include mold flash, protrusions or gate burrs. Mold Flash, protrusion or gate burrs shall not exceed 0.15mm (0.006 in) per side.
3. Dimension E does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. The chamfer on the body is optional. It is not present, a visual index feature must be located within the crosshatched area.
5. L is the length of the terminal for soldering to a substrate.
6. The lead width B as measured 0.36 mm (0.014 in) or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.24 in)
7. Controlling dimension: MILLIMETER.
8. N=Number of terminal position (N=32)
9. Refer to JEDEC MO-119 variation AC.

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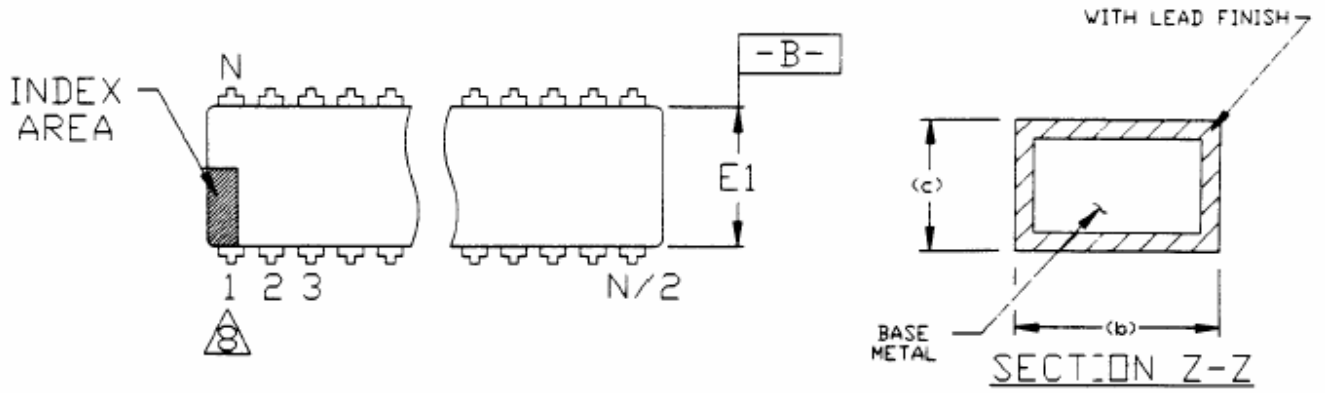
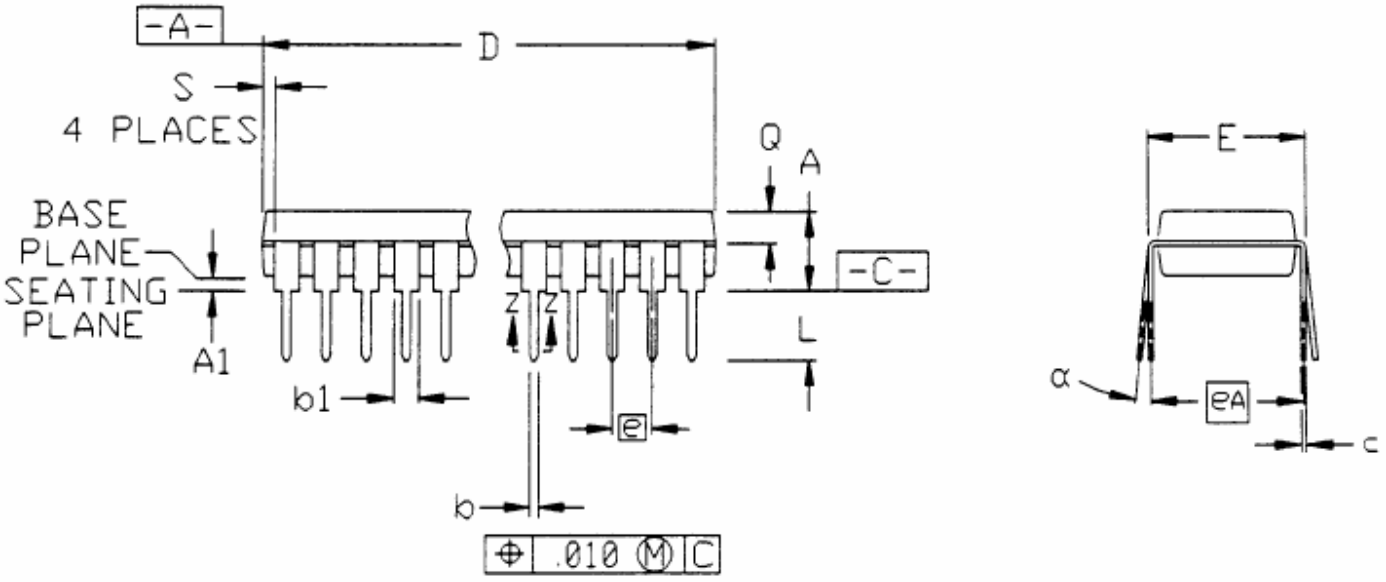
32 PINS, DIP, 600MIL





Symbol	Min.	Nom.	Max.
A	0.170	-	0.200
A1	0.015	-	0.050
B	0.016	-	0.022
B1	0.045	-	0.067
C	0.009	-	0.015
D	1.600	-	1.670
E	0.600	-	0.625
E1	0.530	-	0.560
e1	0.100 BSC.		
eA	0.600 BSC.		
L	0.120	-	0.150
α	0°	-	15°
Q	0.065	-	0.080
S	0.065	-	0.087

Notes:
1. Refer to applicable symbol list.
2. Dimension and tolerancing per ANSI Y14.5-1982
3. αapplies to spread leads prior to installation.
4. N=Number of terminal position (N=32)
5. D & E1 does not include mold flash. Allowable flash is 0.010 per side.
6. Outlines on which the seating plane is coincident with the base plane (A1=0) terminal lead standoffs are not required, and B1 may equal B along any part of the lead above the seating/base plane.
7. Pin 1 identifier must be located in this area.
8. Controlling dimension: INCH.
9. Refer to JEDEC MO-015 variation AP.

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