普誠科技股份有限公司
Princeton Technology Corp.
Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

DESCRIPTION

PT2319 is an audio processor IC specially designed for high fidelity audio applications utilizing advanced CMOS processing technology. Included in the IC are 5 stereo input signal ports, super bass and bass/treble controls, volume control, balance/fader controls and muting.

The internal circuits of PT2319 have undergone meticulous adjustment to achieve the finest possible audio quality. Extremely low signal distortion, strong signal driving ability, and clear dynamic peak and level sound quality at any volume level distinguish PT2319 from other audio processors. PT2319 is the ideal solution for audio systems catering to the most demanding audiophiles.

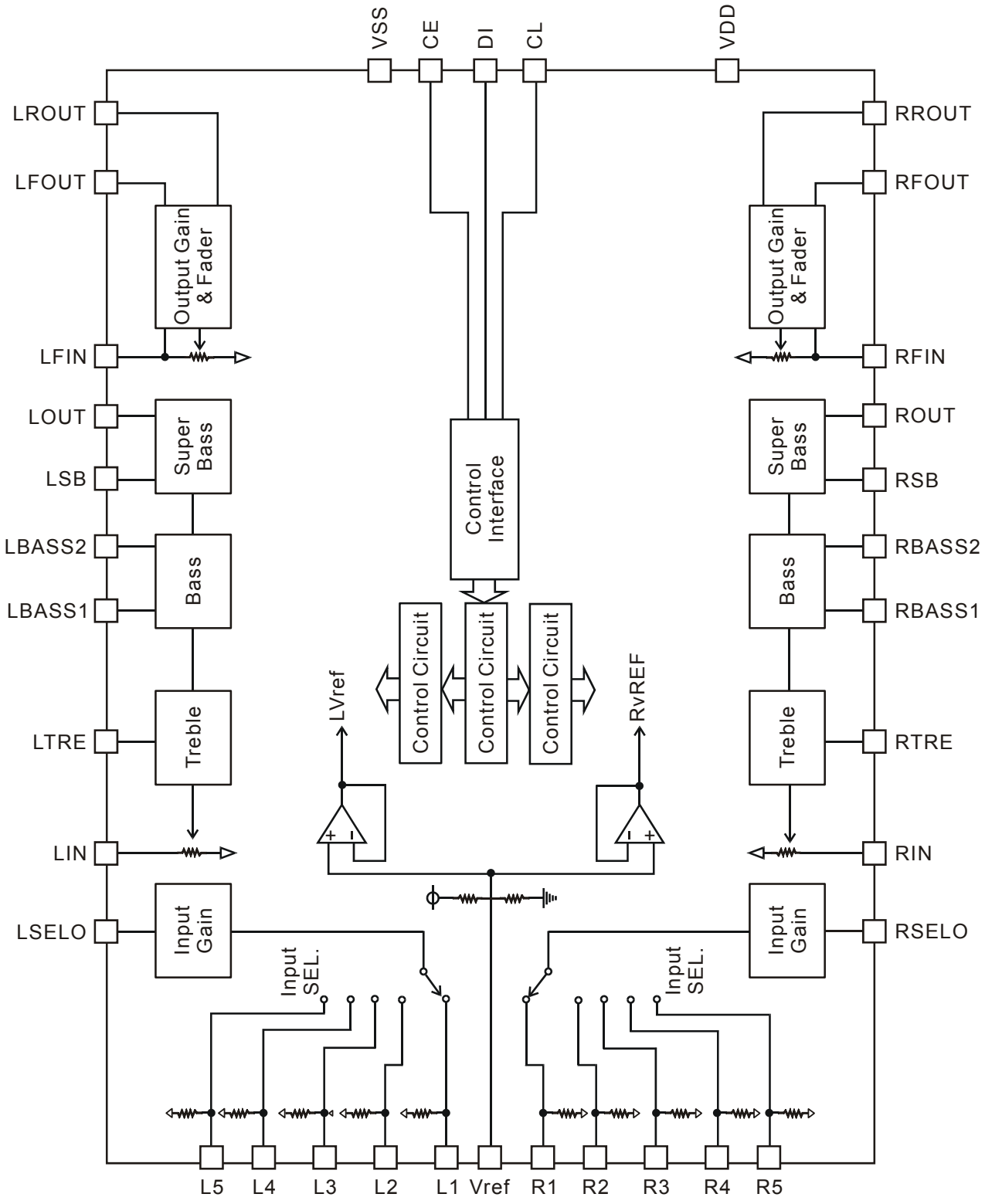
FEATURES

- CMOS process technology
- Low level output signal loss: Typ.=0.003% at VOUT=1Vrms
- High level output driving ability: load impedance as low as 600Ω
- Large output amplitude
- Five stereo input signal ports
- Volume, balance and fader controls
- Super bass, bass and treble controls
- Select Out supports addition of externals circuits
- Built-in automatic power-on reset
- 3-wire digital control interface
- 36-pin SSOP packaging

APPLICATIONS

- High fidelity audio systems
- Car audio systems

BLOCK DIAGRAM



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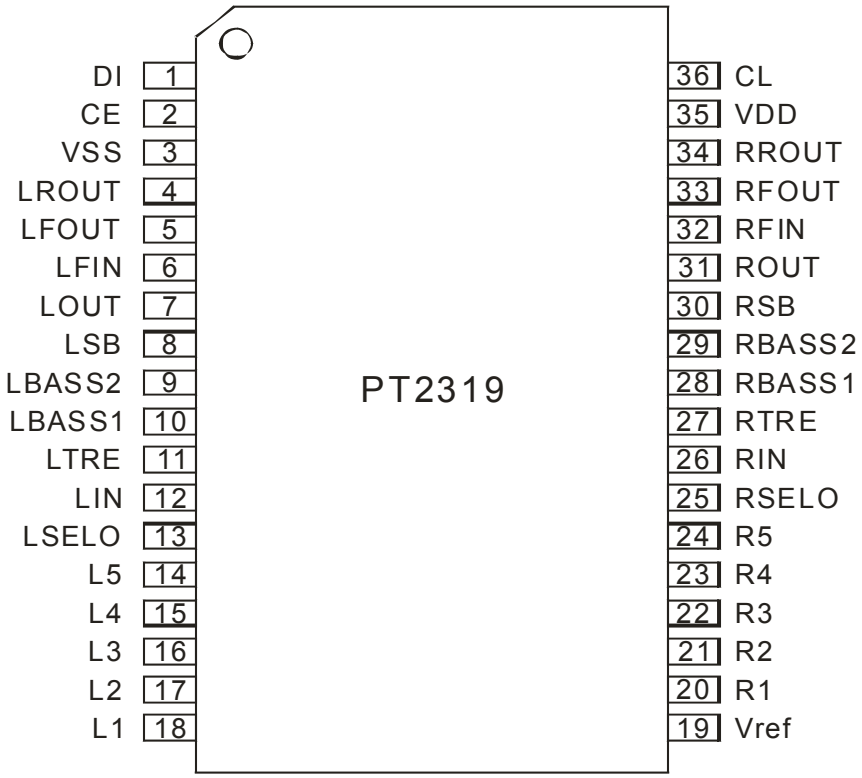
PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Pin Name	Function
1	DI	3-wire serial data pin
2	CE	3-wire chip enable pin
3	VSS	Ground pin
4	LROUT	Left rear channel output pin
5	LFOUT	Left front channel output pin
7	LOUT	Left super bass output and external component connection pin
8	LSB	Left super bass external component connection pin
9	LBASS2	Left bass filter external component connection pin 2
10	LBASS1	Left bass filter external component connection pin 1
11	LTRE	Capacitor connection pin for configuring treble filter (left)
13	LSELO	Input selector output pin (left)
14	L5	Input signal pin 5 (left)
15	L4	Input signal pin 4 (left)
16	L3	Input signal pin 3 (left)
17	L2	Input signal pin 2 (left)
18	L1	Input signal pin 1 (left)
19	Vref	Reference voltage bypass capacitor
20	R1	Input signal pin 1 (right)
21	R2	Input signal pin 2 (right)
22	R3	Input signal pin 3 (right)
23	R4	Input signal pin 4 (right)
24	R5	Input signal pin 5 (right)
25	RSELO	Input selector output pin (right)
27	RTRE	Capacitor connection pin for configuring treble filter (right)
28	RBASS1	Right bass filter external component connection pin 1
29	RBASS2	Right bass filter external component connection pin 2
30	RSB	Right super bass external component connection pin
31	ROUT	Right super bass output and external component connection pin
33	RFOUT	Right front channel output pin
34	RROUT	Right rear channel output pin
35	VDD	Power supply pin
36	CL	3-wire serial clock input pins

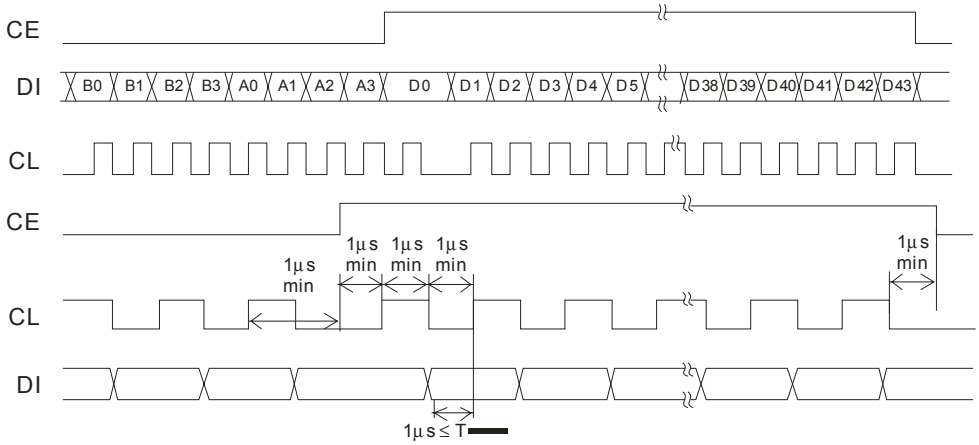
FUNCTION DESCRIPTION

CONTROLLER FUNCTIONS

Function	Scope	Range	Step	Other
Volume Control	81-step gain control	0dB to –79dB Step 81 is -∞	Each step 1dB	Left and right channel gain can be adjusted independently as a balance control.
Output and Fader	Total of 16 steps	0dB to -60dB Step 16 is -∞	0dB to -20dB: 2dB steps -20dB to -25dB: 5dB steps -25dB to -45dB: 10dB steps Then –60dB and -∞	Can select attenuation for either the front or rear channels.
Bass control	Total 15 steps	±11.9dB	Each step 1.9dB	
Treble control	Total 15 steps	±11.9dB	Each step 1.9dB	
Super bass	Total 11 steps	0dB to +20dB	Each step 2dB	Super bass gain boost only
Input selector gain	Total 16 steps	0dB to +18.75dB	Each step 1.25dB	
Output gain	Total 3 steps	0dB, +6.5dB, +8.5dB		
Input signal selector	Total 5 inputs			Stereo inputs

3-WIRE SERIAL BUS INTERFACE

To control any of PT2319's functions, it is necessary to pass the microprocessor control signals through the CE, DI, and CL 3-wire interface. The basic timing sequence of the control codes is shown in the diagram below.



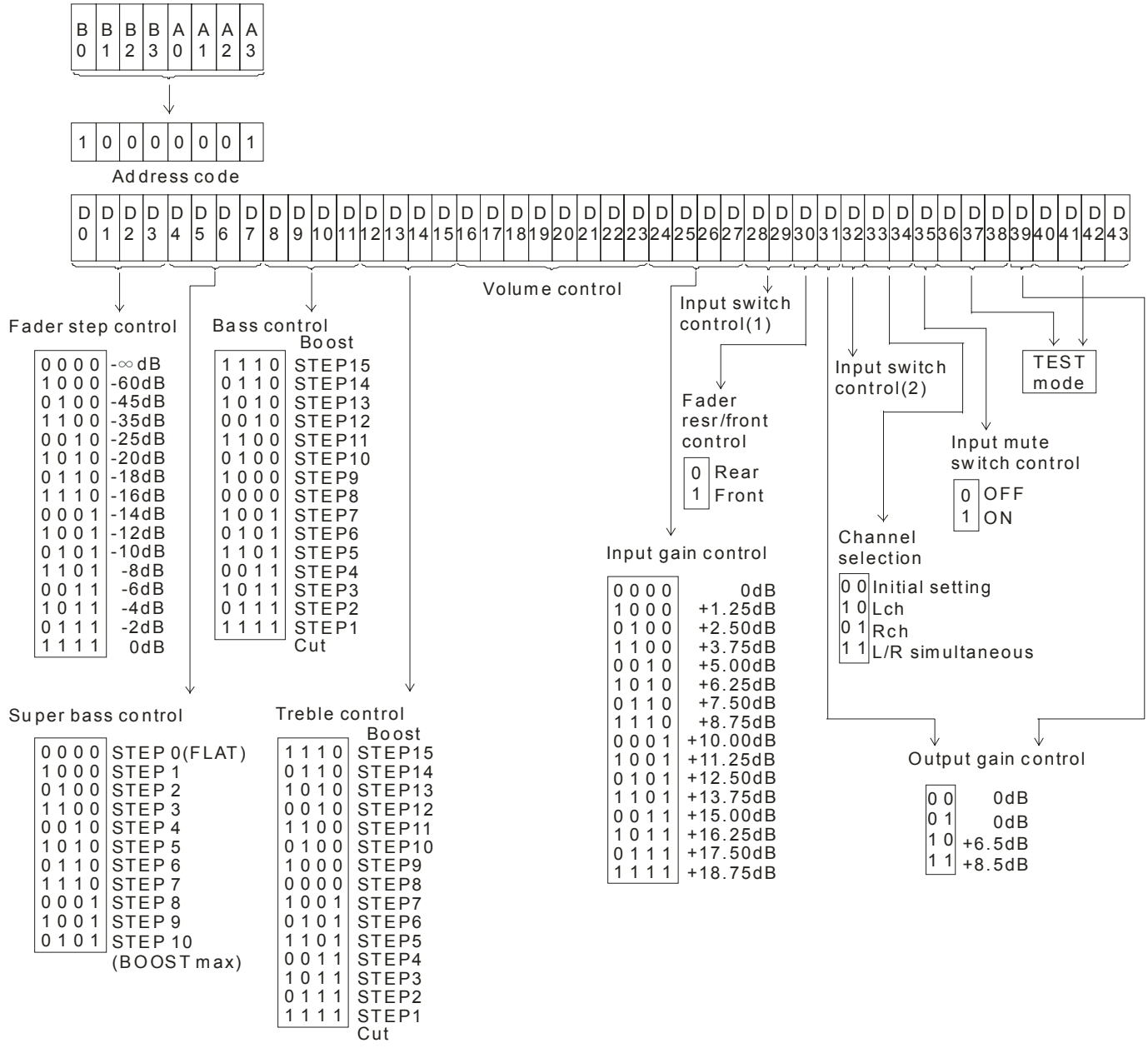
INTERFACE PROTOCOL

The 52-bit control code for PT2319 is composed of an 8-bit address code and a 44-bit data code for a total control code length of 52 bits.

CONTROL CODE DEFINITIONS

Function Name	Application	Register Location	Notes
Fader	Adjust fader gain	D0 ~ D3	
Super Bass	Super bass boost	D4 ~ D7	Only boost
Bass	Bass adjustment	D8 ~ D11	
Treble	Treble adjustment	D12 ~ D15	
Volume	Main volume control	D16 ~ D23	Can independently adjust left and right volumes
Input Gain	Input selector gain	D24 ~ D27	
Input Selector	Input selector	D28, D29, D32	
Fader Front/Rear Sel.	Fader channel selector	D30	
Output Gain	Output gain select	D31, D39	
Balance	Left/right channel select	D33, D34	Operates in conjunction with volume
Input Mute	For muting	D35	
Test Mode	For factory testing	D36 ~ D38, D40 ~ D43	Send all zeroes under normal operation

CONTROL CODE BIT DIAGRAM



VOLUME CONTROL CODE DEFINITIONS

D16	D17	D18	D19	D20	D21	D22	D23	Operation
0	0	1	0	0	1	0	1	0dB
1	1	0	0	0	1	0	1	-1dB
0	1	0	0	0	1	0	1	-2dB
1	0	0	0	0	1	0	1	-3dB
0	0	1	1	1	0	0	1	-4dB
1	1	0	1	1	0	0	1	-5dB
0	1	0	1	1	0	0	1	-6dB
1	0	0	1	1	0	0	1	-7dB
0	0	1	0	1	0	0	1	-8dB
1	1	0	0	1	0	0	1	-9dB
0	1	0	0	1	0	0	1	-10dB
1	0	0	0	1	0	0	1	-11dB
0	0	1	1	0	0	0	1	-12dB
1	1	0	1	0	0	0	1	-13dB
0	1	0	1	0	0	0	1	-14dB
1	0	0	1	0	0	0	1	-15dB
0	0	1	0	0	0	0	1	-16dB
1	1	0	0	0	0	0	1	-17dB
0	1	0	0	0	0	0	1	-18dB
1	0	0	0	0	0	0	1	-19dB
0	0	1	1	1	1	1	0	-20dB
1	1	0	1	1	1	1	0	-21dB
0	1	0	1	1	1	1	0	-22dB
1	0	0	1	1	1	1	0	-23dB
0	0	1	0	1	1	1	0	-24dB
1	1	0	0	1	1	1	0	-25dB
0	1	0	0	1	1	1	0	-26dB
1	0	0	0	1	1	1	0	-27dB
0	0	1	1	0	1	1	0	-28dB
1	1	0	1	0	1	1	0	-29dB
0	1	0	1	0	1	1	0	-30dB
1	0	0	1	0	1	1	0	-31dB
0	0	1	0	0	1	1	0	-32dB
1	1	0	0	0	1	1	0	-33dB
0	1	0	0	0	1	1	0	-34dB
1	0	0	0	0	1	1	0	-35dB
0	0	1	1	1	0	1	0	-36dB
1	1	0	1	1	0	1	0	-37dB
0	1	0	1	1	0	1	0	-38dB
1	0	0	1	1	0	1	0	-39dB
0	0	1	0	1	0	1	0	-40dB
1	1	0	0	1	0	1	0	-41dB

D16	D17	D18	D19	D20	D21	D22	D23	Operation
0	1	0	0	1	0	1	0	-42dB
1	0	0	0	1	0	1	0	-43dB
0	0	1	1	0	0	1	0	-44dB
1	1	0	1	0	0	1	0	-45dB
0	1	0	1	0	0	1	0	-46dB
1	0	0	1	0	0	1	0	-47dB
0	0	1	0	0	0	1	0	-48dB
1	1	0	0	0	0	1	0	-49dB
0	1	0	0	0	0	1	0	-50dB
1	0	0	0	0	0	1	0	-51dB
0	0	1	1	1	1	0	0	-52dB
1	1	0	1	1	1	0	0	-53dB
0	1	0	1	1	1	0	0	-54dB
1	0	0	1	1	1	0	0	-55dB
0	0	1	0	1	1	0	0	-56dB
1	1	0	0	1	1	0	0	-57dB
0	1	0	0	1	1	0	0	-58dB
1	0	0	0	1	1	0	0	-59dB
0	0	1	1	0	1	0	0	-60dB
1	1	0	1	0	1	0	0	-61dB
0	1	0	1	0	1	0	0	-62dB
1	0	0	1	0	1	0	0	-63dB
0	0	1	0	0	1	0	0	-64dB
1	1	0	0	0	1	0	0	-65dB
0	1	0	0	0	1	0	0	-66dB
1	0	0	0	0	1	0	0	-67dB
0	0	1	1	1	0	0	0	-68dB
1	1	0	1	1	0	0	0	-69dB
0	1	0	1	1	0	0	0	-70dB
1	0	0	1	1	0	0	0	-71dB
0	0	1	0	1	0	0	0	-72dB
1	1	0	0	1	0	0	0	-73dB
0	1	0	0	1	0	0	0	-74dB
1	0	0	0	1	0	0	0	-75dB
0	0	1	1	0	0	0	0	-76dB
1	1	0	1	0	0	0	0	-77dB
0	1	0	1	0	0	0	0	-78dB
1	0	0	1	0	0	0	0	-79dB
0	0	0	0	0	0	0	0	-∞dB

INPUT SELECTOR DEFINITIONS

D28	D29	D32	Operation
0	0	1	L1 (R1) ON
1	0	1	L2 (R2) ON
0	1	1	L3 (R3) ON
1	1	1	L4 (R4) ON
0	0	0	L5 (R5) ON

IMPORTANT USER NOTES

SOFTWARE PROGRAMMING NOTES

Notes:

1. Internal registers are not in a set condition when the IC is powered on. To ensure that unusual noise will not be output, it is suggested that an external muting circuit is added before the control codes are sent.
2. After the IC has been powered on, send the IC a “clear register” code (to clear the register: D33 = D34 = 0) followed by initialization values for each register in order.
3. PT2319 control codes constitute a 52-bit signal. Each time a control code is sent, all data in the registry must be written into. When it is necessary to access only one function (for example, volume control only), it is allowed to change only the corresponding register data (in this example, D16 to D23) while the remaining registers are sent original unchanged data.

CIRCUIT LAYOUT NOTES

Notes:

1. To ensure that the 3-wire bus line signals (DI, CL, CE) do not interfere with the audio signals, when designing the circuit layout: 1) place the bus line at a sufficient distance from the audio path, and 2) the bus line and audio path should not be parallel. In addition to this, use a shielded ground pane or use a shielded cable to deliver signals to the interface.
2. To minimize interference between different voltage levels, please ensure that analog and digital grounds are separate. Analog grounds such as PT2319 GND and output terminal grounds should be connected together. The display shield, MCU, key scanning signal and remote control receiver decoder should be connected to a separate ground path. Finally, connect the two grounds at the power supply GND point.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Min.	Max.	Unit
Supply voltage	Vcc		0	11	V
Max. input voltage	VIMAX	CL,DI,CE	-0.3	11	V
		Other than CL,DI,CE	Vss - 0.3	VDD + 0.3	
Operating temperature	Topr	-	-40	+85	℃
Storage temperature	Tstg	-	-65	+150	℃

ELECTRICAL CHARACTERISTICS

(Vcc=9V, Rs=600Ω, RL=10KΩ, f=1KHz, Ta=25℃, Volume, treble and bass=0dB)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Supply voltage	Vcc			5	9	10	V
Supply current	Ic	VDD=5V, No Load		-	11	16	mA
		VDD=9V, No Load		-	15	20	
Total harmonic distortion	THD	Input Selector	Vi=1Vrms	-	0.003	0.01	%
			Vi=0.2Vrms	-	0.005	0.01	
		Volume Control	Vi=1Vrms	-	0.003	0.01	
			Vi=0.2Vrms	-	0.005	0.01	
		Fader	Vi=1Vrms	-	0.003	0.01	
			Vi=0.2Vrms	-	0.005	0.01	
Left and Right channel separation	CTLR	-		100	110	120	dB
Input selector crosstalk	CTIN	-		-	90	95	dB
Noise output	Noise	A-weighted		-	8	12	μV
Signal to noise ratio	S/N	A-weighted		98	100	-	dB
Mute level	Mute	Vin=1Vrms			100	-	dB
Ripple reduction	PSRR	F=100Hz, Vr=0.1V		60	65	-	dB
		F=1KHz, Vr=0.1V		80	85	-	
Input resistance	RIN	Select Input		35	50	65	KΩ
		Volume Control, Fader Input		30	40	50	
Output resistance	ROUT	Select Output, Volume Output, Fader Output		-	15	-	Ω
Recommended lowest impedance load	RLOAD	-		600	-	-	Ω
Maximum output voltage	VOMAX	THD=1%		2.7	2.9	3.0	Vrms
Slew rate	Slew Rate	-		-	4	-	V/μs
Audio signal Bandwidth	ABW	-3dB, HF		-	550	-	KHz
3-Wire Serial Bus Interface							
Input high level	VIH	CL, CE, DI		3.0	-	VDD	V
Input low level	VIL	CL, CE, DI		Vss	-	1.0	V
Pulse width	Tw	CL		1	-	-	μs
Settle time	Tsetup	CL, CE, DI		1	-	-	μs
Hold time	Thold	CL, CE, DI		1	-	-	μs
Input clock	Tclk	CL, CE, DI		-	-	500	KHz

GAIN ADJUSTMENT SCOPE

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Super Bass Control						
Maximum boost	Gsbass	-	-	+20	-	dB
Step adjustment	Gsbstep	-	-	2	-	
Bass Control						
Maximum boost	Gbass	-	+9	+11.9	+14	dB
Maximum attenuation	Gbass	-	-9	-11.9	-14	
Step adjustment	Gbstep	-	1	1.7	3	
Treble Control						
Maximum boost	Gtreble	-	+9	+11.9	+14	dB
Maximum attenuation	Gtreble	-	-9	-11.9	-14	
Step adjustment	Gtstep	-	-	1.7	-	
Input Gain Control						
Minimum gain	INgain	Step 0	-	0	-	dB
Maximum gain	INgain	Step 15	-	+18.75	-	
Step adjustment	INstep		-	+1.25	-	
Volume Control						
Minimum attenuation	VOLgain	Step 80	-	0	-	dB
Maximum attenuation	VOLgain	Step 1	-	-79	-	
		Step 0	-	-∞	-	
Step adjustment	VOLstep	-	-	1	-	
Fader Attenuator						
Minimum attenuation	FADgain	Step 15	-	0	-	dB
Maximum attenuation	FADgain	Step 1	-	-60	-	
		Step 0	-	-∞	-	
Step adjustment	FADstep	0 ~ -20dB	-	2	-	dB
		-20 ~ -25dB	-	5	-	
		-25 ~ -45dB	-	10	-	
		-45 ~ -60dB	-	15	-	
Output Gain						
Minimum gain	OUTgain	Step 0	-	0	-	dB
Step adjustment	OUTstep	Step 1	-	0	-	
		Step 2	-	+6.5	-	
		Step 3	-	+8.5	-	

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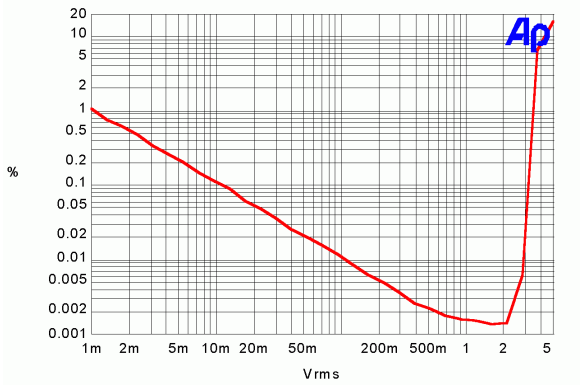
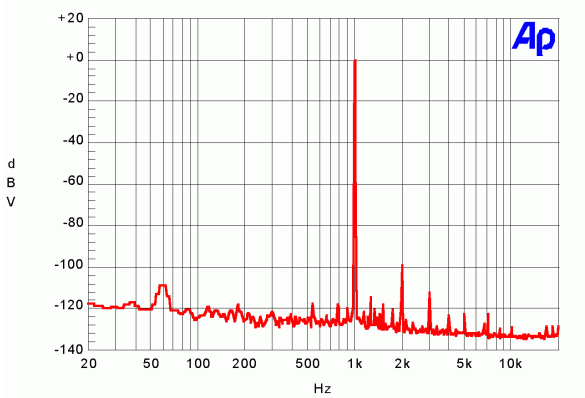
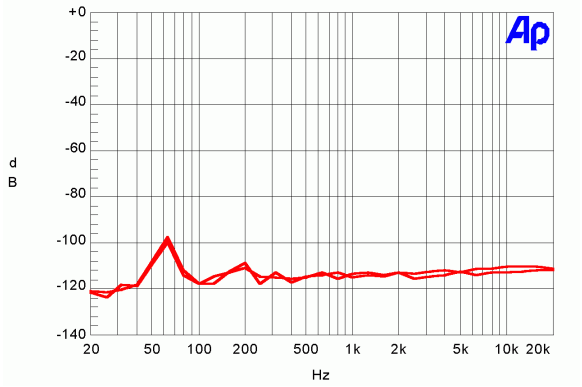
ELECTRICAL CHARACTERISTIC DIAGRAMS



Total Harmonic Distortion and Amplitude

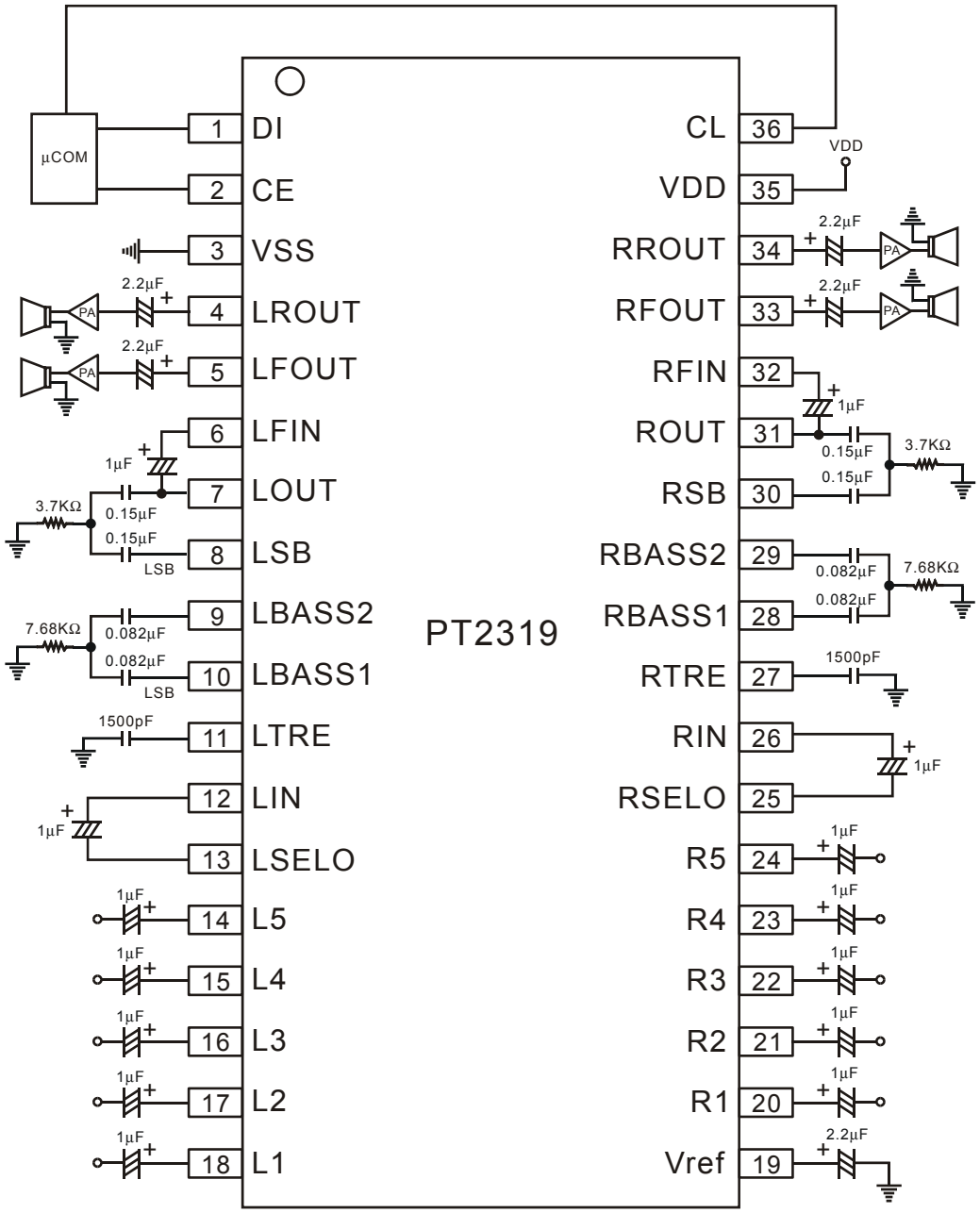


1Vrms Output FFT Analysis



Left and Right Channel Crosstalk

APPLICATION CIRCUIT



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ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT2319	36 Pins, SSOP, 300mil	PT2319

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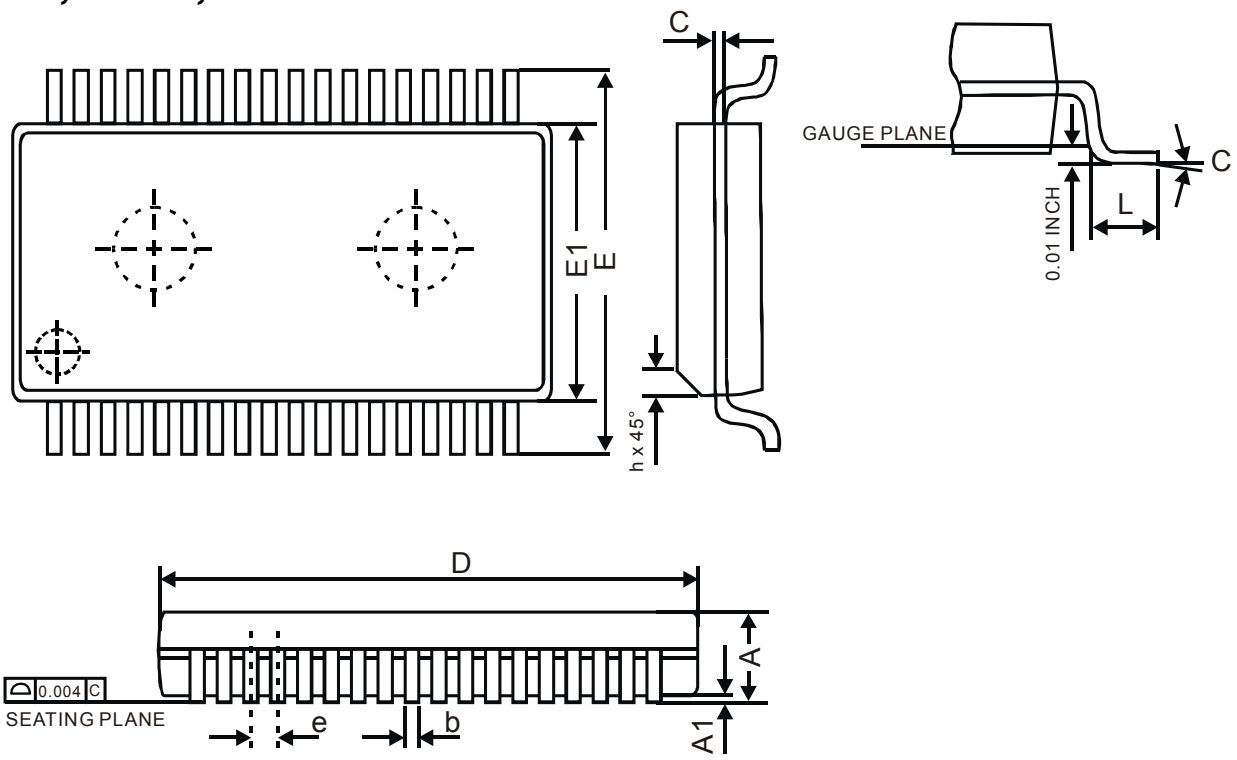
PACKAGE INFORMATION

36 PINS, SSOP, 300 MIL



Symbol	Dimensions In Inches		
	Min	Typ	Max
A	0.095	0.102	0.110
A1	0.008	0.012	0.016
b	0.012		0.018
c	0.005		0.010
e		0.032 Basic	
E	0.395		0.420
E1	0.291	0.295	0.299
h	0.015		0.025
L	0.020		0.040
θ	0		8
D	0.620	0.625	0.630

Notes:
1. Dimension “D” does not include mold flash, protrusions, or gate burrs.
2. Mold flash, protrusions, and gate burrs shall not exceed 0.006 inch. (0.1524mm) per side.
3. Dimension D does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0.15 mm (0.006 in) per side.