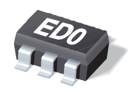
Burr-Brown Products from Texas Instruments



SBAS276A − MARCH 2003 − REVISED NOVEMBER 2003

16-Bit ANALOG-TO-DIGITAL CONVERTER with Onboard Reference

FEATURES

- **COMPLETE DATA ACQUISITION SYSTEM IN A TINY SOT23-6 PACKAGE**
- **ONBOARD REFERENCE:**
  Accuracy: 2.048V ±0.05%
  Drift: 5ppm/°C
- **ONBOARD PGA**
- **ONBOARD OSCILLATOR**
- **16-BITS NO MISSING CODES**
- **INL: 0.01% of FSR max**
- **CONTINUOUS SELF-CALIBRATION**
- **SINGLE-CYCLE CONVERSION**
- **PROGRAMMABLE DATA RATE: 15SPS TO 240SPS**
- **I^2C™ INTERFACE—EIGHT AVAILABLE ADDRESSES**
- **POWER SUPPLY: 2.7V to 5.5V**
- **LOW CURRENT CONSUMPTION: 240µA**

APPLICATIONS

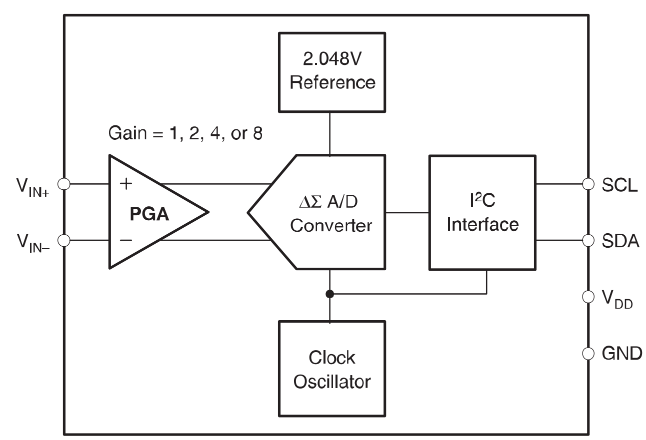
- **PORTABLE INSTRUMENTATION**
- **INDUSTRIAL PROCESS CONTROL**
- **SMART TRANSMITTERS**
- **CONSUMER GOODS**
- **FACTORY AUTOMATION**
- **TEMPERATURE MEASUREMENT**

DESCRIPTION

The ADS1110 is a precision, continuously self−calibrating Analog-to-Digital (A/D) converter with differential inputs and up to 16 bits of resolution in a small SOT23-6 package. The onboard 2.048V reference provides an input range of ±2.048V differentially. The ADS1110 uses an I^2C-compatible serial interface and operates from a single power supply ranging from 2.7V to 5.5V.

The ADS1110 can perform conversions at rates of 15, 30, 60, or 240 samples per second. The onboard programmable gain amplifier (PGA), which offers gains of up to 8, allows smaller signals to be measured with high resolution. In single-conversion mode, the ADS1110 automatically powers down after a conversion, greatly reducing current consumption during idle periods.

The ADS1110 is designed for applications requiring high-resolution measurement, where space and power consumption are major considerations. Typical applications include portable instrumentation, industrial process control, and smart transmitters.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS(1)

V_{DD} to GND	−0.3V to +6V
Input Current	100mA, Momentary
Input Current	10mA, Continuous
Voltage to GND, V_{IN+}, V_{IN-}	−0.3V to V_{DD} + 0.3V
Voltage to GND, SDA, SCL	−0.5V to 6V
Maximum Junction Temperature	+150°C
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−60°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

(1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

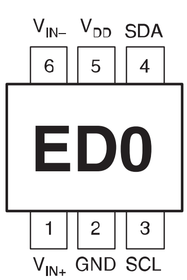
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	I^2C ADDRESS	PACKAGE−LEAD	PACKAGE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS1110	1001 000	SOT23-6	DBV	−40°C to +85°C	ED0	ADS1110A0IDBVT	Tape and Reel, 250
						ADS1110A0IDBVR	Tape and Reel, 3000
ADS1110	1001 001	SOT23-6	DBV	−40°C to +85°C	ED1	ADS1110A1IDBVT	Tape and Reel, 250
						ADS1110A1IDBVR	Tape and Reel, 3000
ADS1110	1001 010	SOT23-6	DBV	−40°C to +85°C	ED2	ADS1110A2IDBVT	Tape and Reel, 250
						ADS1110A2IDBVR	Tape and Reel, 3000
ADS1110	1001 011	SOT23-6	DBV	−40°C to +85°C	ED3	ADS1110A3IDBVT	Tape and Reel, 250
						ADS1110A3IDBVR	Tape and Reel, 3000
ADS1110	1001 100	SOT23-6	DBV	−40°C to +85°C	ED4	ADS1110A4IDBVT	Tape and Reel, 250
						ADS1110A4IDBVR	Tape and Reel, 3000
ADS1110	1001 101	SOT23-6	DBV	−40°C to +85°C	ED5	ADS1110A5IDBVT	Tape and Reel, 250
						ADS1110A5IDBVR	Tape and Reel, 3000
ADS1110	1001 110	SOT23-6	DBV	−40°C to +85°C	ED6	ADS1110A6IDBVT	Tape and Reel, 250
						ADS1110A6IDBVR	Tape and Reel, 3000
ADS1110	1001 111	SOT23-6	DBV	−40°C to +85°C	ED7	ADS1110A7IDBVT	Tape and Reel, 250
						ADS1110A7IDBVR	Tape and Reel, 3000

(1) For the most current specification and package information, refer to our web site at www.ti.com.

Top View **SOT23**



NOTE: Marking text direction indicates pin 1. Marking text depends on I^2C address; see ordering table. Marking for I^2C address 1001000 shown.

ELECTRICAL CHARACTERISTICS

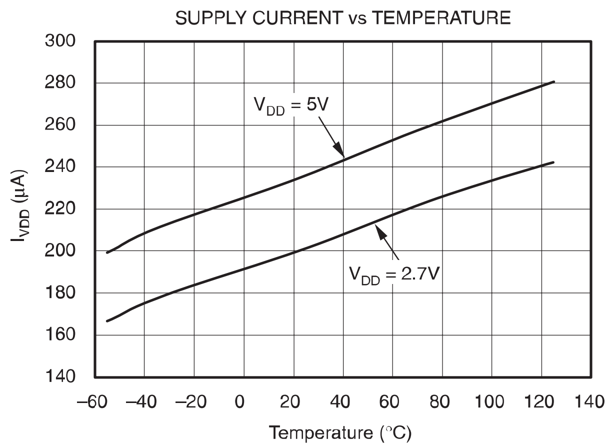
All specifications at −40°C to +85°C, V_{DD} = 5V, and all PGAs, unless otherwise noted.

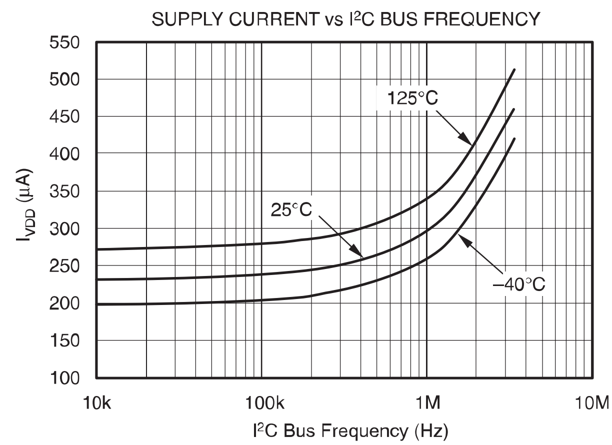
PARAMETER	CONDITIONS	ADS1110 MIN	ADS1110 TYP	ADS1110 MAX	UNIT
ANALOG INPUT					
Full-Scale Input Voltage	$(V_{IN+}) - (V_{IN-})$		±2.048/PGA		V
Analog Input Voltage	V_{IN+} to GND or V_{IN-} to GND	GND − 0.2		V_{DD} + 0.2	V
Differential Input Impedance			2.8/PGA		MΩ
Common-Mode Input Impedance	PGA = 1		3.5		MΩ
	PGA = 2		3.5		MΩ
	PGA = 4		1.8		MΩ
	PGA = 8		0.9		MΩ
SYSTEM PERFORMANCE					
Resolution and No Missing Codes	DR = 00	12		12	Bits
	DR = 01	14		14	Bits
	DR = 10	15		15	Bits
	DR = 11	16		16	Bits
Data Rate	DR = 00	180	240	308	SPS
	DR = 01	45	60	77	SPS
	DR = 10	22	30	39	SPS
	DR = 11	11	15	20	SPS
Output Noise		See Typical Characteristic Curves			
Integral Nonlinearity	DR = 11, PGA = 1, End Point Fit(1)		±0.004	±0.010	% of FSR(2)
Offset Error	PGA = 1		1.2	8	mV
	PGA = 2		0.7	4	mV
	PGA = 4		0.5	2.5	mV
	PGA = 8		0.4	1.5	mV
Offset Drift	PGA = 1		1.2		µV/°C
	PGA = 2		0.6		µV/°C
	PGA = 4		0.3		µV/°C
	PGA = 8		0.3		µV/°C
Offset vs V_{DD}	PGA = 1		800		µV/V
	PGA = 2		400		µV/V
	PGA = 4		200		µV/V
	PGA = 8		150		µV/V
Gain Error(3)			0.05	0.40	%
PGA Gain Error Match(3)	Match Between Any Two PGA Gains		0.02	0.10	%
Gain Error Drift(3)			5	40	ppm/°C
Gain vs V_{DD}			80		ppm/V
Common-Mode Rejection	At DC and PGA = 8	95	105		dB
	At DC and PGA = 1		100		dB
DIGITAL INPUT/OUTPUT					
Logic Level					
V_{IH}		0.7 • V_{DD}		6	V
V_{IL}		GND − 0.5		0.3 • V_{DD}	V
V_{OL}	I_{OL} = 3mA	GND		0.4	V
Input Leakage					
I_H	V_{IH} = 5.5V			10	µA
I_L	V_{IL} = GND	−10			µA
POWER-SUPPLY REQUIREMENTS					
Power-Supply Voltage	V_{DD}	2.7		5.5	V
Supply Current	Power Down		0.05	2	µA
	Active Mode		240	350	µA
Power Dissipation	V_{DD} = 5.0V		1.2	1.75	mW
	V_{DD} = 3.0V		0.675		mW

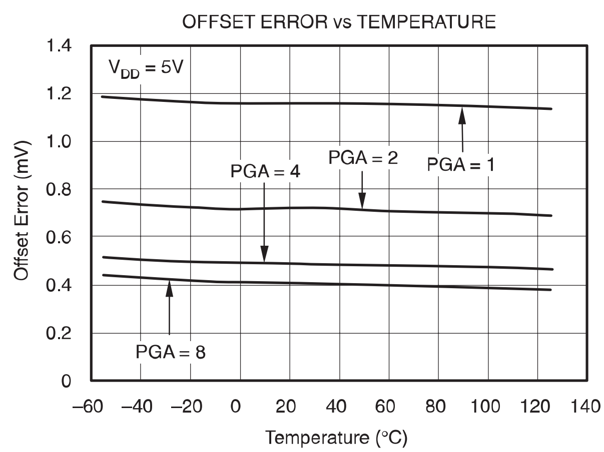
(1) 99% of full-scale.
(2) FSR = full-scale range = 2 × 2.048V/PGA = 4.096V/PGA.
(3) Includes all errors from onboard PGA and reference.

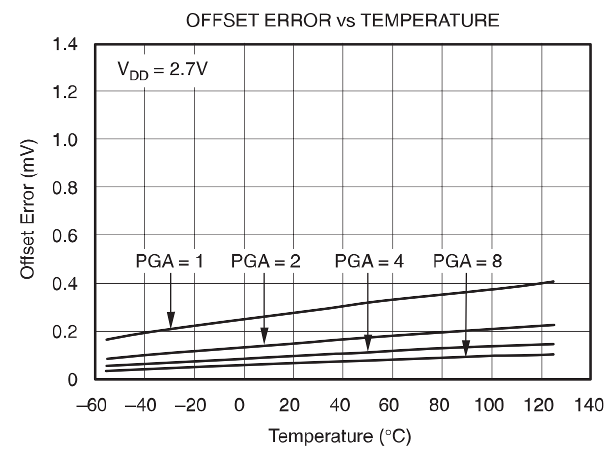
TYPICAL CHARACTERISTICS

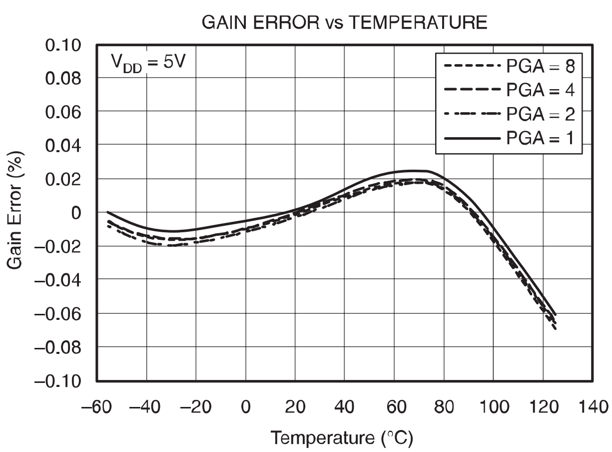
At $T_A = 25°C$ and $V_{DD} = 5V$, unless otherwise noted.

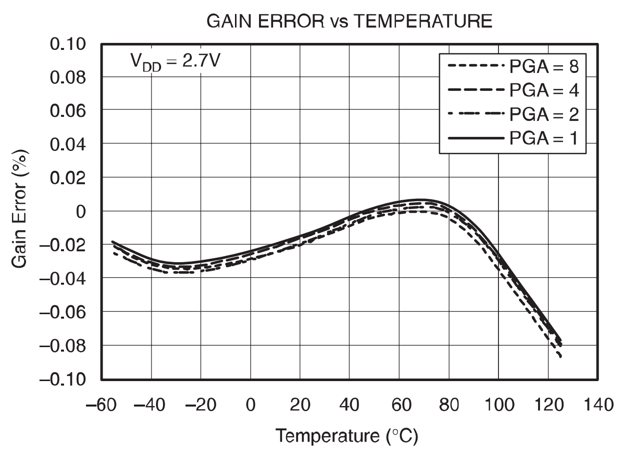








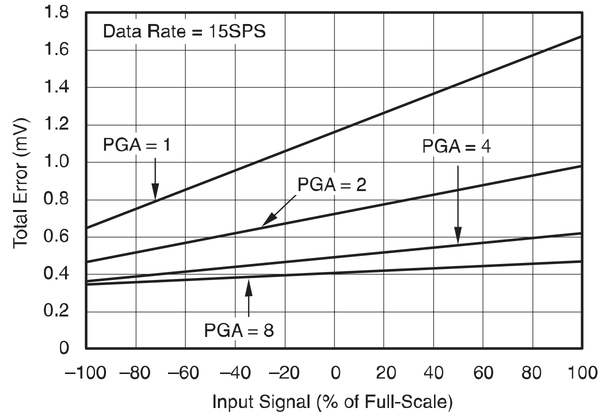




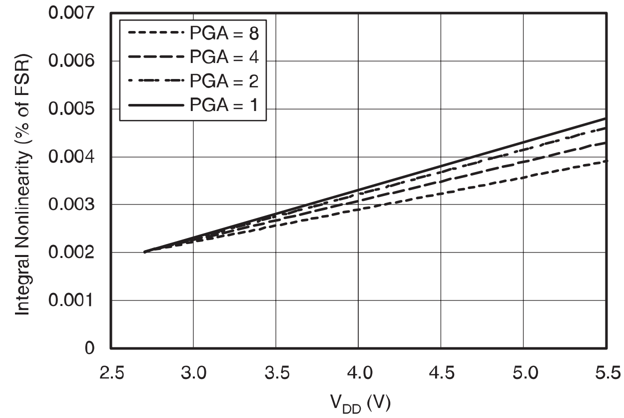
TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C and V_{DD} = 5V, unless otherwise noted.

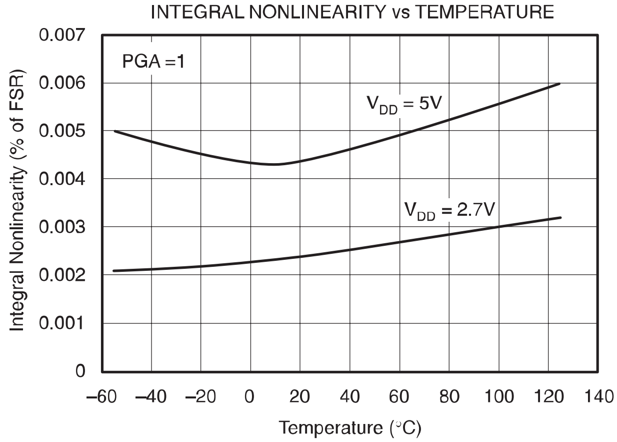
TOTAL ERROR vs INPUT SIGNAL



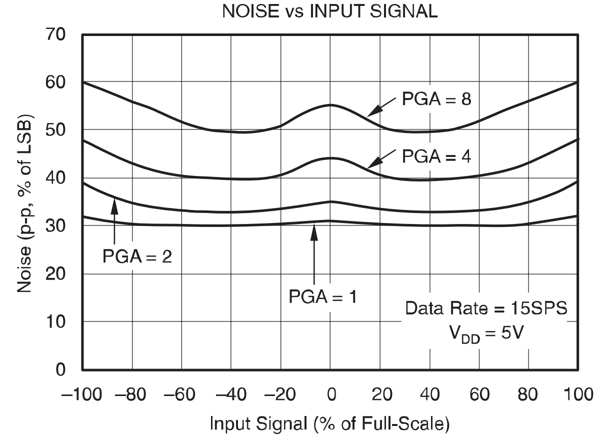
INTEGRAL NONLINEARITY vs SUPPLY VOLTAGE



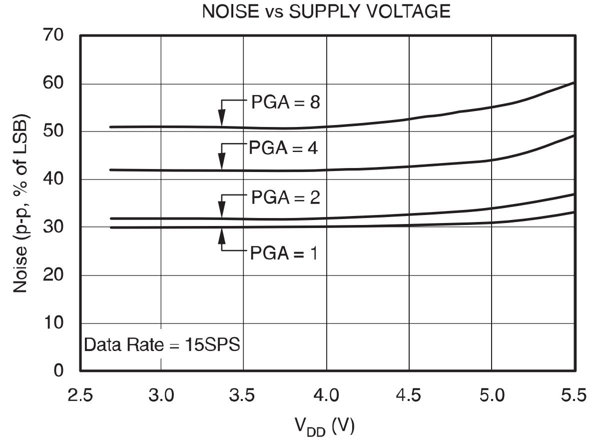
INTEGRAL NONLINEARITY vs TEMPERATURE



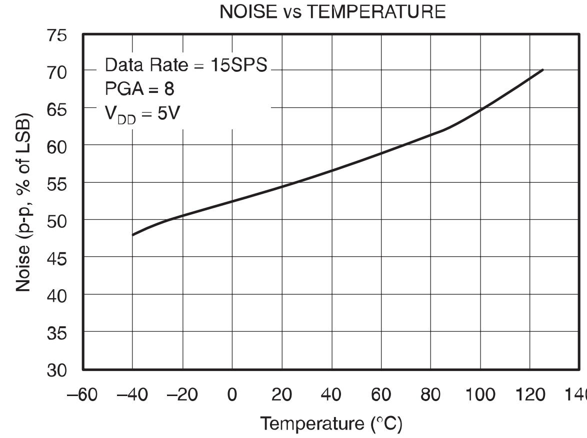
NOISE vs INPUT SIGNAL



NOISE vs SUPPLY VOLTAGE



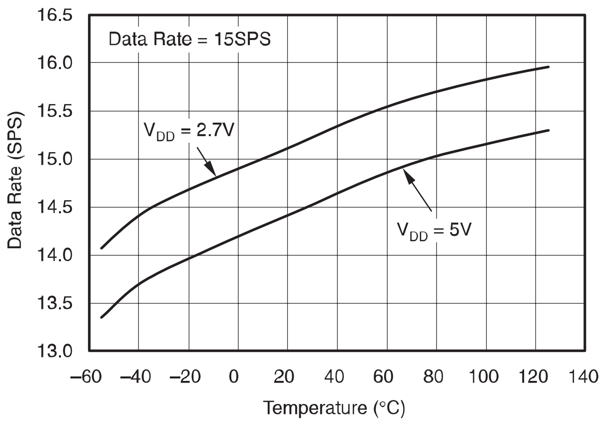
NOISE vs TEMPERATURE



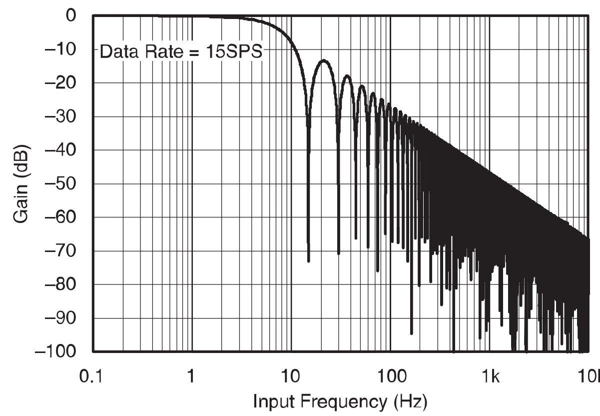
TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C and V_{DD} = 5V, unless otherwise noted.

DATA RATE vs TEMPERATURE



FREQUENCY RESPONSE



THEORY OF OPERATION

The ADS1110 is a fully differential, 16-bit, self-calibrating, delta-sigma A/D converter. Extremely easy to design with and configure, the ADS1110 allows precise measurements to be obtained with a minimum of effort.

The ADS1110 consists of a delta-sigma A/D converter core with adjustable gain, a 2.048V reference, a clock oscillator, and an I^2C interface. Each of these blocks are described in detail in the sections that follow.

ANALOG-TO-DIGITAL CONVERTER

The ADS1110 A/D converter core consists of a differential switched-capacitor delta-sigma modulator followed by a digital filter. The modulator measures the voltage difference between the positive and negative analog inputs and compares it to a reference voltage, which, in the ADS1110, is 2.048V. The digital filter receives a high-speed bitstream from the modulator and outputs a code, which is a number proportional to the input voltage.

VOLTAGE REFERENCE

The ADS1110 contains an onboard 2.048V voltage reference. This reference is always used as the A/D converter's voltage reference; an external reference cannot be connected. The ADS1110's voltage reference is internal only, and cannot be measured directly or used by external circuitry.

The onboard reference's specifications are part of the ADS1110's overall gain and drift specifications. The converter's drift and gain error specifications reflect the performance of the onboard reference as well as the performance of the A/D converter core. There are no separate specifications for the onboard reference itself.

OUTPUT CODE CALCULATION

The output code is a scalar value that is, except for clipping, proportional to the voltage difference between the two analog inputs. The output code is confined to a finite range of numbers; this range depends on the number of bits needed to represent the code. The number of bits needed to represent the output code for the ADS1110 depends on the data rate, as shown in Table 1.

DATA RATE	NUMBER OF BITS	MINIMUM CODE	MAXIMUM CODE
15SPS	16	−32,768	32,767
30SPS	15	−16,384	16,383
60SPS	14	−8192	8191
240SPS	12	−2048	2047

Table 1. Minimum and Maximum Codes

For a minimum output code of Min Code, gain setting of PGA, and positive and negative input voltages of V_{IN+} and V_{IN-}, the output code is given by the expression:

$$\text{Output Code} = -1 \times \text{Min Code} \times \text{PGA} \times \frac{(V_{IN+}) - (V_{IN-})}{2.048V}$$

In the previous expression, it is important to note that the *negated minimum* output code is used. The ADS1110 outputs codes in binary two's complement format, so the absolute values of the minima and maxima are not the same; the maximum n−bit code is $2^{n-1} - 1$, while the minimum n−bit code is $-1 \times 2^{n-1}$.

For example, the ideal expression for output codes with a data rate of 16SPS and PGA = 2 is:

$$\text{Output Code} = 16384 \times 2 \times \frac{(V_{IN+}) - (V_{IN-})}{2.048V}$$

The ADS1110 outputs all codes right-justified and sign-extended. This makes it possible to perform averaging on the higher data rate codes using only a 16-bit accumulator.

Table 2 shows the output codes for various input levels.

SELF-CALIBRATION

The previous expressions for the ADS1110's output code do not account for the gain and offset errors in the modulator. To compensate for these, the ADS1110 incorporates self-calibration circuitry.

The self-calibration system operates continuously and requires no user intervention. No adjustments can be made to the self-calibration system, and none need to be made. The self-calibration system cannot be deactivated.

The offset and gain error figures shown in the Electrical Characteristics include the effects of calibration.

CLOCK OSCILLATOR

The ADS1110 features an onboard clock oscillator, which drives the operation of the modulator and digital filter. The Typical Characteristics show variations in data rate over supply voltage and temperature.

It is not possible to operate the ADS1110 with an external system clock.

INPUT IMPEDANCE

The ADS1110 uses a switched-capacitor input stage. To external circuitry, it looks roughly like a resistance. The resistance value depends on the capacitor values and the rate at which they are switched. The switching frequency is the same as the modulator frequency; the capacitor values depend on the PGA setting. The switching clock is generated by the onboard clock oscillator, so its frequency, nominally 275kHz, is dependent on supply voltage and temperature.

The common-mode and differential input impedances are different. For a gain setting of PGA, the differential input impedance is typically:

$$2.8M\Omega/PGA$$

The common-mode impedance also depends on the PGA setting. See the Electrical Characteristics for details.

The typical value of the input impedance often cannot be neglected. Unless the input source has a low impedance, the ADS1110's input impedance may affect the measurement accuracy. For sources with high output impedance, buffering may be necessary. Bear in mind, however, that active buffers introduce noise, and also introduce offset and gain errors. All of these factors should be considered in high-accuracy applications.

Because the clock oscillator frequency drifts slightly with temperature, the input impedances will also drift. For many applications, this input impedance drift can be neglected, and the expression given above for typical input impedance can be used.

ALIASING

If frequencies are input to the ADS1110 that exceed half the data rate, aliasing will occur. To prevent aliasing, the input signal must be bandlimited. Some signals are inherently bandlimited. For example, a thermocouple's output, which has a limited rate of change, may nevertheless contain noise and interference components. These can fold back into the sampling band just as any other signal can.

The ADS1110's digital filter provides some attenuation of high-frequency noise, but the digital filter's Sinc^1 frequency response cannot completely replace an anti-aliasing filter. For a few applications, some external filtering may be needed; in such applications, a simple RC filter will suffice.

When designing an input filter circuit, remember to take into account the interaction between the filter network and the input impedance of the ADS1110.

DATA RATE	DIFFERENTIAL INPUT SIGNAL				
	−2.048V(1)	−1LSB	ZERO	+1LSB	+2.048V
15SPS	8000_H	$FFFF_H$	0000_H	0001_H	$7FFF_H$
30SPS	$C000_H$	$FFFF_H$	0000_H	0001_H	$3FFF_H$
60SPS	$E000_H$	$FFFF_H$	0000_H	0001_H	$1FFF_H$
240SPS	$F800_H$	$FFFF_H$	0000_H	0001_H	$07FF_H$

(1) Differential input only; do not drive the ADS1110's inputs below −200mV.

Table 2. Output Codes for Different Input Signals

USING THE ADS1110

OPERATING MODES

The ADS1110 operates in one of two modes: continuous conversion or single conversion.

In continuous conversion mode, the ADS1110 continuously performs conversions. Once a conversion has been completed, the ADS1110 places the result in the output register and immediately begins another conversion.

In single conversion mode, the ADS1110 waits until the ST/$\overline{DRDY}$ bit in the conversion register is set to 1. When this happens, the ADS1110 powers up and performs a single conversion. After the conversion completes, the ADS1110 places the result in the output register, resets the ST/$\overline{DRDY}$ bit to 0, and powers down. Writing a 1 to ST/$\overline{DRDY}$ while a conversion is in progress has no effect.

When switched from continuous conversion mode to single conversion mode, the ADS1110 completes the current conversion, resets the ST/$\overline{DRDY}$ bit to 0, and powers down.

RESET AND POWER−UP

When the ADS1110 powers up, it automatically performs a reset. As part of the reset, the ADS1110 sets all of the bits in the configuration register to their default settings.

The ADS1110 responds to the I^2C General Call Reset command. When the ADS1110 receives a General Call Reset, it performs an internal reset, exactly as though it had just been powered on.

I^2C INTERFACE

The ADS1110 communicates through an I^2C (inter-integrated circuit) interface. I^2C is a two-wire open-drain interface supporting multiple devices and masters on a single bus. Devices on the I^2C bus only drive the bus lines LOW by connecting them to ground; they never drive the bus lines HIGH. Instead, the bus wires are pulled HIGH by pull-up resistors, so the bus wires are HIGH when no device is driving them LOW. This way, two devices cannot conflict; if two devices drive the bus simultaneously, there is no driver contention.

Communication on the I^2C bus always takes place between two devices, one acting as the master and the other acting as the slave. Both masters and slaves can read and write, but slaves can only do so under the direction of the master. Some I^2C devices can act as masters or slaves, but the ADS1110 can only act as a slave device.

An I^2C bus consists of two lines, SDA and SCL. SDA carries data; SCL provides the clock. All data is transmitted across the I^2C bus in groups of eight bits. To send a bit on the I^2C bus, the SDA line is driven to the appropriate level while SCL is LOW (a LOW on SDA indicates the bit is zero; a HIGH indicates the bit is one). Once the SDA line has settled, the SCL line is brought HIGH, then LOW. This pulse on SCL clocks the SDA bit into the receiver's shift register.

The I^2C bus is bidirectional: the SDA line is used both for transmitting and receiving data. When a master reads from a slave, the slave drives the data line; when a master sends to a slave, the master drives the data line. The master always drives the clock line. The ADS1110 never drives SCL, because it cannot act as a master. On the ADS1110, SCL is an input only.

Most of the time the bus is idle, no communication is taking place, and both lines are HIGH. When communication is taking place, the bus is active. Only master devices can start a communication. They do this by causing a START condition on the bus. Normally, the data line is only allowed to change state while the clock line is LOW. If the data line changes state while the clock line is HIGH, it is either a START condition or its counterpart, a STOP condition. A START condition is when the clock line is HIGH and the data line goes from HIGH to LOW. A STOP condition is when the clock line is HIGH and the data line goes from LOW to HIGH.

After the master issues a START condition, it sends a byte that indicates which slave device it wants to communicate with. This byte is called the address byte. Each device on an I^2C bus has a unique 7-bit address to which it responds. (Slaves can also have 10-bit addresses; see the I^2C specification for details.) The master sends an address in the address byte, together with a bit that indicates whether it wishes to read from or write to the slave device.

Every byte transmitted on the I^2C bus, whether it is address or data, is acknowledged with an acknowledge bit. When a master has finished sending a byte (eight data bits) to a slave, it stops driving SDA and waits for the slave to acknowledge the byte. The slave acknowledges the byte by pulling SDA LOW. The master then sends a clock pulse to clock the acknowledge bit. Similarly, when a master has finished reading a byte, it pulls SDA LOW to acknowledge this to the slave. It then sends a clock pulse to clock the bit. (Remember that the master always drives the clock line.)

A not-acknowledge is performed by simply leaving SDA HIGH during an acknowledge cycle. If a device is not present on the bus, and the master attempts to address it, it will receive a not−acknowledge because no device is present at that address to pull the line LOW.

When a master has finished communicating with a slave, it may issue a STOP condition. When a STOP condition is issued, the bus becomes idle again. A master may also issue another START condition. When a START condition is issued while the bus is active, it is called a repeated START condition.

A timing diagram for an ADS1110 I^{2}C transaction is shown in Figure 1. The parameters for this diagram are given in Table 3.

ADS1110 I^{2}C ADDRESSES

The ADS1110 I^{2}C address is 1001*aaa*, where *aaa* are bits set at the factory. The ADS1110 is available in eight different versions, each having a different I^{2}C address. For example, the ADS1110A0 has address 1001000, and the ADS1110A3 has address 1001011. See the Ordering Information table for a complete listing.

The I^{2}C address is the only difference between the eight variants. In all other respects, they operate identically.

Each variant of the ADS1110 is marked with ED*x*, where *x* identifies the address variant. For example, the ADS1110A0 is marked ED0, and the ADS1110A3 is marked ED3. See the Package/Ordering Information table for a complete listing.

I^{2}C GENERAL CALL

The ADS1110 responds to a General Call Reset, which is an address byte of 00h followed by a data byte of 06_H. The ADS1110 acknowledges both bytes.

On receiving a General Call Reset, the ADS1110 performs a full internal reset, just as though it had been powered off and then on. If a conversion is in process, it is interrupted; the output register is set to zero, and the configuration register is set to its default setting.

The ADS1110 always acknowledges the General Call address byte of 00_H, but it does not acknowledge any General Call data bytes other than 04_H or 06_H.

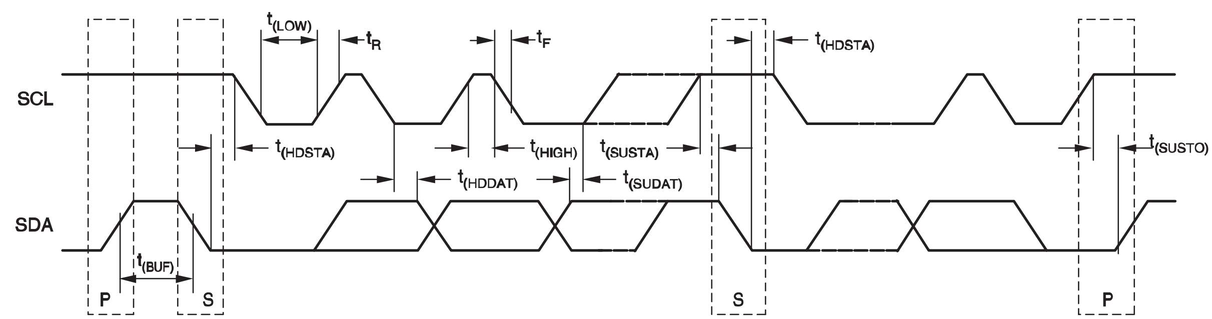


Figure 1. I^{2}C Timing Diagram

PARAMETER		FAST MODE MIN	FAST MODE MAX	HIGH-SPEED MODE MIN	HIGH-SPEED MODE MAX	UNITS
SCLK operating frequency	$t_{(SCLK)}$		0.4		3.4	MHz
Bus free time between START and STOP condition	$t_{(BUF)}$	600		160		ns
Hold time after repeated START condition. After this period, the first clock is generated.	$t_{(HDSTA)}$	600		160		ns
Repeated START condition setup time	$t_{(SUSTA)}$	600		160		ns
Stop condition setup time	$t_{(SUSTO)}$	600		160		ns
Data hold time	$t_{(HDDAT)}$	0		0		ns
Data setup time	$t_{(SUDAT)}$	100		10		ns
SCLK clock LOW period	$t_{(LOW)}$	1300		160		ns
SCLK clock HIGH period	$t_{(HIGH)}$	600		60		ns
Clock/data fall time	t_F		300		160	ns
Clock/data rise time	t_R		300		160	ns

Table 3. Timing Diagram Definitions

I²C DATA RATES

The I²C bus operates in one of three speed modes: Standard, which allows a clock frequency of up to 100kHz; Fast, which allows a clock frequency of up to 400kHz; and High-speed mode (also called Hs mode), which allows a clock frequency of up to 3.4MHz. The ADS1110 is fully compatible with all three modes.

No special action needs to be taken to use the ADS1110 in Standard or Fast modes, but High-speed mode must be activated. To activate High-speed mode, send a special address byte of 00001*xxx* following the START condition, where *xxx* are bits unique to the Hs-capable master. This byte is called the Hs master code. (Note that this is different from normal address bytes: the low bit does not indicate read/write status.) The ADS1110 will not acknowledge this byte; the I²C specification prohibits acknowledgment of the Hs master code. On receiving a master code, the ADS1110 will switch on its Hs mode filters, and communicate at up to 3.4MHz. The ADS1110 will switch out of Hs mode with the next STOP condition.

For more information on High-speed mode, consult the I²C specification.

REGISTERS

The ADS1110 has two registers that are accessible via its I²C port. The output register contains the result of the last conversion; the configuration register allows the user to change the ADS1110 operating mode and query the status of the device.

OUTPUT REGISTER

The 16-bit output register contains the result of the last conversion in binary two's complement format. Following reset or power−up, the output register is cleared to zero; it remains zero until the first conversion is completed.

The output register's format is shown in Table 4.

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 4. Output Register

CONFIGURATION REGISTER

The 8-bit configuration register can be used to control the ADS1110's operating mode, data rate, and PGA settings. The configuration register format is shown in Table 5. The default setting is $8C_H$.

BIT	7	6	5	4	3	2	1	0
NAME	ST/$\overline{\text{DRDY}}$	0	0	SC	DR1	DR0	PGA1	PGA0
DEFAULT	1	0	0	0	1	1	0	0

Table 5. Configuration Register

Bit 7: ST/$\overline{\text{DRDY}}$

The meaning of the ST/$\overline{\text{DRDY}}$ bit depends on whether it is being written to or read from.

In single conversion mode, writing a 1 to the ST/$\overline{\text{DRDY}}$ bit causes a conversion to start, and writing a 0 has no effect. In continuous conversion mode, the ADS1110 ignores the value written to ST/$\overline{\text{DRDY}}$.

When read, ST/$\overline{\text{DRDY}}$ indicates whether the data in the output register is new data. If ST/$\overline{\text{DRDY}}$ is 0, the data just read from the output register is new, and has not been read before. If ST/$\overline{\text{DRDY}}$ is 1, the data just read from the output register has been read before.

The ADS1110 sets ST/$\overline{\text{DRDY}}$ to 0 when it writes data into the output register. It sets ST/$\overline{\text{DRDY}}$ to 1 after any of the bits in the configuration register have been read. (Note that the read value of the bit is independent of the value written to this bit.)

In continuous-conversion mode, use ST/$\overline{\text{DRDY}}$ to determine when new conversion data is ready. If ST/$\overline{\text{DRDY}}$ is 1, the data in the output register has already been read, and is not new. If it is 0, the data in the output register is new, and has not yet been read.

In single-conversion mode, use ST/$\overline{\text{DRDY}}$ to determine when a conversion has completed. If ST/$\overline{\text{DRDY}}$ is 1, the output register data is old, and the conversion is still in process; if it is 0, the output register data is the result of the new conversion.

Note that the output register is returned from the ADS1110 before the configuration register. The state of the ST/$\overline{\text{DRDY}}$ bit applies to the data just read from the output register, and not to the data from the next read operation.

Bits 6−5: Reserved

Bits 6 and 5 must be set to zero.

Bit 4: SC

SC controls whether the ADS1110 is in continuous conversion or single conversion mode. When SC is 1, the ADS1110 is in single conversion mode; when SC is 0, the ADS1110 is in continuous conversion mode. The default setting is 0.

Bits 3−2: DR

Bits 3 and 2 control the ADS1110's data rate, as shown in Table 6.

DR1	DR0	DATA RATE
0	0	240SPS
0	1	60SPS
1	0	30SPS
1[(1)]	1[(1)]	15SPS[(1)]

(1) Default setting.

Table 6. DR Bits

Bits 1−0: PGA

Bits 1 and 0 control the ADS1110's gain setting, as shown in Table 7.

PGA1	PGA0	GAIN
0[(1)]	0[(1)]	1[(1)]
0	1	2
1	0	4
1	1	8

(1) Default setting.

Table 7. PGA Bits

READING FROM THE ADS1110

To read the output register and the configuration register from the ADS1110, address the ADS1110 for reading, then read three bytes. The first two bytes will be the output register's contents, and the third will be the configuration register's contents.

It is not required to read the configuration register byte. It is permissible to read fewer than three bytes during a read operation.

Reading more than three bytes from the ADS1110 has no effect. All bytes following the third will be FF_H.

It is possible to ignore the ST/$\overline{\text{DRDY}}$ bit and read data from the ADS1110's output register at any time, without regard to whether a new conversion is complete. If the output register is read more than once during a conversion cycle, it will return the same data each time. New data will be returned only when the output register has been updated.

A timing diagram of a typical ADS1110 read operation is shown in Figure 2.

WRITING TO THE ADS1110

To write to the configuration register, address the ADS1110 for writing, and send one byte. The byte will be written to the configuration register. Note that the output register cannot be written to.

Writing more than one byte to the ADS1110 has no effect. The ADS1110 will ignore any bytes sent to it after the first one, and it will only acknowledge the first byte.

A timing diagram of a typical ADS1110 write operation is shown in Figure 3.

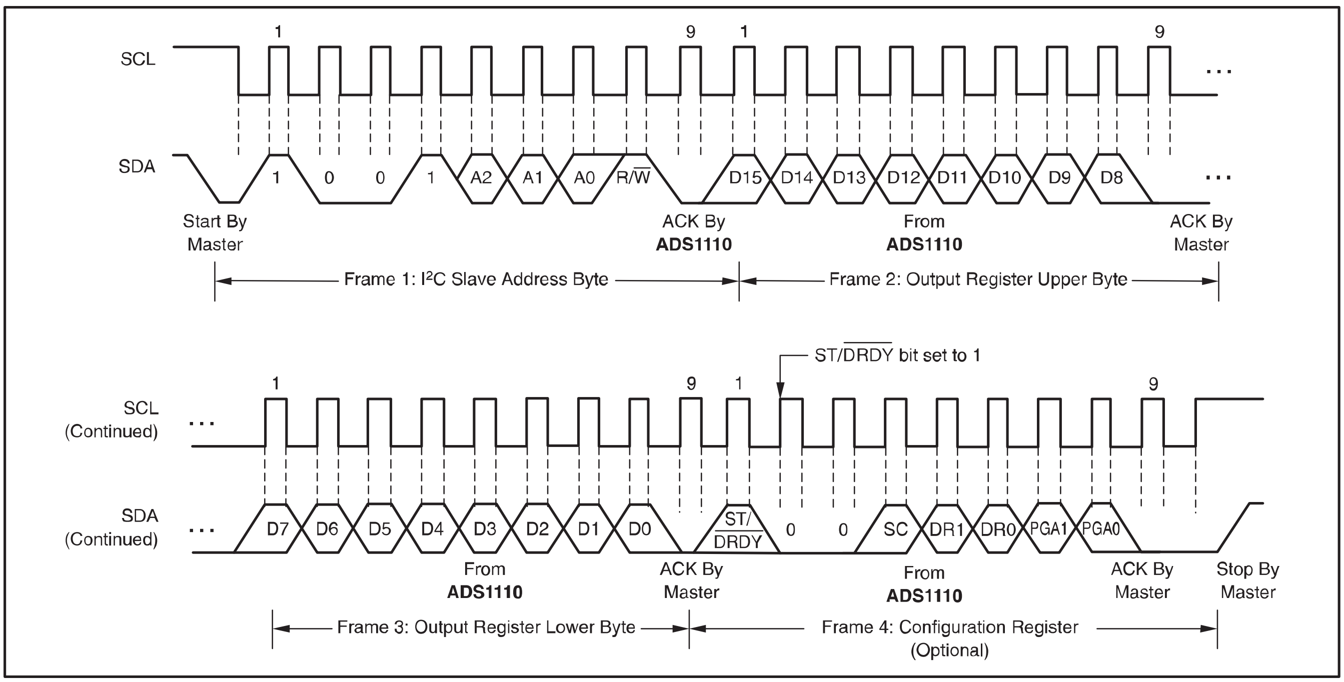


Figure 2. Timing Diagram for Reading From the ADS1110

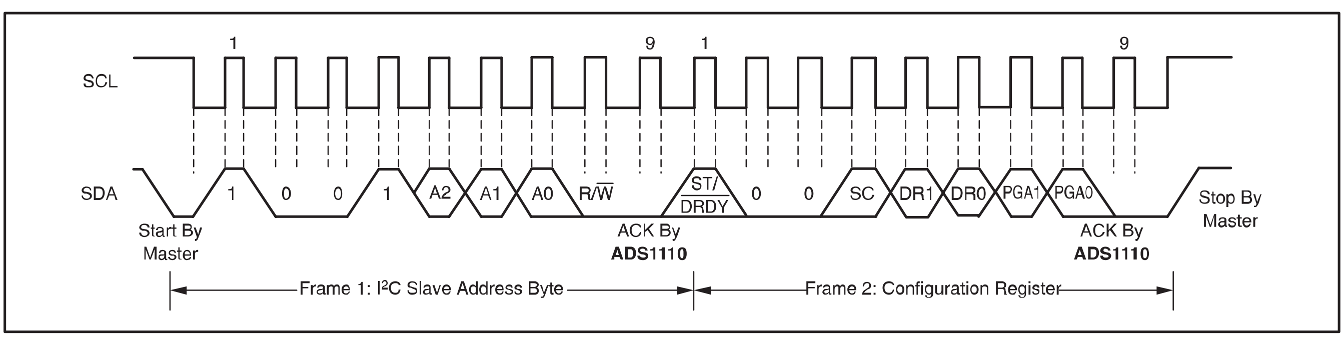


Figure 3. Timing Diagram for Writing To the ADS1110

APPLICATIONS INFORMATION

The sections that follow give example circuits and tips for using the ADS1110 in various situations.

BASIC CONNECTIONS

For many applications, connecting the ADS1110 is extremely simple. A basic connection diagram for the ADS1110 is shown in Figure 4.

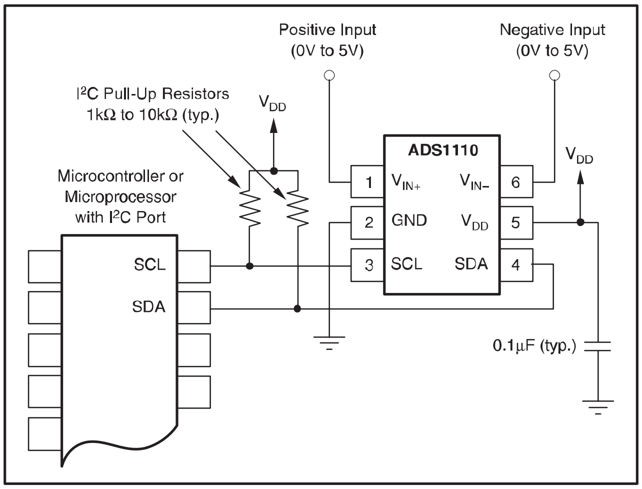


Figure 4. Typical Connections of the ADS1110

The fully differential voltage input of the ADS1110 is ideal for connection to differential sources with moderately low source impedance, such as bridge sensors and thermistors. Although the ADS1110 can read bipolar differential signals, it cannot accept negative voltages on either input. It may be helpful to think of the ADS1110 positive voltage input as non−inverting, and of the negative input as inverting.

When the ADS1110 is converting, it draws current in short spikes. The 0.1µF bypass capacitor supplies the momentary bursts of extra current needed from the supply.

The ADS1110 interfaces directly to standard mode, fast mode, and high−speed mode I^2C controllers. Any microcontroller's I^2C peripheral, including master-only and non-multiple-master I^2C peripherals, will work with the ADS1110. The ADS1110 does not perform clock-stretching (i.e., it never pulls the clock line low), so it is not necessary to provide for this unless clock-stretching devices are on the same I^2C bus.

Pull-up resistors are necessary on both the SDA and SCL lines because I^2C bus drivers are open-drain. The size of these resistors depends on the bus operating speed and capacitance of the bus lines. Higher-value resistors consume less power, but increase the transition times on the bus, limiting the bus speed. Lower-value resistors allow higher speed at the expense of higher power consumption. Long bus lines have higher capacitance and require smaller pull-up resistors to compensate. The resistors should not be too small; if they are, the bus drivers may not be able to pull the bus lines low.

CONNECTING MULTIPLE DEVICES

Connecting multiple ADS1110s to a single bus is trivial. The ADS1110 is available in eight different versions, each of which has a different I^2C address. An example showing three ADS1110s connected on a single bus is shown in Figure 5. Up to eight ADS1110s (provided their addresses are different) can be connected to a single bus.

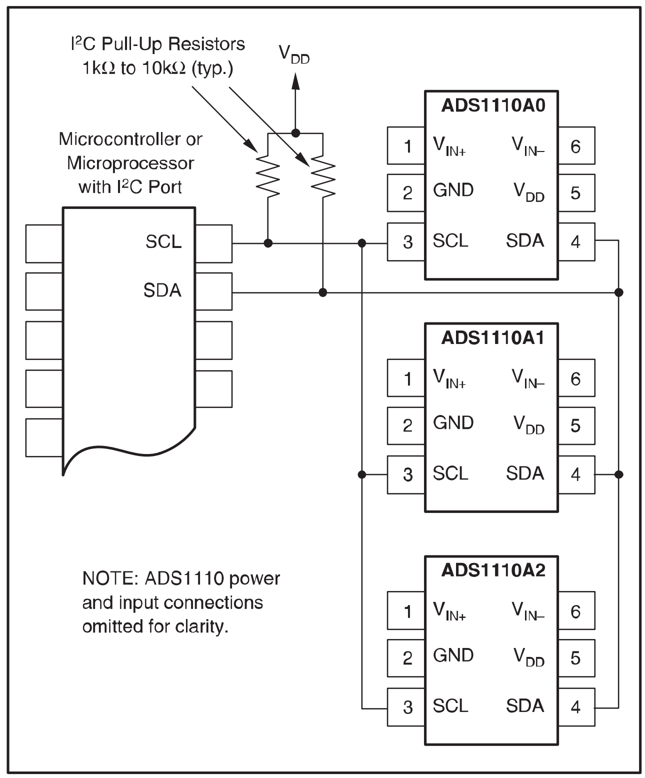


Figure 5. Connecting Multiple ADS1110s

Note that only one set of pull-up resistors is needed per bus. The pull-up resistor values may need to be lowered slightly to compensate for the additional bus capacitance presented by multiple devices and increased line length.

Figure 6 shows a circuit with several different devices connected to a single I2C bus. A Texas Instruments TMP100 temperature sensor and a Texas Instruments DAC8574 4-channel 16-bit digital-to-analog converter share the bus with two ADS1110s.

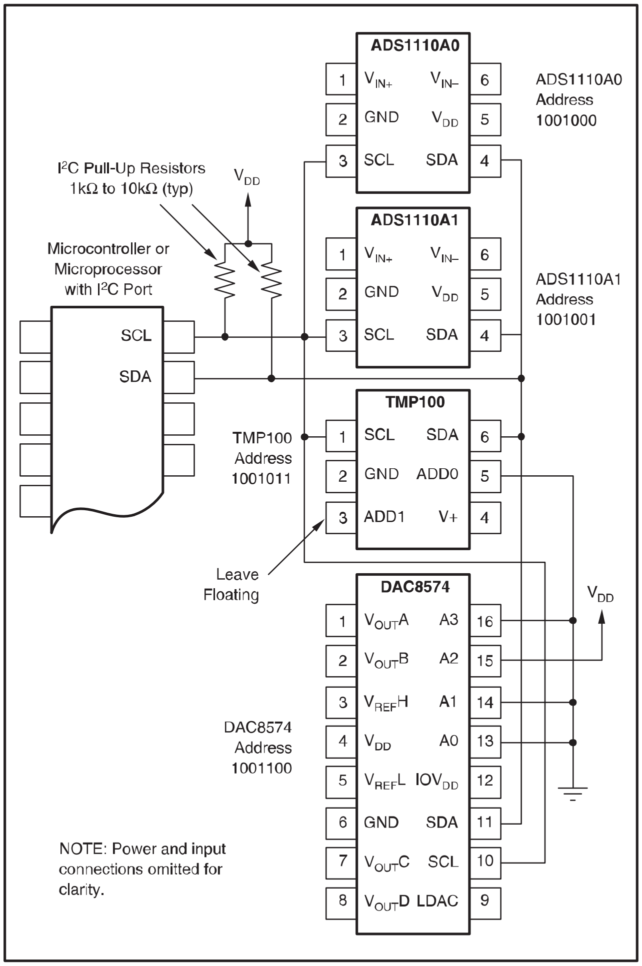


Figure 6. Connecting Multiple Device Types

The TMP100 and DAC8574 devices detect their I2C bus addresses based on the states of pins. In the example, the TMP100 has the address 1001011, and the DAC8574 has the address 1001100. Consult the DAC8574 and TMP100 data sheets, located at www.ti.com, for details.

USING GPIO PORTS FOR I2C

Most microcontrollers have programmable input/output pins that can be set in software to act as inputs or outputs. If an I2C controller is not available, the ADS1110 can be connected to GPIO pins and the I2C bus protocol simulated, or “bit-banged”, in software. An example of this for a single ADS1110 is shown in Figure 7.

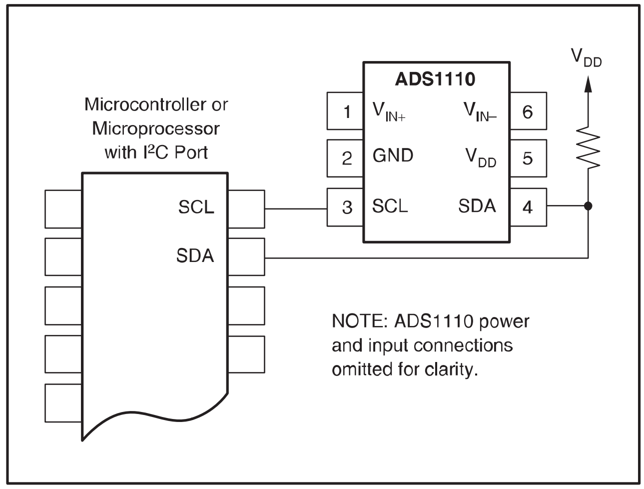


Figure 7. Using GPIO with a Single ADS1110

Bit-banging I2C with GPIO pins can be done by setting the GPIO line to zero and toggling it between input and output modes to apply the proper bus states. To drive the line low, the pin is set to output a zero; to let the line go high, the pin is set to input. When the pin is set to input, the state of the pin can be read; if another device is pulling the line low, this will read as a zero in the port’s input register.

Note that no pull-up resistor is shown on the SCL line. In this simple case, the resistor is not needed; the microcontroller can simply leave the line on output, and set it to one or zero as appropriate. It can do this because the ADS1110 never drives its clock line low. This technique can also be used with multiple devices, and has the advantage of lower current consumption due to the absence of a resistive pull-up.

If there are any devices on the bus that may drive their clock lines low, the above method should not be used; the SCL line should be high-Z or zero and a pull-up resistor provided as usual. Note also that this cannot be done on the SDA line in any case, because the ADS1110 does drive the SDA line low from time to time, as all I2C devices do.

Some microcontrollers have selectable strong pull-up circuits built in to their GPIO ports. In some cases, these can be switched on and used in place of an external pull-up resistor. Weak pull-ups are also provided on some microcontrollers, but usually these are too weak for I2C communication. If there is any doubt about the matter, test the circuit before committing it to production.

SINGLE-ENDED INPUTS

Although the ADS1110 has a fully differential input, it can easily measure single-ended signals. A simple single-ended connection scheme is shown in Figure 8. The ADS1110 is configured for single-ended measurement by grounding either of its input pins, usually V_{IN-}, and applying the input signal to V_{IN+}. The single-ended signal can range from 0V to 2.048V. The ADS1110 loses no linearity anywhere in its input range. Negative voltages cannot be applied to this circuit because the ADS1110 inputs can only accept positive voltages.

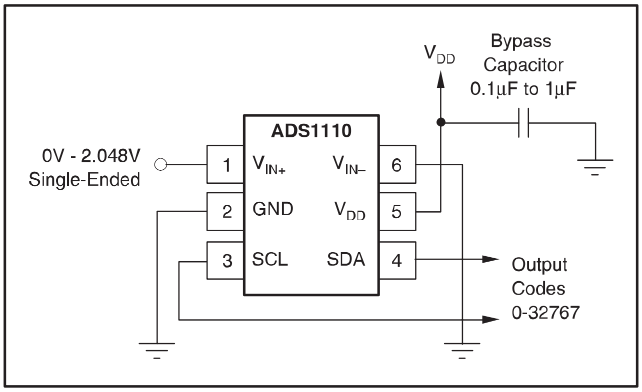


Figure 8. Measuring Single-Ended Inputs

The ADS1110 input range is bipolar differential with respect to the reference, i.e. 2.048V. The single-ended circuit shown in Figure 8 covers only half the ADS1110 input scale because it does not produce differentially negative inputs; therefore, one bit of resolution is lost.

LOW-SIDE CURRENT MONITOR

Figure 9 shows a circuit for a low-side shunt-type current monitor. The circuit reads the voltage across a shunt resistor, which is sized as small as possible while still giving a readable output voltage. This voltage is amplified by an OPA335 low-drift op amp and the result is read by the ADS1110.

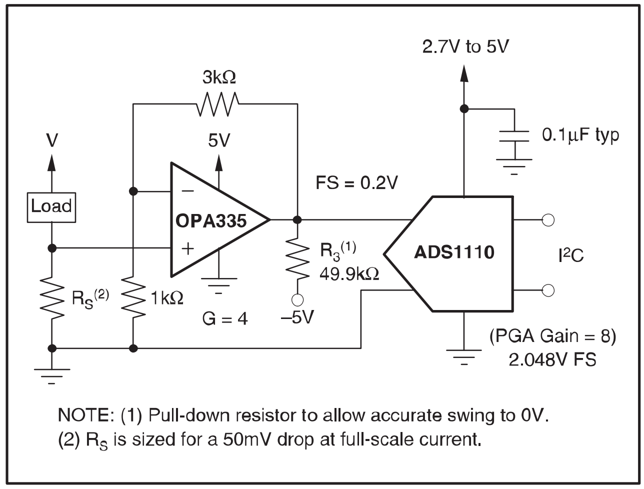


Figure 9. Low-Side Current Measurement

It is suggested that the ADS1110 be operated at a gain of 8. The gain of the OPA335 can then be set lower. For a gain of 8, the op amp should be set up to give a maximum output voltage of no greater than 0.256V. If the shunt resistor is sized to provide a maximum voltage drop of 50mV at full-scale current, the full-scale input to the ADS1110 is 0.2V.

ADVICE

The ADS1110 is fabricated in a small-geometry low-voltage process. The analog inputs feature protection diodes to the supply rails. However, the current-handling ability of these diodes is limited, and the ADS1110 can be permanently damaged by analog input voltages that remain more than approximately 300mV beyond the rails for extended periods. One way to protect against overvoltage is to place current-limiting resistors on the input lines. The ADS1110 analog inputs can withstand momentary currents of as large as 10mA.

The previous paragraph does not apply to the I^2C ports, which can both be driven to 6V regardless of the supply.

If the ADS1110 is driven by an op amp with high-voltage supplies, such as ±12V, protection should be provided, even if the op amp is configured so that it does not output out-of-range voltages. Many op amps seek to one of the supply rails immediately when power is applied, usually before the input has stabilized; this momentary spike can damage the ADS1110. Sometimes this damage is incremental and results in slow, long-term failure—which can be disastrous for permanently installed, low-maintenance systems.

If an op amp or other front-end circuitry is used with the ADS1110, its performance characteristics must be taken into account. A chain is only as strong as its weakest link.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1110A0IDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ED0	Samples
ADS1110A0IDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		ED0	Samples
ADS1110A0IDBVTG4	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		ED0	Samples
ADS1110A1IDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		ED1	Samples
ADS1110A1IDBVRG4	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		ED1	Samples
ADS1110A1IDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		ED1	Samples
ADS1110A1IDBVTG4	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		ED1	Samples
ADS1110A2IDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		ED2	Samples
ADS1110A2IDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		ED2	Samples
ADS1110A2IDBVTG4	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		ED2	Samples
ADS1110A3IDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		ED3	Samples
ADS1110A4IDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		ED4	Samples
ADS1110A4IDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		ED4	Samples
ADS1110A4IDBVTG4	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		ED4	Samples
ADS1110A5IDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		ED5	Samples
ADS1110A5IDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		ED5	Samples
ADS1110A5IDBVTG4	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		ED5	Samples
ADS1110A6IDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		ED6	Samples
ADS1110A7IDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		ED7	Samples
ADS1110A7IDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		ED7	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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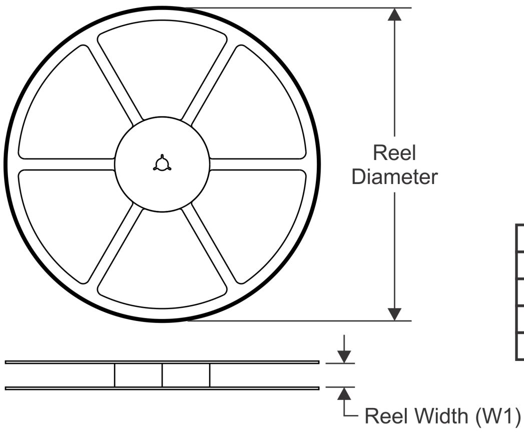
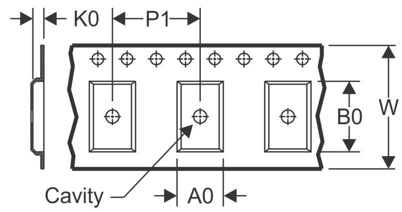
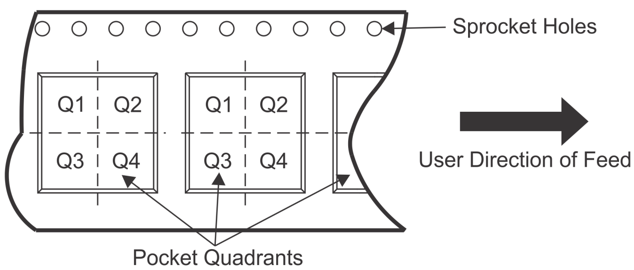
TAPE AND REEL INFORMATION





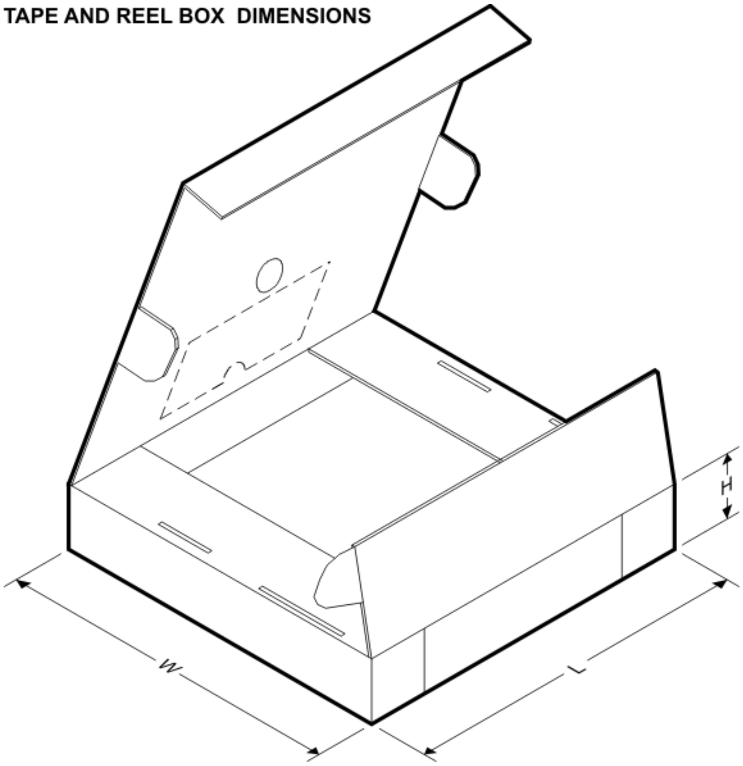
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

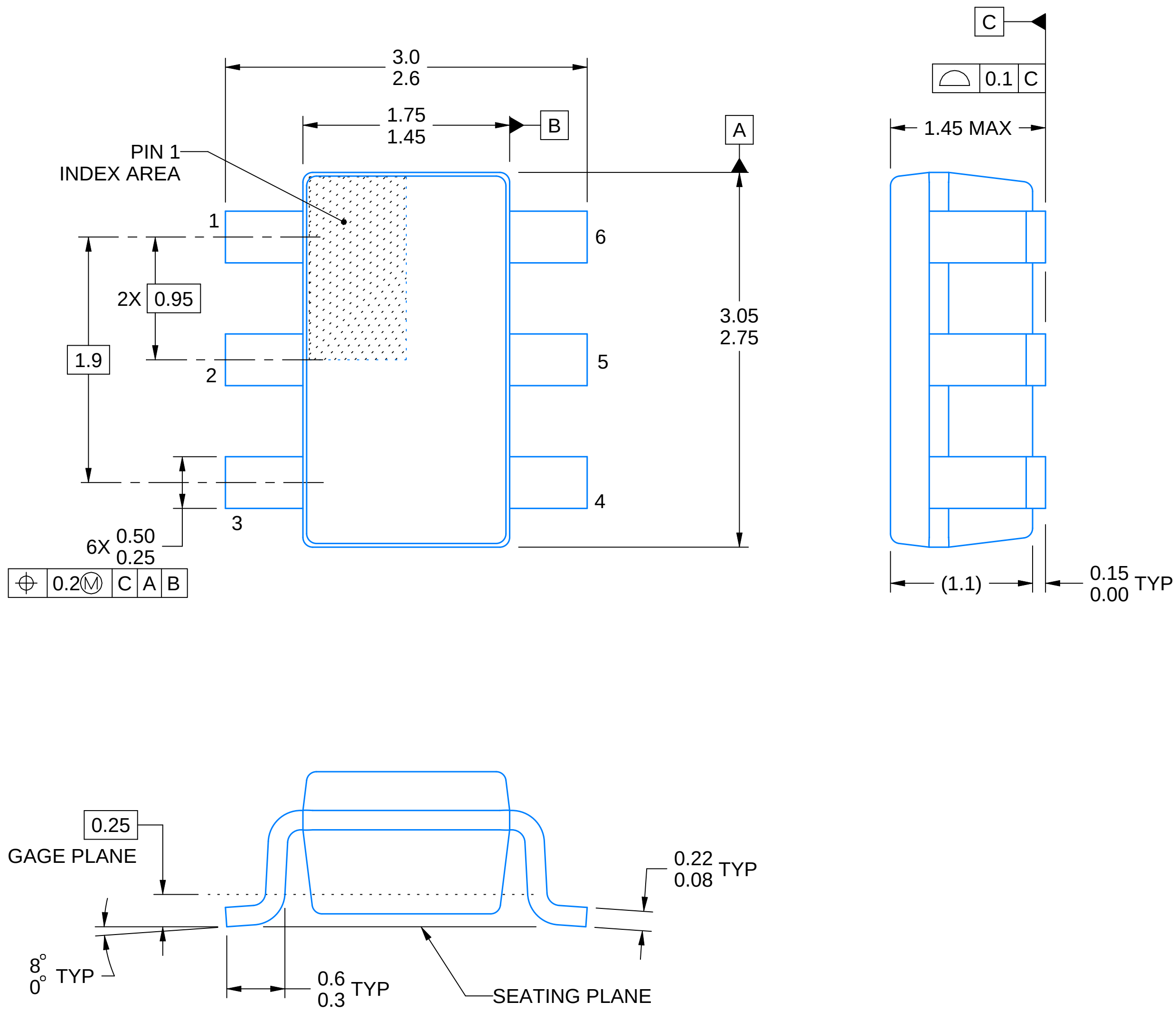
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1110A0IDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
ADS1110A0IDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
ADS1110A1IDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
ADS1110A1IDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
ADS1110A2IDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
ADS1110A2IDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
ADS1110A3IDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
ADS1110A4IDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
ADS1110A4IDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
ADS1110A5IDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
ADS1110A5IDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
ADS1110A6IDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
ADS1110A7IDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
ADS1110A7IDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1110A0IDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
ADS1110A0IDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
ADS1110A1IDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
ADS1110A1IDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
ADS1110A2IDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
ADS1110A2IDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
ADS1110A3IDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
ADS1110A4IDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
ADS1110A4IDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
ADS1110A5IDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
ADS1110A5IDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
ADS1110A6IDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
ADS1110A7IDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
ADS1110A7IDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0



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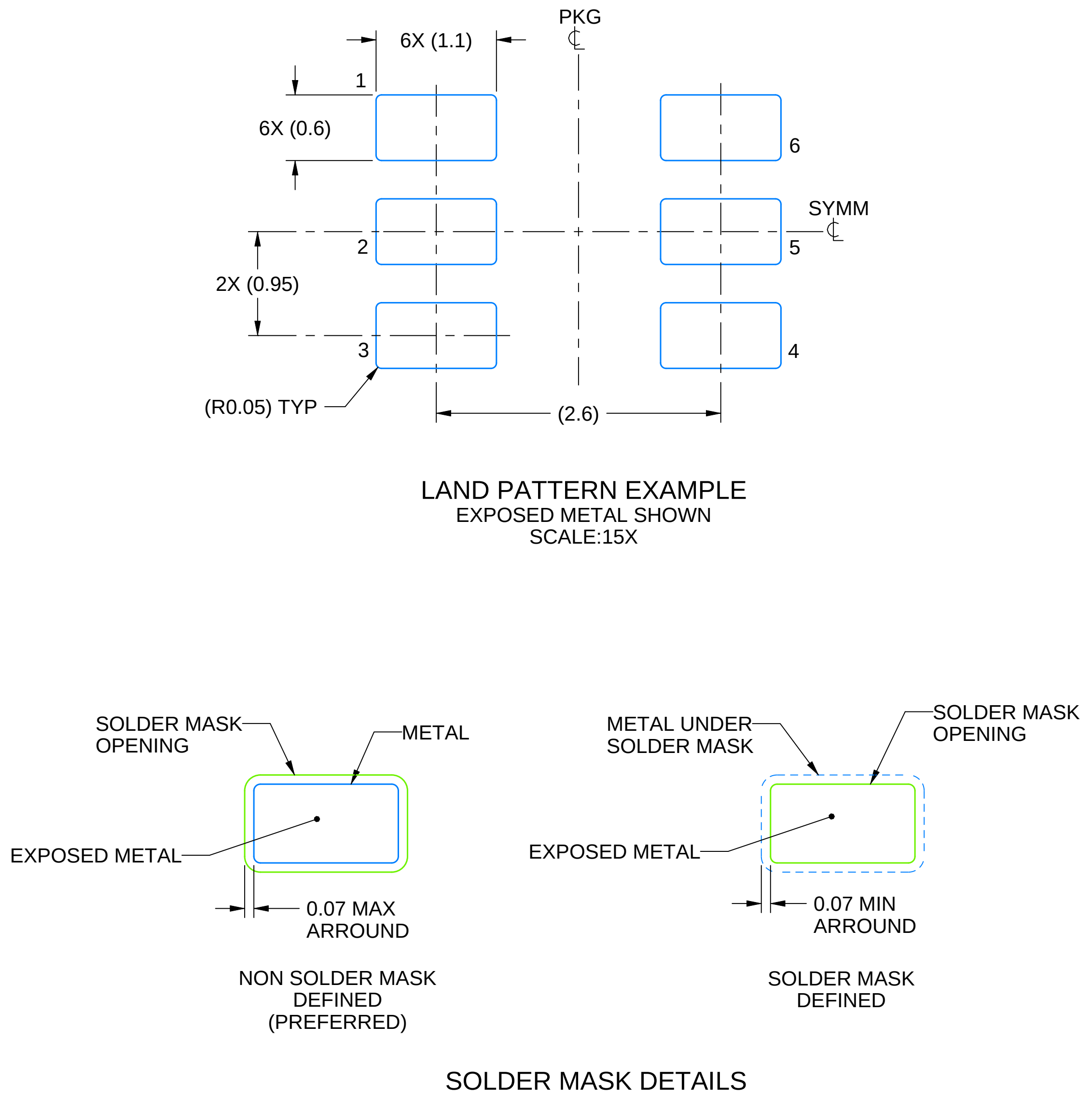
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



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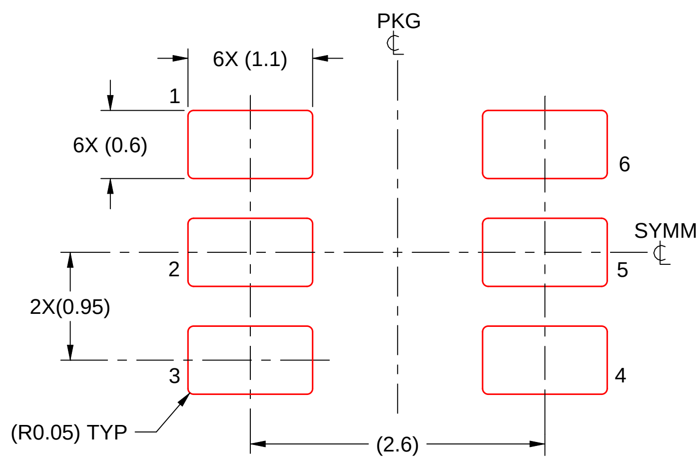
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.