

## LM391 Audio Power Driver

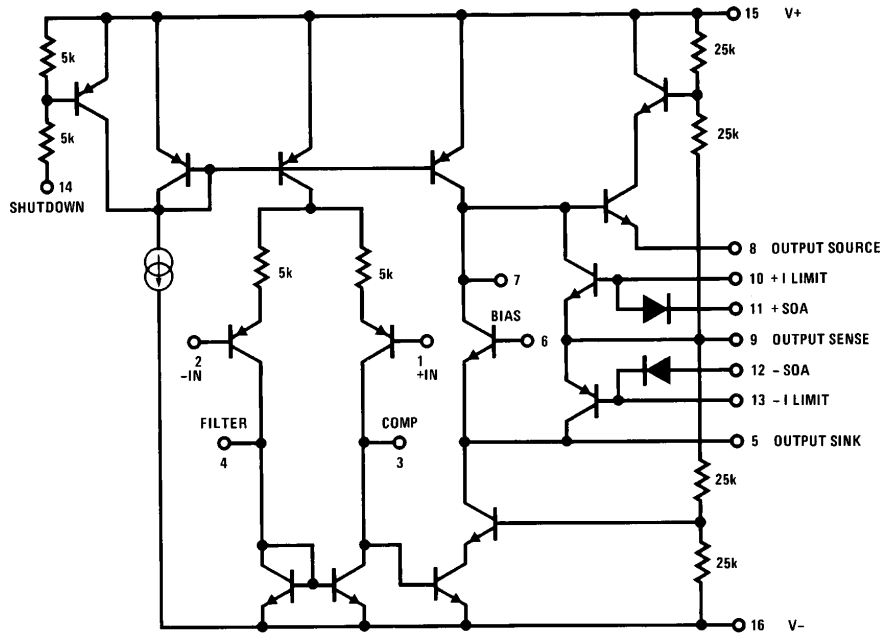
### General Description

The LM391 audio power driver is designed to drive external power transistors in 10 to 100 watt power amplifier designs. High power supply voltage operation and true high fidelity performance distinguish this IC. The LM391 is internally protected for output faults and thermal overloads; circuitry providing output transistor protection is user programmable.

### Features

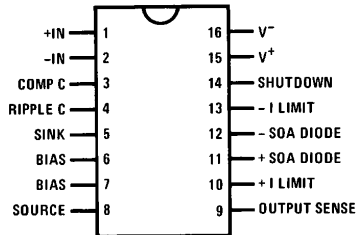
- High Supply Voltage ± 50V max
- Low Distortion 0.01%
- Low Input Noise 3  $\mu$ V
- High Supply Rejection 90 dB
- Gain and Bandwidth Selectable
- Dual Slope SOA Protection
- Shutdown Pin

### Equivalent Schematic and Connection Diagram



TL/H/7146-1

#### Dual-In-Line Package



TL/H/7146-2

#### Top View

Order Number LM391N-100  
See NS Package Number N16A

## Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage LM391N-100	$\pm 50V$ or $+ 100V$	Package Dissipation (Note 1)	1.39W
Input Voltage	Supply Voltage less 5V	Storage Temperature	$-65^{\circ}C$ to $+150^{\circ}C$
Shutdown Current (Pin 14)	1 mA	Operating Temperature	$0^{\circ}C$ to $+70^{\circ}C$
		Lead Temp. (Soldering, 10 sec.)	$260^{\circ}C$
		Thermal Resistance	
		$\theta_{JC}$	$20^{\circ}C/W$
		$\theta_{JA}$	$63^{\circ}C/W$

## Electrical Characteristics $T_A = 25^{\circ}C$ (The following are for $V^+ = 90\% V^+_{MAX}$ and $V^- = 90\% V^-_{MAX}$ .)

Parameter	Conditions	Min	Typ	Max	Units
Quiescent Current LM391N-100	Current in Pin 15 $V_{IN} = 0$		5	6	mA
Output Swing	Positive Negative	$V^+ - 7$ $V^- + 7$	$V^+ - 5$ $V^- + 5$		V
Drive Current	Source (Pin 8) Sink (Pin 5)	5 5			mA mA
Noise (20 Hz–20 kHz)	Input Referred		3		$\mu V$
Supply Rejection	Input Referred	70	90		dB
Total Harmonic Distortion	$f = 1$ kHz $f = 20$ kHz		0.01 0.10	0.25	% %
Intermodulation Distortion	60 Hz, 7 kHz, 4:1		0.01		%
Open Loop Gain	$f = 1$ kHz	1000	5500		V/V
Input Bias Current			0.1	1.0	$\mu A$
Input Offset Voltage			5	20	mV
Positive Current Limit $V_{BE}$	Pin 10–9		650		mV
Negative Current Limit $V_{BE}$	Pin 9–13		650		mV
Positive Current Limit Bias Current	Pin 10		10	100	$\mu A$
Negative Current Limit Bias Current	Pin 13		10	100	$\mu A$

### Pin 14 Current Comments

Minimum pin 14 current required for shutdown is 0.5 mA, and must not exceed 1 mA.

Maximum pin 14 current for amplifier not shut down is 0.05 mA.

The typical shutdown switch point current is 0.2 mA.

**Note 1:** For operation in ambient temperatures above  $25^{\circ}C$ , the device must be derated based on a  $150^{\circ}C$  maximum junction temperature and a thermal resistance of  $90^{\circ}C/W$  junction to ambient.

## Typical Applications

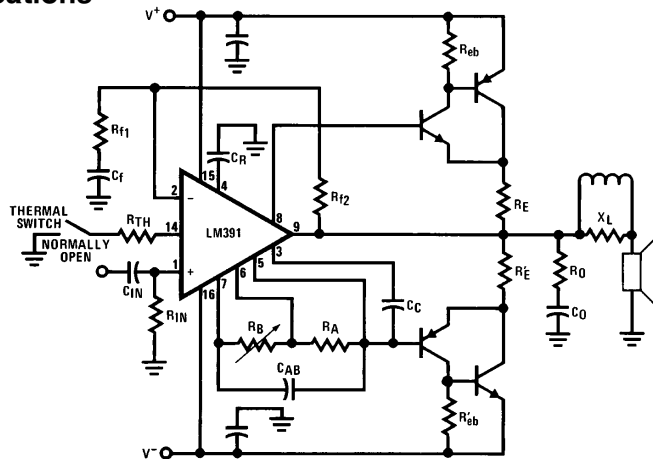
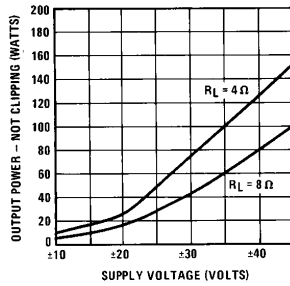


FIGURE 1. LM391 with External Components—Protection Circuitry Not Shown

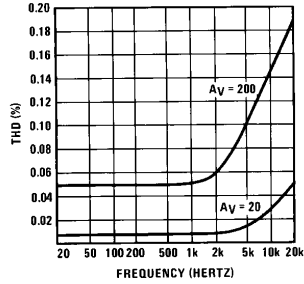
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## Typical Performance Characteristics

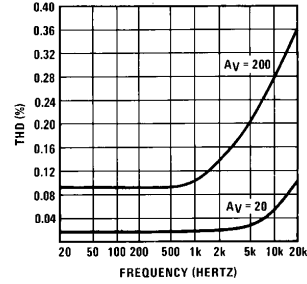
Output Power vs Supply Voltage



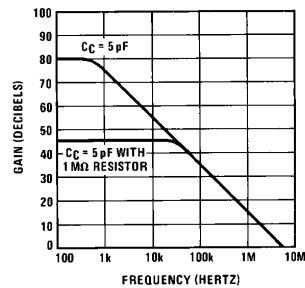
Total Harmonic Distortion vs Frequency ( $R_L = 8\Omega$ )



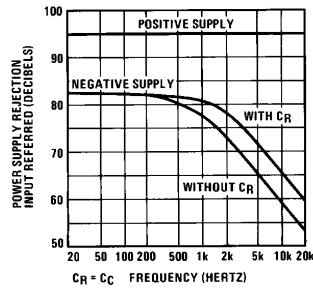
Total Harmonic Distortion vs Frequency ( $R_L = 4\Omega$ )



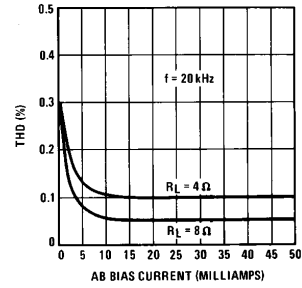
Open Loop Gain vs Frequency



Input Referred Power Supply Rejection vs Frequency



Total Harmonic Distortion vs AB Bias Current



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## Pin Descriptions

Pin No.	Pin Name	Comments
1	+ Input	Audio input
2	- Input	Feedback input
3	Compensation	Sets the dominant pole
4	Ripple Filter	Improves negative supply rejection
5	Sink Output	Drives output devices and is emitter of AB bias $V_{BE}$ multiplier
6	BIAS	Base of $V_{BE}$ multiplier
7	BIAS	Collector of $V_{BE}$ multiplier
8	Source Output	Drives output devices
9	Output Sense	Biases the IC and is used in protection circuits
10	+ Current Limit	Base of positive side protection circuit transistor
11	+ SOA Diode	Diode used for dual slope SOA protection
12	- SOA Diode	Diode used for dual slope SOA protection
13	- Current Limit	Base of negative side protection circuit transistor
14	Shutdown	Shuts off amplifier when current is pulled out of pin
15	$V^+$	Positive supply
16	$V^-$	Negative supply

## External Components (Figure 1)

Component	Typical Value	Comments
$C_{IN}$	1 $\mu$ F	Input coupling capacitor sets a low frequency pole with $R_{IN}$ . $f_L = \frac{1}{2\pi R_{IN} C_{IN}}$
$R_{IN}$	100k	Sets input impedance and DC bias to input.
$R_{f2}$	100k	Feedback resistor; for minimum offset voltage at the output this should be equal to $R_{IN}$ .
$R_{f1}$	5.1k	Feedback resistor that works with $R_{f2}$ to set the voltage gain. $A_V = 1 + \frac{R_{f2}}{R_{f1}}$
$C_f$	10 $\mu$ F	Feedback capacitor. This reduces the gain to unity at DC for minimum offset voltage at the output. Also sets a low frequency pole with $R_{f1}$ . $f_L = \frac{1}{2\pi R_{f1} C_f}$
$C_C$	5 pF	Compensation capacitor. Sets gain bandwidth product and a high frequency pole. $GBW = \frac{1}{2\pi 5000 C_C}, f_h = \frac{GBW}{A_V}$ Max $f_h$ for stable design $\approx$ 500 kHz.
$R_A$	3.9k	AB bias resistor.
$R_B$	10k	AB bias potentiometer. Adjust to set bias current in the output stage.
$C_{AB}$	0.1 $\mu$ F	Bypass capacitor for bias. This improves high frequency distortion and transient response.
$C_R$	5 pF	Ripple capacitor. This improves negative supply rejection at midband and high frequencies. $C_R$ , if used, must equal $C_C$ .
$R_{eb}$	100 $\Omega$	Bleed resistor. This removes stored charge in output transistors.
$R_O$	2.7 $\Omega$	Output compensation resistor. This resistor and $C_O$ compensate the output stage. This value will vary slightly for different output devices.
$C_O$	0.1 $\mu$ F	Output compensation capacitor. This works with $R_O$ to form a zero that cancels $f_\beta$ of the output power transistors.
$R_E$	0.3 $\Omega$	Emitter degeneration resistor. This resistor gives thermal stability to the output stage quiescent current. IRC PW5 type.
$R_{TH}$	39k	Shutdown resistor. Sets the amount of current pulled out of pin 14 during shutdown.
$C_2, C'_2$	1000 pF	Compensation capacitors for protection circuitry.
$X_L$	10 $\Omega$   5 $\mu$ H	Used to isolate capacitive loads, usually 20 turns of wire wrapped around a 10 $\Omega$ , 2W resistor.

## Application Hints

### GENERALIZED AUDIO POWER AMP DESIGN

Given: Power Output  
Load Impedance  
Input Sensitivity  
Input Impedance  
Bandwidth

The power output and load impedance determine the power supply requirements. Output signal swing and current are found from:

$$V_{Opeak} = \sqrt{2 R_L P_O} \quad (1)$$

$$I_{Opeak} = \sqrt{\frac{2 P_O}{R_L}} \quad (2)$$

Add 5 volts to the peak output swing ( $V_{OP}$ ) for transistor voltage to get the supplies, i.e.,  $\pm (V_{OP} + 5V)$  at a current of  $I_{peak}$ . The regulation of the supply determines the unloaded voltage, usually about 15% higher. Supply voltage will also rise 10% during high line conditions.

max supplies  $\approx \pm (V_{Opeak} + 5) (1 + \text{regulation})$  (1.1) (3)

The input sensitivity and output power specs determine the required gain.

$$A_V \geq \frac{\sqrt{P_O R_L}}{V_{IN}} = \frac{V_{ORMS}}{V_{INRMS}} \quad (4)$$

Normally the gain is set between 20 and 200; for a 25 watt, 8 ohm amplifier this results in a sensitivity of 710 mV and 71 mV, respectively. The higher the gain, the higher the THD, as can be seen from the characteristics curves. Higher gain also results in more hum and noise at the output.

The desired input impedance is set by  $R_{IN}$ . Very high values can cause board layout problems and DC offsets at the output. The bandwidth requirements determine the size of  $C_f$  and  $C_C$  as indicated in the external component listing.

The output transistors and drivers must have a breakdown voltage greater than the voltage determined by equation (3). The current gain of the drive and output device must be high enough to supply  $I_{Opeak}$  with 5 mA of drive from the LM391. The power transistors must be able to dissipate approximately 40% of the maximum output power; the drivers must dissipate this amount divided by the current gain of the outputs. See the output transistor selection guide, Table A.

To prevent thermal runaway of the AB bias current the following equation must be valid:

$$\theta_{JA} \leq \frac{R_E (\beta_{MIN} + 1)}{V_{CEQMAX} (K)} \quad (5)$$

where:

$\theta_{JA}$  is the thermal resistance of the driver transistor, junction to ambient, in  $^{\circ}C/W$ .

$R_E$  is the emitter degeneration resistance in ohms.

$\beta_{min}$  is that of the output transistor.

$V_{CEQMAX}$  is the highest possible value of one supply from equation (3).

$K$  is the temperature coefficient of the driver base-emitter voltage, typically 2 mV/ $^{\circ}C$ .

Often the value of  $R_E$  is to be determined and equation (5) is rearranged to be:

$$R_E \geq \frac{\theta_{JA} (V_{CEQMAX}) K}{\beta_{MIN} + 1} \quad (6)$$

The maximum average power dissipation in each output transistor is:

$$\overline{P}_{DMAX} = 0.4 P_{OMAX} \quad (7)$$

The power dissipation in the driver transistor is:

$$\overline{P}_{DRIVER(MAX)} = \frac{\overline{P}_{DMAX}}{\beta_{MIN}} \quad (8)$$

Heat sink requirements are found using the following formulas:

$$\theta_{JA} \leq \frac{T_{JMAX} - T_{AMAX}}{P_D} \quad (9)$$

$$\theta_{SA} \leq \theta_{JA} - \theta_{JC} - \theta_{CS} \quad (10)$$

where:

$T_{JMAX}$  is the maximum transistor junction temperature.

$T_{AMAX}$  is the maximum ambient temperature.

$\theta_{JA}$  is thermal resistance junction to ambient.

$\theta_{SA}$  is thermal resistance sink to ambient.

$\theta_{JC}$  is thermal resistance junction to case.

$\theta_{CS}$  is thermal resistance case to sink, typically 1 $^{\circ}C/W$  for most mountings.

## Application Hints (Continued)

### PROTECTION CIRCUITRY

The protection circuits of the LM391 are very flexible and should be tailored to the output transistor's safe operating area. The protection V-I characteristics, circuitry, and resistor formulas are described below. The diodes from the output to each supply prevent the output voltage from exceeding the supplies and harming the output transistors. The output will do this if the protection circuitry is activated while driving an inductive load.

### TURN-ON DELAY

It is often desirable to delay the turn-ON of the power amplifier. This is easily implemented by putting a resistor in series with a capacitor from pin 14 to ground. The value of the

resistor is set to limit the current to less than 1 mA (the absolute maximum). This resistor with the capacitor gives a time constant of RC. The turn-ON delay is approximately 2 time constants.

Example:

Amplifier with maximum supply of 30V, like the 20W, 8Ω example in the data sheet, requiring a delay of 1 second.

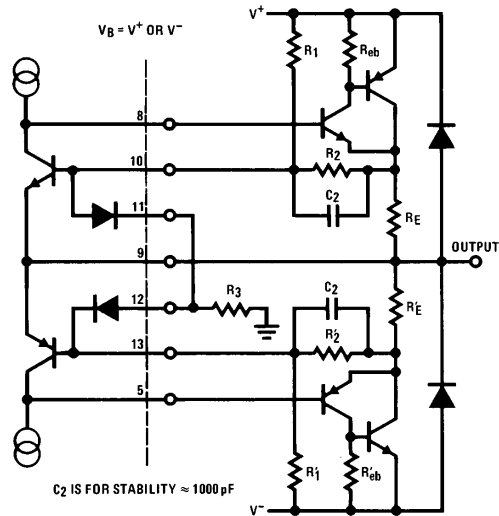
Time delay = 2 RC

$$R = \frac{\text{Max } V^+}{1 \text{ mA}}$$

So:

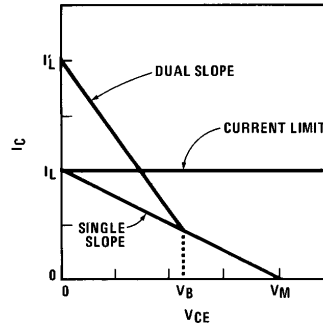
R = 30k. Solving for C gives 16.7 μF. Use C = 20 μF with a 30V rating.

### Protection Circuitry with External Components



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### Protection Characteristics



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### Protection Circuit Resistor Formulas ( $V_B = V^+$ )

Type of Protection	$R_E, R'$	$R_1, R'_1$	$R_2, R'_2$	$R_3, R'_3$
Current Limit	$R_E = \frac{\phi}{I_L}$	Not Required	Short	Not Required
Single Slope SOA Protection	$R_E = \frac{\phi}{I_L}$	$R_1 = R_2 \left( \frac{V_M - \phi}{\phi} \right)$	1 kΩ	Not Required
Dual Slope SOA Protection ( $V_B = V^+$ )	$R_E = \frac{\phi}{I_L}$	$R_1 = R_2 \left( \frac{V_M - \phi}{\phi} \right)$	1 kΩ	$R_3 = R_2 \left[ \frac{V^+}{I_L R_E - \phi} - 1 \right]$

**Note:** φ is the current limit  $V_{BE}$  voltage, 650 mV. Assumptions:  $V^+ \gg \phi$ ,  $V_M \gg \phi$ .  $V^+$  is the load supply voltage.  $V_M$  is the maximum rated  $V_{CE}$  of the output transistors.

## Application Hints (Continued)

### TRANSIENT INTERMODULATION DISTORTION

There has been a lot of interest in recent years about transient intermodulation distortion. Matti Ojala of University of Oulu, Oulu, Finland has published several papers on the subject. The results of these investigations show that the open loop pole of the power amplifier should be above 20 kHz.

To do this with the LM391 is easy. Put a  $1\text{ M}\Omega$  resistor from pin 3 to the output and the open loop gain is reduced to about 46 dB. Now the open loop pole is at 30 kHz. The current in this resistor causes an offset in the input stage that can be cancelled with a resistor from pin 4 to ground. The resistor from pin 4 to ground should be  $910\text{ k}\Omega$  rather than  $1\text{ M}\Omega$  to insure that the shutdown circuitry will operate correctly. The slight difference in resistors results in about 15 mV of offset. The 40W,  $8\Omega$  amplifier schematic shows the hookup of these two resistors.

### BRIDGE AMPLIFIER

A switch can be added to convert a stereo amplifier to a single bridge amplifier. The diagram below shows where the switch and one resistor are added. When operating in the bridge mode the output load is connected between the two outputs, the input is  $V_{IN}\ #1$ , and  $V_{IN}\ #2$  is disconnected.

### OSCILLATIONS & GROUNDING

Most power amplifiers work the first time they are turned on. They also tend to oscillate and have excess THD. Most oscillation problems are due to inadequate supply bypassing and/or ground loops. A  $10\ \mu\text{F}$ , 50V electrolytic on each power supply will stop supply-related oscillations. However, if the signal ground is used for these bypass caps the THD is usually excessive. The signal ground must return to the power supply alone, as must the output load ground. All other grounds—bypass, output R-C, protection, etc., can tie together and then return to supply. This ground is called high frequency ground. On the 40W amplifier schematic all the grounds are labeled.

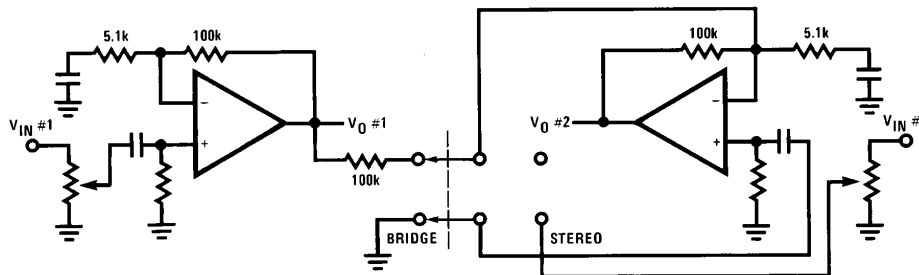
Capacitive loads can cause instabilities, so they are isolated from the amplifier with an inductor and resistor in the output lead.

### AB BIAS CURRENT

To reduce distortion in the output stage, all the transistors are biased ON slightly. This results in class AB operation and reduces the crossover (notch) distortion of the class B stage to a low level, (see performance curve, THD vs AB bias). The potentiometer,  $R_B$ , from pins 6–7 is adjusted to give about 25 mA of current in the output stage. This current is usually monitored at the supply or by measuring the voltage across  $R_E$ .

## Typical Applications (Continued)

Bridge Circuit Diagram



TL/H/7146-7

## Output Transistors Selection Guide

Table A.

Power Output	Driver Transistor		Output Transistor	
	PNP	NPN	PNP	NPN
20W @ $8\Omega$ 30W @ $4\Omega$	MJE711 MJE171 D43C8	MJE721 MJE181 D42C8	TIP42A 2N6490	TIP41A 2N6487
40W @ $8\Omega$ 60W @ $4\Omega$	MJE712 MJE172 D43C11	MJE722 MJE182 D42C11	2N5882	2N5880

## Application Hints (Continued)

### A 20W, 8Ω; 30W, 4Ω AMPLIFIER

Given:

Power Output	20W into 8Ω 30W into 4Ω
Input Sensitivity	1V Max
Input Impedance	100k
Bandwidth	20 Hz–20 kHz ± 0.25 dB

Equations (1) and (2) give:

$$\begin{array}{lll} 20\text{W}/8\Omega & V_{OP} = 17.9\text{V} & I_{OP} = 2.24\text{A} \\ 30\text{W}/4\Omega & V_{OP} = 15.5\text{V} & I_{OP} = 3.87\text{A} \end{array}$$

Therefore the supply required is:

$$\begin{array}{l} \pm 23\text{V} @ 2.24\text{A, reducing to} \dots \\ \pm 21\text{V} @ 3.87\text{A} \end{array}$$

With 15% regulation and high line we get ±29V from equation (3).

Sensitivity and equation (4) set minimum gain:

$$A_V \geq \frac{\sqrt{20 \times 8}}{1} = 12.65$$

We will use a gain of 20 with resulting sensitivity of 632 mV.

Letting  $R_{IN}$  equal 100k gives the required input impedance. For low DC offsets at the output we let  $R_{f2} = 100\text{k}$ . Solving for  $R_{f1}$  gives:

$$\begin{array}{l} R_{f2} = 100\text{k} \\ R_{f1} = \frac{100\text{k}}{20 - 1} = 5.26\text{k}; \text{ use } 5.1\text{k} \end{array}$$

The bandwidth requirement must be stated as a pole, i.e., the 3 dB frequency. Five times away from a pole gives 0.17 dB down, which is better than the required 0.25 dB. Therefore:

$$\begin{array}{l} f_L = \frac{20}{5} = 4 \text{ Hz} \\ f_h = 20\text{k} \times 5 = 100 \text{ kHz} \end{array}$$

Solving for  $C_f$ :

$$C_f \geq \frac{1}{2\pi R_{f1} f_L} = 7.8 \mu\text{F}; \text{ use } 10 \mu\text{F}$$

The recommended value for  $C_C$  is 5 pF for gains of 20 or larger. This gives a gain-bandwidth product of 6.4 MHz and a resulting bandwidth of 320 kHz, better than required.

The breakdown voltage requirement is set by the maximum supply; we need a minimum of 58V and will use 60V. We must now select a 60V power transistor with reasonable beta at  $I_{Opeak}$ , 3.87A. The TIP42, TIP41 complementary pair are 60V, 60W transistors with a minimum beta of 30 at 4A. The driver transistor must supply the base drive given 5 mA drive from the LM391. The MJE711, MJE721 complementary driver transistors are 60V devices with a minimum beta of 40 at 200 mA. The driver transistors should be much faster (higher  $f_T$ ) than the output transistors to insure that the R-C on the output will prevent instability.

To find the heat sink required for each output transistor we use equations (7), (9), and (10):

$$\overline{P}_D = 0.4 (30) = 12\text{W} \quad (7)$$

$$\theta_{JA} \leq \frac{150^\circ\text{C} - 55^\circ\text{C}}{12} = 7.9^\circ\text{C/W} \text{ for } T_{AMAX} = 55^\circ\text{C} \quad (9)$$

$$\theta_{SA} \leq 7.9 - 2.1 - 1.0 = 4.8^\circ\text{C/W} \quad (10)$$

If both transistors are mounted on one heat sink the thermal resistance should be halved to 2.4°C/W.

The maximum average power dissipation in each driver is found using equation (8):

$$\overline{P}_{DRIVER(MAX)} = \frac{12}{30} = 400 \text{ mW}$$

Using equation (9):

$$\theta_{JA} \leq \frac{155 - 55}{0.4} = 237^\circ\text{C/W}$$





## Application Hints (Continued)

### A 40W/8Ω, 60W/4Ω AMPLIFIER

Given:	
Power Output	40W/8Ω 60W/4Ω
Input Sensitivity	1V Max
Input Impedance	100k
Bandwidth	20 Hz–20 kHz ± 0.25 dB

Equations (1) and (2) give:

$$\begin{aligned} 40W/8\Omega \quad V_{O\text{Peak}} &= 25.3V & I_{O\text{Peak}} &= 3.16A \\ 60W/4\Omega \quad V_{O\text{Peak}} &= 21.9V & I_{O\text{Peak}} &= 5.48A \end{aligned}$$

Therefore the supply required is:

$$\begin{aligned} \pm 30.3V @ 3.16A, \text{ reducing to } \dots \\ \pm 26.9V @ 5.48A \end{aligned}$$

With 15% regulation and high line we get ±38.3V using equation (3).

The minimum gain from equation (4) is:

$$A_V \geq 18$$

We select a gain of 20; resulting sensitivity is 900 mV.

The input impedance and bandwidth are the same as the 20 watt amplifier so the components are the same.

$$\begin{aligned} R_{f1} &= 5.1k & R_{fN} &= 100k & C_C &= 5 \mu\text{F} \\ R_{f2} &= 100k & C_f &= 10 \mu\text{F} \end{aligned}$$

The maximum supplies dictate using 80V devices. The 2N5882, 2N5880 pair are 80V, 160W transistors with a minimum beta of 40 at 2A and 20 at 6A. This corresponds to a minimum beta of 22.5 at 5.5A ( $I_{O\text{Peak}}$ ). The MJE712, MJE722 driver pair are 80V transistors with a minimum beta of 50 at 250 mA. This output combination guarantees  $I_{O\text{Peak}}$  with 5 mA from the LM391.

Output transistor heat sink requirements are found using equations (7), (9), and (10):

$$\overline{P}_D = 0.4 (60) = 24W \quad (7)$$

$$\theta_{JA} \leq \frac{200 - 55}{24} = 6.0^\circ\text{C/W for } T_{AMAX} = 55^\circ\text{C} \quad (9)$$

$$\theta_{SA} \leq 6.0 - 1.1 - 1.0 = 3.9^\circ\text{C/W} \quad (10)$$

For both output transistors on one heat sink the thermal resistance should be 1.9°C/W.

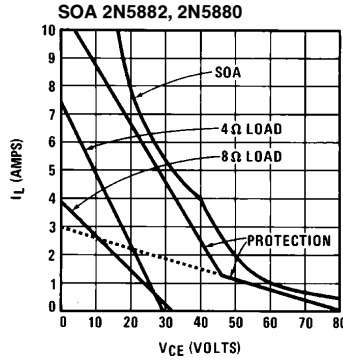
Now using equation (8) we find the power dissipation in the driver:

$$\overline{P}_{\text{DRIVER}} = \frac{24}{20} = 1.2W \quad (8)$$

$$\theta_{JA} \leq \frac{150 - 55}{1.2} = 79^\circ\text{C/W} \quad (9)$$

Since a heat sink is required on the driver, we should investigate the output stage thermal stability at the same time to optimize the design. If we find a value of  $R_E$  that is good for the protection circuitry, we can then use equation (5) to find the heat sink required for the drivers.

The SOA characteristics of the 2N5882, 2N5880 transistors are shown in the following curve along with a desired protection line.



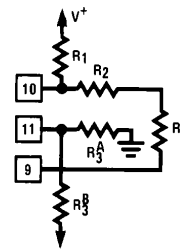
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The desired data points are:

$$V_M = 80V \quad V_B = 47V \quad I_L = 3A \quad I'_L = 11A$$

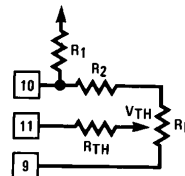
Since the break voltage is not equal to the supply, we will use two resistors to replace  $R_3$  and move  $V_B$ .

#### Circuit Used



TL/H/7146-11

#### Thevenin Equivalent



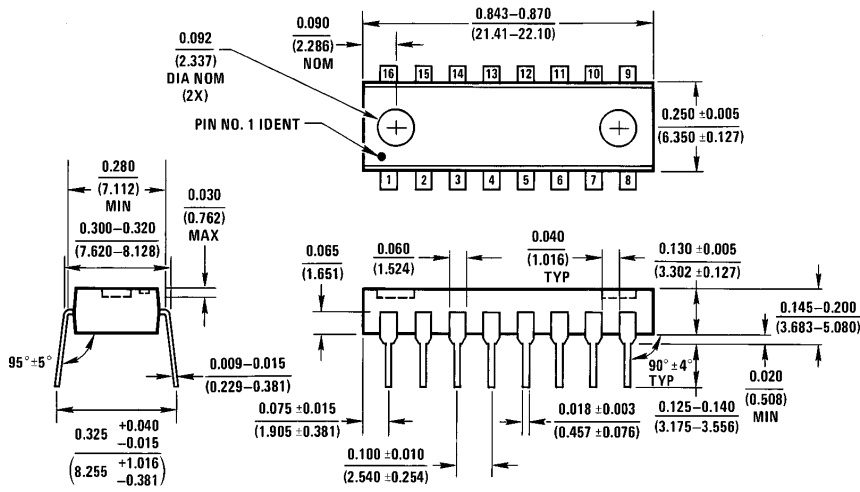
$$\text{Where: } R_{TH} = R_3^A \parallel R_3^B$$

$$V_{TH} = V^- \left[ \frac{R_3^A}{R_3^A + R_3^B} \right]$$

TL/H/7146-12



**Physical Dimensions** inches (millimeters)



**Molded Dual-In-Line Package (N)**  
**Order Number LM391N-100**  
**NS Package Number N16A**

N16A (REV E)

**LIFE SUPPORT POLICY**

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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