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Headphone Driver IC **PT2309**

DESCRIPTION

The PT2309 is a headphone driver IC, it can working on wide supply range. Utilizing CMOS Technology, it has very low power consumption is in stand-by mode. Total harmonic distortion is lower than 0.03% (32Ω load) and the also has low noise output. Built-in mute function can prevents popping sounds happen when power is turned ON or OFF. It is also has built-in over-temperature protection, minimum package size for space saving and suitable for small or portable products.

FEATURES

- CMOS Technology
- Stereo Input
- Drive 32Ω impedance load
- Low noise, Low distortion
- Suppress the pop and click noise when mode changed
- Built-in mute function
- Available in 8 Pins, DIP or SOP Package

APPLICATIONS

- Portable VCD/DVD
- CD-ROM
- PDA
- Sound Card

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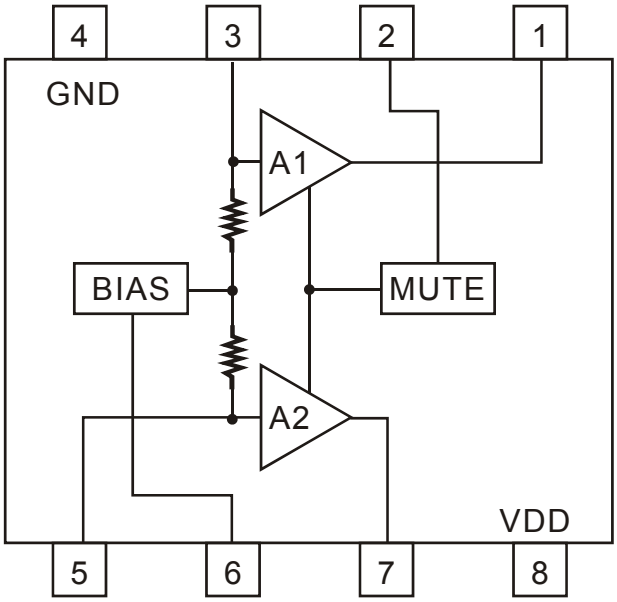
BLOCK DIAGRAM



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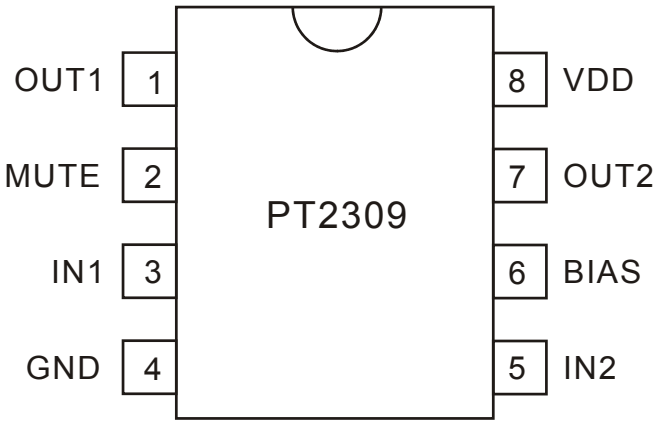
PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
OUT1	O	CH1 Output	1
MUTE	I	Mute Pin	2
IN1	I	CH1 Input	3
GND	-	Ground	4
IN2	I	CH2 Input	5
BIAS	I	Bias Pin	6
OUT2	O	CH2 Output	7
VDD	-	Power Input	8

FUNCTION DESCRIPTION

POWER SUPPLY

The operating voltage of PT2309 is from 3V to 5V, In general operation 5V is recommended.
It should connect a modest bias capacitor nearby the power source terminal. It can improve IC stability and decrease the noise output. Suggestion value of capacitor is from 0.1μF to 10μF.

POP AND CLICK SUPPRESS

For normal operation, the Input/Output port of a power amplifier powered by a single supply voltage must have a stable DC bias. Each time turn on the Vcc the input/output pins will present 1/2 Vcc DC bias voltage. For blocking the DC bias flowing to another circuit, each input/output port should have a DC blocking capacitor, it will charge/discharge when power on or off, the capacitance is relative with the pop noise. In general condition to prevent the pop noise, the time constant of bypass cap (CB) on the bypass pin will be set to maximum. Higher CB value will extend the stable time, and also can suppress the noise heard when power-on. In supply voltage=5V and CB=10μF, stable time is approx 1s. The value of CB also relative with the value of the DC blocking capacitor connected in input terminal. In general condition the time constant of DC blocking capacitor should be less than CB stable time. Recommend parts values please refer to application circuit.

INPUT CAPACITOR

Input capacitor decide the bandwidth and charge time constant, due to there is a 50KΩ impedance, so input terminal charge period constant is:

$$Tin = (2\pi \times 50K\Omega \times Cin)$$

If Cin=1μF, Tin=0.3s, Low frequency lower limit is 3Hz. This capacitor can use a non-polarity SMD capacitor。

OUTPUT CAPACITOR

The headphone driver is designed to drive 32Ω headphone load, it needs a larger capacitance to extending the lower frequency cut off point. If driving a small headphone a 100μF capacitor is a good choice and the low frequency limit is around 50Hz; for better low frequency performance a 220μF capacitor is recommended and it's low frequency can extend to 22Hz. Due to charge/discharge time constant is shorter than CB stable time, so it will not have pop and click noise.

MUTE

When the mute pin is connected to the GND, all of outputs signal will be muted immediately. Connecting the external R/C components on here could prevent the power–on “POP” noises, the mute function also can be active by the external DC voltage.
Due to the built-in pull down resistor (150KΩ), a larger value series resistor connecting to the mute pin may causes mute malfunction because of mute voltage divided by the resistor network. For the detailed connection description please refer to the application circuit.

The attenuation of mute is relation with CB, we suggest CB must be higher then 10μF, the recommend value is 47μF. Higher CB will have better mute characteristic.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Min.	Max.	Unit
Supply Voltage	VDD		0	7	V
Operating Temperature	Topr		-40	+85	℃
Storage Temperature	Tstg		-65	+150	℃
Maximum Input Voltage	Vimax		-0.3	Vcc+0.3	V
Maximum Input Current	Iimax	*	-10	+10	mA

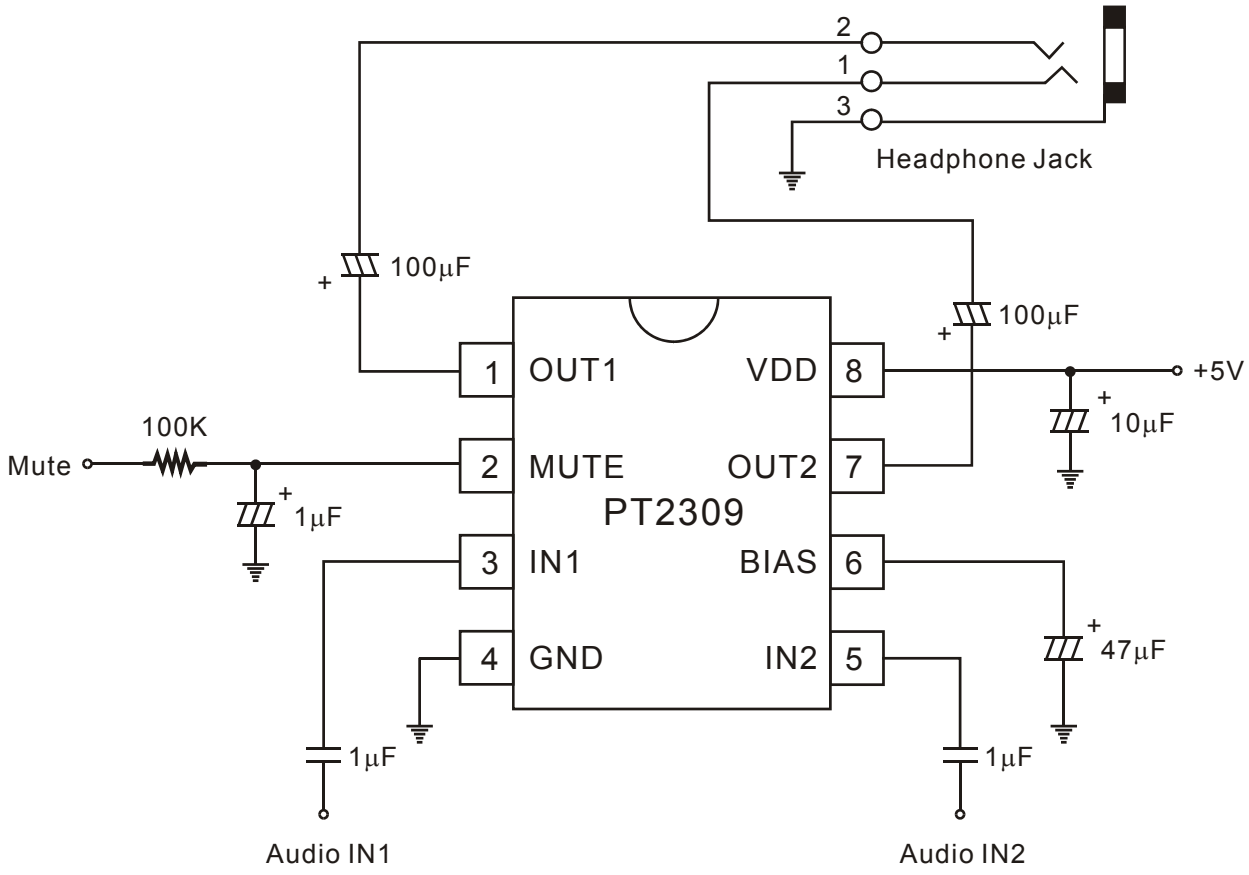
Note: * Input pins surge current can reach 100mA does not induce the CMOS latched up.

ELECTRICAL CHARACTERISTICS

Unless otherwise, Vcc=5V，CB=47μF，bandwidth=22~22KHz

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	VDD		3	5	6	V
Operating Current	Is	Normal Mode	6	7.5	9	mA
		Mute Mode	4.5	6	7.5	mA
Voltage Gain	Vg		-1	0	+1	dB
Two Channels Gain Error	Vgerr		-0.5	0	+0.5	
THD+N	THD	Vin = 1Vrms，RL = 32Ω	0.01	0.03	0.06	%
		Vin = 1Vrms，RL = 5.1KΩ	0.003	0.005	0.01	
Power Output	Po	THD=0.1%，RL=32Ω	35	45	55	mW
		THD=0.1%，RL=16Ω	65	75	85	
Signal-to-Noise Ratio	SNR	Input=GND，A-Weighted	102	105	110	dB
Channel Separation	CS	F=1KHz	90	100	105	dB
		F=100~20KHz	80	90	95	
Power Supply Rejection Ratio	PSRR	Vr=100mVrms，F=100Hz	45	55	65	dB
Mute	mute	MUTE=GND，F=1KHz	60	75	80	dB
Mute Voltage	Vmute	VIH, MUTE= OFF	1	1.1	1.4	Vcc
		VIL, MUTE= ON	0.8	0.9	1	

APPLICATION CIRCUIT



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ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT2309-D	8-Pin, DIP, 300mil	PT2309-D
PT2309-S	8-Pin, SOP, 150mil	PT2309-S
PT2309-D (L)	8-Pin, DIP, 300mil	PT2309-D
PT2309-S (L)	8-Pin, SOP, 150mil	PT2309-S

Notes:
1. (L), (C) or (S) = Lead Free.
2. The Lead Free mark is put in front of the date code.

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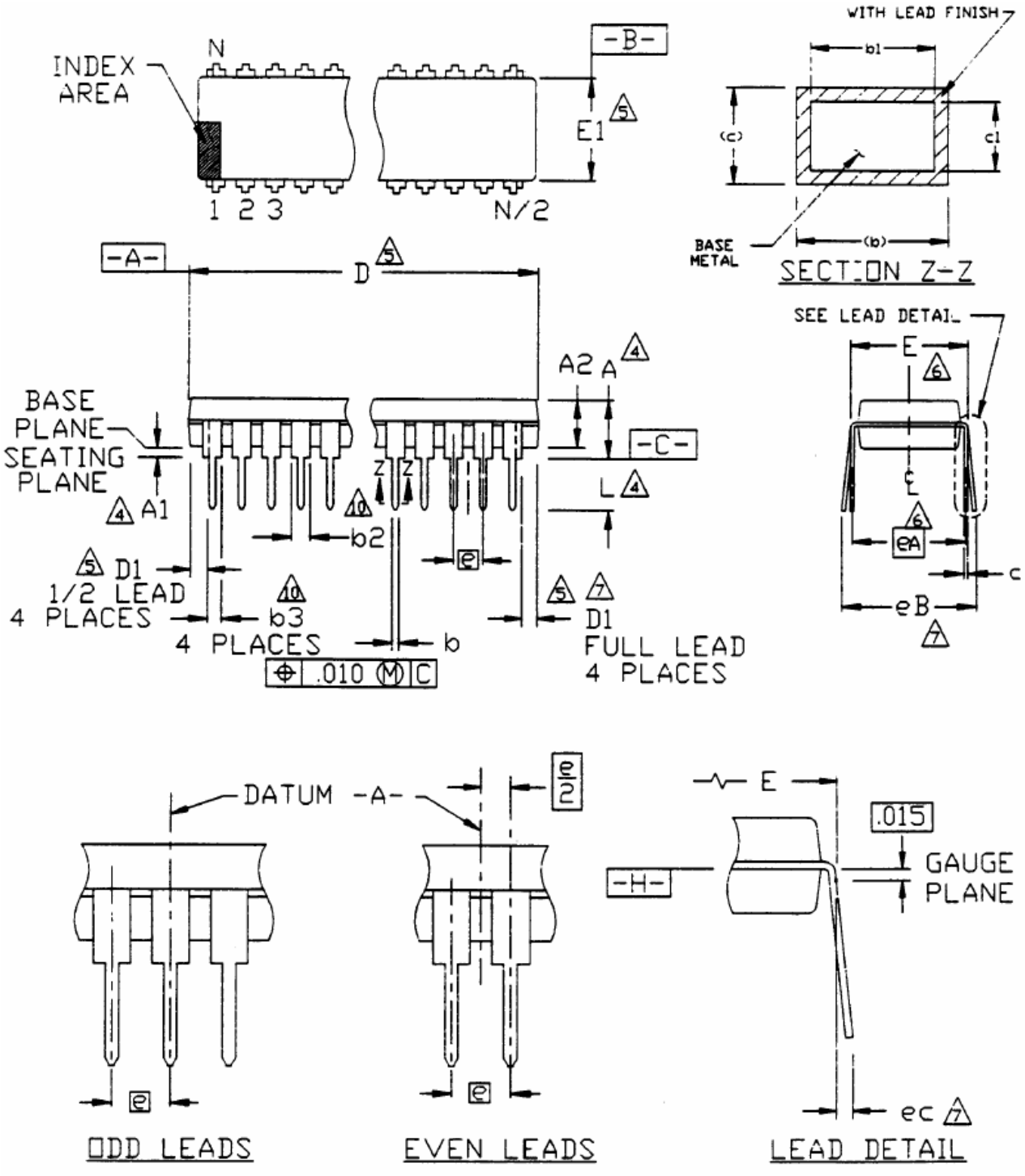
PACKAGE INFORMATION

8 PINS, DIP, 300MIL



Symbol	Min.	Nom.	Max.
A	-	-	0.210
A1	0.015	-	-
A2	0.115	0.130	0.195
b	0.014	0.018	0.022
b1	0.014	0.018	0.020
b2	0.045	0.060	0.070
b3	0.030	0.039	0.045
c	0.008	0.010	0.014
c1	0.008	0.010	0.011
D	0.355	0.365	0.400
D1	0.005	-	
E	0.300	0.310	0.325
E1	0.240	0.250	0.280
e	0.100 bsc.		
eA	0.300 bsc.		
eB	-	-	0.430
eC	0.000	-	0.060
L	0.115	0.130	0.150

Note:
1. Controlling Dimensions: INCHES.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol LIST” in Section 2.2 of Publication No.95.
4. Dimension A, A1 and L are measured with the package seated in JEDEC Seating Plane Gauge GS-3.
5. D, D1 and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch.
6. E and eA measured with the leads constrained to be perpendicular to data -c- .
7. eB and eC are measured at the lead tips with the leads unconstrained.
8. N is the number of leads (N=8)
9. Pointed or rounded lead tips are preferred to ease insertion.
10. b2 and b3 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm)
11. Variation BA has a b3 dimension and is 1/2 lead package.
12. Distance between the leads including dambar protrusions to be 0.005 inch minimum.
13. Datum plane -H- coincident with the bottom of lead, where lead exits the body.
14. Refer to JEDEC MS-001, Variation BA.

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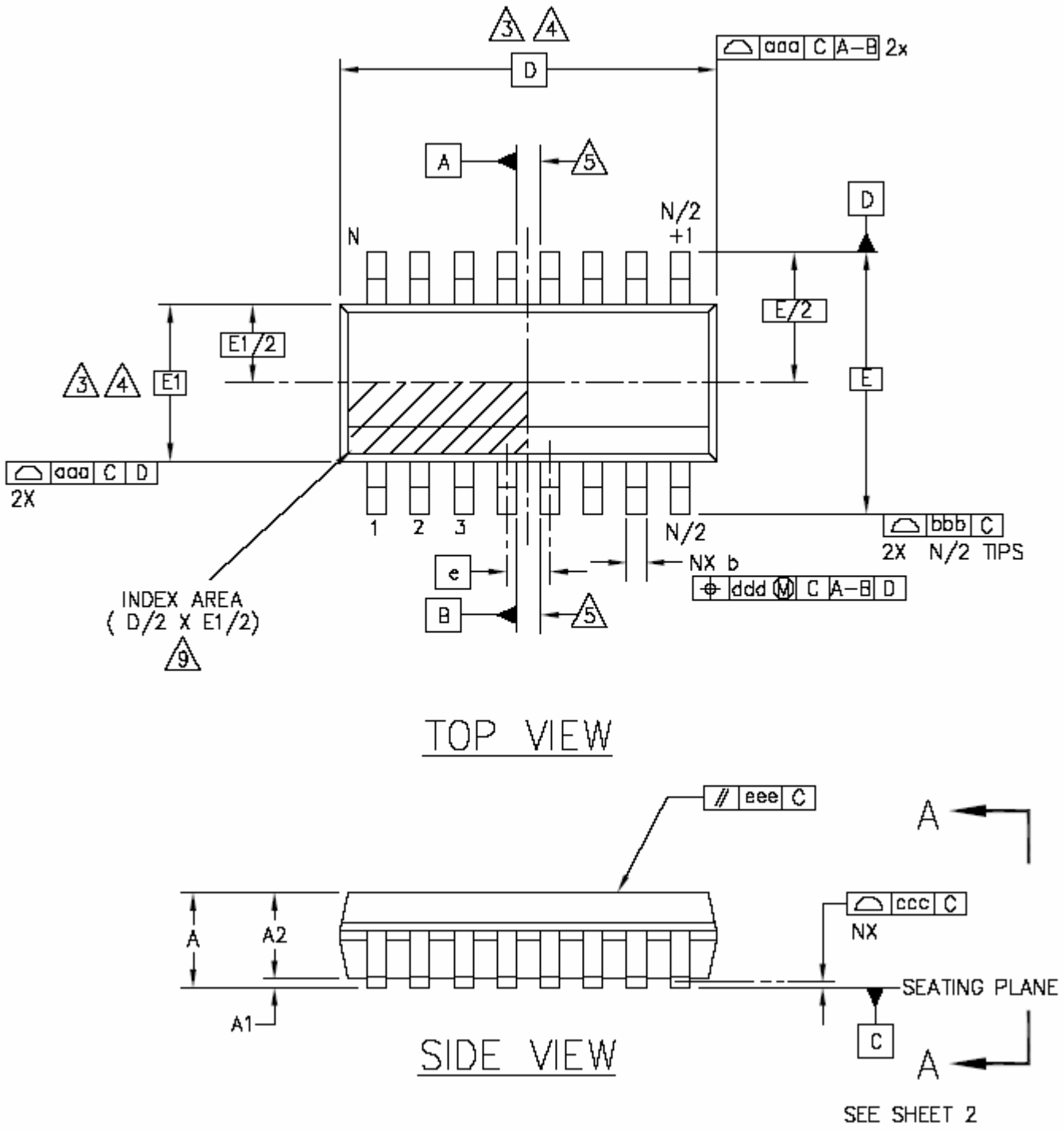
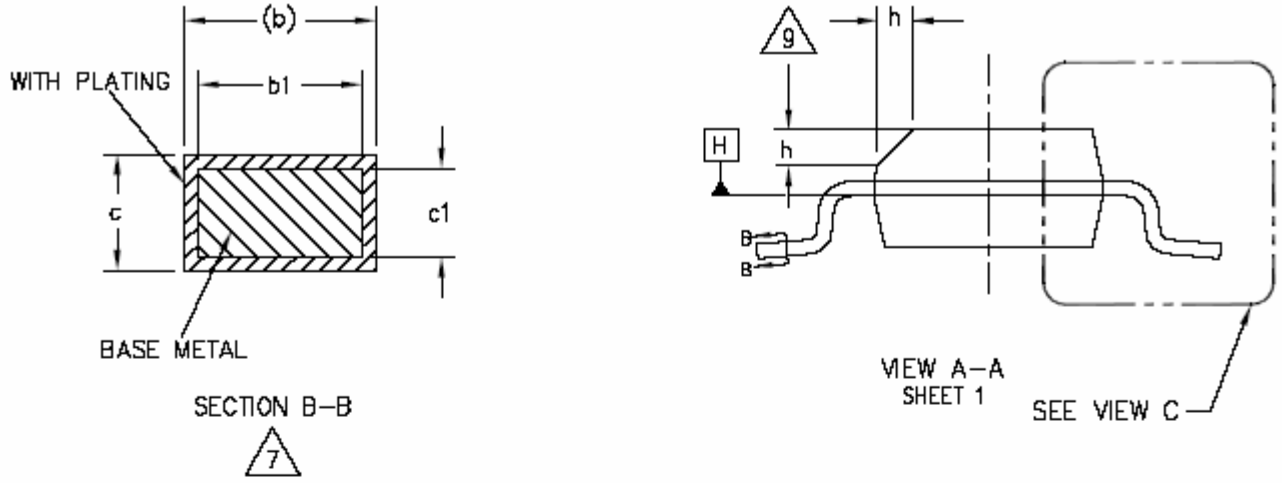
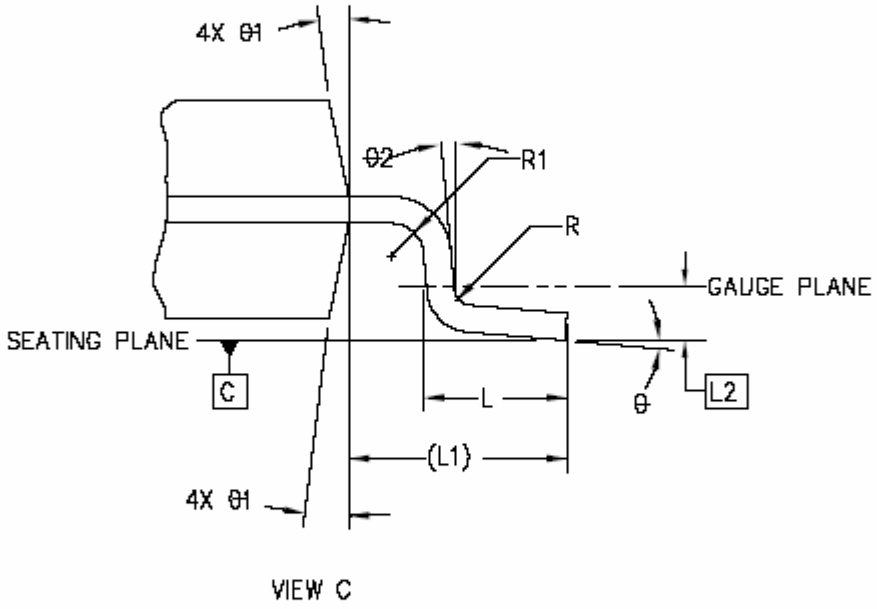
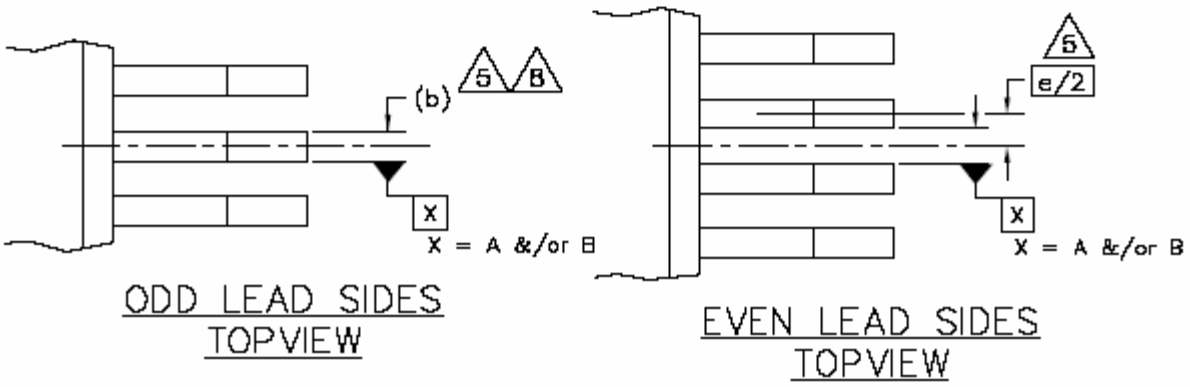
8 PINS, SOP, 150 MIL




(b)
WITH PLATING
b1
c
c1
BASE METAL
SECTION B–B
7
9
h
H
h
B
B
VIEW A–A
SHEET 1
SEE VIEW C


4X θ1
θ2
R1
R
GAUGE PLANE
SEATING PLANE
C
L
θ
L2
(L1)
4X θ1

VIEW C


(b)
5
B
X
X = A &/or B
ODD LEAD SIDES
TOPVIEW
5
e/2
X
X = A &/or B
EVEN LEAD SIDES
TOPVIEW

Symbol	Min.	Typ.	Max.
A	1.35	-	1.75
A1	0.10	-	0.25
A2	1.25	-	1.65
b	0.31	-	0.51
b1	0.28	-	0.48
c	0.17	-	0.25
c1	0.17	-	0.23
D	4.90 BSC.		
E	6.00 BSC.		
E1	3.90 BSC.		
e	1.27 BSC.		
L	0.40	-	1.27
L1	1.04 REF.		
L2	0.25 BSC.		
R	0.07	-	-
R1	0.07		-
h	0.25	-	0.50
θ	0°	-	8°
θ1	5°	-	15°
θ2	0°	-	-

Note:
1. Dimensioning and tolerancing per ANSI Y 14.5M-1994
2. Controlling Dimension: MILLIMETERS.
3. Dimension D does not include mold flash protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm (0.006 in) per end. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side. D and E1 dimensions are determined at datum H.
4. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
5. Datums A & B to be determined at datum H.
6. N is the number of terminal positions. (N=8)
7. The dimensions apply to the flat section of the lead between 0.10 to 0.25mm from the lead tip.
8. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of the “b” dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.
9. This chamfer feature is optional. If it is not present, then a pin 1 identifier must be located within the index area indicated.
10. Refer to JEDEC MS-012, Variation AA.
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