

PHOTO DIODE SIGNAL PROCESSOR FOR COMPACT DISC PLAYERS

GENERAL DESCRIPTION

The TDA5708 is a bipolar integrated circuit designed for use in compact disc players with a single spot read-out system. It amplifies the photo-diode signals and processes the error signals for the focus- and radial control network.

Features

- Data amplifier with equalizer and A.G.C.
- Offset-free pre-amplifier with A.G.C. for the servo signals
- Trackloss and drop-out detection
- Normalizing focus error output signal to minimize radial error interference
- Laser supply amplifier and reference source
- Possibility for car application
- Single and dual supply application
- TTL compatible digital input/outputs

QUICK REFERENCE DATA

Supply voltage range	V_{DD}	8 to 12 V
Quiescent supply current	I_Q	typ. 11 mA
HF input current (peak-to-peak value) for $V_{HFout(p-p)}$	$I_{HFin(p-p)}$	typ. 8 μA
LF input current (for each diode input)	I_D	typ. 2 μA
Laser supply output current	I_{L0}	typ. 2 mA
Operating ambient temperature range	T_{amb}	-30 to +85 $^{\circ}C$

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

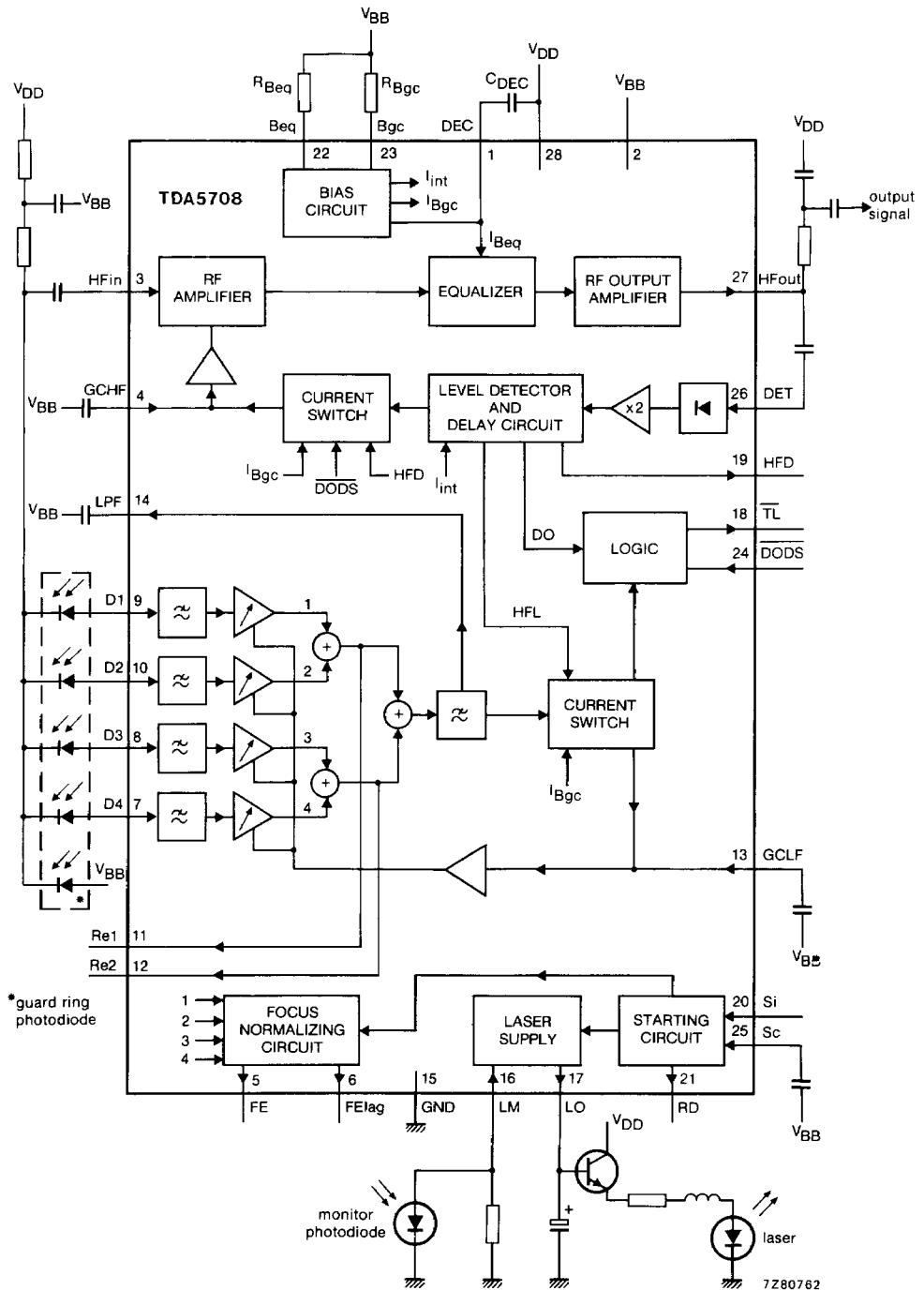


Fig. 1 Block diagram.

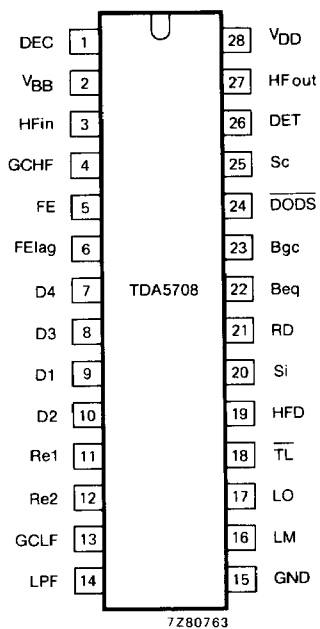


Fig. 2 Pinning diagram; for pin description see next page.

PIN DESCRIPTION

Pin No.	Symbol	Description
1.	DEC	Decoupling bias-current HF part.
2	V _{BB}	Negative supply connection (also substrate connection).
3	HFin	HF current input.
4	GCHF	Gain control input of HF amplifier. Current output from HF amplitude detector.
5	FE	Current output of normalized, switched focus error signal.
6	FE _{lag}	Current output of switched focus error signal, intended for lag network.
7, 8	D4, D3	LF photo diode current input.
9, 10	D1, D2	LF photo diode current input.
11	Re1	Summation of amplified currents D1 and D2.
12	Re2	Summation of amplified currents D3 and D4.
13	GCLF	Gain control input of LF amplifiers. Current output from LF amplitude detector.
14	LPF	Low pass filter for I_{ret} , used in track loss (TL) detector and LF control part ($I_{ret} = I_{Re1} + I_{Re2}$).
15	GND	Laser supply ground. Logic ground.
16	LM	Laser monitor diode input.
17	LO	Laser amplifier current output.
18	$\overline{TL}$	Track loss.
19	HFD	High frequency detector output.
20	Si	On/off control, laser supply and focus circuitry.
21	RD	Ready signal output; starting up procedure finished.
22	Beq	Bias current input for equalizer and HF input parts.
23	Bgc	Bias current input for HF output part and LF gain control, TL and FE circuitry.
24	$\overline{DODS}$	Drop out detector suppression.
25	Sc	Starting up input.
26	DET	HF detector voltage input.
27	HFout	HF amplifier and equalizer voltage output.
28	V _{DD}	Positive supply voltage.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges

pin 28 — pin 2

 V_{DD} —0,3 to + 13 V

pin 15 — pin 2

 V_{GND} —0,3 to + 13 V

pin 16 (open loop)

 V_{LM} V_{BB} to V_{DD} V

Total power dissipation

 P_{tot} see Fig. 3

Storage temperature range

 T_{stg} —55 to + 150 °C

Operating ambient temperature range

 T_{amb} —30 to + 85 °C

Operating junction temperature

 T_j max. 150 °C

DEVELOPMENT DATA

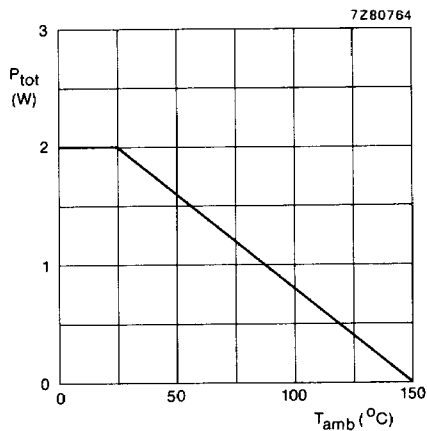


Fig. 3 Power derating curve.

CHARACTERISTICS

$V_{DD} = 10\text{ V}$; $V_{BB} = 0\text{ V}$; $V_{GND} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $R_{Beq} = 12\text{ k}\Omega$; $R_{Bgc} = 24\text{ k}\Omega$; all voltages with respect to V_{BB} ; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage (pin 28)	V_{DD}	8	—	12	V
Laser ground	V_{GND}	V_{BB}	—	$V_{DD} - 3$	V
Quiescent supply current	I_Q	—	11	—	mA
H.F. input (pin 3)					
D.C. voltage level	V_{HFin}	—	1,4	—	V
Input current range (peak-to-peak value) at $f = 100\text{ kHz}$	$I_{HFin(p-p)}$	3	—	10	μA
Input impedance	$ Z_{HFin} $	0,5	1	2	$\text{k}\Omega$
H.F. output (pin 27)					
Output voltage at $I_{HFin} = 0\text{ }\mu\text{A}$; $V_{GCHF} = 2,8\text{ V}$	V_{HFout}	$V_{DD} - 5$	—	$V_{DD} - 3$	V
at $I_{HFin} = 0\text{ }\mu\text{A}$; $V_{GCHF} = 6,3\text{ V}$	V_{HFout}	—	$V_{DD} - 4,4$	—	V
Output voltage (note 1; Fig. 6) (peak-to-peak value) at $I_{HFin(p-p)} = 6\text{ }\mu\text{A}$	$V_{O1(p-p)}$	—	1	—	V
at $I_{HFin(p-p)} = 3\text{ to }10\text{ }\mu\text{A}$	$V_{O(p-p)}$	—	M_1	—	V
Output impedance (note 1; Fig. 6)	$ Z_{HFout} $	—	50	—	Ω
Bias input (pin 22)					
D.C. voltage level at $R_{Beq} = 12\text{ k}\Omega$	V_{Beq}	—	590	—	mV
Input current	I_{Beq}	—	—50	—	μA
Bias input (pin 23)					
D.C. voltage level at $R_{Bgc} = 24\text{ k}\Omega$	V_{Bgc}	—	1,28	—	V
Input current	I_{Bgc}	—	—50	—	μA
Decoupling output (pin 1)					
Output voltage	V_{DEC}	—	$V_{DD} - 1,5$	—	V
Output impedance	$ Z_{DEC} $	—	2	—	$\text{k}\Omega$
Level detector input (pin 26)					
D.C. voltage level	V_{DET}	—	0,82	—	V
Input current range	I_{DET}	—100	—	+ 100	μA
Input impedance	$ Z_{DET} $	—	10	—	$\text{k}\Omega$

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Reference current (HF part)					
Positive reference current (Fig. 7)	I_{refp}	—	55	—	μA
Negative reference current (Fig. 8; note 13)	I_{refn}	—	M5	—	μA
Gain control (pin 4)					
Input voltage for:					
minimum h.f. gain	V_{GCHF}	—	2,8	—	V
maximum h.f. gain	V_{GCHF}	—	6,3	—	V
Input impedance at $V_{\text{GCHF}} = 2,8$ to $6,3$ V	$ Z_{\text{GCHF}} $	—	10	—	$\text{M}\Omega$
Output current					
at $I_{\text{DET}} = 0$; $\overline{\text{DODS}} = \text{HIGH}$ or LOW	I_{GCHF}	—	−0,4	—	μA
at $I_{\text{DET}} < 0,5 I_{\text{refp}}$; $\overline{\text{DODS}} = \text{HIGH}$ or LOW	I_{GCHF}	—	−0,4	—	μA
at $I_{\text{DET}} > 0,5 I_{\text{refp}}$; $\overline{\text{DODS}} = \text{HIGH}$	I_{GCHF}	—	−4,6	—	μA
at $I_{\text{DET}} > 0,5 I_{\text{refp}}$; $\overline{\text{DODS}} = \text{LOW}$	I_{GCHF}	—	−0,4	—	μA
at $I_{\text{DET}} < I_{\text{refp}}$; $\overline{\text{DODS}} = \text{HIGH}$	I_{GCHF}	—	−4,6	—	μA
at $I_{\text{DET}} < I_{\text{refp}}$; $\overline{\text{DODS}} = \text{LOW}$	I_{GCHF}	—	−0,4	—	μA
at $I_{\text{DET}} > I_{\text{refp}}$; $\overline{\text{DODS}} = \text{LOW}$	I_{GCHF}	—	94	—	μA
at $I_{\text{DET}} > I_{\text{refp}}$; $\overline{\text{DODS}} = \text{HIGH}$	I_{GCHF}	—	94	—	μA
at $I_{\text{DET}} > 0,5 I_{\text{refn}}$; $\overline{\text{DODS}} = \text{HIGH}$ or LOW	I_{GCHF}	—	−0,4	—	μA
at $I_{\text{DET}} < 0,5 I_{\text{refn}}$; $\overline{\text{DODS}} = \text{HIGH}$	I_{GCHF}	—	−4,6	—	μA
at $I_{\text{DET}} > I_{\text{refn}}$; $\overline{\text{DODS}} = \text{HIGH}$	I_{GCHF}	—	−4,6	—	μA
at $I_{\text{DET}} < I_{\text{refn}}$; $\overline{\text{DODS}} = \text{HIGH}$	I_{GCHF}	—	94	—	μA
HFD output (pin 19)					
Output voltage LOW					
at $I_{\text{HFD}} = 400 \mu\text{A}$ (sink current); $I_{\text{DET}} < 0,5 I_{\text{refp}}$	V_{HFD}	—	$V_{\text{GND}} + 0,1$	$V_{\text{GND}} + 0,4$	V
Output voltage HIGH					
at $I_{\text{HFD}} = 50 \mu\text{A}$ (source current); $I_{\text{DET}} > 0,5 I_{\text{refp}}$	V_{HFD}	$V_{\text{GND}} + 2,4$	$V_{\text{GND}} + 9,9$	—	V
Output sink current at $I_{\text{DET}} = 0$	I_{HFD}	—	1,5	—	mA
Output source current at $I_{\text{DET}} > 0,5 I_{\text{refp}}$	I_{HFD}	—	−108	—	μA
Delay time (note 2)	τ_1, τ_2	—	15	—	μs

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
L.F. photo diode inputs (pins 7 to 10) (values given for each input)					
D.C. voltage level	V_D	—	1,5	—	V
Input current range	I_D	0	—	6	μA
Input impedance at 1 MHz; $I_D = 1 \mu A$	$ Z_D $	—	2	—	k Ω
Gain control (pin 13)					
Input voltage for: minimum l.f. gain	V_{GCLF}	—	3	—	V
maximum l.f. gain	V_{GCLF}	—	$V_{DD} - 1,5$	—	V
Input impedance	$ Z_{GCLF} $	—	4	—	M Ω
Output current (note 3) at $I_{DET} < 0,625 I_{refp}$	I_{GCLF}	—	$-0,1 I_{Bgc}$	—	μA
at $I_{DET} > 0,625 I_{refp}$ $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 0$	I_{GCLF}	—	$-1,1 I_{Bgc}$	—	μA
at $I_{DET} > 0,625 I_{refp}$ $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 1 \mu A$	I_{GCLF}	—	$M_4 - 2,1 I_{Bgc}$	—	μA
Re1, Re2 outputs (pin 11, pin 12)					
Output current (see Fig. 9) at $I_{D1} = I_{D2} = 0$; $I_{D3} = I_{D4} = 1 \mu A$; $V_{GCLF} = V_{DD}$	I_{Re2}	—	136	170	μA
at $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 0$; $V_{GCLF} = V_{DD}$	I_{Re2}	—	0	—	μA
at $I_{D1} = I_{D2} = 1 \mu A$; $I_{D3} = I_{D4} = 0$; $V_{GCLF} = V_{DD}$	I_{Re1}	—	136	170	μA
at $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 0$; $V_{GCLF} = V_{DD}$	I_{Re1}	—	0	—	μA
Output voltage at $V_{GCLF} = V_{DD}$; $I_{Re1} = 150 \mu A$	V_{Re1}	—	$V_{BB} + 1,4$	—	V
at $V_{GCLF} = V_{DD}$; $I_{Re2} = 150 \mu A$	V_{Re2}	—	$V_{BB} + 1,4$	—	V
Output impedance (pin 11)	$ Z_{Re1} $	—	5	—	M Ω
Output impedance (pin 12)	$ Z_{Re2} $	—	5	—	M Ω
LPF output (pin 14)					
D.C. voltage level	V_{LPF}	—	3	—	V
Input impedance	$ Z_{LPF} $	—	2	—	k Ω

parameter	symbol	min.	typ.	max.	unit
FElag output (pin 6)					
Output voltage					
at $V_{Sc} = V_{GCLF} = V_{DD}$; $I_{FElag} = +100 \mu A$	V_{FElag}	—	—	$V_{BB} + 1$	V
at $V_{Sc} = V_{GCLF} = V_{DD}$; $I_{FElag} = -100 \mu A$	V_{FElag}	$V_{DD} - 1,5$	—	—	V
Output impedance	$ Z_{FElag} $	—	4	—	M Ω
Output current (Fig. 10)					
at $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 1 \mu A$; $V_{Sc} = V_{DD}$	I_{FElag}	—	0	—	μA
at $I_{D1} = I_{D4} = 1 \mu A$; $I_{D2} = I_{D3} = 1 \mu A$; $V_{Sc} = V_{DD}$	I_{FElag}	—	-130	—	μA
at $I_{D1} = I_{D4} = 1 \mu A$; $I_{D2} = I_{D3} = 2 \mu A$; $V_{Sc} = V_{BB} + 0,7 V$	I_{FElag}	—	0	—	μA
at $I_{D1} = I_{D4} = 2 \mu A$; $I_{D2} = I_{D3} = 1 \mu A$; $V_{Sc} = V_{DD}$	I_{FElag}	—	130	—	μA
at $I_{D1} = I_{D4} = 2 \mu A$; $I_{D2} = I_{D3} = 1 \mu A$; $V_{Sc} = V_{BB} + 0,7 V$	I_{FElag}	—	0	—	μA
FE output (pin 5)					
Output voltage					
at $V_{Sc} = V_{GCLF} = V_{DD}$; $I_{FE} = +100 \mu A$	V_{FE}	—	—	$V_{BB} + 1$	V
at $V_{Sc} = V_{GCLF} = V_{DD}$; $I_{FE} = -100 \mu A$	V_{FE}	$V_{DD} - 1,5$	—	—	V
Output impedance	$ Z_{FE} $	—	4	—	M Ω
Output current (see Fig. 10)					
at $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 1 \mu A$; $V_{Sc} = V_{DD}$	I_{FE}	—	0	—	μA
at $I_{D1} = I_{D4} = 1 \mu A$; $I_{D2} = I_{D3} = 2 \mu A$; $V_{Sc} = V_{DD}$	I_{FE}	—	-66	—	μA
at $I_{D1} = I_{D4} = 2 \mu A$; $I_{D2} = I_{D3} = 1 \mu A$; $V_{Sc} = V_{DD}$	I_{FE}	—	66	—	μA
at $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 1 \mu A$; $V_{Sc} = V_{BB} + 0,7 V$; $V_{Si} = LOW$	I_{FE}	—	-300	—	μA
at $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 1 \mu A$; $V_{Sc} = V_{BB} + 1,4 V$; $V_{Si} = LOW$	I_{FE}	—	-100	—	μA
$\overline{DODS}$ logic input (pin 24)					
Switching levels					
input voltage LOW	$\overline{V_{DODS}}$	—	—	$V_{GND} + 0,8$	V
input voltage HIGH	$\overline{V_{DODS}}$	$V_{GND} + 2$	—	—	V
Input source current	$\overline{I_{DODS}}$	—	-29	—	μA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Starting input (pin 25)					
Output voltage at $V_{Si} = \text{LOW}$	V_{Sc}	—	—	$V_{BB} + 0,7$	V
at $V_{Si} = \text{HIGH}$	V_{Sc}	$V_{DD} - 0,5$	—	—	V
Output source current at $V_{Si} = \text{LOW}$	I_{Sc}	—	—1	—	μA
Output sink current at $V_{Si} = \text{HIGH}$	I_{Sc}	—	1,2	—	mA
Si logic input (pin 20)					
Switching levels					
input voltage LOW	V_{Si}	—	—	$V_{GND} + 0,8$	V
input voltage HIGH	V_{Si}	$V_{GND} + 2$	—	—	V
Input source current	I_{Si}	—	—29	—	μA
TL logic output (pin 18)					
Output voltage level LOW (see Table 1) at $I_{TL} = 400 \mu\text{A}$ (sink current)	V_{TL}	—	—	$V_{GND} + 0,4$	V
Output voltage level HIGH (see Table 1) at $I_{TL} = 50 \mu\text{A}$ (source current)	V_{TL}	$V_{GND} + 2,4$	—	—	V
Output sink current at $V_{TL} = \text{LOW}$	I_{TL}	—	2	—	mA
Output source current at $V_{TL} = \text{HIGH}$	I_{TL}	—	—100	—	μA
Delay times (note 4)	τ_3, τ_4	—	15	—	μs
Delay times (note 4)	τ_5, τ_6	—	15	—	μs
RD logic output (pin 21)					
Output voltage level LOW (see Table 2) at $I_{RD} = 400 \mu\text{A}$ (sink current)	V_{RD}	—	—	$V_{GND} + 0,4$	V
Output voltage level HIGH (see Table 2) at $I_{RD} = 50 \mu\text{A}$ (source current; $V_{Sc} = 3 \text{ V}; V_{Si} = \text{LOW}$)	V_{RD}	$V_{GND} + 2,4$	—	—	V
Output sink current at $V_{Sc} = V_{DD}; V_{Si} = \text{HIGH}$	I_{RD}	—	2,9	—	mA
Output source current at $V_{Sc} = V_{DD}; V_{Si} = \text{LOW}$	I_{RD}	—	—105	—	μA

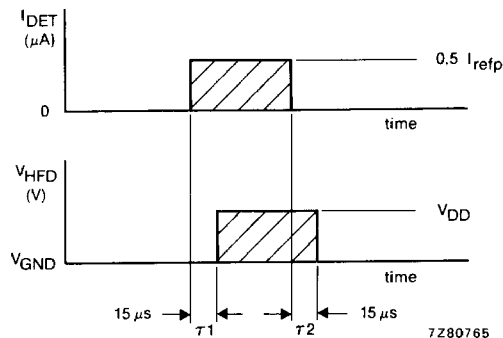
parameter	symbol	min.	typ.	max.	unit
LO output (pin 17) (see Figs 11 and 12)					
Output voltage ($V_{DD} - V_{LO}$)	V_{LO}	0,5	—	25	V
Output impedance	$ Z_{LO} $	—	95	—	k Ω
Output leakage current at $V_{Si} = \text{HIGH}$	I_{LO}	—	—	-10	μA
Maximum output current at $V_{Si} = \text{LOW}$	I_{LO}	—	-4,5	—	mA
LM input (pin 16) (see Figs 11 and 12)					
Input voltage ($V_{LM} - V_{GND}$) (closed loop conditions)	V_{LM}	170	188	220	mV
Input bias current	I_{LM}	—	—	-2	μA
H.F. part					
D.C. characteristics					
$G1 = \frac{\Delta V_{HFout}}{\Delta I_{HFin}} ; I_{HFin} \leq 1 \mu\text{A}$					
at $\Delta I_{HFin} = 1 \mu\text{A}; V_{GCHF} = 6,3 \text{ V}$	$G1(\text{max})$	—	$45 \cdot 10^4$	—	V/A
at $\Delta I_{HFin} = 1 \mu\text{A}; V_{GCHF} = 2,8 \text{ V}$	$G1(\text{min})$	—	0	—	V/A
A.C. characteristics (see Fig. 13)					
$G2 = 20 \log \frac{V_{01}}{V_{02}} ; (\text{note } 5)$					
	$G2$	—	6	—	dB
Phase of input/output signal at 1 MHz (note 6)	ϕ	—	$\pi/2$	—	rad.
Group delay (note 6) at $f_{HFin} = 300 \text{ kHz} + \Delta f$	τ_{300}	—	270	—	ns
Flatness (note 6) between 0,1 and 1 MHz	$\Delta\tau$	—	0	—	ns
LF part					
Maximum d.c. gain (note 7; Fig. 9)					
for: $A_1 = \left \frac{I_{Re2}}{I_{D3} + I_{D4}} \right ;$					
$I_{D1} = I_{D2} = 0; V_{GCLF} = 6,3 \text{ V}$					
at $I_{D3} = 0 \mu\text{A}; I_{D4} = 1 \mu\text{A}$	A_1	—	68	—	
at $I_{D3} = 1 \mu\text{A}; I_{D4} = 0 \mu\text{A}$	A_1	$M_2 - 10\%$	M_2	$M_2 + 10\%$	
for: $A_2 = \left \frac{I_{Re1}}{I_{D1} + I_{D2}} \right ;$					
$I_{D3} = I_{D4} = 0; V_{GCLF} = 6,3 \text{ V}$					
at $I_{D1} = 0 \mu\text{A}; I_{D2} = 1 \mu\text{A}$	A_2	$M_2 - 10\%$	M_2	$M_2 + 10\%$	
at $I_{D1} = 1 \mu\text{A}; I_{D2} = 0 \mu\text{A}$	A_2	$M_2 - 10\%$	M_2	$M_2 + 10\%$	

CHARACTERISTICS (continued)

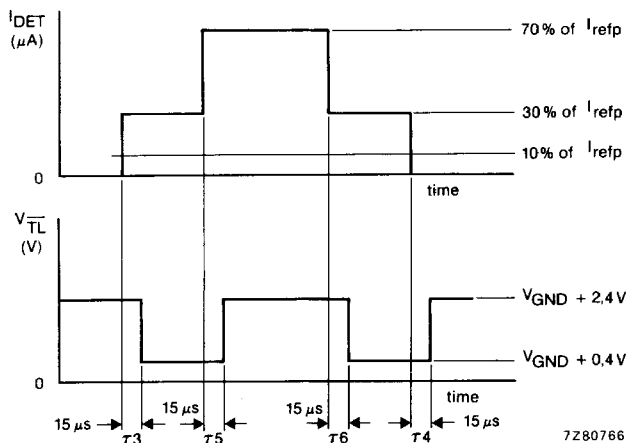
parameter	symbol	min.	typ.	max.	unit
LF part (continued)					
Minimum d.c. gain (note 8; Fig. 9)					
for: $A_3 = \left \frac{I_{Re2}}{I_{D3} + I_{D4}} \right ;$					
$I_{D1} = I_{D2} = 0; V_{GCLF} = 3,0 \text{ V}$					
at $I_{D3} = 0 \text{ } \mu\text{A}; I_{D4} = 1 \text{ } \mu\text{A}$	A_3	—	0,5	—	
at $I_{D3} = 1 \text{ } \mu\text{A}; I_{D4} = 0 \text{ } \mu\text{A}$	A_3	$M_3 - 10\%$	M_3	$M_3 + 10\%$	
for: $A_4 = \left \frac{I_{Re1}}{I_{D1} + I_{D2}} \right ;$					
$I_{D4} = I_{D3} = 0; V_{GCLF} = 3,0 \text{ V}$					
at $I_{D1} = 0 \text{ } \mu\text{A}; I_{D2} = 1 \text{ } \mu\text{A}$	A_4	$M_3 - 10\%$	M_3	$M_3 + 10\%$	
at $I_{D1} = 1 \text{ } \mu\text{A}; I_{D2} = 0 \text{ } \mu\text{A}$	A_4	$M_3 - 10\%$	M_3	$M_3 + 10\%$	
A.C. gain (note 9; Fig. 14)					
for $G_4 = 20 \log P_1; I_{D3} = I_{D4} = 0$					
at $I_{D1} = 0; I_{D2(p-p)} = 1 \text{ } \mu\text{A}$	G_4	—	−3,3	—	dB
at $I_{D1(p-p)} = 1 \text{ } \mu\text{A}; I_{D2} = 0$	G_4	—	−3,3	—	dB
A.C. gain (note 10; Fig. 14)					
for $G_5 = 20 \log P_2; I_{D1} = I_{D2} = 0$					
at $I_{D3} = 0; I_{D4(p-p)} = 1 \text{ } \mu\text{A}$	G_5	—	−3,3	—	dB
at $I_{D3(p-p)} = 1 \text{ } \mu\text{A}; I_{D4} = 0$	G_5	—	−3,3	—	dB
Reference current					
(closed loop conditions; see Fig. 15)					
$I_{ret} = I_{Re1} + I_{Re2}$					
at $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 2 \text{ } \mu\text{A}$	I_{ret}	—	200	—	μA
Laser supply					
Transconductance					
For d.c. (note 11)					
at $V_{S1} = \text{LOW}$	G_{LDC}	—	0,5	—	A/V
at $V_{Si} = \text{HIGH}$	G_{LDC}	—	0	—	A/V
For a.c. (note 12)					
delay time	τ_{11}	—	tbf	—	ns

Notes to the characteristics

1. H.F. part output voltage and output impedance for closed loop conditions: $f_{HFin} = 0,1$ to 1 MHz.
 M_1 is the measured value of V_{O1} .
2. HFD delay times τ_1 and τ_2 measured as shown in Fig. 4.

Fig. 4 Delay time τ between I_{DET} and V_{HFD} .

3. $M_4 = \frac{(I_{D1} + I_{D2} + I_{D3} + I_{D4})}{2}$. M_2 ; (M_2 see note 7) with $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 1 \mu A$ and $Re1$, $Re2$ connected to $1,5$ V.
4. $\overline{TL}$ delay times τ_3 , τ_4 , τ_5 and τ_6 measured as shown in Fig. 5.

Fig. 5 Delay times between I_{DET} and $V_{\overline{TL}}$.

5. Voltage output signal V_{O1} measured at $f_{HFin} = 100$ kHz; $I_{HFin(p-p)} = 3 \mu A$; $V_{GCHF} = 6,3$ V.
Voltage output signal V_{O2} measured at $f_{HFin} = 1$ MHz; $I_{HFin(p-p)} = 3 \mu A$; $V_{GCHF} = 6,3$ V.

Notes to the characteristics (continued)

6. Phase of input/output signal, group delay and flatness measured at $I_{HFin(p-p)} = 1 \mu A$; $V_{GCHF} = 6,3 V$.

$$\text{Group delay: } \tau = \frac{d\phi}{d\omega}; \Delta f \approx 50 \text{ kHz.}$$

$$\text{Flatness: } \Delta\tau = \tau_{\max} - \tau_{\min}.$$

7. M_2 is the measured value of $A_1 = \left| \frac{I_{Re2}}{I_{D3} + I_{D4}} \right|$
for $I_{D1} = I_{D2} = I_{D3} = 0$; $I_{D4} = 1 \mu A$ and $V_{GCLF} = 6,3 V$.

8. M_3 is the measured value of $A_3 = \left| \frac{I_{Re2}}{I_{D3} + I_{D4}} \right|$
for $I_{D1} = I_{D2} = I_{D3} = 0$; $I_{D4} = 1 \mu A$ and $V_{GCLF} = 3,0 V$.

9. P_1 is the measured value of $\frac{I_{Re1} (1)}{I_{D1} (1) + I_{D2} (1)} \cdot \frac{I_{D1} (2) + I_{D2} (2)}{I_{Re1} (2)}$

Where:

(1) are the current levels at $f_i = 25 \text{ kHz}$.

(2) are the current levels at $f_i = 1 \text{ kHz}$.

Measured taken at $V_{GCLF} = 6,3 V$.

10. P_2 is the measured value of $\frac{I_{Re2} (1)}{I_{D3} (1) + I_{D4} (1)} \cdot \frac{I_{D3} (2) + I_{D4} (2)}{I_{Re2} (2)}$

Where:

(1) are the current levels at $f_i = 25 \text{ kHz}$.

(2) are the current levels at $f_i = 1 \text{ kHz}$.

Measured taken at $V_{GCLF} = 6,3 V$.

11. Laser supply transconductance for d.c.

$$G_{LDC} = \frac{\Delta I_{LO}}{\Delta V_{LM}} \quad (0 < -I_{LO} < 2 \text{ mA}).$$

12. Laser supply transconductance for a.c.

$$G_{LAC} = G_{LDC} \cdot \frac{1}{1 + S \cdot \tau_{11}}$$

Where: S is the laplace operator in the frequency domain.

13. M_5 is the measured value of I_{refp} .

Table 1 Test conditions for track loss output ($\overline{\text{TL}}$)

conditions	$\overline{\text{DODS}}$	inputs		output level $\overline{\text{TL}}$
		$I_{\text{D(tot)}}$	I_{DET}	
1	HIGH	$< 4,9 I_{\text{Bgc}}$	independent	HIGH
2	HIGH	$> 5,1 I_{\text{Bgc}}$	10% of I_{refp}	HIGH
3	HIGH	$> 5,1 I_{\text{Bgc}}$	30% of I_{refp}	LOW
4	HIGH	$> 5,1 I_{\text{Bgc}}$	70% of I_{refp}	HIGH
5	LOW	$< 4,9 I_{\text{Bgc}}$	independent	HIGH
6	LOW	$> 5,1 I_{\text{Bgc}}$	10% of I_{refp}	LOW
7	LOW	$> 5,1 I_{\text{Bgc}}$	30% of I_{refp}	LOW
8	LOW	$> 5,1 I_{\text{Bgc}}$	70% of I_{refp}	HIGH

Where:

$$\overline{\text{DODS}} = \text{HIGH} \quad \overline{\text{DODS}} \geq V_{\text{GND}} + 2,4 \text{ V.}$$

$$\overline{\text{DODS}} = \text{LOW} \quad \overline{\text{DODS}} \leq V_{\text{GND}} + 0,8 \text{ V.}$$

$$I_{\text{D(tot)}} = (I_{\text{D1}} + I_{\text{D2}} + I_{\text{D3}} + I_{\text{D4}}) \cdot G3 \cdot G4 \cdot G5.$$

For G3, G4, G5 see transfer functions description of TDA5708.

Table 2 Test condition for ready output (RD)

conditions	inputs		output level RD
	V_{Sc}	V_{Si}	
1	$\geq 4V_j + V_{\text{OFF}}$	HIGH	LOW
2	$\leq 4V_j - V_{\text{OFF}}$	HIGH	LOW
3	$\geq 4V_j + V_{\text{OFF}}$	LOW	HIGH
4	$\leq 4V_j - V_{\text{OFF}}$	LOW	LOW

Where:

$$V_{\text{OFF}} \approx 120 \text{ mV.}$$

 V_j is the junction voltage (0,7 V typ.).

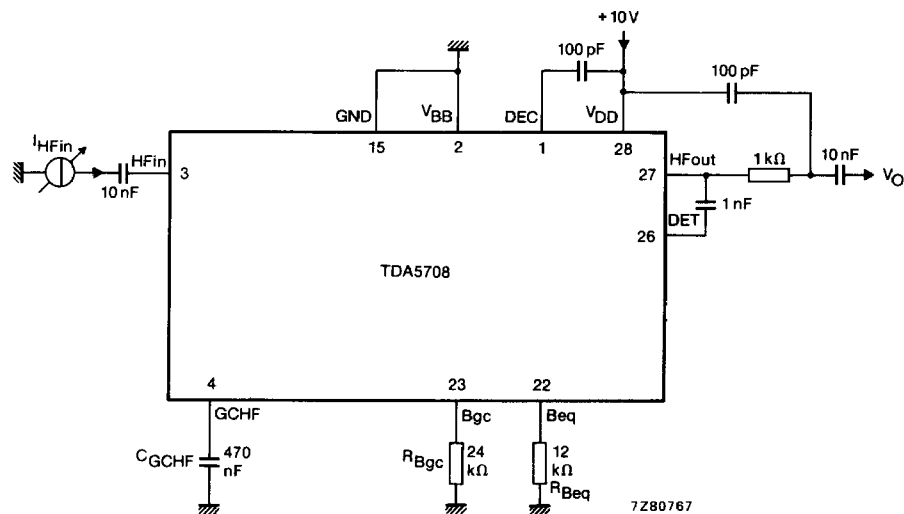
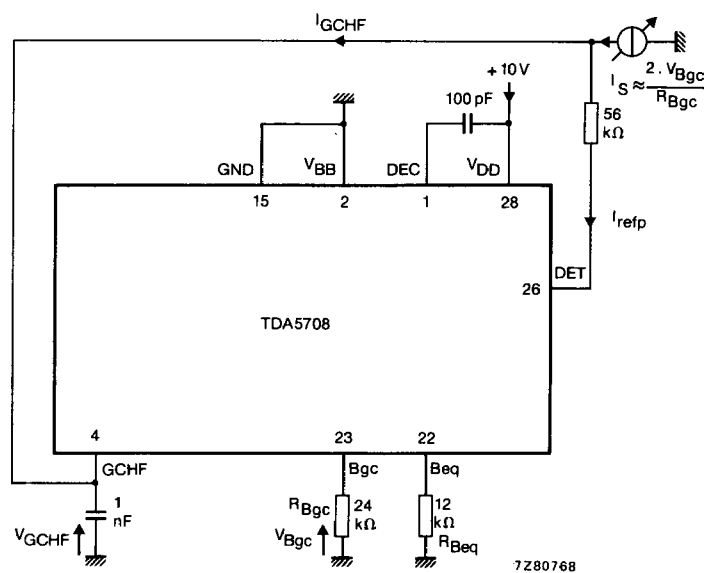
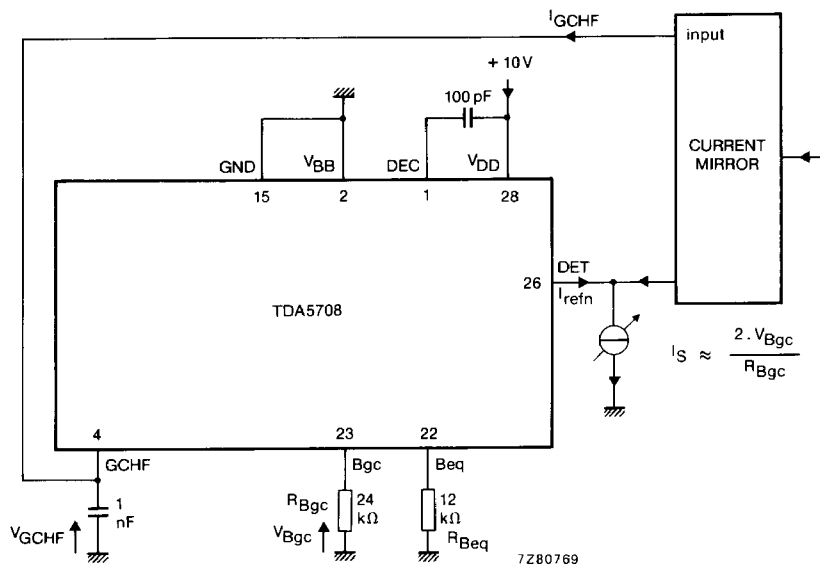


Fig. 6 Test circuit for HF-part; closed-loop condition.



Condition: $\overline{DODS} = \text{LOW}$; $V_{GCHF} = 2,8 \text{ to } 6,3 \text{ V}$.

Fig. 7 Test circuit for positive reference current (I_{refp}).



Condition: $\overline{\text{DODS}} = \text{LOW}$; $V_{\text{GCHF}} = 2,8 \text{ to } 6,3 \text{ V}$.

Fig. 8 Test circuit for negative reference current (I_{refn}).

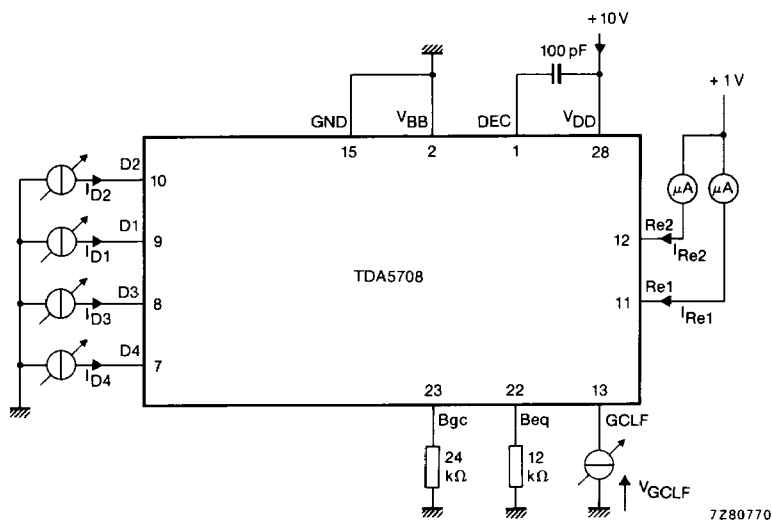


Fig. 9 Test circuit for output current I_{Re1} and I_{Re2} .

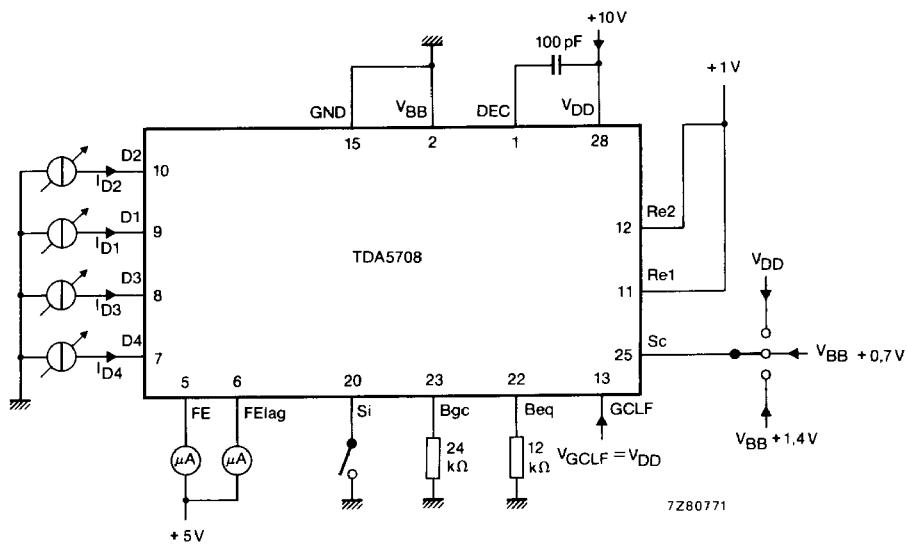


Fig. 10 Test circuit for output current I_{FE} and I_{FElag} .

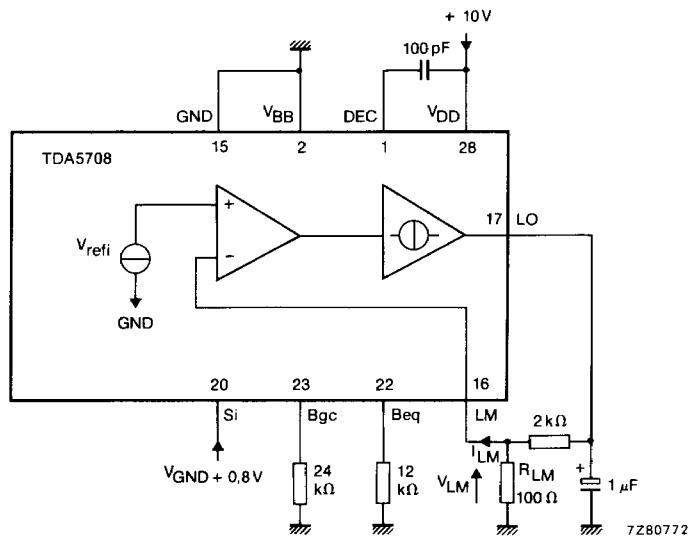


Fig. 11 Test circuit for V_{LM} ($V_{refi} \approx V_{LM}$) and I_{LM} .

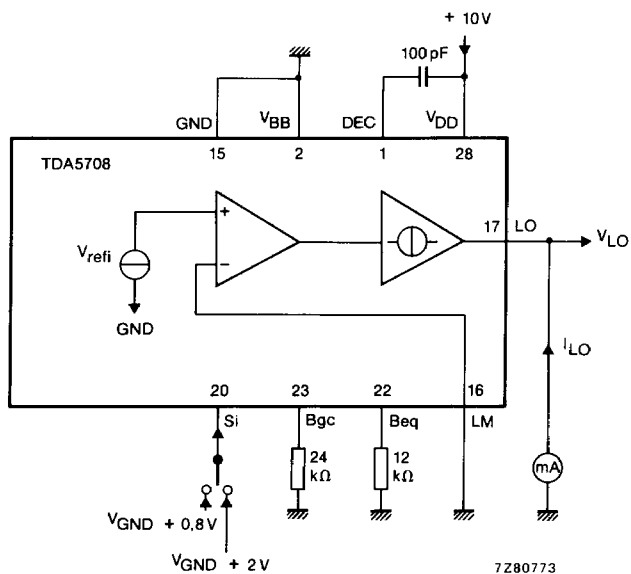
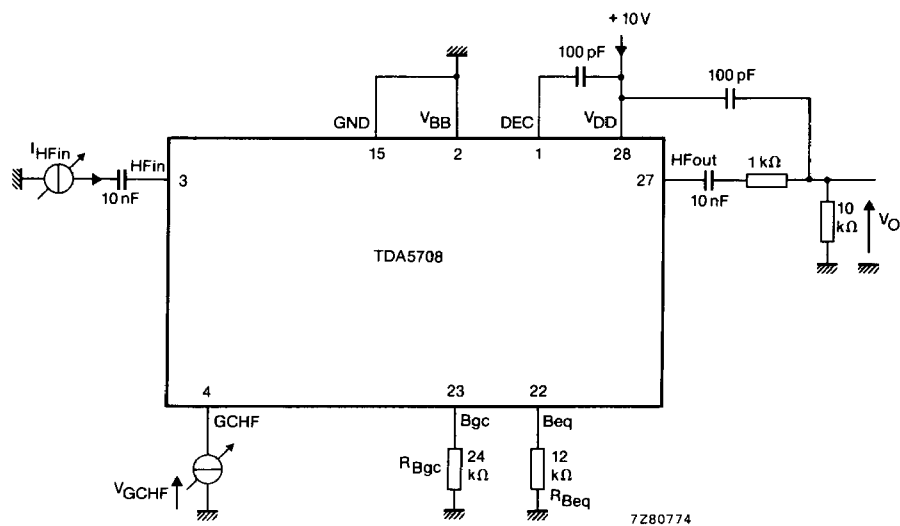
Fig. 12 Test circuit for V_{LO} and I_{LO} .

Fig. 13 Test circuit for HF part; a.c. characteristics.

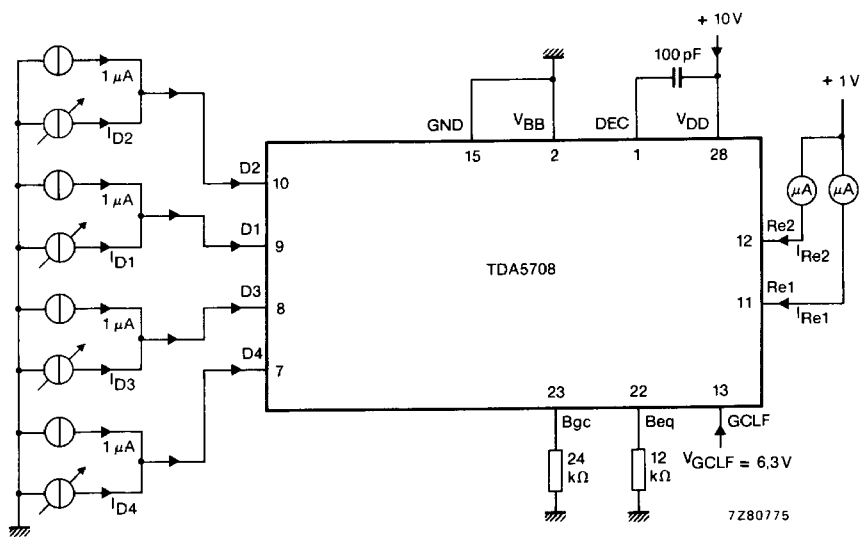
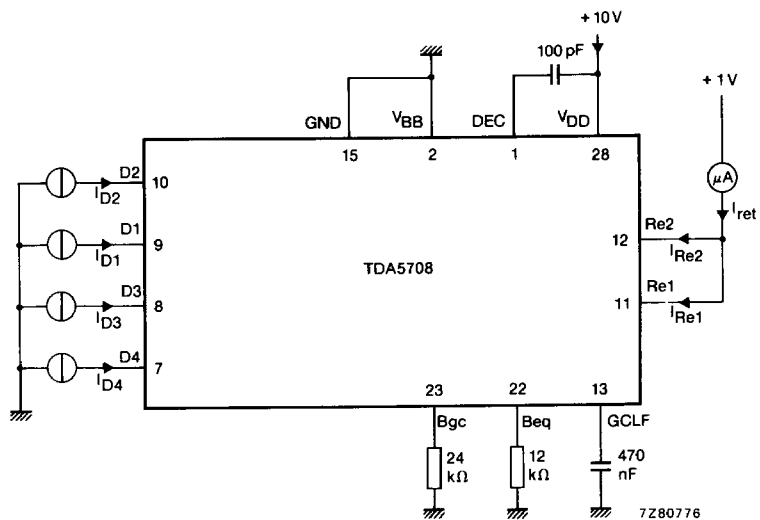


Fig. 14 Test circuit for LF part; a.c. gain.

Fig. 15 Test circuit for total reference current I_{ret} .