

## Wireless Components

ASK/FSK 868MHz Wireless Transceiver
TDA 5250 D2
Version 1.6

Specification July 2002

| confidential |  |  |
| :--- | :--- | :--- |
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| Current Version: Preliminary Specification V1.6 as of 09.07.02 describing design step D2 |  |  |
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| Page <br> (in previous <br> Version) | Page <br> (in current <br> Version) | Subjects (major changes since last revision) |
| $3-6,3-23$ | $3-6,3-23$ | Data pin (Pin 28) tied to GND in powerdown mode |
| $3-24$ to 3-26 | $3-24$ to 3-26 | Clock output setup time |
| $4-42$ | $4-43$ | Section „Datarates and Sensitivity" added |
| $4-43$ | $4-44$ | Explanation added |
| $5-3$ to 5-4 | $5-3$ to $5-4$ | Clock output setup time |
| $5-10$ | $5-10$ | Clock DIV line |
| $5-12$ | $5-12$ | Bill of Material completed |
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## Product Info

General Description The IC is a low power consumption single chip FSK/ASK Transceiver for half duplex low datarate communication in the $868-870 \mathrm{MHz}$ band. The IC offers a very high level of integration and needs only a few external components. It contains a highly efficient power amplifier, a low noise amplifier (LNA) with AGC, a double balanced mixer, a complex direct conversion stage, I/Q limiters with RSSI generation, an FSK demodulator, a fully integrated VCO and PLL synthesizer, a tuneable crystal oscillator, an onboard data filter, a data comparator (slicer), positive and negative peak detectors, a data rate detection circuit and a $2 / 3-$ wire bus interface. Additionally there is a power down feature to save battery power.

## Package



- On-chip low pass channel select filter and data filter with tuneable bandwidth
- Data slicer with self-adjusting threshold and 2 peak detectors
- FSK sensitivity $<-109 \mathrm{dBm}$, ASK sensitivity $<-109 \mathrm{dBm}$
- Transmit power up to +13dBm

■ Datarates up to $64 \mathrm{kBit} / \mathrm{s}$

- Self-polling logic with ultra fast data rate detection
- Alarm Systems

■ Telemetry Systems

- Electronic Metering

■ Home Automation Systems

| Type | Ordering Code | Package |
| :--- | :--- | :--- |
| TDA 5250 |  | P-TSSOP-38-1 |

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## Product Description

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### 2.1 Overview

The IC is a low power consumption single chip FSK/ASK Transceiver for the frequency band $868-870 \mathrm{MHz}$. The IC combines a very high level of integration and minimum external part count. The device contains a low noise amplifier (LNA), a double balanced mixer, a fully integrated VCO, a PLL synthesizer, a crystal oscillator with FSK modulator, a limiter with RSSI generator, an FSK demodulator, a data filter, a data comparator (slicer), a positive and a negative data peak detector, a highly efficient power amplifier and a complex digital timing and control unit with $\mathrm{I}^{2} \mathrm{C} / 3$-wire microcontroller interface. Additionally there is a power down feature to save battery power.

The transmit section uses direct ASK modulation by switching the power amplifier, and crystal oscillator detuning for FSK modulation. The necessary detuning load capacitors are external. The capacitors for fine tuning are integrated. The receive section is using a novel single-conversion/direct-conversion scheme that is combining the advantages of both receive topologies. The IF is contained on the chip, no RF channel filters are necessary as the channel filter is also on the chip.

The self-polling logic can be used to let the device operate autonomously as a master for a decoding microcontroller.

### 2.2 Applications

[^0]
### 2.3 Features

- Low supply current ( $\mathrm{I}_{\mathrm{s}}=9 \mathrm{~mA}$ typ. receive, $\mathrm{I}_{\mathrm{s}}=12 \mathrm{~mA}$ typ. transmit mode, both at 3 V supply voltage, $25^{\circ} \mathrm{C}$ )
- Supply voltage range 2.1 V to 5.5 V
- Operating temperature range $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$
- Power down mode with very low supply current consumption
- FSK and ASK modulation and demodulation capability without external circuitry changes, FM demodulation capability
- Fully integrated VCO and PLL synthesizer and loop filter on-chip with onchip crystal oscillator tuning, therefore no additional external components necessary
- Differential receive signal path completely on-chip, therefore no external filters are necessary
- On-chip low pass channel select and data filter with tuneable bandwith
- Data slicer with self-adjusting threshold and 2 peak detectors
- Self-polling logic with adjustable duty cycle and ultrafast data rate detection and timer mode providing periodical interrupt
■ FSK and ASK sensitivity <-109 dBm
- Adjustable LNA gain
- Digital RSSI and Battery Voltage Readout
- Provides Clock Out Pin for external microcontroller
- Transmit power up to +13 dBm in $50 \Omega$ load at 5 V supply voltage
- Maximum datarate up to 64 kBaud
- $\mathrm{I}^{2} \mathrm{C} / 3$-wire microcontroller interface, working at max. 400kbit/s
- meets the ETSI EN300 220 regulation and CEPT ERC 7003 recommendation


### 2.4 Package Outline



1) Does not include plastic or metal protusion of 0.15 max. per side 2) Does not include dambar protrusion of 0.08 max. per side
2) Does not include plastic or metal protrusion of 0.25 max. per side

P-TSSOP-38-1.EPS

Figure 2-1 P-TSSOP-38-1 package outlines

## 3 <br> Functional Description

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### 3.1 Pin Configuration



5250D1_pin_conf.wmf
Figure 3-1 Pin configuration

### 3.2 Pin Definition and Function

| Pin No. | Symbol | Equivalent I/O-Schematic | Function |
| :---: | :---: | :---: | :---: |
| 1 | VCC |  | Analog supply (antiparallel diodes between VCC, VCC1, VDD) |
| 2 | BUSMODE |  | Bus mode selection $\left(I^{2} \mathrm{C} / 3\right.$ wire bus mode selection) |
| 3 | LF |  | Loop filter and VCO control voltage |
| 4 | ASK $\overline{F S K}$ |  | ASK/FSK- mode switch input |
| 5 | RXTX |  | RX/TX-mode switch input/output |
| 6 | LNI |  | RF input to differential Low Noise Amplifier (LNA) |


|  | Complementary RF input to differ- <br> ential LNA |  |  |
| :--- | :--- | :--- | :--- | :--- |
| 8 | Gnd1 |  | Amplifier (PA) driver stage |

## confidential

Functional Description

| 17 | BUSCLK |  | Bus clock input |
| :---: | :---: | :---: | :---: |
|  |  |  |  |
| 18 | VSS | see Pin 8 | Ground for digital section |
| 19 | XOUT |  | Crystal oscillator output, can also be used as external reference frequency input. |
| 20 | XSWF |  | FSK modulation switch |
| 21 | XIN | see Pin 20 |  |
| 22 | XSWA |  | ASK modulation/FSK center frequency switch |
| 23 | XGND | see Pin 22 | Crystal oscillator ground return |
| 24 | $\overline{\mathrm{EN}}$ |  | 3-wire bus enable input |
| 25 | RESET |  | Reset of the entire system (to default values), active low |

## confidential

26 CLKDIV

### 3.3 Functional Block Diagram



TDA5250D1 blockdiagram aktuell.wmf
Figure 3-2 Main Block Diagram

### 3.4 Functional Blocks

### 3.4.1 Power Amplifier (PA)

The power amplifier is operating in C-mode. It can be used in either high or low power mode. In high-power mode the transmit power is approximately +13 dBm into 50 Ohm at 5 V and +4 dBm at 2.1 V supply voltage. In low power mode the transmit power is approximately -7 dBm at 5 V and -32 dBm at 2.1 V supply voltage using the same matching network. The transmit power is controlled by the DO-bit of the CONFIG register (subaddress 00 H ) as shown in the following Table 3-2. The default output power mode is high power mode.

| Table 3-2 Sub Address 00H: CONFIG |  |  |  |
| :---: | :---: | :--- | :---: |
| Bit | Function | Description | Default |
| D0 | PA_PWR | $0=$ low TX Power, 1= high TX Power | 1 |

In case of ASK modulation the power amplifier is turned fully on and off by the transmit baseband data, i.e. 100\% On-Off-Keying.

### 3.4.2 Low Noise Amplifier (LNA)

The LNA is an on-chip cascode amplifier with a voltage gain of 15 to 20 dB and symmetrical inputs. It is possible to reduce the gain to 0 dB via logic.

Table 3-3 Sub Address 00H: CONFIG

| Bit | Function | Description | Default |
| :---: | :--- | :--- | :---: |
| D4 | LNA_GAIN | 0= low Gain, 1= high Gain | 1 |

### 3.4.3 Downconverter $1^{\text {st }}$ Mixer

The Double Balanced $1^{\text {st }}$ Mixer converts the input frequency (RF) in the range of $868-870 \mathrm{MHz}$ to down to the intermediate frequency (IF) at approximately 290 MHz . The local oscillator frequency is generated by the PLL synthesizer that is fully implemented on-chip as described in Section 3.4.5. This local oscillator operates at approximately 1157 MHz in receive mode providing the above mentioned IF frequency of 290 MHz . The mixer is followed by a low pass filter with a corner frequency of approximately 350 MHz in order to prevent RF and LO signals from appearing the 290 MHz IF.

### 3.4.4 Downconverter $2^{\text {nd }} \mathrm{I} / \mathrm{Q}$ Mixers

The Low pass filter is followed by 2 mixers (inphase I and quadrature $Q$ ) that convert the 289 MHz IF signal down to zero-IF. These two mixers are driven by a signal that is generated by dividing the local oscillator signal by 4, thus equalling the IF frequency.

### 3.4.5 PLL Synthesizer

The Phase Locked Loop synthesizer consists of two VCOs (i.e. transmit and receive VCO), a divider by 4 , an asynchronous divider chain with selectable overall division ratio, a phase detector with charge pump and a loop filter and is fully implemented on-chip. The VCOs are including spiral inductors and varactor diodes. The center frequency of the transmit VCO is 868 MHz , the center frequency of the receive VCO is 1156 MHz .

Generally in receive mode the relationship between local oscillator frequency $f_{\text {osc }}$, the receive RF frequency $f_{R F}$ and the IF frequency $f_{I F}$ and thus the frequency that is applied to the I/Q Mixers is given in the following formula:
$f_{\text {OSC }}=4 / 3 f_{R F}=4 f_{I F}$

The VCO signal is applied to a divider by 4 which is producing approximately 289 MHz signals in quadrature. The overall division ratio of the divider chain following the divider by 4 is 12 in transmit mode and 16 in receive mode as the nominal crystal oscillator frequency is 18.083 MHz . The division ratio is controlled by the RxTx pin (pin 5) and the D10 bit in the CONFIG register.

### 3.4.6 I/Q Filters

The I/Q IF to zero-IF mixers are followed by baseband $6^{\text {th }}$ order low pass filters that are used for RF-channel filtering.


Figure 3-3 One I/Q Filter stage

The bandwidth of the filters is controlled by the values set in the filter-register. It can be adjusted between 50 and 350 kHz in 50 kHz steps via the bits D1 to D3 of the LPF register (subaddress 03H).

### 3.4.7 I/Q Limiters

The I/Q Limiters are DC coupled multistage amplifiers with offset-compensating feedback circuit and an overall gain of approximately 80dB each in the frequency range of 100 Hz up to 350 kHz . Receive Signal Strength Indicator (RSSI) generators are included in both limiters which produce DC voltages that are directly proportional to the input signal level in the respective channels. The resulting I- and Q-channel RSSI-signals are summed to the nominal RSSI signal.

### 3.4.8 FSK Demodulator

The output differential signals of the I/Q limiters are fed to a quadrature correlator circuit that is used to demodulate frequency shift keyed (FSK) signals. The demodulator gain is $2.4 \mathrm{mV} / \mathrm{kHz}$, the maximum frequency deviation is $\pm 300 \mathrm{kHz}$ as shown in Figure 3-4 below.
The demodulated signal is applied to the ASK/FSK mode switch which is connected to the input of the data filter. The switch can be controlled by the ASK $\overline{F S K}$ pin (pin 4) and via the D11 bit in the CONFIG register.


Qaudricorrelator.wmf
Figure 3-4 Quadricorrelator Demodulation Characteristic

### 3.4.9 Data Filter

The 2-pole data filter has a Sallen-Key architecture and is implemented fully onchip. The bandwidth can be adjusted between approximately 5 kHz and 102 kHz via the bits D4 to D7 of the LPF register as shown in Table 4-10.

data_filter.wmf
Figure 3-5 Data Filter architecture

### 3.4.10 Data Slicer

The data slicer is a fast comparator with a bandwidth of 100 kHz . The selfadjusting threshold is generated by a RC-network (LPF) or by use of one or both peak detectors depending on the baseband coding scheme as described in Section 4.6. This can be controlled by the D15 bit of the CONFIG register as shown in the following table.

| Table 3-4 Sub Address 00H: CONFIG |  |  |  |  |
| :---: | :--- | :--- | :---: | :---: |
| Bit | Function | Description | Default |  |
| D15 | SLICER | 0= Lowpass Filter, 1= Peak Detector | 0 |  |

### 3.4.11 Peak Detectors

Two separate Peak Detectors are available. They are generating DC voltages in a fast-attack and slow-release manner that are proportional to the positive and negative peak voltages appearing in the data signal. These voltages may be used to generate a threshold voltage for non-Manchester encoded signals, for example. The time-constant of the fast-attack/slow-release action is determined by external RC networks.

### 3.4.12 Crystal Oscillator

The reference oscillator is an NIC oscillator type (Negative Impedance Converter) with a crystal operating in serial resonance. The nominal operating frequency of 18.083 MHz and the frequencies for FSK modulation can be adjusted via 3 external capacitors. Via microcontroller and bus interface the chip-internal capacitors can be used for finetuning of the nominal and the FSK modulation frequencies. This finetuning of the crystal oscillator allows to eliminate frequency errors due to crystal or component tolerances.

### 3.4.13 Bandgap Reference Circuitry

A Bandgap Reference Circuit provides a temperature stable 1.2 V reference voltage for the device. A power down mode is available to switch off all subcircuits that are controlled by the bidirectional Powerdown\&DataDetect Pwd $\overline{\mathrm{DD}}$ pin (pin 27) as shown in the following table. The supply current in this mode is typically 100 nA .

Table 3-5 PwdDD Pin Operating States

| Pwd $\overline{\mathrm{DD}}$ | Operating State |
| :---: | :---: |
| VDD | Powerdown Mode |
| Ground/VSS | Device On |

### 3.4.14 Timing and Data Control Unit

The timing and data control unit contains a wake-up logic unit, an $\mathrm{I}^{2} \mathrm{C} / 3$-wire microcontroller interface, a "data valid" detection unit and a set of configuration registers as shown in the subsequent figure.


Figure 3-6 Timing and Data Control Unit

The $\mathrm{I}^{2} \mathrm{C} / 3$-wire Bus Interface gives an external microcontroller full control over important system parameters at any time.

It is possible to set the device in three different modes: Slave Mode, Self Polling Mode and Timer Mode. This is done by a state machine which is implemented in the WAKEUP LOGIC unit. A detailed description is given in Section 3.4.16.

The DATA VALID DETECTOR contains a frequency window counter and an RSSI threshold comparator. The window counter uses the incoming data signal from the data slicer as the gating signal and the crystal oscillator frequency as the timebase to determine the actual datarate. The result is compared with the expected datarate.
The threshold comparator compares the actual RSSI level with the expected RSSI level.

If both conditions are true the Pwd $\overline{\mathrm{DD}}$ pin is set to LOW in self polling mode as you can see in Section 3.4.1.6. This signal can be used as an interrupt for an external $\mu \mathrm{P}$. Because the PwdDD pin is bidirectional and open drain driven by an internal pull-up resistor it is possible to apply an external LOW thus enabling the device.

### 3.4.15 Bus Interface and Register Definition

The TDA5250 supports the $\mathrm{I}^{2} \mathrm{C}$ bus protocol (2 wire) and a 3-wire bus protocol. Operation is selectable by the BusMode pin (pin 2) as shown in the following table. All bus pins (BusData, BusCLK, EN, BusMode) have a Schmitt-triggered input stage. The BusData pin is bidirectional where the output is open drain driven.

| Table 3-6 Bus Interface Format |  | BusCLK | BusData |  |
| :--- | :--- | :--- | :--- | :--- |
| Function | BusMode | $\overline{\text { EN }}$ | Bus |  |
| $\left.\right\|^{2}$ C Mode | Low | High= inactive, <br> Low= active | Clock input | Data in/out |
| 3-wire Mode | High |  |  |  |


i2c_3w_bus.wmf
Figure 3-7 Bus Interface

Note: The Interface is able to access the internal registers at any time, even in POWER DOWN mode. There is no internal clock necessary for Interface operation.

## $I^{2} \mathrm{C}$ Bus Mode

In this mode the BusMode pin (pin 2) = LOW and the EN pin (pin 24) = LOW.
Data Transition:
Data transition on the pin BusData can only occur when BusCLK is LOW. BusData transitions while BusCLK is HIGH will be interpreted as start or stop condition.

## Start Condition (STA):

A start condition is defined by a HIGH to LOW transition of the BusData line while BusCLK is HIGH. This start condition must precede any command and initiate a data transfer onto the bus.

Stop Condition (STO):
A stop condition is defined by a LOW to HIGH transition of the BusData line while BusCLK is HIGH. This condition terminates the communication between the devices and forces the bus interface into the initial state.

## Acknowledge (ACK):

Indicates a successful data transfer. The transmitter will release the bus after sending 8 bit of data. During the 9th clock cycle the receiver will set the SDA line to LOW level to indicate it has received the 8 bits of data correctly.

## Data Transfer Write Mode:

To start the communication, the bus master must initiate a start condition (STA), followed by the 8bit chip address. The chip address for the TDA5250 is fixed as „1110000" (MSB at first). The last bit (LSB=A0) of the chip address byte defines the type of operation to be performed:
$A 0=0$, a write operation is selected and $A 0=1$ a read operation is selected.
After this comparison the TDA5250 will generate an ACK and awaits the desired sub address byte ( $00 \mathrm{H} . . .0 \mathrm{FH}$ ) and data bytes. At the end of the data transition the master has to generate the stop condition (STO).

## Data Transfer Read Mode:

To start the communication in the read mode, the bus master must initiate a start condition (STA), followed by the 8 bit chip address (write: A0=0), followed by the sub address to read $(80 \mathrm{H}, 81 \mathrm{H})$, followed by the chip address (read: $\quad A 0=1$ ). After that procedure the data of the selected register $(80 \mathrm{H}, 81 \mathrm{H})$ is read out. During this time the data line has to be kept in HIGH state and the chip sends out the data. At the end of data transition the master has to generate the stop condition (STO).

## Bus Data Format in $\mathrm{I}^{2} \mathrm{C}$ Mode

| Table 3-7 Chip address Organization |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :--- |
| MSB |  |  |  |  |  |  | LSB | Function |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | Chip Address Write |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | Chip Address Read |


| Table 3-8 ${ }^{2} \mathrm{C}$ Bus Write Mode 8 Bit |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | MSB | CHIP ADDRESS (WRITE) |  |  |  |  |  | LSB | MSB |  | SUB ADDRESS (WRITE) $00 \mathrm{H} . . .08 \mathrm{H}, 0 \mathrm{DH}, 0 \mathrm{EH}, 0 \mathrm{FH}$ |  |  |  |  |  | LSB | MSB |  | DATA IN |  |  |  |  | LSB |  |  |  |
| STA | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | ACK | S7 | S6 | S5 | S4 | S3 | S2 | S1 | S0 | ACK | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | ACK | STO |




|  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| MSB | DATA OUT FROM SUB ADDRESS | R4 | LSB |  |  |  |  |  |  |
| R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 | ACK* | STO |

* mandatory HIGH


## 3-wire Bus Mode

In this mode pin 2 (BusMode)= HIGH and Pin 16 (BusData) is in the data input/ output pin. Pin $24(\overline{\mathrm{EN}})$ is used to activate the bus interface to allow the transfer of data to / from the device. When pin $24(\overline{\mathrm{EN}})$ is inactive (HIGH), data transfer is inhibited.

## Data Transition:

Data transition on pin 16 (BusData) can only occur if the clock BusCLK is LOW. To perform a data transfer the interface has to be enabled. This is done by setting the EN line to LOW. A serial transfer is done via BusData, BusCLK and EN . The bit stream needs no chip address.

## Data Transfer Write Mode:

To start the communication the EN line has to be set to LOW. The desired sub address byte and data bytes have to follow. The subaddress ( $00 \mathrm{H} . . .0 \mathrm{FH}$ ) determines which of the data bytes are transmitted. At the end of data transition the EN must be HIGH.

Data transfer Read Mode:
To start the communication in the read mode, the $\overline{E N}$ line has to be set to LOW followed by the sub address to read $(80 \mathrm{H}, 81 \mathrm{H})$. Afterwards the device is ready to read out data. At the end of data transition $\overline{\mathrm{EN}}$ must be HIGH.

## Bus Data Format 3-wire Bus Mode

| Table 3-113-wire Bus Write Mode |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| MSB | SUB ADDRESS (WRITE) <br> $00 \mathrm{H} . . .08 \mathrm{H}, 0 \mathrm{DH}, 0 \mathrm{EH}, 0 \mathrm{FH}$ |  |  |  |  |  | LSB | MSB | DAT | N X | (X=7 | 1 1 |  |  | LSB |
| S7 | S6 | S5 | S4 | S3 | S2 | S1 | S0 | DX | ... | D5 | D4 | D3 | D2 | D1 | D0 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Table 3-12 3-wire Bus Read Mode |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| MSB | $\begin{aligned} & \text { SUB ADDRESS (READ) } \\ & \text { 80H, 81H } \end{aligned}$ |  |  |  |  |  | LSB | MSB | DATA OUT FROM SUB ADDRESS |  |  |  |  |  | LSB |
| S7 | S6 | S5 | S4 | S3 | S2 | S1 | S0 | R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 |

## Register Definition

## Sub Addresses Overview



Figure 3-8 Sub Addresses Overview

## Subaddress Organization

## Table 3-13 Sub Addresses of Data Registers Write

| MSB |  |  |  |  |  |  | LSB | HEX | Function | Description | Bit Length |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :--- | :--- | :--- | :--- | :--- | :---: |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00h | CONFIG | General definition of status bits | 16 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 h | FSK | Values for FSK-shift | 16 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | $02 h$ | XTAL_TUNING | Nominal frequency | 16 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 03h | LPF | I/Q and data filter cutoff frequencies | 8 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04 | ON_TIME | ON time of wakeup counter | 16 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | $05 h$ | OFF_TIME | OFF time of wakeup counter | 16 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | $06 h$ | COUNT_TH1 | Lower threshold of window counter | 16 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 07h | COUNT_TH2 | Higher threshold of window counter | 16 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 08h | RSSI_TH3 | Threshold for RSSI signal | 8 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | ODh | CLK_DIV | Configuration and Ratio of clock divider | 8 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0Eh | XTAL_CONFIG | XTAL configuration | 8 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0Fh | BLOCK_PD | Building Blocks Power Down | 16 |


| Table 3-14 Sub Addresses of Data Registers Read |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :--- | :---: |
| MSB |  |  |  |  |  | LSB | HEX | Function | Description | Bit Length |  |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $80 h$ | STATUS | Results of comparison: ADC \& WINDOW | 8 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 81 h | ADC | ADC data out | 8 |

## Data Byte Specification

| Table 3-15 Sub Address 00H: CONFIG |  |  |  |  |
| :---: | :---: | :--- | :---: | :---: |
| Bit | Function | Description | Default |  |
| D15 | SLICER | $0=$ Lowpass, $1=$ Peak Detector | 0 |  |
| D14 | ALL_PD | $0=$ normal operation, $1=$ all Power down | 0 |  |
| D13 | TESTMODE | $0=$ normal operation, $1=$ Testmode | 0 |  |
| D12 | CONTROL | 0= RX/TX and ASK/FSK external controlled, $1=$ Register <br> controlled | 0 |  |
| D11 | ASK_NFSK | $0=$ FSK, $1=$ ASK | 0 |  |
| D10 | RX_NTX | $0=$ TX, $1=$ RX | 1 |  |
| D9 | CLK_EN | $0=$ CLK off during power down, $1=$ always CLK on, ever in PD | 0 |  |
| D8 | RX_DATA_INV | $0=$ no Data inversion, $1=$ Data inversion | 0 |  |
| D7 | D_OUT | $0=$ Data out if valid, $1=$ always Data out | 1 |  |
| D6 | ADC_MODE | $0=$ one shot, $1=$ continuous | 1 |  |
| D5 | F_COUNT_MODE | $0=$ one shot, $1=$ continuous | 1 |  |
| D4 | LNA_GAIN | $0=$ low gain, $1=$ high gain | 1 |  |
| D3 | EN_RX | $0=$ disable receiver, $1=$ enable receiver (in self polling and <br> timer mode) $*$ | 1 |  |
| D2 | MODE_2 | $0=$ slave mode, $1=$ timer mode | 0 |  |
| D1 | MODE_1 | $0=$ slave or timer mode, $1=$ self polling mode | 0 |  |
| D0 | PA_PWR | $0=$ low TX Power, $1=$ high TX Power | 1 |  |

Note D3: Function is only active in selfpolling and timer mode. When D3 is set to LOW the RX path is not enabled if Pwd $\overline{\mathrm{DD}}$ pin is set to LOW. A delayed setting of D3 results in a delayed power ON of the RX building blocks.

Table 3-16 Sub Address 01H: FSK

| Bit | Function | Value | Description | Default |
| :---: | :---: | :---: | :---: | :---: |
| D15 |  |  | not used | 0 |
| D14 |  |  | not used | 0 |
| D13 | FSK+5 | 8pF | Setting for positive frequency shift: +FSK or ASK-RX | 0 |
| D12 | FSK+4 | 4pF |  | 0 |
| D11 | FSK+3 | 2 pF |  | 1 |
| D10 | FSK+2 | 1 pF |  | 0 |
| D9 | FSK+1 | 500fF |  | 1 |
| D8 | FSK+0 | 250fF |  | 0 |
| D7 |  |  | not used | 0 |
| D6 |  |  | not used | 0 |
| D5 | FSK-5 | 4pF | Setting for negative frequency shift: -FSK | 0 |
| D4 | FSK-4 | 2 pF |  | 0 |
| D3 | FSK-3 | 1 pF |  | 1 |
| D2 | FSK-2 | 500fF |  | 1 |
| D1 | FSK-1 | 250fF |  | 0 |
| D0 | FSK-0 | 125fF |  | 0 |


| Bit | Function | Description | Default |
| :---: | :---: | :---: | :---: |
| D7 | Datafilter_3 | 3dB cutoff frequency of data filter | 0 |
| D6 | Datafilter_2 |  | 0 |
| D5 | Datafilter_1 |  | 0 |
| D4 | Datafilter_0 |  | 1 |
| D3 | IQ_Filter_2 | 3dB cutoff frequency of IQ-filter | 1 |
| D2 | IQ_Filter_1 |  | 0 |
| D1 | IQ_Filter_0 |  | 0 |
| D0 | not used |  | 0 |

Table 3-17 Sub Address 02H: XTAL_TUNING

| Bit | Function | Value | Description | Default |
| :---: | :---: | :---: | :---: | :---: |
| D15 |  |  | not used | 0 |
| D14 |  |  | not used | 0 |
| D13 |  |  | not used | 0 |
| D12 |  |  | not used | 0 |
| D11 |  |  | not used | 0 |
| D10 |  |  | not used | 0 |
| D9 |  |  | not used | 0 |
| D8 |  |  | not used | 0 |
| D7 |  |  | not used | 0 |
| D6 |  |  | not used | 0 |
| D5 | Nominal_Frequ_5 | 8pF | Setting for nominal frequency | 0 |
| D4 | Nominal_Frequ_4 | 4 pF |  | 1 |
| D3 | Nominal_Frequ_3 | 2 pF |  | 0 |
| D2 | Nominal_Frequ_2 | 1 pF | ASK-TX FSK-RX | 0 |
| D1 | Nominal_Frequ_1 | 500fF |  | 1 |
| D0 | Nominal_Frequ_0 | 250fF |  | 0 |


| Table 3-19 Sub Addresses 04H / 05H: ON/OFF_TIME |  |  |  |
| :--- | :--- | :---: | :---: |
| Bit | Function | Default <br> ON_TIME | Default <br> OFF_TIME |
| D15 | ON_15 / OFF_15 | 1 | 1 |
| D14 | ON_14 / OFF_14 | 1 | 1 |
| D13 | ON_13 / OFF_13 | 1 | 1 |
| D12 | ON_12 / OFF_12 | 1 | 1 |
| D11 | ON_11 / OFF_11 | 1 | 0 |
| D10 | ON_10 / OFF_10 | 1 | 0 |
| D9 | ON_9 / OFF_9 | 1 | 1 |
| D8 | ON_8 / OFF_8 | 0 | 1 |
| D7 | ON_7 / OFF_7 | 1 | 1 |
| D6 | ON_6 / OFF_6 | 1 | 0 |
| D5 | ON_5 / OFF_5 | 0 | 0 |
| D4 | ON_4 / OFF_4 | 0 | 0 |
| D3 | ON_3 / OFF_3 | 0 | 0 |
| D2 | ON_2 / OFF_2 | 0 | 0 |
| D1 | ON_1 / OFF_1 | 0 | 0 |
| D0 | ON_0 / OFF_0 | 0 | 0 |
|  |  |  |  |

Table 3-21 Sub Address 07H: COUNT_TH2

| Bit | Function | Default |
| :--- | :--- | :---: |
| D15 | not used | 0 |
| D14 | not used | 0 |
| D13 | not used | 0 |
| D12 | not used | 0 |
| D11 | TH2_11 | 0 |
| D10 | TH2_10 | 0 |
| D9 | TH2_9 | 0 |
| D8 | TH2_8 | 0 |
| D7 | TH2_7 | 0 |
| D6 | TH2_6 | 0 |
| D5 | TH2_5 | 0 |
| D4 | TH2_4 | 0 |
| D3 | TH2_3 | 0 |
| D2 | TH2_2 | 0 |
| D1 | TH2_1 | 0 |
| D0 | TH2_0 | 1 |


| Table 3-22 Sub Address 08H: RSSI_TH3 |  |  |  |
| :---: | :---: | :---: | :---: |
| Bit | Function | Description | Default |
| D7 | not used |  | 1 |
| D6 | SELECT | 0= VCC, 1= RSSI | 1 |
| D5 | TH3_5 |  | 1 |
| D4 | TH3_4 |  | 1 |
| D3 | TH3_3 |  | 1 |
| D2 | TH3_2 |  | 1 |
| D1 | TH3_1 |  | 1 |
| D0 | TH3_0 |  | 1 |


| Table 3-23 Sub Address 0DH: CLK_DIV |  |  |
| :---: | :---: | :---: |
| Bit | Function | Default |
| D7 | not used | 0 |
| D6 | not used | 0 |
| D5 | DIVMODE_1 | 0 |
| D4 | DIVMODE_0 | 0 |
| D3 | CLKDIV_3 | 1 |
| D2 | CLKDIV_2 | 0 |
| D1 | CLKDIV_1 | 0 |
| D0 | CLKDIV_0 | 0 |


| Table 3-24 Sub Address 0EH: XTAL_CONFIG |  |
| :---: | :---: | :---: | :---: |
| Bit Function Description <br> D7  not used <br> D6  not used <br> D5  not used <br> D4  not used <br> D3  not used <br> D2 FSK-Ramp 0 only in bipolar mode <br> D1 FSK-Ramp 1  <br> D0 Bipolar_FET 0 <br>   0 |  |


| Table 3-25 Sub Address 0FH: BLOCK_PD |  |  |  |
| :---: | :--- | :--- | :---: |
| Bit | Function | Description | Default |
| D15 | REF_PD | 1= power down Band Gap Reference | 1 |
| D14 | RC_PD | 1= power down RC Oscillator | 1 |
| D13 | WINDOW_PD | 1= power down Window Counter | 1 |
| D12 | ADC_PD | 1= power down ADC | 1 |
| D11 | PEAK_DET_PD | 1= power down Peak Detectors | 1 |
| D10 | DATA_SLIC_PD | 1= power down Data Slicer | 1 |
| D9 | DATA_FIL_PD | 1= power down Data Filter | 1 |
| D8 | QUAD_PD | 1= power down Quadri Correlator | 1 |
| D7 | LIM_PD | 1= power down Limiter | 1 |
| D6 | I/Q_FIL_PD | 1= power down I/Q Filters | 1 |
| D5 | MIX2_PD | 1= power down I/Q Mixer | 1 |
| D4 | MIX1_PD | 1= power down 1st Mixer | 1 |
| D3 | LNA_PD | 1= power down LNA | 1 |
| D2 | PA_PD | 1= power down Power Amplifier | 1 |
| D1 | PLL_PD | 1= power down PLL | 1 |
| D0 | XTAL_PD | 1= power down XTAL Oscillator | 1 |


| Table 3-26 Sub Address 80H: STATUS |  |  |
| :---: | :--- | :--- |
| Bit | Function | Description |
| D7 | COMP_LOW | 1 if data rate $<$ TH1 |
| D6 | COMP_IN | 1 if TH1 $<$ data rate $<$ TH2 |
| D5 | COMP_HIGH | 1 if TH2 $<$ data rate |
| D4 | COMP_0,5*LOW | 1 if data rate $<0,5^{*}$ TH1 |
| D3 | COMP_0, $5^{\star}$ IN | 1 if $0,5^{*}$ TH1 $<$ data rate $<0,5^{\star} \mathrm{TH} 2$ |
| D2 | COMP_0,5*HIGH | 1 if $0,5^{*} \mathrm{TH} 2<$ data rate |
| D1 | RSSI=TH3 | 1 if RSI value is equal TH3 |
| D0 | RSSI>TH3 | 1 if RSSI value is greater than TH3 |


| Table 3-27 Sub Address 81H: ADC |  |  |
| :--- | :--- | :--- |
| Bit | Function | Description |
| D7 | PD_ADC | ADC power down feedback Bit |
| D6 | SELECT | SELECT feedback Bit |
| D5 | RSSI_5 | RSSI value Bit5 |
| D4 | RSSI_4 | RSSI value Bit4 |
| D3 | RSSI_3 | RSSI value Bit3 |
| D2 | RSSI_2 | RSSI value Bit2 |
| D1 | RSSI_1 | RSSI value Bit1 |
| D0 | RSSI_0 | RSSI value Bit0 |

### 3.4.16 Wakeup Logic



Figure 3-9 Wakeup Logic States

| Table 3-28 MODE settings: CONFIG register |  |  |
| :---: | :---: | :---: |
| MODE_1 | MODE_2 | Mode |
| 0 | 0 | SLAVE MODE |
| 0 | 1 | TIMER MODE |
| 1 | X | SELF POLLING MODE |

SLAVE MODE: The receive and transmit operation is fully controlled by an external control device via the respective RxTx, AskFsk, Pwd $\overline{D D}$, and Data pins. The wakeup logic is inactive in this case.

After RESET or $1^{\text {st }}$ Power-up the chip is in SLAVE MODE. By setting MODE_1 and MODE_2 in the CONFIG register the mode may be changed.

SELF POLLING MODE: The chip turns itself on periodically to receive using a built-in 32 kHz RC oscillator. The timing of this is determined by the ON_TIME and OFF_TIME registers, the duty cycle can be set between 0 and $100 \%$ in $31.25 \mu$ s increments. The data detect logic is enabled and a $15 \mu \mathrm{~L}$ LOW impulse is provided at PwdDD pin (Pin 27), if the received data is valid.

timing_selfpllmode.wmf
Figure 3-10 Timing for Self Polling Mode (ADC \& Data Detect in one shot mode)
Note: The time delay between start of ON time and the $15 \mu$ LOW impulse is $2.6 \mathrm{~ms}+3$ period of data rate.

If ADC \& Data Detect Logic are in continuous mode the $15 \mu \mathrm{LOW}$ impulse is applied at Pwd $\overline{\mathrm{DD}}$ after each data valid decision.
In self polling mode if D9=0 (Register 00h) and when PwdDD pin level is HIGH the CLK output is on during ON time and off during OFF time. If $\mathrm{D} 9=1$, the CLK output is always on.

TIMER MODE: Only the internal Timer (determined by the ON_TIME and OFF_TIME registers) is active to support an external logic with periodical Interrupts. After ON_TIME + OFF_TIME a $15 \mu$ s LOW impulse is applied at the Pwd $\overline{D D}$ pin (Pin 27).

timing_timermode.wmf
Figure 3-11 Timing for Timer Mode

### 3.4.17 Data Valid Detection, Data Pin

Data signals generate a typical spectrum and this can be used to determine if valid data is on air.


Figure 3-12 Frequency and RSSI Window

The "data valid" criterion is generated from the result of RSSI-TH3 comparison and $t_{\text {GATE }}$ between TH1 and TH2 result as shown below. In case of Manchester coding the $0,5^{*} \mathrm{TH} 1$ and $0,5^{*} \mathrm{TH} 2$ gives improved performance.

The use of permanent data valid recognition makes it absolutely necessary to set the RSSI-ADC and the Window counter into continuous mode (Register 00H, Bit D5 = D6 = 1).

data_valid.wmf
Figure 3-13 Data Valid Circuit

D_OUT and RX_DATA_INV from the CONFIG register determine the output of data at Pin 28. RxTxint and TX_ON are internally generated signals.

In RX and power down mode Data pin (Pin 28) is tied to GND.


Figure 3-14 Data Input/Output Circuit

### 3.4.18 Sequence Timer

The sequence timer has to control all the enable signals of the analog components inside the chip. The time base is the 32 kHz RC oscillator.

After the first POWER ON or RESET a 1 MHz clock is available at the clock output pin. This clock output can be used by an external $\mu \mathrm{P}$ to set the system into the desired state and outputs valid data after $500 \mu$ (see Figure 3-15 and Figure 3-16, $\mathrm{t}_{\mathrm{CLKSU}}$ )

There are two possibilities to start the device after a reset or first power on:

- PWD $\overline{D D}$ pin is LOW: Normal operation timing is performed after $t_{\text {SYSSU }}$ (see Figure 3-15).
- PWDDD pin is HIGH (device in power down mode): A clock is offered at the clock output pin until the device is activated (PWDDD pin is pulled to LOW). After the first activation the time $\mathrm{t}_{\text {SYSSU }}$ is required until normal operation timing is performed (see Figure 3-16).
This could be used to extend the clock generation without device programming or activation.

Note: It is required to activate the device for the duration of $\mathrm{t}_{\text {SYSSU }}$ after first power on or a reset. Only if this is done the normal operation timing is performed.

With default settings the clock generating units are disabled during PD, therefore no clock is available at the clock output pin. It is possible to offer a clock signal at the clock output pin every time (also during PD) if the CLK_EN Bit in the CONFIG register is set to HIGH.


Figure 3-15 $\quad 1^{\text {st }}$ start or reset in active mode

Note: The time values are typical values


Figure 3-16 1st start or reset in PD mode

Note: The time values are typical values
This means that the device needs $t_{\text {DDSU }}$ setup time to start the data detection after RX is activated. When activating TX it requires $t_{\text {TXSU }}$ setup time to enable the power amplifier.

For timing information refer to Table 5-3.

For Test purposes a TESTMODE is provided by the Sequencer as well. In this mode the BLOCK_PD register be set to various values. This will override the Sequencer timing. Depending on the settings in Config Register 00H the corresponding building blocks are enabled, as shown in the subsequent figure.


Figure 3-17 Sequencer's capability

### 3.4.19 Clock Divider

It supports an external logic with a programmable Clock at pin 26 (CLKDIV).

clk_div.wmf
Figure 3-18 Clock Divider

The Output Selection and Divider Ratio can be set in the CLK_DIV register.

| Table 3-29 CLK_DIV Output Selection |  |  |
| :---: | :---: | :--- |
| D5 | D4 | Output |
| $\mathbf{0}$ | $\mathbf{0}$ | Output from Divider (default) |
| 0 | 1 | 18.089 MHz |
| 1 | 0 | 32 kHz |
| $\mathbf{1}$ | 1 | Window Count Complete |

Note: Data are valid $500 \mu \mathrm{~s}$ after the crystal oscillator is enabled (see Figure 315 and Figure 3-16, $\mathrm{t}_{\text {CLKSU }}$ ).

| Table 3-30 CLK_DIV Setting |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| D3 | D2 | D1 | D0 | Total Divider Ratio | Output Frequency [MHz] |
| 0 | 0 | 0 | 0 | 2 | 9,0 |
| 0 | 0 | 0 | 1 | 4 | 4,5 |
| 0 | 0 | 1 | 0 | 6 | 3,0 |
| 0 | 0 | 1 | 1 | 8 | 2,25 |
| 0 | 1 | 0 | 0 | 10 | 1,80 |
| 0 | 1 | 0 | 1 | 12 | 1,50 |
| 0 | 1 | 1 | 0 | 14 | 1,28 |
| 0 | 1 | 1 | 1 | 16 | 1,125 |
| $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{1 8}$ | $\mathbf{1 , 0 0}$ (default) |
| 1 | 0 | 0 | 1 | 20 | 0,90 |
| 1 | 0 | 1 | 0 | 22 | 0,82 |
| 1 | 0 | 1 | 1 | 24 | 0,75 |
| 1 | 1 | 0 | 0 | 26 | 0,69 |
| 1 | 1 | 0 | 1 | 28 | 0,64 |
| 1 | 1 | 1 | 0 | 30 | 0,60 |
| 1 | 1 | 1 | 1 | 32 | 0,56 |

Note: As long as default settings are used, there is no clock available at the clock output during Power Down. It is possible to enable the clock during Power Down by setting CLK_EN (Bit D9) in the Config Register (00H) to HIGH.

### 3.4.20 RSSI and Supply Voltage Measurement

The input of the 6Bit-ADC can be switched between two different sources: the RSSI voltage (default setting) or a resistor network dividing the Vcc voltage by 5.

| Table 3-31 Source for 6Bit-ADC Selection (Register 08H) |  |
| :---: | :--- |
| SELECT | Input for 6Bit-ADC |
| 0 | Vcc / 5 |
| $\mathbf{1}$ | RSSI (default) |

To prevent wrong interpretation of the ADC information (read from Register 81H: ADC) you can use the ADC- Power Down feedback Bit (D7) and the SELECT feedback Bit (D6) which correspond to the actual measurement.

Note: As shown in section 3.4.18 there is a setup time of 2.6 ms after RX activating. Thus the measurement of RSSI voltage does only make sense after this setup time.

## 4

Applications

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### 4.1 LNA and PA Matching

### 4.1.1 RX/TX Switch



RX/TX_Switch.wm
Figure 4-1 RX/TX Switch

The RX/TX-switch combines the PA-output and the LNA-input into a single 50 Ohm SMA-connector. Two pin-diodes are used as switching elements. If no current flows through a pin diode, it works as a high impedance for RF with very low capacitance. If the pin-diode is forward biased, it provides a low impedance path for RF. (some $\Omega$ )

### 4.1.1.1 Switch in RX-Mode

The RX/TX-switch is set to the receive mode by either applying a high level or an open to the RX/TX-jumper on the evalboard or by leaving it open. Then both pin-diodes are not biased and therefore have a high impedance.


The RF-signal is able to run from the RF-input-SMA-connector to the LNA-input-pin LNI via C1, C2, C7, L3 and C9. R1 does not affect the matching circuit due to its high resistance. The other input of the differential LNA LNIX can always be AC-grounded using a large capacitor without any loss of performance. In this case the differential LNA can be used as a single ended LNA, which is easier to match. The S11 of the LNA at pin LNI on the evalboard is $0.945 /-47^{\circ}$ (equals a resistor of 1.43 kOhm in parallel to a capacitor of 1.6 pF ) for both high and low-gain-mode of the LNA. (pin LNIX AC-grounded) This impedance has to be matched to 50 Ohm with the parts C9, L3, C7 and C2. C1 is DC-decoupling-capacitor. On the evalboard the most important matching components are (shunt) L3 and (series) C2. The capacitors C7 and C9 are mainly DC-decoupling-capacitors and may be used for some fine tuning of the matching circuit. A good CAE tool (featuring smith-chart) may be used for the calculation of the values of the components. However, the final values of the matching components always have to be found on the board because of the parasitics of the board, which highly influence the matching circuit at RF.

Measured Magnitude of S11 of evalboard:


Figure 4-3 S11 measured

Above you can see the measured S11 of the evalboard. The -3dB-points are at 810 MHz and 930 MHz . So the 3dB-bandwidth is:

$$
\begin{equation*}
B=f_{U}-f_{L}=930 \mathrm{MHz}-810 \mathrm{MHz}=120 \mathrm{MHz} \tag{4-1}
\end{equation*}
$$

The loaded Q of the resonant circuit is:

$$
\begin{equation*}
Q_{L}=\frac{f_{\text {center }}}{B}=\frac{868,3 \mathrm{MHz}}{120 \mathrm{MHz}}=7.2 \tag{4-2}
\end{equation*}
$$

The unloaded $Q$ of the resonant circuit is equal to the $Q$ of the inductor due to its losses.
$Q_{U}=Q_{\text {INDUCTOR }} \approx 36 @ 868 \mathrm{MHz}$

An approximation of the losses of the input matching network can be made with the formula:

$$
\text { Loss }=-20 * \log \left(1-\frac{Q_{L}}{Q_{U}}\right)=-20 * \log \left(1-\frac{7.2}{36}\right)=2 d B \quad[4-4]
$$

The noise figure of the LNA-input-matching network is equal to its losses. The input matching network is always a compromise of sensitivity and selectivity. The loaded $Q$ should not get too high because of 2 reasons:
more losses in the matching network and hence less sensitivity
tolerances of components affect matching too much. This will cause problems in a tuning-free mass production of the application. A good CAE-tool will help to see the effects of component tolerances on the input matching more accurate by tweaking each value.

A very high selectivity can be reached by using SAW-filters at the expense of higher cost and lower sensitivity which will be reduced by the losses of the SAW-Filter of approx. 4dB.

## Image-suppression:

Due to the quite high $1^{\text {st }}$-IF of the frontend, the image frequency is quite far away. The image frequency of the receiver is at:
$f_{\text {IMAGE }}=f_{\text {SIGNAL }}+2 * f_{I F}=868.3 \mathrm{MHz}+2 * 289.4=1447.2 \mathrm{MHz} \quad[4-5]$

The image suppression on the evalboard is about 16 dB .

## LO-leakage:

The LO of the $1^{\text {st }}$ Mixer is at:
$f_{\text {LO }}=f_{\text {RECEVE }} * \frac{4}{3}=868.3 \mathrm{MHz}^{*} * \frac{4}{3}=1157.73 \mathrm{MHz} \quad[4-6]$

The LO-leakage of the evalboard on the RF-input is about -98 dBm . This is far below the ETSI-radio-regulation-limit for LO-leakage.

### 4.1.1.2 Switch in TX-Mode

The evalboard can be set into the TX-Mode by grounding the RX/TX-jumper on the evalboard or programming the TDA5250 to operate in the TX-Mode. If the IC is programmed to operate in the TX-Mode, the RX/TX-pin will act as an open drain output at a logical LOW. Then a DC-current can flow from VCC to GND via L1, L2, D1, R1 and D2.
$I_{\text {PIN-DIODE }}=\frac{V c c-2 * V_{\text {FORWARD,PIN-DIODE }}}{R_{1}} \quad[4-7]$
Now both pin-diodes are biased with a current of approx. $0.3 \mathrm{~mA} @ 3 \mathrm{~V}$ and have a very low impedance for RF.


TX_Mode.wmf
Figure 4-4 TX_Mode

R1 does not influence the matching because of its very high resistance. Due to the large capacitance of $\mathrm{C} 1, \mathrm{C} 6$ and C 5 the circuit can be further simplified for RF:


TX_Mode_simplified.wmf
Figure 4-5 TX_Mode_simplified

The LNA-matching is RF-grounded now, so no power is lost in the LNA-input. The PA-matching consists of C2, C3 L2, C4 and L1.

When designing the matching of the PA, C2 must not be changed anymore because its value is already fixed to the LNA-input-matching

### 4.1.2 Power-Amplifier

The power amplifier operates in a high efficient class $C$ mode. This mode is characterized by a pulsed operation of the power amplifier transistor at a current flow angle of $\theta \ll \pi$. A frequency selective network at the amplifier output passes the fundamental frequency component of the pulse spectrum of the collector current to the load. The load and its resonance transformation to the collector of the power amplifier can be generalized by the equivalent circuit of Figure 4-6. The tank circuit $\mathrm{L} / / \mathrm{C} / / \mathrm{RL}$ in parallel to the output impedance of the transistor should be in resonance at the operating frequency of the transmitter.


Equivalent_power_wmf.
Figure 4-6 Equivalent power amplifier tank circuit

The optimum load at the collector of the power amplifier for "critical" operation under idealized conditions at resonance is:

$$
R_{L C}=\frac{V_{S}^{2}}{2 P_{O}}
$$

$$
[4-8]
$$

A typical value of $R_{L C}$ for an RF output power of $P_{0}=13 \mathrm{~mW}$ is:

$$
R_{L C}=\frac{3^{2}}{2 * 0.013}=350 \Omega
$$

"Critical" operation is characterized by the RF peak voltage swing at the collector of the PA transistor to just reach the supply voltage $\mathrm{V}_{\mathrm{S}}$. The high efficiency under "critical" operating conditions can be explained by the low power loss at the transistor.
During the conducting phase of the transistor there is no or only a very small collector voltage present, thus minimizing the power loss of the transistor ( $\mathrm{i}_{\mathrm{C}}{ }^{*} \mathrm{u}_{\mathrm{CE}}$ ). This is particularly true for low current flow angles of $\theta \ll \pi$. In practice the RF-saturation voltage of the PA transistor and other parasitics will reduce the "critical" $R_{\text {LC }}$.

The output power $P_{o}$ will be reduced when operating in an "overcritical" mode at a $R_{L}>R_{L C}$. As shown in Figure 4-7, however, power efficiency $E$ (and bandwidth) will increase by some degree when operating at higher $R_{L}$. The collector efficiency $E$ is defined as

$$
\begin{equation*}
E=\frac{P_{o}}{V_{S} I_{C}} \tag{4-10}
\end{equation*}
$$

The diagram of Figure 4-7 has been measured directly at the PA-output at $\mathrm{V}_{\mathrm{S}}=3 \mathrm{~V}$. A power loss in the matching circuit of about 2 dB will decrease the output power. As shown in the diagram, 240 Ohm is the optimum impedance for operation at 3 V . For an approximation of $\mathrm{R}_{\text {OPT }}$ and $\mathrm{P}_{\text {OUT }}$ at other supply voltages those 2 formulas can be used:

$$
R_{O P T} \sim V_{S} \quad[4-11]
$$

and

$$
\begin{equation*}
P_{O U T} \sim R_{O P T} \tag{4-12}
\end{equation*}
$$



Power E vs RL.wmf
Figure 4-7 Output power $P_{\mathrm{O}}(\mathrm{mW})$ and collector efficiency $E$ vs. load resistor $R_{L}$.

The DC collector current $I_{c}$ of the power amplifier and the RF output power $P_{o}$ vary with the load resistor $R_{L}$. This is typical for overcritical operation of class $C$ amplifiers. The collector current will show a characteristic dip at the resonance frequency for this type of "overcritical" operation. The depth of this dip will increase with higher values of $R_{L}$.

As Figure 4-8 shows, detuning beyond the bandwidth of the matching circuit results in a significant increase of collector current of the power amplifier and in some loss of output power. This diagram shows the data for the circuit of the test board at the frequency of 868 MHz . The effective load resistor of this circuit is $R_{L}=2400 \mathrm{hm}$, which is the optimum impedance for operation at 3 V . This will lead to a dip of the collector current of approx. $20 \%$.

pout_vs_frequ.wmf
Figure 4-8 Power output and collector current vs. frequency

C 4 , L2 and C 3 IIC 2 are the main matching components which are used to transform the 50 Ohm load at the SMA-RF-connector to a higher impedance at the PA-output (2400hm@3V). L1 can be used for finetuning of the resonance frequency but should not be too low in order to keep its loss low.

The transformed impedance of $2400 h m+j 0$ at the PA-output-pin can be verified with a network analyzer using this measurement procedure:

1. Calibrate your network analyzer.
2. Connect a short, low-loss 50 Ohm cable to your network analyzer with an open end on one side. Semirigid cable works best.
3. Use the „Port Extension" feature of your network analyzer to shift the reference plane of your network analyzer to the open end of the cable.
4. Connect the center-conductor of the cable to the solder pad of the pin „PA" of the IC. The shield has to be grounded. Very short connections must be used. Do not remove the IC or any part of the matching-components!
5. Screw a 500hm-dummy-load on the RF-I/O-SMA-connector
6. The TDA5250 has to be in ASK-TX-Mode, Data-Input=LOW.
7. Be sure that your network analyzer is AC-coupled and turn on the power supply of the IC.
8. Measure the S-parameter


Figure 4-9 Sparam_measured 200 M

Above you can see the measurement of the evalboard with a span of 200 MHz . The evalboard has been optimized for 3 V . The load is about $240+\mathrm{jO}$ at 868.3MHz.

A tuning-free realization requires a careful design of the components within the matching network. A simple linear CAE-tool will help to see the influence of tolerances of matching components.

Suppression of spurious harmonics may require some additional filtering within the antenna matching circuit. Both can be seen in Figure 4-10 and Figure 4-11 The total spectrum of the evalboard can be summarized as:

| Carrier fc | +9 dBm |
| :--- | :--- |
| $\mathrm{fc}-18.1 \mathrm{MHz}$ | -62 dBm |
| $\mathrm{fc}+18.1 \mathrm{MHz}$ | -66 dBm |
| $2^{\text {nd }}$ harmonic | -40 dBm |
| $3^{\text {rd }}$ harmonic | -44 dBm |



Figure 4-10 Transmit Spectrum 13.2GHz

spektrum_10r_3v.tif
Figure 4-11 Transmit Spectrum 300MHz

Regarding CEPT ERC recommendation 70-03 and ETSI regulation EN 300220 both of the following figures show full compliance in case of ASK and FSK modulation spectrum. Data signal is a Manchester encoded PRBS9 (Pseudo Random Binary Sequence), RF output power is +9 dBm at a supply voltage of 3 V . With these settings ASK allows a maximum data rate of 25 kBaud , in FSK case 40 kBaud are possible. See also Section 5.1.4


ASK_25kBaud_Manch_PRBS9_10dBm_3V_Spectrum_CEPT_ERC7003.wm
Figure 4-12 ASK Transmit Spectrum 25kBaud, Manch, PRBS9, 9dBm, 3V


FSK 40kBaud Manch PRBS9 10dBm 3V Spectrum CEPT ERC7003.wmf
Figure 4-13 FSK Transmit Spectrum 40kBaud, Manch, PRBS9, 9dBm, 3V

### 4.2 Crystal Oscillator

The equivalent schematic of the crystal with its parameters specified by the crystal manufacturer can be taken from the subsequent figure.

Here also the load capacitance of the crystal $C_{L}$, which the crystal wants to see in order to oscillate at the desired frequency, can be seen.


Crystal.wmf
Figure 4-14 Crystal
$L_{1}$ : motional inductance of the crystal
$\mathrm{C}_{1}$ : motional capacitance of the crystal
$\mathrm{C}_{0}$ : shunt capacitance of the crystal

Therefore the Resonant Frequency $\mathbf{f}_{\mathrm{s}}$ of the crystal is defined as:

$$
\begin{equation*}
f_{S}=\frac{1}{2 \pi \sqrt{L_{1} * C_{L}}} \tag{4-13}
\end{equation*}
$$

The Series Load Resonant Frequency $\mathbf{f}_{S}$ ' of the crystal is defined as:

$$
f_{S} `=\frac{1}{2 \pi \sqrt{L_{1} * C_{1}}} * \sqrt{1+\frac{C_{1}}{C_{0}+C_{L}}}
$$

regarding Figure 4-14
$f_{s}$ ' is the nominal frequency of the crystal with a specified load when tested by the crystal manufacturer.

Pulling Sensitivity of the crystal is defined as the magnitude of the relative change in frequency relating to the variation of the load capacitor.

$$
\begin{equation*}
\frac{\delta D}{\delta C_{L}}=\frac{\delta f_{S}^{\prime} / f_{S}}{\delta C_{L}}=\frac{-C_{1}}{2\left(C_{0}+C_{L}\right)^{2}} \tag{4-15}
\end{equation*}
$$

Choosing $\mathrm{C}_{\mathrm{L}}$ as large as possible results in a small pulling sensitivity. On the other hand a small $C_{L}$ keeps the influence of the serial inductance and the tolerances associated to it small (see formula [4-17]).

## Start-up Time

$$
\begin{equation*}
t_{\text {Start }} \sim \frac{L_{1}}{|-R|-R_{e x t}} \tag{4-16}
\end{equation*}
$$

where: -R: is the negative impedance of the oscillator (see fig. [4-15])
$R_{\text {ext }}$ : is the sum of all external resistances (e.g. $R_{1}$ or any other resistance that may be present in the circuit, see figure [4-14]

The proportionality of $L_{1}$ and $C_{1}$ of the crystal is defined by formula [4-13]. For a crystal with a small $\mathrm{C}_{1}$ the start -up time will also be slower. Typically the lower the value of the crystal frequency, the lower the $\mathrm{C}_{1}$.

A short conclusion regarding crystal and crystal oscillator dependencies is shown in the following table:

Table 4-1 Crystal and crystal oscilator dependency
Result

| Independent variable | Relative <br> Tolerance | Result <br> Meviation | $\mathbf{t}_{\text {Start-up }}$ |
| :--- | :---: | :---: | :---: |

The crystal oscillator in the TDA5250 is a NIC (negative impedance converter) oscillator type. The input impedance of this oscillator is a negative impedance in series to an inductance. Therefore the load capacitance of the crystal $C_{L}$ (specified by the crystal supplier) is transformed to the capacitance $\mathrm{C}_{\mathrm{v}}$ as shown in formula [4-17].


Figure 4-15 Crystal Oscillator

$$
C_{L}=\frac{1}{\frac{1}{C_{V}}-\omega^{2} L_{O S C}} \leftrightarrow C_{V}=\frac{1}{\frac{1}{C_{L}}+\omega^{2} L_{O S C}}
$$

$C_{L}$ : crystal load capacitance for nominal frequency
$\omega$ : angular frequency
Losc: inductivity of the crystal oscillator - typ: $2.7 \mu \mathrm{H}$

With the aid of this formula it becomes obvious that the higher the serial capacitance $C_{V}$ is, the higher is the influence of $L_{\text {Osc }}$.

The tolerance of the internal oscillator inductivity is much higher, so the inductivity is the dominating value for the tolerance.

FSK modulation and tuning are achieved by a variation of $\mathrm{C}_{\mathrm{v}}$.
In case of small frequency deviations (up to +/- 1000 ppm ), the desired load capacitances for FSK modulation are frequency depending and can be calculated with the formula below.

$$
\begin{equation*}
\mathrm{C}_{\mathrm{L} \pm}=\frac{\mathrm{C}_{\mathrm{L}} \mp \mathrm{C}_{0} \cdot \frac{\Delta \mathrm{f}}{\mathrm{~N} \cdot \mathrm{f}} \cdot\left(1+\frac{2 \cdot\left(\mathrm{C}_{0}+\mathrm{C}_{\mathrm{L}}\right)}{\mathrm{C}_{1}}\right)}{1 \pm \frac{\Delta \mathrm{f}}{\mathrm{~N} \cdot \mathrm{f}} \cdot\left(1+\frac{2 \cdot\left(\mathrm{C}_{0}+\mathrm{C}_{\mathrm{L}}\right)}{\mathrm{C}_{1}}\right)} \tag{4-18}
\end{equation*}
$$

$\mathrm{C}_{\mathrm{L}}$ : crystal load capacitance for nominal frequency
$\mathrm{C}_{0}$ : shunt capacitance of the crystal
$\mathrm{C}_{1}$ : motional capacitance of the crystal
f: crystal oscillator frequency
N : division ratio of the PLL
$\Delta \mathrm{f}$ : peak frequency deviation

With $\mathrm{C}_{\mathrm{L}_{+}}$and $\mathrm{C}_{\mathrm{L}}$ the necessary $\mathrm{C}_{\mathrm{V}+}$ for FSK HIGH and $\mathrm{C}_{\mathrm{V}-}$ for FSK LOW can be calculated.
Alternatively, an external AC coupled ( 10 nF in series to $1 \mathrm{k} \Omega$ ) signal can be applied at pin 19 (Xout). The drive level should be approximately 100mVpp.

### 4.2.1 Synthesizer Frequency setting

Generating ASK and FSK modulation 3 setable frequencies are necessary.

### 4.2.1.1 Possible crystal oscillator frequencies

The resulting possible crystal oscillator frequencies are shown in the following Figure 4-16


Figure 4-16 possible crystal oscillator frequencies

In ASK receive mode the crystal oscillator is set to frequency $f_{2}$ to realize the necessary frequency offset to receive the ASK signal at $\mathrm{f}_{0}{ }^{*} \mathrm{~N}(\mathrm{~N}$ : division ratio of the PLL)

To set the 3 different frequencies 3 different $C_{v}$ are necessary. Via internal switches 3 external capacitors can be combined to generate the necessary $C_{v}$ in case of ASK- or FSK-modulation. Internal banks of switchable capacitors allow the finetuning of these frequencies.

### 4.2.2 Transmit/Receive ASK/FSK Frequency Assignment

Depending on whether the device operates in transmit or receive mode or whether it operates in ASK or FSK the following cases can be distinguished:

### 4.2.2.1 FSK-mode:

In transmit mode the two frequencies representing logical HIGH and LOW data states have to be adjusted depending on the intended frequency deviation and separately according to the following formulas:
$\mathrm{f}_{\mathrm{COSC}} \mathrm{HI}=\left(\mathrm{f}_{\mathrm{RF}}+\mathrm{f}_{\mathrm{DEV}}\right) / 48 \quad \mathrm{f}_{\mathrm{COSC}}$ LOW $=\left(\mathrm{f}_{\mathrm{RF}}-\mathrm{f}_{\mathrm{DEV}}\right) / 48 \quad[4-19]$
e.g.

$$
\begin{aligned}
& \mathrm{f}_{\mathrm{COSCHI}}=(868,3 \mathrm{E} 6+50 \mathrm{E} 3) / 48=18.08438 \mathrm{MHz} \\
& \mathrm{f}_{\mathrm{COSC} \text { LOW }}=(868,3 \mathrm{E} 6-50 \mathrm{E} 3) / 48=18.08229 \mathrm{MHz}
\end{aligned}
$$

with a frequency deviation of 50 kHz .
Figure 4-17 shows the configuration of the switches and the capacitors to achieve the 2 desired frequencies. Gray parts of the schematics indicate inactive parts. For FSK modulation the ASK-switch is always open.

For FSK LOW the FSK-switch is closed and $\mathrm{C}_{\mathrm{v} 2}$ and $\mathrm{C}_{\text {tune2 }}$ are bypassed. The effective $\mathrm{C}_{\mathrm{V} \text { - }}$ is given by:

$$
C_{V-}=C_{v 1}+C_{\text {tune1 }}
$$

For finetuning $\mathrm{C}_{\text {tune1 }}$ can be varied over a range of 8 pF in steps of 125 fF . The switches of this C-bank are controlled by the bits D0 to D5 in the FSK register (subaddress 01 H , see Table 4-6).

For FSK HIGH the FSK-switch is open. So the effective $\mathrm{C}_{\mathrm{v}+}$ is given by:

$$
\begin{equation*}
\mathrm{C}_{\mathrm{v}+}=\frac{\left(\mathrm{C}_{\mathrm{v} 1}+\mathrm{C}_{\text {tune } 1}\right) \cdot\left(\mathrm{C}_{\mathrm{v} 2}+\mathrm{C}_{\text {tune } 2}\right)}{\mathrm{C}_{\mathrm{v} 1}+\mathrm{C}_{\text {tune } 1}+\mathrm{C}_{\mathrm{v} 2}+\mathrm{C}_{\text {tune } 2}} \tag{4-21}
\end{equation*}
$$

The C-bank $C_{\text {tune2 }}$ can be varied over a range of 16 pF in steps of 250 fF for finetuning of the FSK HIGH frequency. The switches of this C-bank are controlled by the bits D8 to D13 in the FSK register (subaddress 01H, see Table 4-6).


Figure 4-17 FSK modulation

In receive mode the crystal oscillator frequency is set to yield a direct-to-zero conversion of the receive data. Thus the frequency may be calculated as

$$
\mathrm{f}_{\mathrm{COSC}}=\mathrm{f}_{\mathrm{RF}} / 48
$$

e.g.

$$
f_{\operatorname{COSC}}=868,3 E 6 / 48=18.0833 \mathrm{MHz}
$$

which is identical to the ASK transmit case.


Figure 4-18 FSK receive

In this case the ASK-switch is closed. The necessary $\mathrm{C}_{\mathrm{vm}}$ is given by:

$$
\begin{equation*}
\mathrm{C}_{\mathrm{vm}}=\frac{\left(\mathrm{C}_{\mathrm{v} 1}+\mathrm{C}_{\text {tune } 1}\right) \cdot\left(\mathrm{C}_{\mathrm{v} 2}+\mathrm{C}_{\mathrm{v} 3}+\mathrm{C}_{\text {tune } 2}\right)}{\mathrm{C}_{\mathrm{v} 1}+\mathrm{C}_{\text {tune } 1}+\mathrm{C}_{\mathrm{v} 2}+\mathrm{C}_{\mathrm{v} 3}+\mathrm{C}_{\text {tune } 2}} \tag{4-23}
\end{equation*}
$$

The C-bank $C_{\text {tune2 }}$ can be varied over a range of 16 pF in steps of 250 fF for finetuning of the FSK receive frequency. In this case the switches of the C-bank are controlled by the bits D0 to D5 of the XTAL_TUNING register (subaddress 02H, see Table 4-5).

### 4.2.2.2 ASK-mode:

In transmit mode the crystal oscillator frequency is the same as in the FSK receive case, see Figure 4-18.

In receive mode a receive frequency offset is necessary as the limiters feedback is AC-coupled. This offset is achieved by setting the oscillator frequency to the FSK HIGH transmit frequency, see Figure 4-17.

### 4.2.3 Parasitics

For the correct calculation of the external capacitors the parasitic capacitances of the pins and the switches $\left(\mathrm{C}_{20}, \mathrm{C}_{21}, \mathrm{C}_{22}\right)$ have to be taken into account.


Figure 4-19 parasitics of the switching network

| Table 4-2 Typical values of parasitic capacitances |  |
| :---: | :---: |
| Name | Value |
| $\mathrm{C}_{20}$ | $4,5 \mathrm{pF}$ |
| $\mathrm{C}_{21}$ | FSK-: $2,8 \mathrm{pF} / \mathrm{FSK}+$ \&ASK: 2.3 pF |
| $\mathrm{C}_{22}$ | $1,3 \mathrm{pF}$ |

With the given parasitics the actual $\mathrm{C}_{\mathrm{v}}$ can be calculated:

$$
\begin{gathered}
\mathrm{C}_{\mathrm{v}-}=\mathrm{C}_{\mathrm{v} 1}+\mathrm{C}_{\text {tune } 1}+\mathrm{C}_{21} \\
\mathrm{C}_{\mathrm{v}+}=\frac{\left(\mathrm{C}_{\mathrm{v} 1}+\mathrm{C}_{\text {tune }}\right) \cdot\left(\mathrm{C}_{\mathrm{v} 2}+\mathrm{C}_{20}+\mathrm{C}_{\text {tune } 2}\right)}{\mathrm{C}_{\mathrm{v} 1}+\mathrm{C}_{\text {tune } 1}+\mathrm{C}_{\mathrm{v} 2}+\mathrm{C}_{20}+\mathrm{C}_{\text {tune } 2}}+\mathrm{C}_{21} \\
\mathrm{C}_{\mathrm{vm}}=\frac{\left(\mathrm{C}_{\mathrm{v} 1}+\mathrm{C}_{\text {tune } 1}\right) \cdot\left(\mathrm{C}_{\mathrm{v} 2}+\mathrm{C}_{20}+\mathrm{C}_{\mathrm{v} 3}+\mathrm{C}_{22}+\mathrm{C}_{\text {tune } 2}\right)}{\mathrm{C}_{\mathrm{v} 1}+\mathrm{C}_{\text {tune } 1}+\mathrm{C}_{\mathrm{v} 2}+\mathrm{C}_{20}+\mathrm{C}_{\mathrm{v} 3}+\mathrm{C}_{22}+\mathrm{C}_{\text {tune } 2}}+\mathrm{C}_{21}
\end{gathered}
$$

Note: Please keep in mind also to include the Pad parasitics of the circuit board.

### 4.2.4 Calculation of the external capacitors

1. Determination of necessary crystal frequency using formula [4-19].
e.g. $\mathrm{f}_{\mathrm{FSK}}=\mathrm{f}_{\mathrm{COSC}}$ Low
2. Determine corresponding $C_{\text {Load }}$ applying formula [4-18].
e.g. $C_{L F S K}=C_{L \pm}$
3. Necessary $\mathrm{C}_{\mathrm{V}}$ using formula [4-17].
e.g.

$$
C_{V-}=\frac{1}{\frac{1}{C_{L, F S K-}}+\left(2 \pi f_{F S K-}\right)^{2} * L_{O S C}}
$$

4. When the necessary $\mathrm{C}_{\mathrm{v}}$ for the 3 frequencies ( $\mathrm{C}_{\mathrm{v}}$ - for FSK LOW, $\mathrm{C}_{\mathrm{v}+}$ for FSK HIGH and $\mathrm{C}_{\mathrm{vm}}$ for FSK-receive) are known the external capacitors and the internal tuning caps can be calculated using the following formulas:
-FSK:

$$
\mathrm{C}_{\mathrm{v} 1}+\mathrm{C}_{\text {tune } 1}=\mathrm{C}_{\mathrm{v}-}-\mathrm{C}_{21}
$$

$$
[4-27]
$$

+FSK:

$$
\begin{equation*}
\mathrm{C}_{\mathrm{v} 2}+\mathrm{C}_{\text {tune } 2}=\frac{\left(\mathrm{C}_{\mathrm{v} 1}+\mathrm{C}_{\text {tune } 1}\right) \cdot\left(\mathrm{C}_{\mathrm{v}+}-\mathrm{C}_{21}\right)}{\left(\mathrm{C}_{\mathrm{v} 1}+\mathrm{C}_{\text {tune } 1}\right)-\left(\mathrm{C}_{\mathrm{v}+}-\mathrm{C}_{21}\right)}-\mathrm{C}_{20} \tag{4-28}
\end{equation*}
$$

FSK_RX:

$$
\begin{equation*}
\mathrm{C}_{\mathrm{v} 3}+\mathrm{C}_{\text {tune } 2}=\frac{\left(\mathrm{C}_{\mathrm{v} 1}+\mathrm{C}_{\text {tune } 1}\right) \cdot\left(\mathrm{C}_{\mathrm{vm}}-\mathrm{C}_{21}\right)}{\left(\mathrm{C}_{\mathrm{v} 1}+\mathrm{C}_{\text {tune } 1}\right)-\left(\mathrm{C}_{\mathrm{vm}}-\mathrm{C}_{21}\right)}-\mathrm{C}_{20}-\mathrm{C}_{\mathrm{v} 2}-\mathrm{C}_{22} \tag{4-29}
\end{equation*}
$$

To compensate frequency errors due to crystal and component tolerance $\mathrm{C}_{\mathrm{v} 1}$, $\mathrm{C}_{\mathrm{v} 2}$ and $\mathrm{C}_{\mathrm{v} 3}$ have to be varied. To enable this correction, half of the necessary capacitance variation has to be realized with the internal C-banks.

If no finetuning is intended it is recommended to leave XIN (Pin 21) open. So the parasitic capacitance of Pin 21 has no effect.

Note: Please keep in mind also to include the Pad parasitics of the circuit board.
In the suitable range for the serial capacitor, either capacitors with a tolerance of 0.1 pF or $1 \%$ are available.

A spreadsheet, which can be used to predict the total frequency error by simply entering the crystal specification, may be obtained from Infineon.

### 4.2.5 FSK-switch modes

The FSK-switch can be used either in a bipolar or in a FET mode. The mode of this switch is controlled by bit DO of the XTAL_CONFIG register (subaddress 0EH).

In the bipolar mode the FSK-switch can be controlled by a ramp function. This ramp function is set by the bits D1 and D2 of the XTAL_CONFIG register (subadress 0 EH ). With these modes of the FSK-switch the bandwidth of the FSK spectrum can be influenced.

When working in the FET mode the power consumption can be reduced by about $200 \mu \mathrm{~A}$.

The default mode is bipolar switch with no ramp function ( $\mathrm{D} 0=1, \mathrm{D} 1=\mathrm{D} 2=0$ ), which is suitable for all bitrates.

Table 4-3 Sub Address 0EH: XTAL_CONFIG

| D0 | D1 | D2 | Switch mode | Ramp time | Max. Bitrate |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | n.a. | n.a. | FET | $<0.2 \mu \mathrm{~s}$ | $>32 \mathrm{kBit} / \mathrm{s}$ NRZ |
| $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | bipolar (default) | $<\mathbf{0 . 2} \boldsymbol{\mu s}$ | $>\mathbf{3 2} \mathbf{~ k B i t} / \mathrm{s}$ NRZ |
| $\mathbf{1}$ | 1 | 0 | bipolar | $4 \mu \mathrm{~s}$ | $32 \mathrm{kBit} / \mathrm{s} \mathrm{NRZ}$ |
| $\mathbf{1}$ | 0 | 1 | bipolar | $8 \mu \mathrm{~s}$ | $16 \mathrm{kBit} / \mathrm{s} \mathrm{NRZ}$ |
| $\mathbf{1}$ | 1 | 1 | bipolar | $12 \mu \mathrm{~s}$ | $12 \mathrm{kBit} / \mathrm{s} \mathrm{NRZ}$ |

### 4.2.6 Finetuning and FSK modulation relevant registers

Case FSK-RX or ASK-TX ( $\mathrm{C}_{\text {tune2 }}$ ):

| Table 4-4 | Sub Address 02H: XTAL_TUNING |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| Bit | Function | Value | Description | Default |
| D5 | Nominal_Frequ_5 | 8pF | Setting for nominal frequency | 0 |
| D4 | Nominal_Frequ_4 | 4 pF |  | 1 |
| D3 | Nominal_Frequ_3 | 2 pF | ASK-TX FSK-RX | 0 |
| D2 | Nominal_Frequ_2 | 1 pF |  | 0 |
| D1 | Nominal_Frequ_1 | 500fF | $\left(\mathrm{C}_{\text {tune2 }}\right)$ | 1 |
| D0 | Nominal_Frequ_0 | 250fF |  | 0 |

Case FSK-TX or ASK-RX ( $\mathrm{C}_{\text {tune } 1}$ and $\left.\mathrm{C}_{\text {tune2 }}\right)$ :

| Table 4-5 | Sub Address 01H: FSK |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| Bit | Function | Value | Description | Default |
| D13 | FSK+5 | 8pF | Setting for positive frequency shift: +FSK or ASK-RX | 0 |
| D12 | FSK+4 | 4pF |  | 0 |
| D11 | FSK+3 | 2pF |  | 1 |
| D10 | FSK+2 | 1 pF |  | 0 |
| D9 | FSK+1 | 500fF | ( $\mathrm{C}_{\text {tune2 }}$ ) | 1 |
| D8 | FSK+0 | 250fF |  | 0 |
| D5 | FSK-5 | 4pF | Setting for negative frequency shift: -FSK | 0 |
| D4 | FSK-4 | 2 pF |  | 0 |
| D3 | FSK-3 | 1 pF |  | 1 |
| D2 | FSK-2 | 500fF | (C $\mathrm{C}_{\text {tune1 }}$ ) | 1 |
| D1 | FSK-1 | 250fF |  | 0 |
| D0 | FSK-0 | 125fF |  | 0 |

## Default values

In case of using the evaluation board, the crystal with its typical parameters ( $\mathrm{fp}=18.08958 \mathrm{MHz}, \mathrm{C}_{1}=8 \mathrm{fF}, \mathrm{C}_{0}=2,08 \mathrm{pF}, \mathrm{C}_{\mathrm{L}}=12 \mathrm{pF}$ ) and external capacitors with $\mathrm{Cv} 1=4.7 \mathrm{pF}, \mathrm{Cv} 2=1.8 \mathrm{pF}, \mathrm{Cv} 3=12 \mathrm{pF}$ each are used the following default states are set in the device.

| Table 4-6 Default oscillator settings |  |
| :---: | :---: |
| Operating state | Frequency |
| ASK-TX / FSK-RX | 868.3 MHz |
| +FSK-TX / ASK-RX | +50 kHz |
| -FSK-TX | -50 kHz |

### 4.2.7 Chip and System Tolerances


Cv1=4.7pF, Cv2=1.8pF, Cv3=12pF

| Table 4-7 Internal Tuning | Frequency <br> tolerance @ <br> 868 MHz | Rel. <br> tolerance |
| :---: | :---: | :---: |
| Frequency set accuracy | $+/-3 \mathrm{kHz}$ | $+/-3.5 \mathrm{ppm}$ |
| Temperature $(-40 \ldots+85 \mathrm{C})$ | $+/-5 \mathrm{kHz}$ | $+/-6 \mathrm{ppm}$ |
| Supply Voltage(2.1...5.5V) | $+/-1.5 \mathrm{kHz}$ | $+/-1.5 \mathrm{ppm}$ |
| Total | $+/-9.5 \mathrm{kHz}$ | $+/-11 \mathrm{ppm}$ |


| Table 4-8 Default Setup (without internal tuning \& without Pin21 usage) |  |  |
| :---: | :---: | :---: |
| Part | Frequency <br> tolerance @ <br> $\mathbf{8 6 8 M H z}$ | Rel. <br> tolerance |
| Internal capacitors (+/- 10\%) | $+/-8 \mathrm{kHz}$ | $+/-9 \mathrm{ppm}$ |
| Inductivity of the crystal oscillator | $+/-18 \mathrm{kHz}$ | $+/-21 \mathrm{ppm}$ |
| Temperature (-40... $+85 \mathrm{C})$ | $+/-5 \mathrm{kHz}$ | $+/-6 \mathrm{ppm}$ |
| Supply Voltage $(2.1 \ldots 5.5 \mathrm{~V})$ | $+/-1 \mathrm{kHz}$ | $+/-1.5 \mathrm{ppm}$ |
| Total | $+/-32 \mathrm{kHz}$ | $+/-37.5 \mathrm{ppm}$ |

Tolerance values in Table 4-9 are valid, if pin 21 is not connected. Establishing the connection to pin 21 the tolerances increase by $+/-23.5 \mathrm{ppm}$ (internal capacitors $+/-20 \mathrm{ppm}$, frequency set accurancy $+/-3.5 \mathrm{ppm}$ ), if internal tuning is not used.

Concerning the frequency tolerances of the whole system also crystal tolerances (tuning tolerances, temperature stability, tolerance of $\mathrm{C}_{\mathrm{L}}$ ) have to be considered.

In addition to the chip tolerances also the crystal and external component tolerances have to be considered in the tuning and non-tuning case.

In case of internal tuning: The crystal on the evaluation board has a temperature stability of $+/-20 \mathrm{ppm}$ (or $+/-17 \mathrm{kHz}$ ), which must be added to the total tolerances.

In case of default setup (without internal tuning and without usage of pin 21) the temperature stability and tuning tolerance of the crystal as well as the tolerance of the external capacitors ( $+/-0.1 \mathrm{pF}$ ) have to be added. The crystal on the evaluation board has a temperature stability of $+/-20 \mathrm{ppm}$ (or $+/-17 \mathrm{kHz}$ ) and a tuning tolerance of $+/-10 \mathrm{ppm}$ (or $+/-8.5 \mathrm{kHz}$ ). The external capacitors add a tolerance of $+/-4 \mathrm{ppm}$ (or $+/-3.5 \mathrm{kHz}$ ).

The frequency stabilities of both the receiver and the transmitter and the modulation bandwidth set the limit for the bandwidth of the IQ filter. To achieve a high receiver sensitivity and efficient suppression of adjacent interference signals, the narrowest possible IQ bandwidth should be realized (see Section 4.3).

### 4.3 IQ-Filter

The IQ-Filter should be set to values corresponding to the RF-bandwidth of the received RF signal via the D1 to D3 bits of the LPF register (subaddress 03H).

| Table 4-9 3dB cutoff frequencies I/Q Filter |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| D3 | D2 | D1 | nominal $\mathbf{f}$-3dB in $\mathbf{~ k H z}$ <br> (programmable) | resulting effective <br> channel <br> bandwidth in $\mathbf{~ k H z}$ |
| 0 | 0 | 0 | not used |  |
| 0 | 0 | 1 | 350 | 700 |
| 0 | 1 | 0 | 250 | 500 |
| 0 | 1 | 1 | 200 | 400 |
| $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{1 5 0}$ (default) |  |
| 1 | 0 | 1 | 100 | $\mathbf{3 0 0}$ |
| 1 | 1 | 0 | 50 | 200 |
| $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ | not used | 100 |



Figure 4-20 I/Q Filter Characteristics

iq_char.wmf
Figure 4-21 IQ Filter and frequency characteristics of the receive system

### 4.4 Data Filter

The Data-Filter should be set to values corresponding to the bandwidth of the transmitted Data signal via the D4 to D7 bits of the LPF register (subaddress 03H).

| Table 4-10 3dB cutoff frequencies Data Filter |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| D7 | D6 | D5 | D4 | nominal $\mathbf{f}_{-3 d B}$ in $\mathbf{k H z}$ |
| 0 | 0 | 0 | 0 | 5 |
| $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{7}$ (default) |
| 0 | 0 | 1 | 0 | 9 |
| 0 | 0 | 1 | 1 | 11 |
| 0 | 1 | 0 | 0 | 14 |
| 0 | 1 | 0 | 1 | 18 |
| 0 | 1 | 1 | 0 | 23 |
| 0 | 1 | 1 | 1 | 28 |
| 1 | 0 | 0 | 0 | 32 |
| 1 | 0 | 0 | 1 | 39 |
| 1 | 0 | 1 | 0 | 49 |
| 1 | 0 | 1 | 1 | 55 |
| 1 | 1 | 0 | 0 | 64 |
| 1 | 1 | 0 | 1 | 73 |
| 1 | 1 | 1 | 0 | 86 |
| 1 | 1 | 1 | 1 | 102 |

### 4.5 Limiter and RSSI

The I/Q Limiters are DC coupled multistage amplifiers with offset-compensating feedback circuit and an overall gain of approximately 80 dB each in the frequency range of 100 Hz up to 350 kHz . Receive Signal Strength Indicator (RSSI) generators are included in both limiters which produce DC voltages that are directly proportional to the input signal level in the respective channels. The resulting I- and Q-channel RSSI-signals are summed to the nominal RSSI signal.


Figure 4-22 Limiter and Pinning

The DC offset compensation needs 2.2 ms after Power On or Tx/Rx switch. This time is hard wired and independent from external capacitors $C_{C}$ on pins 31 to 38 . The maximum value for this capacitors is 47 nF .

RSSI accuracy settling time $=2.2 \mathrm{~ms}+5^{*} \mathrm{RC}=2.2 \mathrm{~ms}+5 * 37 \mathrm{k}^{*} 2.2 \mathrm{nF}=2.6 \mathrm{~ms}$
R - internal resistor; C - external capacitor at Pin 29

| Table 4-11 Limiter Bandwidth | f3dB <br> lowe limit <br> $[\mathrm{Hz}]$ | f3dB <br> upper <br> limit | Comment |
| :---: | :---: | :---: | :---: |
| $[\mathrm{nF}]$ | 100 | IQ Filter | setup time not <br> guaranteed <br> setup time not <br> guaranteed |
| 220 | 220 | - II - | Eval Board |
| 100 | 470 | - II - |  |
| 47 | 1000 | - II - |  |
| 22 | 2200 | $-I I-$ |  |
| 10 |  |  |  |


limiter_char.wmf
Figure 4-23 Limiter frequency characteristics


Figure 4-24 Typ. RSSI Level (Eval Board) @3V

### 4.6 Data Slicer - Slicing Level

The data slicer is an analog-to-digital converter. It is necessary to generate a threshold value for the negative comparator input (data slicer). The TDA5250 offers an RC integrator and a peak detector which can be selected via logic. Independent of the choice, the peak detector outputs are always active.

### 4.6.1 RC Integrator

| Table 4-12 Sub Address 00H: CONFIG |  |  |  |  |  |
| :---: | :--- | :--- | :---: | :---: | :---: |
| Bit | Function | Description | Default | SET |  |
| D15 | SLICER | $0=$ LP, 1= Peak Detector | 0 | $\mathbf{0}$ |  |

Necessary external component (Pin14): $\mathrm{C}_{\text {SLC }}$
This integrator generates the mean value of the data filter output. For a stable threshold value, the cut-off frequency has to be lower than the lowest signal frequency. The cutoff frequency results from the internal resistance $R=100 \mathrm{k} \Omega$ and the external capacitor $\mathrm{C}_{\text {SLC }}$ on Pin14.

Cut-off frequency:

$$
f_{\text {cut-off }}=\frac{1}{2 \pi \cdot 100 k \Omega \cdot C_{S L C}}<\operatorname{Min}\left\{f_{\text {Signal }}\right\} \quad[4-30]
$$

Component calculation: (rule of thumb)
$T_{L}$ - longest period of no signal change

$$
\begin{equation*}
C_{S L C} \geq \frac{3 \cdot T_{L}}{100 k \Omega} \tag{4-31}
\end{equation*}
$$



Figure 4-25 Slicer Level using RC Integrator

### 4.6.2 Peak Detectors

| Table 4-13 Sub Address 00H: CONFIG |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Bit | Function | Description | Default | SET |  |
| D15 | SLICER | $0=$ LP, $1=$ Peak Detector | 0 | 1 |  |

The TDA5250 has two peak detectors built in, one for positive peaks in the data stream and the other for the negative ones.

Necessary external components: - Pin12: $\mathrm{C}_{\mathrm{N}}$

- Pin13: $C_{P}$


SLC_PkD.wmf
Figure 4-26 Slicer Level using Peak Detector

For applications requiring fast attack and slow release from the threshold value it is reasonable to use the peak detectors. The threshold value is generated by an internal voltage divider. The release time is defined by the internal resistance values and the external capacitors.

$$
\begin{align*}
& \tau_{\text {posPkD }}=100 \mathrm{k} \Omega \cdot C_{p}  \tag{4-32}\\
& \tau_{n e g P k D}=100 \mathrm{k} \Omega \cdot C_{n} \tag{4-33}
\end{align*}
$$



Figure 4-27 Peak Detector timing

Component calculation: (rule of thumb)
$\mathrm{C}_{\mathrm{p}} \geq \frac{2 \cdot \mathrm{~T}_{\mathrm{L} 1}}{100 \mathrm{k} \Omega}$
$T_{L 1}$ - longest period of no signal change (LOW signal) ${ }^{[4-34]}$
$\mathrm{C}_{\mathrm{n}} \geq \frac{2 \cdot \mathrm{~T}_{\mathrm{L} 2}}{100 \mathrm{k} \Omega}$
$\mathrm{T}_{\mathrm{L} 2}$ - longest period of no signal change (HIGH signal ${ }^{[4-35]}$

### 4.6.3 Peak Detector - Analog output signal

The TDA5250 data output can be digital (pin 28) or in analog form by using the peak detector output and changing some settings.

To get an analog data output the slicer must be set to lowpass mode (Reg. 0, $\mathbf{D 1 5}=\mathbf{L P}=\mathbf{0}$ ) and the peak detector capacitor at pin 12 or 13 has to be changed to a resistor of about 47kOhm.


Figure 4-28 Peak Detector as analog Buffer (v=1)

### 4.6.4 Peak Detector - Power Down Mode

For a safe and fast threshold value generation the peak detector is turned on by the sequencer circuit (see Section 3.4.18) only after the entire receiving path is active.

In the off state the output of the positive peak detector is tied down to GND and the output of the negative peak detector is pulled up to VCC.


Figure 4-29 Peak detector - power down mode


Figure 4-30 Power down mode

### 4.7 Data Valid Detection

In order to detect valid data two criteria must be fulfilled.
One criteria is the data rate, which can be set in register 06h and 07h. The other one is the received RF power level, which can be set in register 08h in form of the RSSI threshold voltage. Thus for using the data valid detection FSK modulation is recommended.

Timing for data detection looks like the following. Two settings are possible: „Continuous" and „Single Shot", which can be set by D5 and D6 in register 00H.


Frequ_Detect_Timing_continuous.wmf
Figure 4-31 Frequency Detection timing in continuous mode

Note 1: Chip internal signal „Sequencer enables data detection" has a LOW to HIGH transition about 2.6 ms after RX is activated (see Figure 3-15).
Note 2: The positive edge of the „Window Count Complete" signal latches the result of comparison of the analog to digital converted RSSI voltage with TH3 (register 08 H ). A logic combination of this output and the result of the comparison with single/double $\mathrm{TH}_{\mathrm{x}}$ defines the internal signal "data_valid".

Figure 4-31 shows that the logic is ready for the next conversion after 3 periods of the data signal.

Timing in Single Shot mode can be seen in the subsequent figure:


Frequ_Detect_Timing_singleShot_wmf
Figure 4-32 Frequency Detection timing in Single Shot mode

### 4.7.1 Frequency Window for Data Rate Detection

The high time of data is used to measure the frequency of the data signal. For Manchester coding either the data frequency or half of the data frequency have to be detected corresponding to one high time or twice the high time of data signal.

A time period of $3^{*} 2^{*} T$ is necessary to decide about valid or invalid data.


Figure 4-33 Window Counter timing

Example to calculate the thresholds for a given data rate:

- Data signal manchester coded
- Data Rate: 2kbit/s
$-\mathrm{f}_{\mathrm{Clk}}=18,0896 \mathrm{MHz}$
Then the period equals to

$$
\begin{equation*}
2 \cdot \mathrm{~T}=\frac{1}{2 \mathrm{kbit} / \mathrm{s}}=0,5 \mathrm{~ms} \tag{4-36}
\end{equation*}
$$

respectively the high time is $0,25 \mathrm{~ms}$.
We set the thresholds to $+-10 \%$ and get: $\mathrm{T} 1=0,225 \mathrm{~ms}$ and $\mathrm{T} 2=0,275 \mathrm{~ms}$

The thresholds TH1 and TH2 are calculated with following formulas:

$$
\begin{align*}
& \mathrm{TH} 1=\mathrm{T} 1 \cdot \frac{\mathrm{f}_{\mathrm{clk}}}{4}  \tag{4-37}\\
& \mathrm{TH} 2=\mathrm{T} 2 \cdot \frac{\mathrm{f}_{\mathrm{clk}}}{4}
\end{align*}
$$

[4-38]

This yields the following results:

$$
\begin{aligned}
& \text { TH1~ 1017 }=00111111001_{\mathrm{b}} \\
& \text { TH2~ 1243 }=010011011011_{\mathrm{b}}
\end{aligned}
$$

which have to be programmed into the D0 to D11 bits of the COUNT_TH1 and COUNT_TH2 registers (subaddresses 06H and 07H), respectively.

Default values (window counter inactive):
$\mathrm{TH} 1=000000000000_{\mathrm{b}}$
$\mathrm{TH} 2=000000000001_{\mathrm{b}}$
Note: The timing window of $+-10 \%$ of a given high time T in general does not correspond to a frequency window $+-10 \%$ of the calculated data frequency.

### 4.7.2 RSSI threshold voltage - RF input power

The RF input power level is corresponding to a certain RSSI voltage, which can be seen in Section 4.5. The threshold TH3 of this RSSI voltage can be calculated with the following formula:
TH3 $=\frac{\text { desired } \quad \text { RSSI } \quad \text { threshold } \quad \text { voltage }}{1.2 \mathrm{~V}} \cdot\left(2^{6}-1\right) \quad[4-39]$

As an example a desired RSSI threshold voltage of 500 mV results in TH3~26=011010 b which has to be written into D0 to D5 of the RSSI_TH3 register (sub address 08 H ).

Default value (RSSI detection inactive):
TH3 $=111111_{b}$

### 4.8 Calculation of ON_TIME and OFF_TIME

$O N=\left(2^{16}-1\right)-\left(f_{R C}{ }^{*} t_{O N}\right)$
$O F F=\left(2^{16}-1\right)-\left(f_{R C}{ }^{*} t_{O F F}\right)$
$f_{R C}=$ Frequency of internal RC Oszillator

Example: $t_{O N}=0,005 \mathrm{~s}, \mathrm{t}_{\mathrm{OFF}}=0,055 \mathrm{~s}, \mathrm{f}_{\mathrm{RC}}=32300 \mathrm{~Hz}$
$O N=65535-(32300 * 0,005) \sim 65373=1111111101011101_{\mathrm{b}}$
$O F F=65535-\left(32300^{*} 0,055\right) \sim 63758=1111100100001110_{b}$

The values have to be written into the D0 to D15 bits of the ON_TIME and OFF_TIME registers (subaddresses 04H and 05H).

Default values:
$\mathrm{ON}=65215=1111111011000000_{\mathrm{b}}$
$O F F=62335=1111001110000000_{b}$
$\mathrm{t}_{\mathrm{ON}} \sim 10 \mathrm{~ms}$ @ $\mathrm{f}_{\mathrm{RC}}=32 \mathrm{kHz}$
$t_{\text {OFF }} \sim 100 \mathrm{~ms}$ @ $f_{R C}=32 \mathrm{kHz}$

### 4.9 Example for Self Polling Mode

The settings for Self Polling Mode depend very much on the timing of the transmitted Signal. To create an example we consider following data structure transmitted in FSK.

data_timing011.wmf
Figure 4-34 Example for transmitted Data-structure

According to existing synchronization techniques there are some synchronization bursts in front of the data added (code violation!). A minimum of 4 Frames is transmitted. Data are preferably Manchester encoded to get fastest respond out of the Data Rate Detection.

## Target Application:

- received Signal has code violation as described before
- total mean current consumption below 1 mA
- data reception within max. 400ms after first transmitted frame


## One possible Solution:

$\mathrm{t}_{\mathrm{ON}}=15 \mathrm{~ms}, \mathrm{t}_{\mathrm{OFF}}=135 \mathrm{~ms}$
This gives 15 ms ON time of a total period of 150 ms which results in max. 0.9 mA mean current consumption in Self Polling Mode. The resulting worst case timing is shown in the following figure:


Figure 4-35 3 possible timings

## Description:

Assumption: the ON time comes right after the first frame (Case A). If OFF time is 135 ms the receiver turns on during Sync-pulses and the Pwd $\overline{\mathrm{DD}}$ - - pulse wakes up the $\mu \mathrm{P}$.
If the ON time is in the center of the 50 ms gap of transmission (Case B), the Data Detect Logic will wake up the $\mu \mathrm{P} 135 \mathrm{~ms}$ later.
If ON time is over just before Sync-pulses (Case C), next ON time is during Data transmission and Data Detect Logic will trigger a PwdDD- pulse to wake up the $\mu \mathrm{P}$.
Note: In this example it is recommended to use the Peak Detector for slicer threshold generation, because of its fast attack and slow release characteristic. To overcome the data zero gap of 50 ms larger external capacitors than noted in Section 5.4 at pin12 and 13 are recommended. Further information on calculating these components can be taken from Section 4.6.2.

### 4.10 Sensitivity Measurements

### 4.10.1 Test Setup

The test setup used for the measurements is shown in the following figure. In case of ASK modulation the Rohde \& Schwarz SMIQ generator, which is a vector signal generator, is connected to the I/Q modulation source AMIQ. This "baseband signal generator" is in turn controlled by the PC based software WinQSIM via a GPIB interface. The AMIQ generator has a pseudo random binary sequence (PRBS) generator and a bit error test set built in. The resulting I/Q signals are applied to the SMIQ to generate a ASK (OOK) spectrum at the desired RF frequency.

Data is demodulated by the TDA5250 and then sent back to the AMIQ to be compared with the originally sent data. The bit error rate is calculated by the bit error rate equipment inside the AMIQ.

Baseband coding in the form of Manchester is applied to the I signal as can be seen in the subsequent figure.


TestSetup.wmf
Figure 4-36 BER Test Setup

In the following figures the RF power level shown is the average power level.
These investigations have been made on an Infineon evaluation board using a data rate of $4 \mathrm{kBit} / \mathrm{s}$ with manchester encoding and a data filter bandwidth of 7 kHz . This is the standard configuration of our evaluation boards. All these measurements have been performed with several evaluation boards, so that production scattering and component tolerances are already included in these results.

Regarding the data filter bandwidth it has to be mentioned that a data rate of $4 \mathrm{kBit} / \mathrm{s}$ using manchester encoding results in a data frequency of 2 kHz to 4 kHz depending on the occurring data pattern. The test pattern given by the AMIQ is a pseudo random binary sequency (PRBS9) with a 9 bit shift register. This pattern varies the resulting data frequency up to 4 kHz .

The best sensitivity performance can be achieved using a data filter bandwidth of 1.25 times the maximum occuring data frequency.

The IQ filter setting is depending on the modulation type. ASK needs an IQ filter of $50 \mathrm{kHz}, 50 \mathrm{kHz}$ deviation at FSK recommend a 100 kHz IQ filter and 100 kHz deviation were measured with a 150 kHz IQ filter

A very practicable configuration is to set the chip-internal adjustable IQ filter to the sum of FSK peak deviation and maximum datafrequency. Concerning these aspects the bandwidth should be chosen small enough. With respect to both, the crystal tolerances and the tolerances of the crystal oscillator circuit of receiver and transmitter as well, a too small IQ filter bandwidth will reduce the sensitivity again. So a compromise has to be made. For further details on chip tolerances see also Section 4.2.7

### 4.10.2 Sensitivity depending on the ambient Temperature

Demonstrating a wide band of application possibilities the temperature behavior must not be forgotten. In automotive systems the required temperature range is from $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$. The receivers very good performance is documented in the following graph. The selected supply voltage is 5 V , the influence of the supply voltage can be seen in the following Section 4.10.3

The IQ filter setting can be taken from the legend of Figure 4-37.


BER_Temp_5V.wmf
Figure 4-37 Temperature Behaviour

Figure 4-37 shows that ASK as well as FSK sensitivity is in the range of -110 to -111 dBm at $20^{\circ} \mathrm{C}$ ambient temperature for a BER of $2 \mathrm{E}-3$.

Notice that the sensitivity variation in this temperature range of $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ is only about 1.5 to 2 dB .

### 4.10.3 BER performance depending on Supply Voltage

Due to the wide supply voltage range of this transeiver chip also the sensitivity behaviour over this parameter is documented is the subsequent graph.


Figure 4-38 BER supply voltage

Please notice the tiny sensitivity changes of 1.5 to 2.5 dB , when variing the supply voltage.

### 4.10.4 Datarates and Sensitivity

The TDA 5250 can handle datarates up to $64 \mathrm{kbit} / \mathrm{s}$, as can be taken from the following figure. (see also Section 5.1.4)


BER_Datarate.wmf
Figure 4-39 Datarates and Sensitivity

### 4.10.5 Sensitivity at Frequency Offset

Applying the test setup in Figure 4-36 even a wide offset in the received frequency spectrum results only in a slight decrease of receiving sensitivity. At an offset of 100 kHz one of the two 50 kHz FSK peaks is at the 3 dB border of the IQ filter ( 150 kHz ), which is the reason for the decline of the sensitivity (see point A in Figure 4-40).

A frequency offset of 50 kHz (FSK deviation: 50 kHz ) increases the data jitter of the demodulated signal and therefore results in little loss of sensitivity (see point $B$ in Figure 4-40).
In this case one of the peaks of the FSK-spectrum lies in the DC-blocking notch of the baseband limiters.

BER Performance at Frequency Offset of RKE Receiver TDA5250 ( 3 V, Manchester encoded data, $20^{\circ} \mathrm{C}$ )


Figure 4-40 BER Frequency Offset

### 4.11 Default Setup

Default setup is hard wired on chip and effective after a reset or return of power supply.

| Parameter | Value | IFX- <br> Board | Comment |
| :---: | :---: | :---: | :---: |
| IQ-Filter Bandwidth | 150 kHz |  |  |
| Data Filter Bandwidth | 7 kHz |  |  |
| Limiter lower fg | 470 Hz | 47nF |  |
| Slicing Level Generation | RC | 10nF |  |
| Nom. Frequency Capacity intern (ASK TX, FSK RX) | 4.5 pF | 868.3 MHz |  |
| FSK+ Frequency Capacity intern (FSK+, ASK RX) | 2.5 pF | +50kHz |  |
| FSK- Frequency Capacity intern (FSK-) | 1.5 pF | -50kHz |  |
| LNA Gain | HIGH |  |  |
| Power Amplifier | HIGH | +10dBm |  |
| RSSI accuracy settling time | 2.6 ms | 2.2nF |  |
| ADC measurement | RSSI |  |  |
| ON-Time | 10 ms |  |  |
| OFF-Time | 100 ms |  |  |
| Clock out RX PowerON | 1 MHz |  |  |
| Clock out TX PowerON | 1 MHz |  |  |
| Clock out RX PowerDOWN | - |  |  |
| Clock out TX PowerDOWN | - |  |  |
|  |  |  |  |
| XTAL modulation switch | bipolar |  |  |
| XTAL modulation shaping | off |  |  |
|  |  |  |  |
| RX / TX | - | Jumper |  |
| ASK/FSK | - | Jumper |  |
| PwdDD | PWDN | Jumper removed |  |
| Operating Mode | Slave |  |  |

## 5 TDA 5250 D2 Reference

## Contents of this Chapter

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### 5.1 Electrical Data

### 5.1.1 Absolute Maximum Ratings



## WARNING

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC will result.

| Table 5-1 Absolute Maximum Ratings |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| \# | Parameter | Symbol | Limit Values |  | Unit | Remarks |
|  |  |  | min | max |  |  |
| 1 | Supply Voltage | $\mathrm{V}_{\mathrm{s}}$ | -0.3 | 5.8 | V |  |
| 2 | Junction Temperature | $\mathrm{T}_{\mathrm{j}}$ | -40 | +125 | ${ }^{\circ} \mathrm{C}$ |  |
| 3 | Storage Temperature | $\mathrm{T}_{\text {s }}$ | -40 | +150 | ${ }^{\circ} \mathrm{C}$ |  |
| 4 | Thermal Resistance | $\mathrm{R}_{\text {thJA }}$ |  | 114 | K/W |  |
| 5 | ESD integrity, all pins | $V_{\text {ESD }}$ | tbd | tbd | kV | HBM according to MIL STD 883D, method 3015.7 |

### 5.1.2 Operating Range

Within the operational range the IC operates as explained in the circuit description.

| \# | Parameter | Symbol | Limit Values |  | Unit | Test Conditions | L | Item |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | min | max |  |  |  |  |
| 1 | Supply voltage | $\mathrm{V}_{\mathrm{S}}$ | 2.1 | 5.5 | V |  |  |  |
| 2 | Ambient temperature | $\mathrm{T}_{\mathrm{A}}$ | -40 | 85 | ${ }^{\circ} \mathrm{C}$ |  |  |  |
| 3 | Receive frequency | $\mathrm{f}_{\mathrm{RX}}$ | 868 | 870 | MHz |  |  |  |
| 4 | Transmit frequency | $\mathrm{f}_{\text {TX }}$ | 868 | 870 | MHz |  |  |  |

### 5.1.3 AC/DC Characteristics

AC/DC characteristics involve the spread of values guaranteed within the specified voltage and ambient temperature range. Typical characteristics are the median of the production.

## Table 5-3 AC/DC Characteristics with $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{VCc}}=2.1 \ldots 5.5 \mathrm{~V}$

| \# | Parameter | Symbol | Limit Values |  |  | Unit | Test Conditions | L | Item |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | min | typ | max |  |  |  |  |

RECEIVER Characteristics


Table 5-3 AC/DC Characteristics with $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{VCC}}=2.1 \ldots 5.5 \mathrm{~V}$

| \# | Parameter | Symbol | Limit Values |  |  | Unit | Test Conditions | L | Item |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | min | typ | max |  |  |  |  |

## TRANSMITTER Characteristics

| 1 | Supply current TX, FSK | $\mathrm{I}_{\text {TX }}$ |  | 9.4 |  | mA | 2.1 V , high power |  | 1 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 2 | Supply current TX, FSK | $\mathrm{I}_{\text {TX }}$ |  | 11.9 |  | mA | 3 V , high power |  | 1 |
| 3 | Supply current TX, FSK | $\mathrm{I}_{\text {TX }}$ |  | 14.6 |  | mA | 5 V , high power |  | 1 |
| 4 | Output power | $\mathrm{P}_{\text {out }}$ |  | 6 |  | dBm | 2.1 V , high power | ■ |  |
| 5 | Output power | $P_{\text {out }}$ |  | 9 |  | dBm | 3 V , high power | ■ |  |
| 6 | Output power | $P_{\text {out }}$ |  | 13 |  | dBm | 5 V , high power | $\square$ |  |
| 7 | Supply current TX, FSK | $\mathrm{I}_{\text {TX }}$ |  | 4.1 |  | mA | 2.1V, low power |  | 1 |
| 8 | Supply current TX, FSK | $I_{\text {TX }}$ |  | 4.9 |  | mA | 3 V , low power |  | 1 |
| 9 | Supply current TX, FSK | $\mathrm{I}_{\text {TX }}$ |  | 6.8 |  | mA | 5 V , low power |  | 1 |
| 10 | Output power | Pout_low |  | -30 |  | dBm | 2.1 V , low power | ■ |  |
| 11 | Output power | $\mathrm{P}_{\text {out_low }}$ |  | -22 |  | dBm | 3 V , low power | ■ |  |
| 12 | Output power | Pout_low |  | -3 |  | dBm | 5 V , low power | $\square$ |  |
| 13 | Power down current | $\mathrm{I}_{\text {PWDN_TX }}$ |  | 5 |  | nA | 5.5V, all power down |  |  |
| 14 | Clock Out setup time | ${ }^{\text {t CLKSSU }}$ |  | 0.5 |  | ms | stable CLKDIV output signal |  |  |
| 15 | Transmitter setup time | $t_{\text {TXSU }}$ | 0.77 | 1.1 | 1.43 | ms | $\begin{gathered} \text { PWDN-->PON or } \\ \text { RX-->TX } \end{gathered}$ | ■ |  |
| 16 | Spurious $\mathrm{f}_{\mathrm{RF}}{ }^{+/-\mathrm{f}_{\text {clock }}}$ | $\mathrm{P}_{\text {clock }}$ |  |  |  | dBm | 3V, 50Ohm Board, <br> Default ( 1 MHz ) | $\square$ |  |
| 17 | Spurious $\mathrm{f}_{\text {RF }}{ }^{+/-\mathrm{f}_{\text {XTAL }}}$ | $\mathrm{P}_{1 \text { st }}$ |  | -66 |  | dBm | $3 \mathrm{~V}, 50 \mathrm{Ohm}$ Board | $\square$ |  |
| 18 | Spurious 2nd harmonic | $\mathrm{P}_{2 \text { nd }}$ |  | -40 |  | dBm | $3 \mathrm{~V}, 50 \mathrm{Ohm}$ Board | ■ |  |
| 19 | Spurious 3rd harmonic | $\mathrm{P}_{3 \text { rd }}$ |  | -50 |  | dBm | 3V, 50Ohm Board | ■ |  |

1: without pin diode current (RX/TX-switch)
130uA@2.1V; 310uA@3V; 720uA@5V

| \# | Parameter | Symbol | Limit Values |  |  | Unit | Test Conditions | L | Item |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | min | typ | max |  |  |  |  |

GENERAL Characteristics

| 1 | Power down current timer mode (standby) | IPWDN_32k |  | 9 |  | uA | $3 \mathrm{~V}, 32 \mathrm{kHz}$ clock on |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 2 | Power down current timer mode (standby) | IPWDN_32k |  | 11 |  | uA | $5 \mathrm{~V}, 32 \mathrm{kHz}$ clock on |  |
| 3 | Power down current with XTAL ON | IPWDN_XtI |  | 750 |  | uA | $3 \mathrm{~V}, \mathrm{CONFIG9}=1$ |  |
| 4 | Power down current with XTAL ON | $\mathrm{I}_{\text {PWDN_XtI }}$ |  | 860 |  | uA | 5V, CONFIG9=1 |  |
| 5 | 32 kHz oscillator freq. | $\mathrm{f}_{32 \mathrm{kHz}}$ | 24 | 32 | 40 | kHz |  |  |
| 6 | XTAL startup time | $\mathrm{t}_{\text {XTAL }}$ |  | 0.5 |  | ms | IFX Board with Crystal Q1 as specified in Section 5.4 | ■ |
| 7 | Load capacitance | $\mathrm{C}_{\text {COmax }}$ |  | 5 |  | pF |  | ■ |
| 8 | Serial resistance of the crystal | $\mathrm{R}_{\text {Rmax }}$ |  |  | 100 | $\Omega$ |  | ■ |
| 9 | Input inductance XOUT | Losc |  | 2.7 |  | uH |  | $\square$ |
| 10 | FSK demodulator gain | $\mathrm{G}_{\text {FSK }}$ |  | 2.4 |  | $\begin{aligned} & \mathrm{mV} / \\ & \mathrm{kHz} \end{aligned}$ |  |  |
| 11 | RSSI@-120dBm | $\mathrm{U}_{-120 \mathrm{dBm}}$ |  | 0.35 |  | V | default setup | $\square$ |
| 12 | RSSI@-100dBm | $\mathrm{U}_{-100 \mathrm{dBm}}$ |  | 0.55 |  | V | default setup | $\square$ |
| 13 | RSSI@-70dBm | $\mathrm{U}_{-70 \mathrm{dBm}}$ |  | 1 |  | V | default setup | ■ |
| 14 | RSSI@-50dBm | $\mathrm{U}_{-50 \mathrm{dBm}}$ |  | 1.2 |  | V | default setup | ■ |
| 15 | RSSI Gradient | $\mathrm{G}_{\text {RSSI }}$ |  | 14 |  | $\mathrm{mV} /$ | default setup | ■ |
| 16 | IQ-Filter bandwidth | $\mathrm{f}_{3 \mathrm{~dB} \text { _IQ }}$ | 115 | 150 | 185 | kHz | Default setup | $\square$ |
| 17 | Data Filter bandwidth | $\mathrm{f}_{3 \mathrm{~dB}}$ LP | 5.3 | 7 | 8.7 | kHz | Default setup | ■ |
| 18 | Vcc-Vtune RX, Pin3 | $\mathrm{V}_{\text {cc-tune, }} \mathrm{RX}$ | 0.5 | 1 | 1.6 | V | $\mathrm{f}_{\text {Ref }}=18.08956 \mathrm{MHz}$ |  |
| 19 | Vcc-Vtune TX, Pin3 | $\mathrm{V}_{\text {cc-tune, }}$ TX | 0.5 | 1.1 | 1.6 | V | $\mathrm{f}_{\text {Ref }}=18.08956 \mathrm{MHz}$ |  |

### 5.1.4 Digital Characteristics

$I^{2} C$ Bus Timing


Figure 5-1 $\quad I^{2} C$ Bus Timing

3-wire Bus Timing

BUS_MODE $=$ HIGH


Figure 5-2 3 -wire Bus Timing

| Table 5-5 Digital Characteristics with $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\text {Vdd }}=2.1 \ldots 5.5 \mathrm{~V}$ |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| \# | Parameter | Symbol | Limit Values |  |  | Unit | Test Conditions | L | Item |
|  |  |  | min | typ | max |  |  |  |  |
| 1 | Data rate TX ASK | $\mathrm{f}_{\text {TX.ASK }}$ |  | 10 | 25 | kBaud | PRBS9, <br> Manch.@+10dBm | $\square$ | 1 |
| 2 | Data rate TX ASK | $\mathrm{f}_{\text {TX.ASK }}$ |  | 10 | 64 | kBaud | PRBS9, Manch.@-5dBm | $\square$ | 1 |
| 3 | Data rate TX FSK | $\mathrm{f}_{\text {TX.FSK }}$ |  | 10 | 40 | kBaud | PRBS9, Manch.@+10dBm @ 50 kHz dev. | $\square$ | 1 |
| 4 | Data rate RX ASK | $\mathrm{f}_{\text {RX.ASK }}$ |  | 10 | 64 | kBaud | PRBS9, Manch. | $\square$ |  |
| 5 | Data rate RX FSK | $\mathrm{f}_{\text {RX.FSK }}$ |  | 10 | 64 | kBaud | $\begin{gathered} \text { PRBS9, } \\ \text { Manch.@100kHz dev. } \end{gathered}$ | ■ |  |
|  |  |  |  |  |  |  |  |  |  |
| 6 | Digital Inputs High-level Input Voltage Low-level Input Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{~V}_{\mathrm{IL}} \end{aligned}$ | $\begin{gathered} \mathrm{V}_{\mathrm{dd}}-0.2 \\ 0 \end{gathered}$ |  | $\begin{aligned} & V_{\text {dd }} \\ & 0.2 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |  | ■ |  |
| 7 | RXTX Pin 5 <br> TX operation, int. controlled | $\mathrm{V}_{\mathrm{OL}}$ |  | $\begin{gathered} 0.4 \\ 1.15 \end{gathered}$ |  | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ | $\begin{gathered} @ V d d=3 \mathrm{~V} \\ \text { Isink=800uA } \\ \text { Isink }=3 \mathrm{~mA} \end{gathered}$ | ■ |  |
| 8 | CLKDIV Pin 26 <br> $\mathrm{t}_{\text {rise }}\left(0.1^{*} \mathrm{Vdd}\right.$ to $0.9^{*} \mathrm{Vdd}$ ) <br> $\mathrm{t}_{\text {fall }}\left(0.9^{*} \mathrm{Vdd}\right.$ to $0.1^{*} \mathrm{~V}$ dd $)$ <br> Output High Voltage Output Low Voltage | $\begin{gathered} \mathrm{t}_{\mathrm{r}} \\ \mathrm{t}_{\mathrm{f}} \\ \mathrm{~V}_{\mathrm{OH}} \\ \mathrm{~V}_{\mathrm{OL}} \end{gathered}$ |  | $\begin{gathered} 35 \\ 30 \\ \text { Vdd-0.4 } \\ 0.4 \end{gathered}$ |  | ns ns V V | ```@Vdd=3V load 10pF load 10pF Isorce=350uA Isink=400uA``` | ■ |  |

Bus Interface Characteristics

|  |  |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |


| \# | Parameter | Symbol | Limit Values |  |  | Unit | Test Conditions | L | Item |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | min | typ | max |  |  |  |  |
| 17 | Data hold time | $\mathrm{t}_{\text {HD. DAT }}$ | 0 |  |  | ns | $\mathrm{V}_{\mathrm{dd}}=5 \mathrm{~V}$ | $\square$ |  |
| 18 | Data setup time | $\mathrm{t}_{\text {SU.DAT }}$ | 100 |  |  | ns | $V_{\text {dd }}=5 \mathrm{~V}$ | ■ |  |
| 19 | Rise, fall time of both BusData and BusCLK signals | $t_{R}, t_{F}$ | $\begin{gathered} 20+ \\ 0.1 C_{b} \end{gathered}$ |  | 300 | ns | $\mathrm{V}_{\mathrm{dd}}=5 \mathrm{~V}$ | ■ | 2 |
| 20 | Setup time for STOP condition | $\mathrm{t}_{\text {SU.Sto }}$ | 0.6 |  |  | $\mu \mathrm{s}$ | $\begin{aligned} & \text { only } I^{2} C \text { mode } \\ & V_{d d}=5 \mathrm{~V} \end{aligned}$ | $\square$ |  |
| 21 | Capacitive load for each bus line | $\mathrm{C}_{\mathrm{b}}$ |  |  | 400 | pF | $\mathrm{V}_{\mathrm{dd}}=5 \mathrm{~V}$ | ■ |  |
| 22 | Setup time for BusCLK to EN | $\underset{\mathrm{N}}{\mathrm{t}_{\text {SU.SCE }}}$ | 0.6 |  |  | $\mu \mathrm{s}$ | only 3-wire mode $V_{d d}=5 \mathrm{~V}$ | ■ |  |
| 23 | H-pulsewidth (EN) | $t_{\text {WHEN }}$ | 0.6 |  |  | $\mu \mathrm{s}$ | $V_{\text {dd }}=5 \mathrm{~V}$ | ■ |  |

1: limited by transmission channel bandwidth and depending on transmit power level; ETSI regulation EN 300220 fullfilled, see Section 4.1
2: $C_{b}=$ capacitance of one bus line

### 5.2 Test Circuit

The device performance parameters marked with $\square$ in Section 5.1 . 3 were measured on an Infineon evaluation board (IFX board).


TDA5250_v41.schematic.pdf
Figure 5-3 Schematic of the Evaluation Board

### 5.3 Test Board Layout

Gerberfiles for this Testboard are available on request.


TDA5250_v41_layout.pdf
Figure 5-4 Layout of the Evaluation Board

Note: The LNA and PA matching network was designed for minimum required space and maximum performance and thus via holes were deliberately placed into solder pads.

In case of reproduction please bear in mind that this may not be suitable for all automatic soldering processes.

Note 2: Please keep in mind not to layout the CLKDIV line directly in the neighborhood of the crystal and the associated components.

### 5.4 Bill of Materials

| Reference | Value | Specification | Tolerance |
| :---: | :---: | :---: | :---: |
| R1 | 4k7 | 0603 | +/-5\% |
| R2 | $10 \Omega$ | 0603 | +/-5\% |
| R3 | --- | 0603 | +/-5\% |
| R4 | 1M | 0603 | +/-5\% |
| R5 | 4k7 | 0603 | +/-5\% |
| R6 | 4k7 | 0603 | +/-5\% |
| R7 | 4k7 | 0603 | +/-5\% |
| R8 | 6 k 8 | 0603 | +/-5\% |
| R9 | 180 | 0603 | +/-5\% |
| R10 | 180 | 0603 | +/-5\% |
| R11 | 270 | 0603 | +/-5\% |
| R12 | 15k | 0603 | +/-5\% |
| R13 | 10k | 0603 | +/-5\% |
| R14 | 180 | 0603 | +/-5\% |
| R15 | 180 | 0603 | +/-5\% |
| R16 | 1M | 0603 | +/-5\% |
| R17 | 1M | 0603 | +/-5\% |
| R18 | 1M | 0603 | +/-5\% |
| R19 | 560 | 0603 | +/-5\% |
| R20 | 1k | 0603 | +/-5\% |
| R21 | 10 | 0603 | +/-5\% |
| R22 | 0 | 0603 | +/-5\% |
| R23 | 10 | 0603 | +/-5\% |
| C1 | 22pF | 0603 | +/-1\% |
| C2 | 1 pF | 0603 | +/-0,1pF |
| C3 | 5,6pF | 0603 | +/-0,1pF |
| C4 | 2,2pF | 0603 | $+/-0,1 \mathrm{pF}$ |
| C5 | 1 nF | 0603 | +/-5\% |
| C6 | 1 nF | 0603 | +/-5\% |
| C7 | 15pF | 0603 | +/-1\% |
| C8 | --- | 0603 | +/-0,1pF |
| C9 | 47pF | 0603 | +/-1\% |
| C10 | 22pF | 0603 | +/-1\% |
| C11 | --- | 0603 | +/-5\% |
| C12 | 10nF | 0603 | +/-10\% |
| C13 | 10 nF | 0603 | +/-10\% |


| Table 5-6 Bill of Materials |  |  |  |
| :---: | :---: | :---: | :---: |
| Reference | Value | Specification | Tolerance |
| C14 | 10 nF | 0603 | +/-10\% |
| C15 | 4.7pF | 0603 | +/-0,1pF |
| C16 | 1.8pF | 0603 | +/-0,1pF |
| C17 | 12pF | 0603 | +/-1\% |
| C18 | 10 nF | 0603 | +/-10\% |
| C19 | 2,2nF | 0603 | +/-10\% |
| C20 | 47 nF | 0603 | +/-10\% |
| C21 | 47nF | 0603 | +/-10\% |
| C22 | 47 nF | 0603 | +/-10\% |
| C23 | 47 nF | 0603 | +/-10\% |
| C24 | 100 nF | 0603 | +/-10\% |
| C25 | 100 nF | 0603 | +/-10\% |
| C26 | --- | 0603 | +/-10\% |
| C27 | 100 nF | 0603 | +/-10\% |
| C28 | 100 nF | 0603 | +/-10\% |
| C29 | 100nF | 0603 | +/-10\% |
| C30 | --- | 0603 | +/-10\% |
| L1 | 68nH | $\begin{aligned} & \text { SIMID 0603-C } \\ & \text { (EPCOS) } \end{aligned}$ | +/-2\% |
| L2 | 12 nH | SIMID 0603-C (EPCOS) | +/-2\% |
| L3 | 8.2nH | SIMID 0603-C (EPCOS) | +/-0.2nH |
| IC1 | TDA5250 D2 | PTSSOP38 |  |
| IC2 | ILQ74 |  |  |
| IC3 | SFH6186 |  |  |
| Q1 | 18.08958 MHz | Telcona: $\mathrm{C} 0=2,1 \mathrm{pF}$ | $\mathrm{C} 1=8 \mathrm{fF}, \mathrm{C}_{\mathrm{L}}=12 \mathrm{pF}$ |
| S1 | 1-pol. |  |  |
| T1 | BC847B | SOT-23 (Infineon) |  |
| D1, D2 | BAR63-02W | SCD-80 (Infineon) |  |
| X1, X2 | SMA-socket |  |  |
| X5 | SubD 25p. |  |  |


[^0]:    - Low Bitrate Communication Systems
    - Keyless Entry Systems
    - Remote Control Systems
    - Alarm Systems
    - Telemetry Systems
    - Electronic Metering
    - Home Automation Systems

