

# DATA SHEET

## **TEA1039**

Control circuit for switched-mode  
power supply

Product specification  
File under Integrated Circuits, IC02

August 1982

**Control circuit for switched-mode power supply****TEA1039****GENERAL DESCRIPTION**

The TEA1039 is a bipolar integrated circuit intended for the control of a switched-mode power supply. Together with an external error amplifier and a voltage regulator (e.g. a regulator diode) it forms a complete control system. The circuit is capable of directly driving the SMPS power transistor in small SMPS systems.

It has the following features:

- Suited for frequency and duty factor regulation.
- Suited for flyback converters and forward converters.
- Wide frequency range.
- Adjustable input sensitivity.
- Adjustable minimum frequency or maximum duty factor limit.
- Adjustable overcurrent protection limit.
- Supply voltage out-of-range protection.
- Slow-start facility.

**QUICK REFERENCE DATA**

Supply voltage	$V_{CC}$	nom.	14 V
Supply current	$I_{CC}$	max.	13 mA
Output pulse repetition frequency range	$f_o$	1 Hz to 100	kHz
Output current LOW	$I_{OL}$	max.	1 A
Operating ambient temperature range	$T_{amb}$	-25 to +125	°C

**PACKAGE OUTLINE**

9-lead SIL; plastic (SOT-110B); SOT110-1; 1996 November 18.

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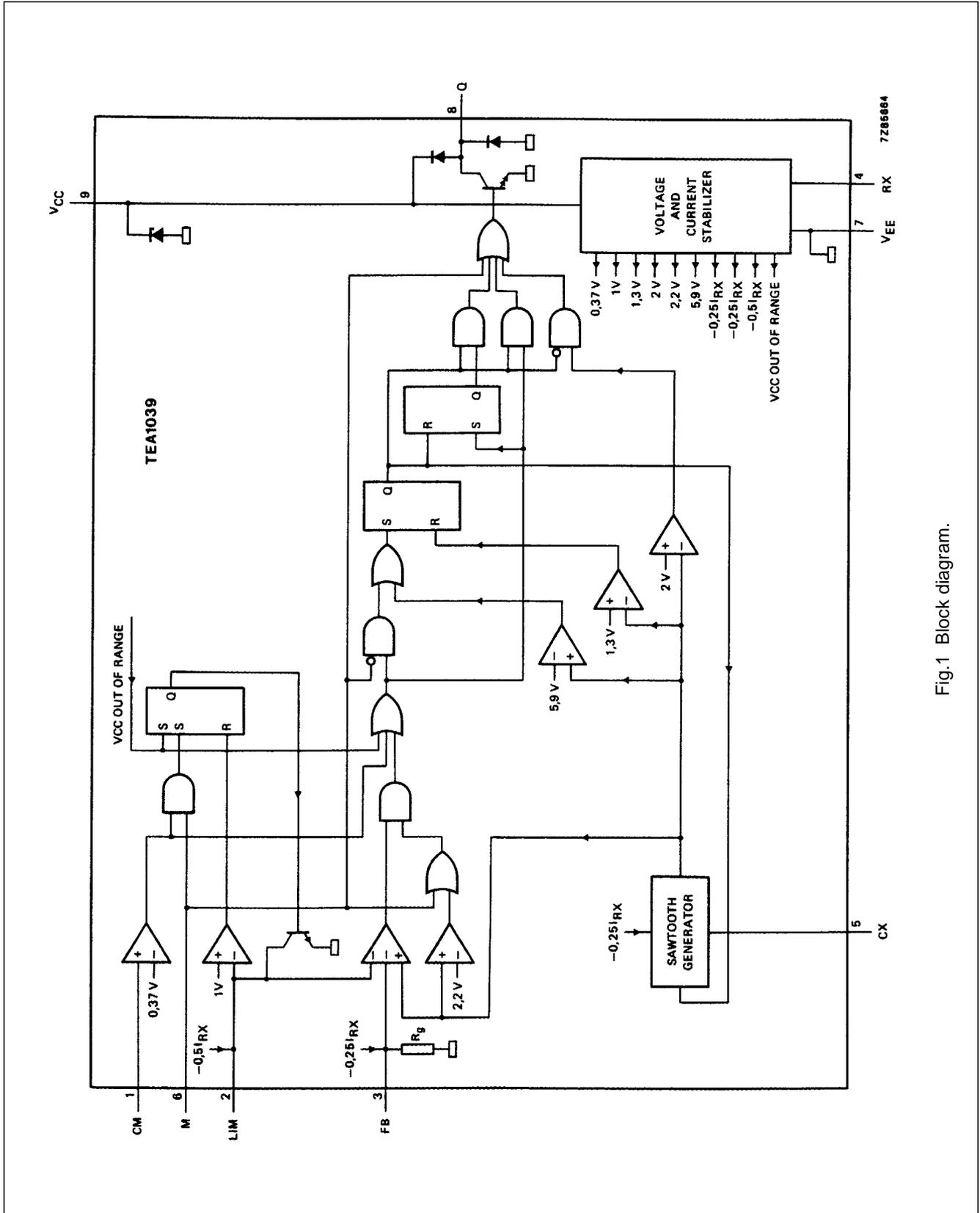
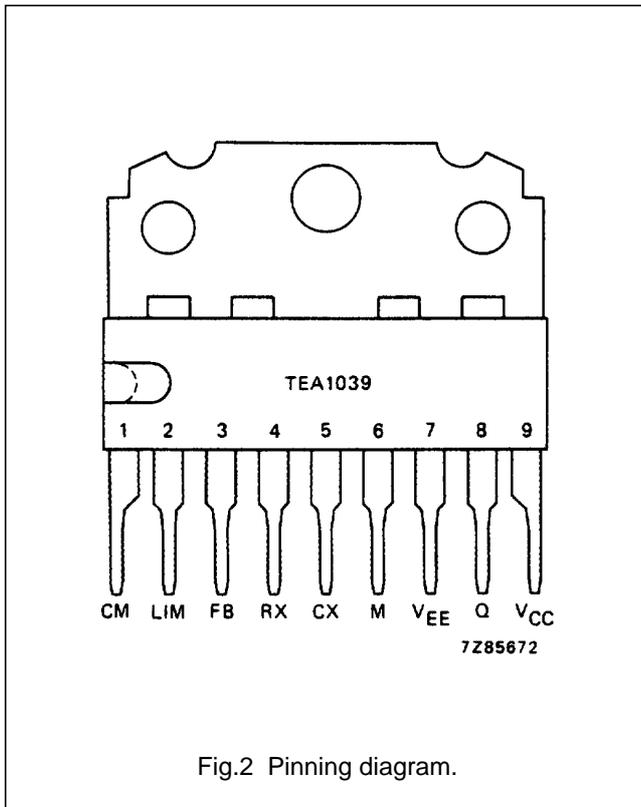


Fig.1 Block diagram.

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**PINNING**

1	CM	overcurrent protection input
2	LIM	limit setting input
3	FB	feedback input
4	RX	external resistor connection
5	CX	external capacitor connection
6	M	mode input
7	$V_{EE}$	common
8	Q	output
9	$V_{CC}$	positive supply connection

**FUNCTIONAL DESCRIPTION**

The TEA1039 produces pulses to drive the transistor in a switched-mode power supply. These pulses may be varied either in frequency (frequency regulation mode) or in width (duty factor regulation mode).

The usual arrangement is such that the transistor in the SMPS is ON when the output of the TEA1039 is HIGH, i.e. when the open-collector output transistor is OFF. The duty factor of the SMPS is the time that the output of the TEA1039 is HIGH divided by the pulse repetition time.

**Supply  $V_{CC}$  (pin 9)**

The circuit is usually supplied from the SMPS that it regulates. It may be supplied either from its primary d.c. voltage or from its output voltage. In the latter case an auxiliary starting supply is necessary.

The circuit has an internal  $V_{CC}$  out-of-range protection. In the frequency regulation mode the oscillator is stopped; in the duty factor regulation mode the duty factor is made zero. When the supply voltage returns within its range, the circuit is started with the slow-start procedure.

When the circuit is supplied from the SMPS itself, the out-of-range protection also provides an effective protection against any interruption in the feedback loop.

**Mode input M (pin 6)**

The circuit works in the frequency regulation mode when the mode input M is connected to ground ( $V_{EE}$ , pin 7). In this mode the circuit produces output pulses of a constant width but with a variable pulse repetition time.

The circuit works in the duty factor regulation mode when the mode input M is left open. In this mode the circuit produces output pulses with a variable width but with a constant pulse repetition time.

**Oscillator resistor and capacitor connections RX and CX (pins 4 and 5)**

The output pulse repetition frequency is set by an oscillator whose frequency is determined by an external capacitor C5 connected between the CX connection (pin 5) and ground ( $V_{EE}$ , pin 7), and an external resistor R4 connected between the RX connection (pin 4) and ground. The capacitor C5 is charged by an internal current source, whose current level is determined by the resistor R4. In the frequency regulation mode these two external

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components determine the minimum frequency; in the duty factor regulation mode they determine the working frequency (see Fig.4). The output pulse repetition frequency varies less than 1% with the supply voltage over the supply voltage range.

In the frequency regulation mode the output is LOW from the start of the cycle until the voltage on the capacitor reaches 2 V. The capacitor is further charged until its voltage reaches the voltage on either the feedback input FB or the limit setting input LIM, provided it has exceeded 2,2 V. As soon as the capacitor voltage reaches 5,9 V the capacitor is discharged rapidly to 1,3 V and a new cycle is initiated (see Figs 5 and 6).

For voltages on the FB and LIM inputs lower than 2,2 V, the capacitor is charged until this voltage is reached; this sets an internal maximum frequency limit.

In the duty factor regulation mode the capacitor is charged from 1,3 V to 5,9 V and discharged again at a constant rate. The output is HIGH until the voltage on the capacitor exceeds the voltage on the feedback input FB; it becomes HIGH again after discharge of the capacitor (see Figs 7 and 8). An internal maximum limit is set to the duty factor of the SMPS by the discharging time of the capacitor.

### Feedback input FB (pin 3)

The feedback input compares the input current with an internal current source whose current level is set by the external resistor R4. In the frequency regulation mode, the higher the voltage on the FB input, the longer the external capacitor C5 is charged, and the lower the frequency will be. In the duty factor regulation mode external capacitor C5 is charged and discharged at a constant rate, the voltage on the FB input now determines the moment that the output will become LOW. The higher the voltage on the FB input, the longer the output remains HIGH, and the higher the duty factor of the SMPS.

### Limit setting input LIM (pin 2)

In the frequency regulation mode this input sets the minimum frequency, in the duty factor regulation mode it sets the maximum duty factor of the SMPS. The limit is set by an external resistor R2 connected from the LIM input to ground (pin 7) and by an internal current source, whose current level is determined by external resistor R4.

A slow-start procedure is obtained by connecting a capacitor between the LIM input and ground. In the frequency regulation mode the frequency slowly decreases from  $f_{max}$  to the working frequency. In the duty factor regulation mode the duty factor slowly increases from zero to the working duty factor.

### Overcurrent protection input CM (pin 1)

A voltage on the CM input exceeding 0,37 V causes an immediate termination of the output pulse. In the duty factor regulation mode the circuit starts again with the slow-start procedure.

### Output Q (pin 8)

The output is an open-collector n-p-n transistor, only capable of sinking current. It requires an external resistor to drive a n-p-n transistor in the SMPS (see Figs 9 and 10).

The output is protected by two diodes, one to ground and one to the supply.

At high output currents the dissipation in the output transistor may necessitate a heatsink. See the power derating curve (Fig.3).

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**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range, voltage source	$V_{CC}$	-0,3 to +20 V
Supply current range, current source	$I_{CC}$	-30 to +30 mA
Input voltage range, all inputs	$V_I$	-0,3 to +6 V
Input current range, all inputs	$I_I$	-5 to +5 mA
Output voltage range	$V_{8-7}$	-0,3 to +20 V
Output current range		
output transistor ON	$I_B$	0 to 1 A
output transistor OFF	$I_B$	-100 to +50 mA
Storage temperature range	$T_{stg}$	-55 to +150 °C
Operating ambient temperature range (see Fig.3)	$T_{amb}$	-25 to +125 °C
Power dissipation (see Fig.3)	$P_{tot}$	max. 2 W

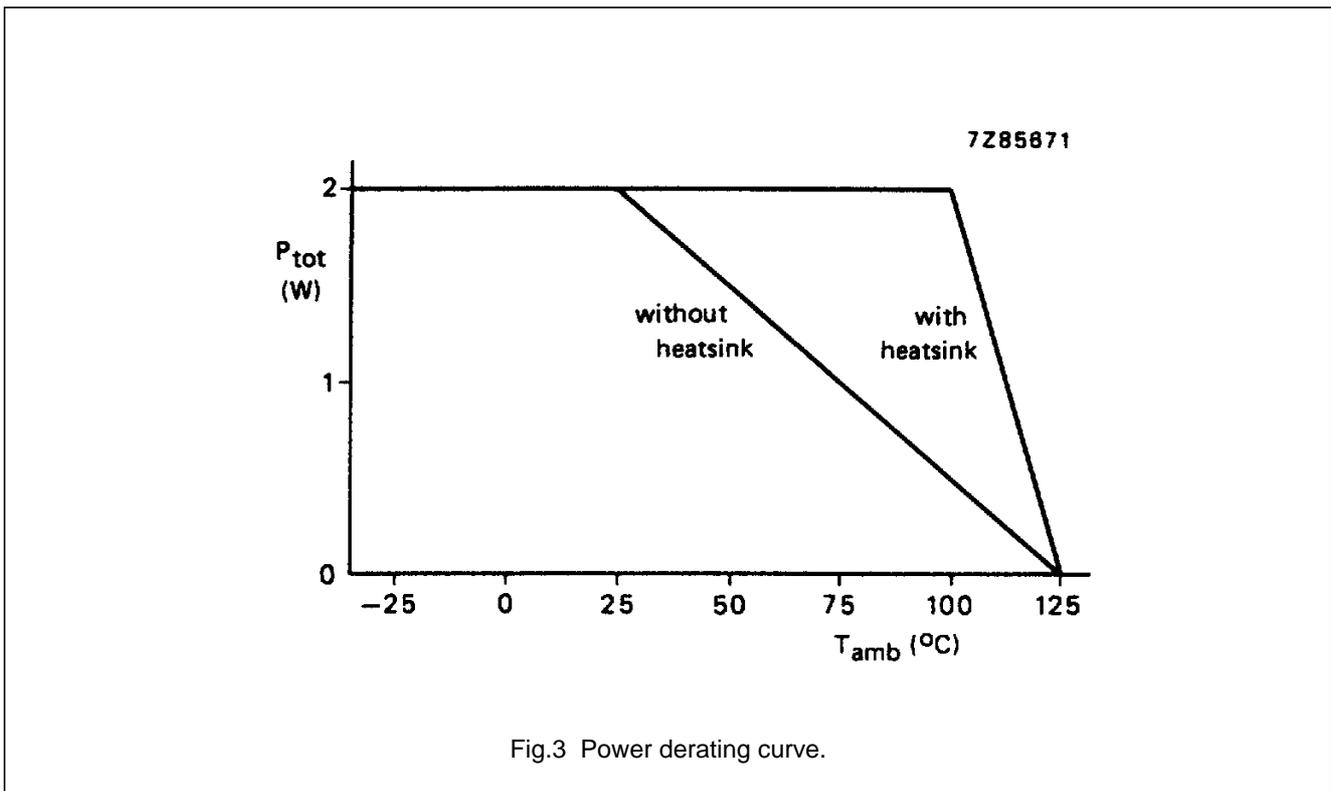


Fig.3 Power derating curve.

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**CHARACTERISTICS** $V_{CC} = 14\text{ V}$ ;  $T_{amb} = 25\text{ °C}$  unless otherwise specified

	SYMBOL	MIN.	TYP.	MAX.	UNIT
<b>Supply <math>V_{CC}</math> (pin 9)</b>					
Supply voltage, operating	$V_{CC}$	11	14	20	V
Supply current					
at $V_{CC} = 11\text{ V}$	$I_{CC}$	–	7,5	11	mA
at $V_{CC} = 20\text{ V}$	$I_{CC}$	–	9	12	mA
variation with temperature	$\frac{\Delta I_{CC}/I_{CC}}{\Delta T}$	–	–0,3	–	%/K
Supply voltage, internally limited					
at $I_{CC} = 30\text{ mA}$	$V_{CC}$	23,5	–	28,5	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	18	–	mV/K
Low supply threshold voltage	$V_{CCmin}$	9	10	11	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	–5	–	mV/K
High supply threshold voltage	$V_{CCmax}$	21	23	24,6	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	10	–	mV/K
<b>Feedback input FB (pin 3)</b>					
Input voltage for duty factor = 0; M input open	$V_{3-7}$	0	–	0,3	V
Internal reference current	$-I_{FB}$	–	$0,5I_{RX}$	–	mA
Internal resistor $R_g$	$R_g$	–	130	–	k $\Omega$
<b>Limit setting input LIM (pin 2)</b>					
Threshold voltage	$V_{2-7}$	–	1	–	V
Internal reference current	$-I_{LIM}$	–	$0,25I_{RX}$	–	mA
<b>Overcurrent protection input CM (pin 1)</b>					
Threshold voltage	$V_{1-7}$	300	370	420	mV
variation with temperature	$\Delta V_{1-7}/\Delta T$	–	0,2	–	mV/K
Propagation delay, CM input to output	$t_{PHL}$	–	500	–	ns

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	SYMBOL	MIN.	TYP.	MAX.	UNIT
<b>Oscillator connections RX and CX (pins 4 and 5)</b>					
Voltage at RX connection					
at $-I_4 = 0,15$ to $1$ mA	$V_{4-7}$	6,2	7,2	8,1	V
variation with temperature	$\Delta V_{4-7}/\Delta T$	–	2,1	–	mV/K
Lower sawtooth level	$V_{LS}$	–	1,3	–	V
Threshold voltage for output H to L transition in F mode	$V_{FT}$	–	2	–	V
Threshold voltage for maximum frequency in F mode	$V_{FM}$	–	2,2	–	V
Higher sawtooth level	$V_{HS}$	–	5,9	–	V
Internal capacitor charging current, CX connection	$-I_{CX}$	–	$0,25I_{RX}$	–	mA
Oscillator frequency (output pulse repetition frequency)	$f_o$	1	–	$10^5$	Hz
Minimum frequency in F mode, initial deviation	$\Delta f/f$	–10	–	10	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	0,034	–	%/K
Maximum frequency in F mode, initial deviation	$\Delta f/f$	–20	–	+20	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	–0,16	–	%/K
Output LOW time in F mode, initial deviation	$\Delta t/t$	–25	–	+25	%
variation with temperature	$\frac{\Delta t/t}{\Delta T}$	–	0,2	–	%/K
Pulse repetition frequency in D mode, initial deviation	$\Delta f/f$	–10	–	10	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	0,034	–	%/K
Minimum output LOW time in D mode at $C_5 = 3,6$ nF	$t_{OLmin}$	–	1	–	$\mu s$
variation with temperature	$\frac{\Delta t/t}{\Delta T}$	–	0,2	–	%/K
<b>Output Q (pin 8)</b>					
Output voltage LOW at $I_8 = 100$ mA	$V_{8-7}$	–	0,8	1,2	V
variation with temperature	$\Delta V_{8-7}/\Delta T$	–	1,5	–	mV/K
Output voltage LOW at $I_8 = 1$ A	$V_{8-7}$	–	1,7	2,1	V
variation with temperature	$\Delta V_{8-7}/\Delta T$	–	–1,4	–	mV/K

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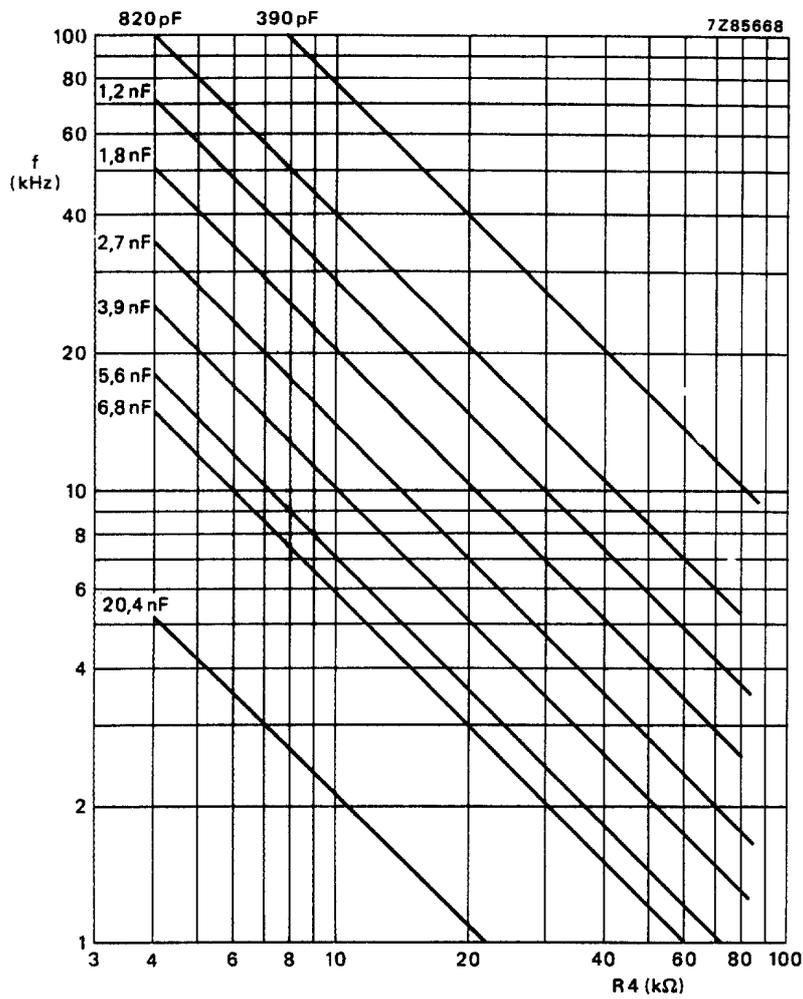


Fig.4 Minimum pulse repetition frequency in the frequency regulation mode, and working pulse repetition frequency in the duty factor regulation mode, as a function of external resistor R4 connected between RX and ground with external capacitor C5 connected between CX and ground as a parameter.

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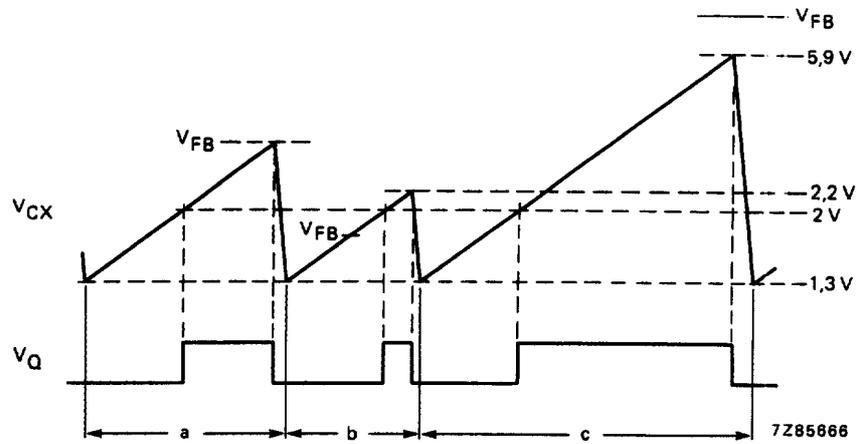


Fig.5 Timing diagram for the frequency regulation mode showing the voltage on external capacitor C5 connected between CX and ground and the output voltage as a function of time for three combinations of input signals. *a*: The voltages on inputs FB or LIM are between 2,2 V and 5,9 V. The circuit is in its normal regulation mode. *b*: The voltage on input FB or input LIM is lower than 2,2 V. The circuit works at its maximum frequency. *c*: The voltages on inputs FB and LIM are higher than 5,9 V. The circuit works at its minimum frequency.

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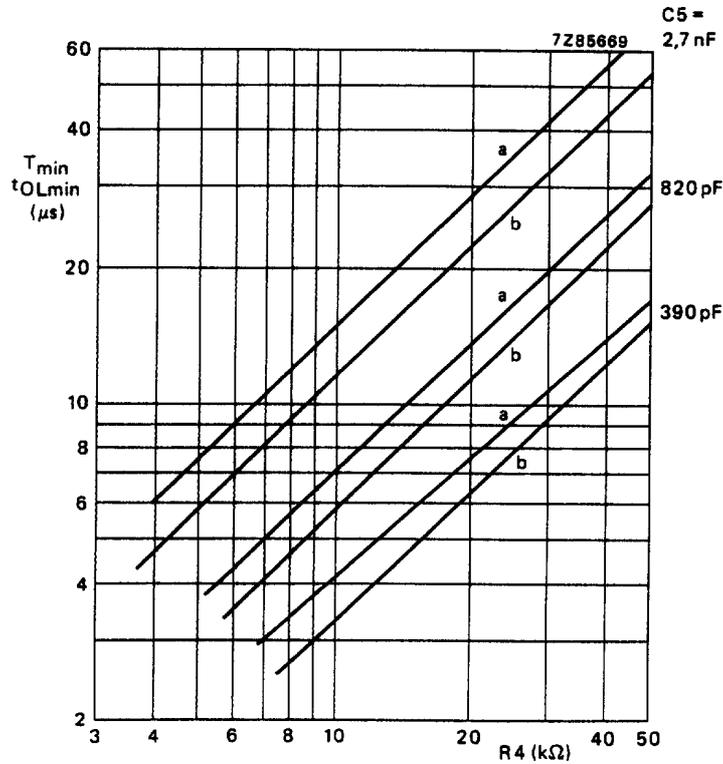


Fig.6 Minimum output pulse repetition time  $T_{min}$  (curves a) and minimum output LOW time  $t_{OLmin}$  (curves b) in the frequency regulation mode as a function of external resistor  $R4$  connected between RX and ground with external capacitor  $C5$  connected between CX and ground as a parameter.

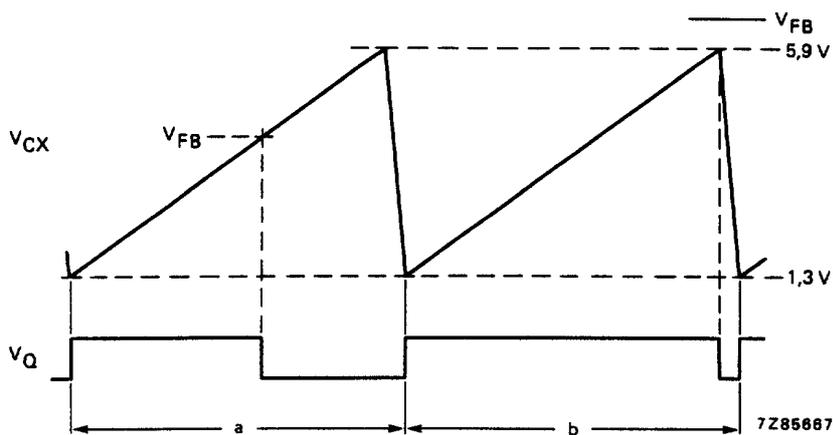


Fig.7 Timing diagram for the duty factor regulation mode showing the voltage on external capacitor  $C5$  connected between CX and ground and the output voltage as a function of time for two combinations of input signals. a: The voltages on inputs FB or LIM are below 5,9 V. The circuit is in its normal regulation range. b: The voltages on inputs FB and LIM are higher than 5,9 V. The circuit produces its minimum output LOW time, giving the maximum duty factor of the SMPS.

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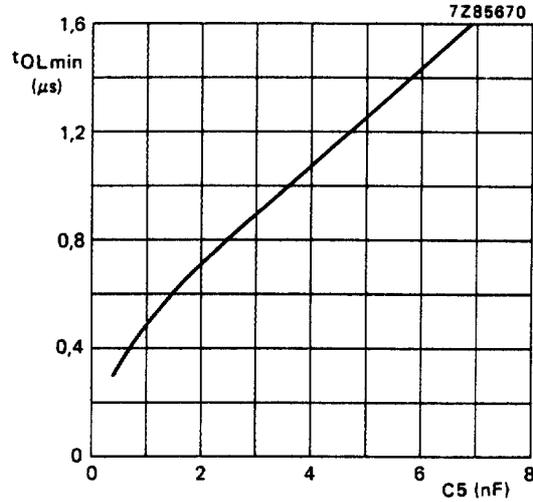


Fig.8 Minimum output LOW time  $t_{OLmin}$  in the duty factor regulation mode as a function of external capacitor  $C5$  connected between CX and ground. In this mode the minimum output LOW time is independent of  $R4$  for values of  $R4$  between 4 k $\Omega$  and 80 k $\Omega$ .

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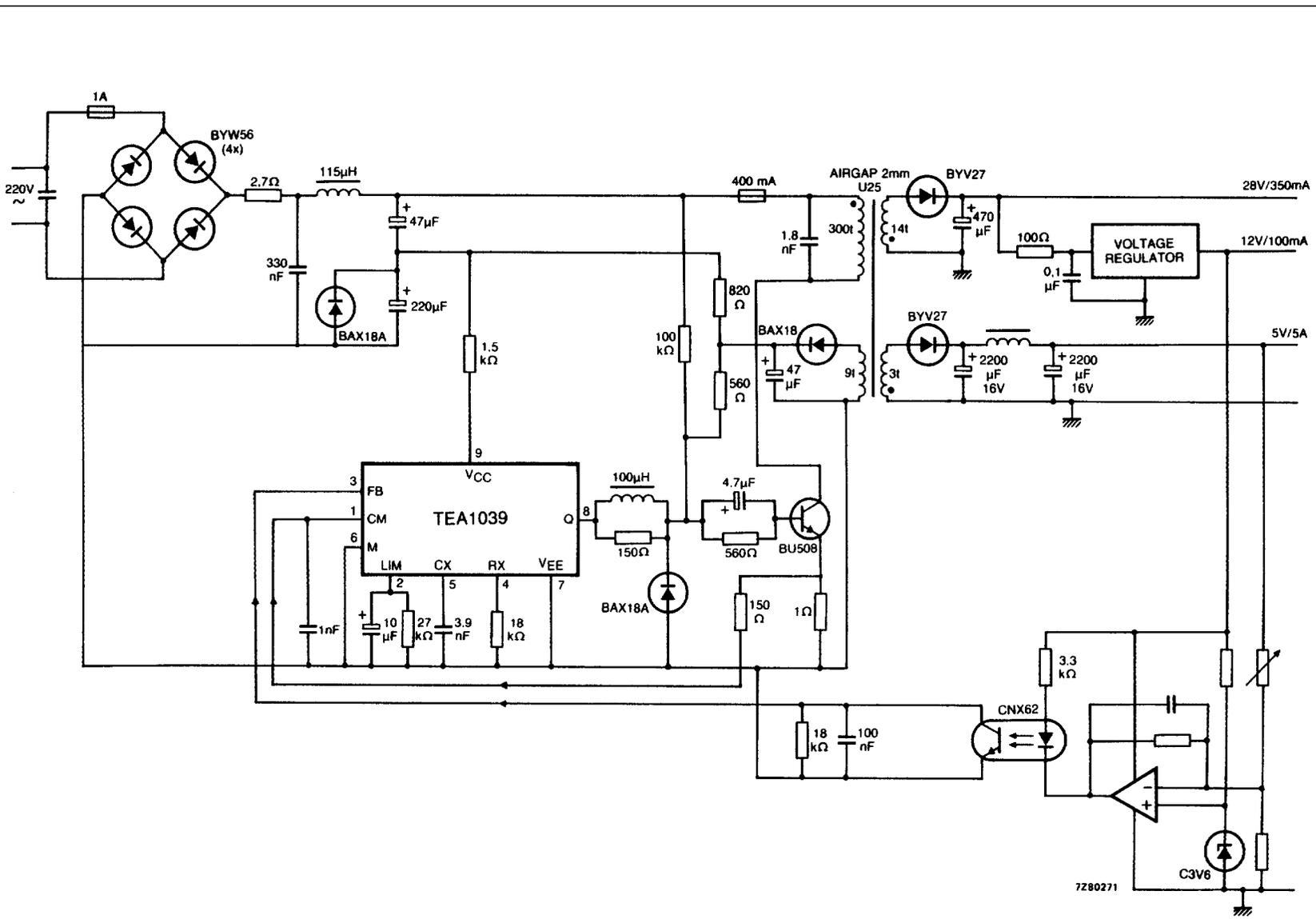


Fig.9 Typical application of the TEA1039 in a variable-frequency flyback converter switched-mode power supply. An optocoupler CNX62 is used for voltage separation.

APPLICATION INFORMATION SUPPLIED ON REQUEST.



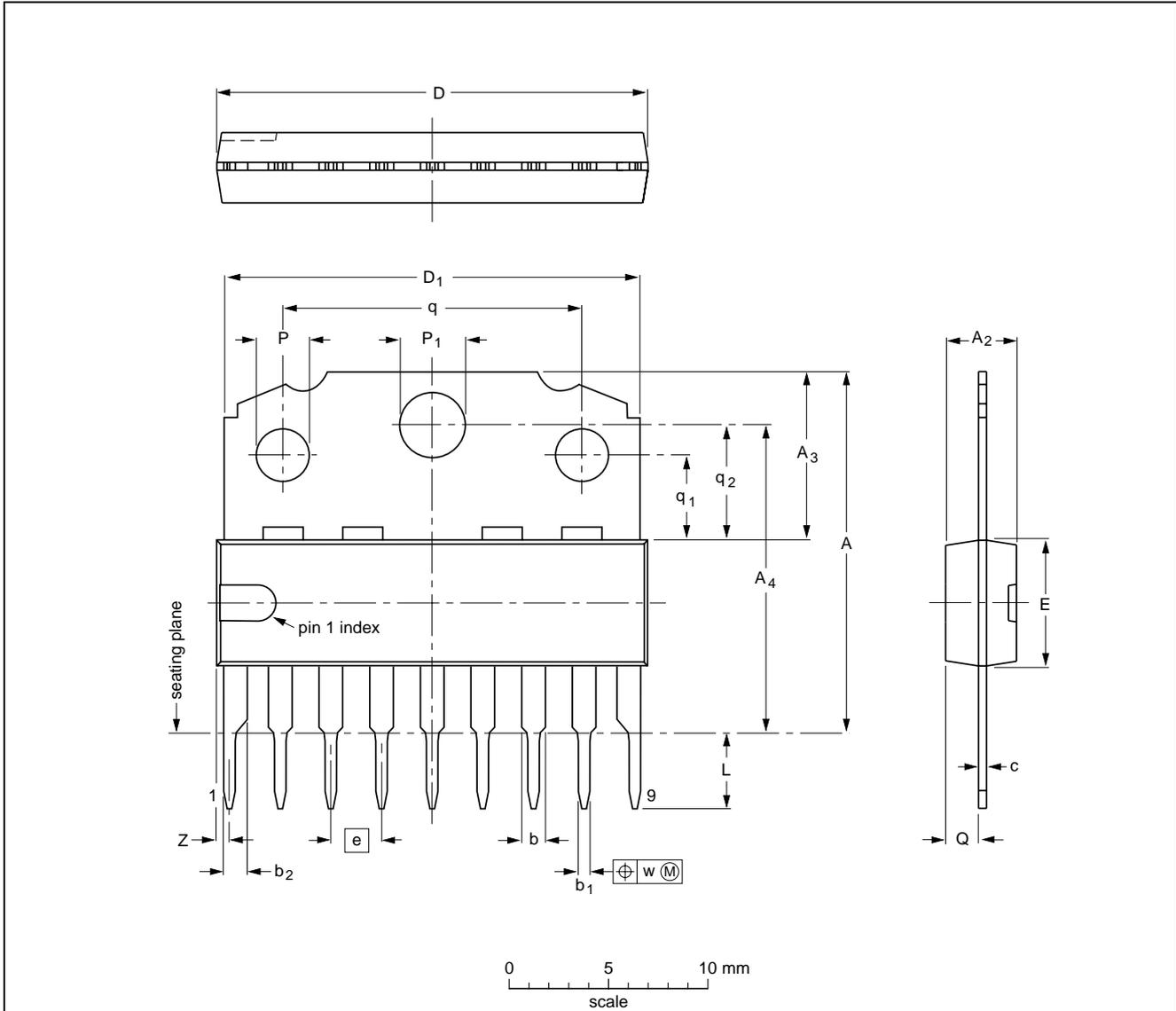
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PACKAGE OUTLINE

SIL9MPF: plastic single in-line medium power package with fin; 9 leads

SOT110-1



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>2</sub> max.	A <sub>3</sub>	A <sub>4</sub>	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	D <sub>1</sub>	E <sup>(1)</sup>	e	L	P	P <sub>1</sub>	Q	q	q <sub>1</sub>	q <sub>2</sub>	w	Z <sup>(1)</sup> max.
mm	18.5 17.8	3.7	8.7 8.0	15.8 15.4	1.40 1.14	0.67 0.50	1.40 1.14	0.48 0.38	21.8 21.4	21.4 20.7	6.48 6.20	2.54	3.9 3.4	2.75 2.50	3.4 3.2	1.75 1.55	15.1 14.9	4.4 4.2	5.9 5.7	0.25	1.0

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT110-1						92-11-17 95-02-25

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## SOLDERING

### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

### Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg\ max}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

### Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

## DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

## LIFE SUPPORT APPLICATIONS

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