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C-MOS ENHANCED MULTI INTERFACE FOR LBP
-TOP VIEW-
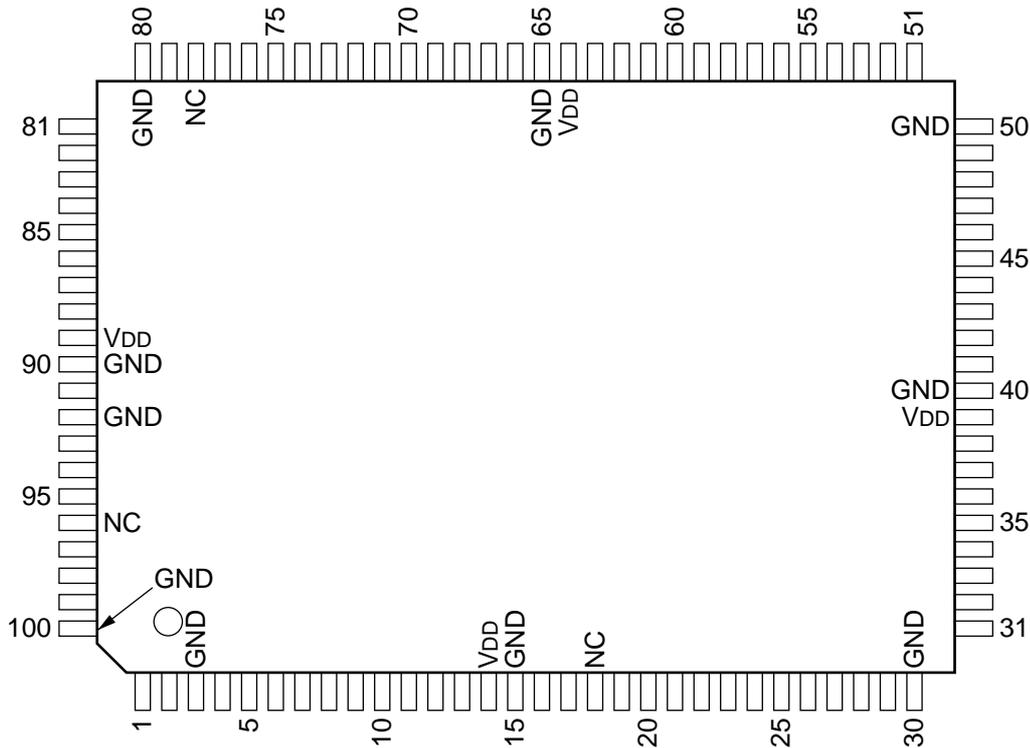
PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	i$\overline{RST}$	21	I	iS0	41	I/O	P1bD4	61	O	BPo$\overline{FT}$	81	I	HDiD/$\overline{C}$
2	I	iCIS	22	I	iA2	42	I/O	P1bD3	62	O	BPoSE	82	I	HDiRXD
3	—	GND	23	I	iA1	43	I/O	P1bD2	63	I/O	BPbD7	83	I	UTiRXD
4	I/O	bD7	24	I	iA0	44	I/O	P1bD1	64	—	V$_{DD}$	84	I	UTi$\overline{DSR}$
5	I/O	bD6	25	O	HDo$\overline{INT}$	45	I/O	P1bD0	65	—	GND	85	I	UTi$\overline{CTS}$
6	I/O	bD5	26	O	BPo$\overline{INT0}$	46	I/O	P2bD7	66	I/O	BPbD6	86	O	UToTXD
7	I/O	bD4	27	O	UTo$\overline{INT}$	47	I/O	P2bD6	67	I/O	BPbD5	87	O	UTo$\overline{DTR}$
8	I/O	bD3	28	O	IOo$\overline{INT1}$	48	I/O	P2bD5	68	I/O	BPbD4	88	O	UTo$\overline{RTS}$
9	I/O	bD2	29	O	IOo$\overline{INT2}$	49	I/O	P2bD4	69	I/O	BPbD3	89	—	V$_{DD}$
10	I/O	bD1	30	—	GND	50	—	GND	70	I/O	BPbD2	90	—	GND
11	I/O	bD0	31	I	UTiECK	51	I/O	P2bD3	71	I/O	BPbD1	91	I	BPiCLK
12	I	i$\overline{RD/RW}$	32	I	P3iD1	52	I/O	P2bD2	72	I/O	BPbD0	92	—	GND
13	I	i$\overline{WR/EN}$	33	I	P3iD2	53	I/O	P2bD1	73	O	HDo$\overline{RTS}$	93	O	BPoRT
14	—	V$_{DD}$	34	O	BPo$\overline{INT1}$	54	I/O	P2bD0	74	O	HDo$\overline{SYNC}$	94	I	BPiCLS
15	—	GND	35	O	BPo$\overline{INT2}$	55	I	BPi$\overline{SEI}$	75	O	HDo$\overline{TRXC}$	95	O	BPo$\overline{DRQ}$
16	I	iCLK	36	I/O	P1bD7	56	I	BPi$\overline{AF}$	76	O	HDoTXD	96	—	NC
17	I	i$\overline{CS}$	37	I/O	P1bD6	57	I	BPi$\overline{STB}$	77	O	HDo$\overline{W/Q}$	97	O	PBo$\overline{DEND}$
18	—	NC	38	I/O	P1bD5	58	O	BPoPE	78	—	NC	98	I	BPi$\overline{DAK}$
19	I	iS2	39	—	V$_{DD}$	59	O	BPo$\overline{ACK}$	79	I	HDiPCLK	99	I	BPiINI
20	I	iS1	40	—	GND	60	O	BPoBY	80	—	GND	100	—	GND

INPUT

BPi$\overline{\text{AF}}$	;	COMPATIBILITY = n AUTO Fd
BPiCLK	;	I/O PARALLEL INTERFACE CLOCK
BPiCLS	;	COMPATIBILITY MODE LEVEL SELET
BPi$\overline{\text{DAK}}$	;	DMAC ACKNOWLEDGE
BPiINI	;	COMPATIBILITY = n INITIAL
BPiINT	;	COMPATIBILITY = n INT
BPi$\overline{\text{SEI}}$	;	COMPATIBILITY = n SELECT IN
BPi$\overline{\text{STB}}$	;	COMPATIBILITY = n STROBE
HDiD/$\overline{\text{C}}$	;	HDLC DATA/COMMAND SELECT
HDiPCLK	;	HDLC P CLOCK
HDiRXD	;	HDLC RECEIVE DATA
iA0-iA2	;	ADDRESS
iCIS	;	CPU INTERFACE SELECT
iCLK	;	CLOCK (3.6864 MHz)
i$\overline{\text{CS}}$	;	CHIP SELECT
i$\overline{\text{RD}}$/R$\overline{\text{W}}$	;	READ/READ WRITE SELECT
i$\overline{\text{RST}}$	;	RESET
iS0-iS2	;	BLOCK SELECT
i$\overline{\text{WR}}$/$\overline{\text{EN}}$	;	WRITE/ENABLE
P3iD1, P3iD2	;	EXTERNAL INTERRUPT
UTi$\overline{\text{CTS}}$	;	UART CTS
UTi$\overline{\text{DSR}}$	;	UART DATA SET READY
UTiECK	;	EXTERNAL UART CLOCK
UTiRXD	;	UART RECEIVE DATA

OUTPUT

BPo$\overline{\text{ACK}}$	;	COMPATIBILITY = n ACK
BPoBY	;	COMPATIBILITY = BUSY
BPo$\overline{\text{DEND}}$	;	DMAC END
BPo$\overline{\text{DRQ}}$	;	DMAC REQUEST
BPo$\overline{\text{FT}}$	;	COMPATIBILITY = n FAULT
BPo$\overline{\text{INT0}}$-BPo$\overline{\text{INT2}}$	;	INTERRUPT REQUEST 0-2
BPoPE	;	COMPATIBILITY = P ERROR
BPoRT	;	INDICATE REVERSE TRANSFER
BPoSE	;	COMPATIBILITY = SELECT
HDo$\overline{\text{INT}}$	;	HDLC INTERRRUPT
HDo$\overline{\text{RTS}}$	;	HDLC REQUEST TO SEND
HDo$\overline{\text{SYNC}}$	;	HDLC SYNC
HDo$\overline{\text{TRXC}}$	;	HDLC TRANSMIT/RECEIVE CLOCK
HDoTXD	;	HDLC TRANSMIT DATA
HDo$\overline{\text{W}}$/$\overline{\text{Q}}$	;	HDLC WAIT/REQUEST
IOo$\overline{\text{INT1}}$, IOo$\overline{\text{INT2}}$	;	INTERRUPT
UTo$\overline{\text{DTR}}$	;	UART DATA TERMINAL READY
UTo$\overline{\text{INT}}$	;	UART INTERRUPT
UTo$\overline{\text{RTS}}$	;	UART REQUEST TO SEND
UToTXD	;	UART TRANSMIT DATA

INPUT/OUTPUT

bD0-bD7	;	DATA BUS
BPbD0-BPbD7	;	COMPATIBILITY = DATA
P1bD0-P1bD7	;	PARALLEL PORT1
P2bD0-P2bD7	;	PARALLEL PORT2

HDiPCLK 79 | iCLK 16

iRST 1 | iCIS 2 | iCS 17

HDiD/C̄ 81
HDoW̄/Q̄ 77
HDoTXD 76
HDiRXD 82
HDoTRXC̄ 75
HDoSYNC̄ 74
HDoRTS̄ 73

HDLC

DATA BUS
ADDRESS BUS
CONTROL

CPU INTERFACE

4-11 → bD7-0
21-19 → iS2-0
24-22 → iA2-0
12 → iRD/RW̄
13 → iWR̄/EN̄

UToTXD 86
UTiRXD 83
UToDTR̄ 87
UToRTS̄ 88
UTiDSR̄ 84
UTiCTS̄ 85
UTiECK 31

UART

INTERRUPT CONTROL

32 → P3iD1
33 → P3iD2
25, 27-29
26, 34, 35 → HDoINT̄, UToINT̄, IOoINT̄1, IOoINT̄2, BPoINT̄0, BPoINT̄1, BPoINT̄2

BPiINI 99
BPiSEI̅ 55
BPiAF̄ 56
BPiSTB̅ 57
BPoPE 58
BPoACK̄ 59
BPoBY 60
BPoFT̄ 61
BPoSE 62
BPoRT 93
BPbD7-0 72-66,63
BPiCLS 94
BPiCLK 91

BI-DIRECTIONAL PARALLEL

PARALLEL PORT

36-38, 41-45 → P1bD7-0
46-49, 51-54 → P2bD7-0

DMA CONTROL

95 → BPoDRQ̄
98 → BPiDAK̄
97 → BPoDEND̄