SHARP

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ISSUE:	Jan. 16 1996

To ;

SPECIFICATIONS

Product Type 256kx4 bit DRAM (262,144 x 4bit)

LH64256CZ-70

Model No. (LH645C2Z)

※This specifications contains 23 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

DATE:

BY:

SHARP CORPORATION IC GROUP 1.30'97. MAIL DATE

PRESENTED

BY: T. Kuzumoto

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REVIEWED BY: M. Honda

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●When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.

(1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).
- ·Office electronics
- ·Instrumentation and measuring equipment
- ·Machine tools
- ·Audiovisual equipment
- ·Home appliances
- ·Communication equipment other than for trunk lines

(2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.
- ·Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
- ·Mainframe computers
- ·Traffic control systems
- ·Gas leak detectors and automatic cutoff devices
- ·Rescue and security equipment
- ·Other safety devices and safety equipment, etc.

(3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.
- ·Aerospace equipment
- ·Communications equipment for trunk lines
- ·Control equipment for the nuclear power industry
- ·Medical equipment related to life support, etc.

(4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

●Please direct all queries regarding the products covered herein to a sales representative of the company.

Contents

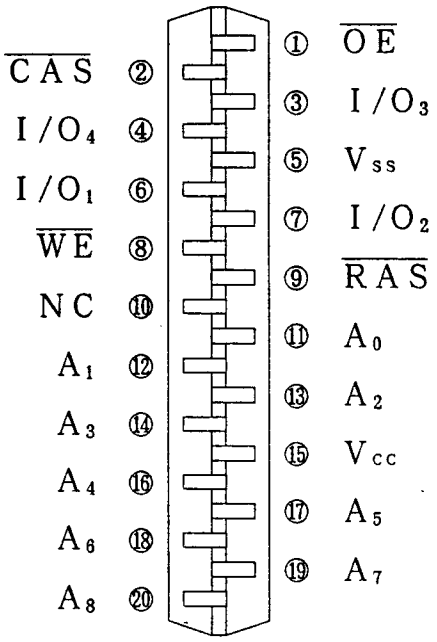
1. General

SHARP LH64256CZ-70 is a 262,144word x 4bit Dynamic Random Access Memory which allows fast page mode access. The LH64256CZ-70 is fabricated on SHARP's advanced CMOS double-level polysilicon gate technology. With its input multiplexed and packaged in the standard 20pin ZIP, it is easy to realize the memory systems with low power dissipation and large memory capacity. The LH64256CZ-70 operates on a single +5.0V power supply and the built-in biasing voltage generator circuit.

2. Features

- 262,144word x 4bit
- Standard 10.16mm 20pin ZIP(ZPT20-P-400) plastic package
- Access time 70ns (Max.)
- Cycle time 130ns (Min.)
- Fast page mode with cycle time 50ns (Min.)
- Power supply +5.0V±10%
- Power consumption (Max.) 467.5mW (Operating : t_{RC}=130ns)
  11mW (Standby : TTL input level)
  5.5mW (Standby : CMOS input level)
- Built-in latch circuit for Row-address, Column-address and Input-data
- $\overline{OE}$=Don't care in early write operation
- $\overline{RAS}$ only refresh, Hidden refresh and $\overline{CAS}$ before $\overline{RAS}$ refresh capability
- On-chip refresh counter
- 512 refresh cycle / 8ms
- Not designed or rated as radiation hardened
- P-type bulk silicon CMOS process
- Operating temperature range : 0 to +70℃

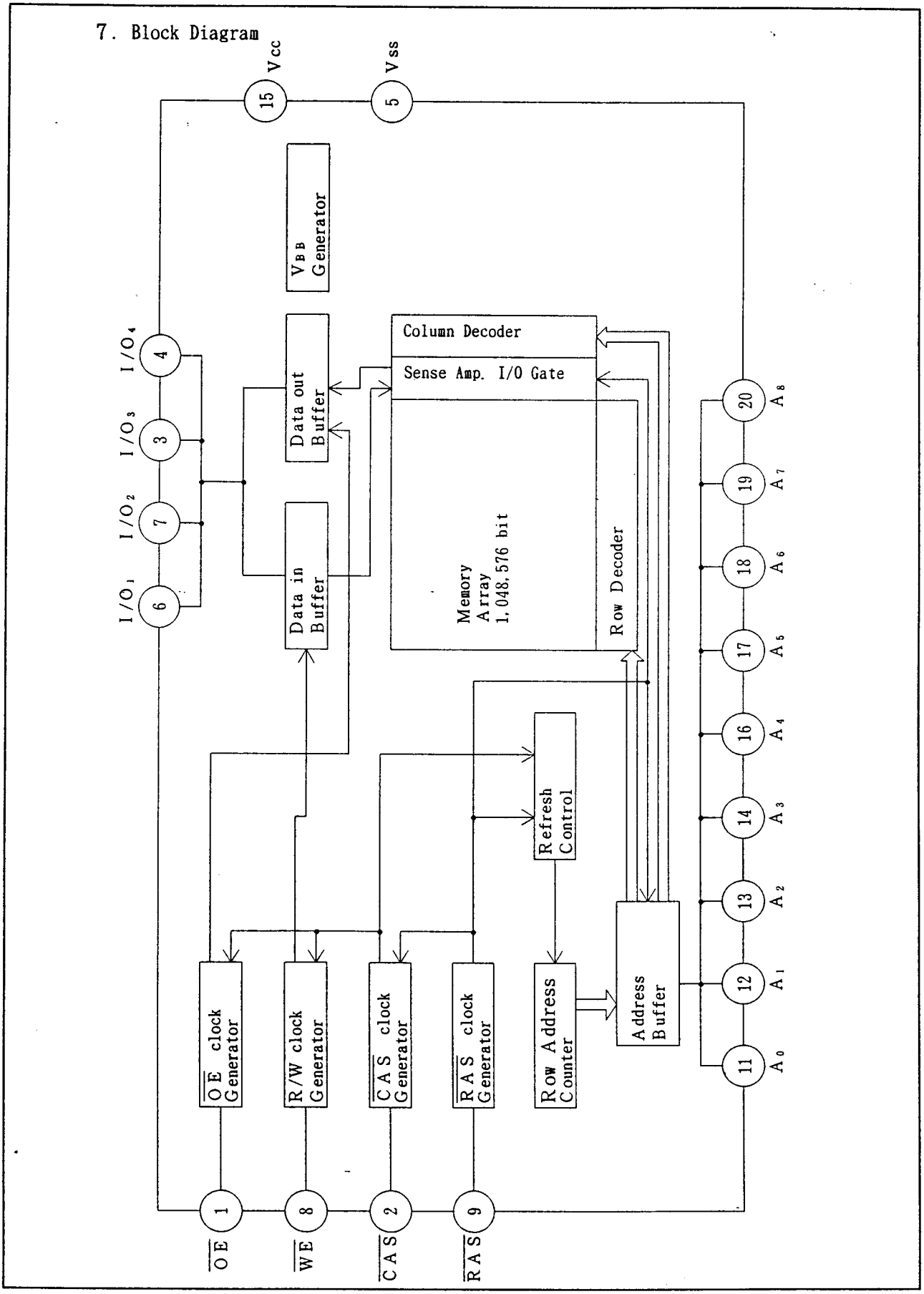
3. Pin configuration



[Bottom View]

Symbol	Pin Name
A_0 to A_8	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O_1 to I/O_4	Data Input/Output
V_{CC}	Power Supply(+5.0V)
V_{SS}	Power Supply(0V)
NC	No-Connection

7. Block Diagram



5. Absolute Maximum Ratings

Parameter	Rating	Unit	Note
Applied voltage on all pins	−1.0 to +7.0	V	1
Operating temperature	0 to +70	℃	
Storage temperature	−65 to +150	℃	
Output short circuit current	50	mA	
Power dissipation	600	mW	2

Note 1. With respect to Vss.

Note 2. Ta=25℃

6. Recommended Operating Conditions

(Ta=0 to +70℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	note
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input voltage	V_{IH}	2.4		Vcc+0.3V	V	
	V_{IL}	−0.3		0.8	V	

7. Pin Capacitance

(Ta=0 to +70℃, V_{CC}=5.0V±10%, f=1MHz)

Parameter		Symbol	MIN.	MAX.	Unit
Input capacitance	A_0 to A_8	C_{IN1}	−	7	pF
	$\overline{RAS}$, $\overline{OE}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	−	7	pF
Input/Output capacitance	I/O_1 to I/O_4	C_{OUT1}	−	8	pF

8. DC Electrical Characteristics

(Ta=0 to +70℃, V_{CC}=5.0V±10%)

Parameter			Symbol	MIN.	MAX.	Unit	Note
Average supply current in normal operation t_{RC}=MIN.			I_{CC1}	–	85	mA	3,4
Average supply current in standby mode	TTL	$\overline{RAS}$=$\overline{CAS}$=V_{IH}	I_{CC2}	–	2.0	mA	3
	CMOS	$\overline{RAS}$=$\overline{CAS}$≧V_{CC}-0.2V		–	1.0	mA	
Average supply current in fast page mode t_{CP}=MIN.			I_{CC4}	–	65	mA	3,4
Average supply current in $\overline{CAS}$ before $\overline{RAS}$ refresh cycle			I_{CC6}	–	85	mA	3,4
Average supply current in $\overline{RAS}$ only refresh cycle			I_{CC3}	–	85	mA	3,4
Input leakage current	0V≦V_{IN}≦6.5V 0V except on test pins		I_{LI}	-10	10	μA	
Output leakage current	0V≦V_{OUT}≦Vcc+0.3V Output=Disable		I_{LO}	-10	10	μA	5
Output "High" voltage	I_{OH}=-5mA		V_{OH}	2.4	–	V	
Output "Low" voltage	I_{OL}=4.2mA		V_{OL}	–	0.4	V	

Note 3. The output pins are in high impedance state.

4. I_{CC1}, I_{CC4}, I_{CC6} and I_{CC3} depend on cycle time.

5. The output pins are disabled by $\overline{RAS}$=$\overline{CAS}$=V_{IH} or $\overline{CAS}$=V_{IH}.

9. A C Electrical Characteristics (Note 6, 7, 8, 9)

Read Cycle (Ta=0 to +70℃, Vcc=5.0V ±10%)

Parameter	Symbol	MIN.	MAX.	Unit	Note
Random read or write cycle time	t_{RC}	130	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	70	ns	14
Access time from column address	t_{AA}	–	35	ns	14
Access time from $\overline{CAS}$	t_{CAC}	–	25	ns	14
Access time from $\overline{OE}$	t_{OEA}	–	20	ns	14
Row address set-up time	t_{ASR}	0	–	ns	
Row address hold time	t_{RAH}	10	–	ns	
Column address set-up time	t_{ASC}	0	–	ns	
Column address hold time ($\overline{RAS}$)	t_{CAH}	15	–	ns	
Column address delay time ($\overline{RAS}$)	t_{RAD}	15	35	ns	10
Column address lead time ($\overline{RAS}$)	t_{RAL}	35	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	ns	
$\overline{RAS}$ precharge time	t_{RP}	50	–	ns	
$\overline{CAS}$ precharge time ($\overline{RAS}\downarrow$)	t_{CRP}	10	–	ns	
$\overline{CAS}$ delay time ($\overline{RAS}$)	t_{RCD}	20	45	ns	11
$\overline{CAS}$ lead time ($\overline{RAS}$)	t_{RSL}	25	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	70	–	ns	
$\overline{OE}$ lead time ($\overline{RAS}$)	t_{ROL}	0	–	ns	
Output data disable time ($\overline{CAS}$)	t_{OFF}	–	20	ns	
Output data disable time ($\overline{OE}$)	t_{OEZ}	–	20	ns	
Output data hold time ($\overline{CAS}$)	t_{SOH}	0	–	ns	
Output data hold time ($\overline{OE}$)	t_{OOH}	0	–	ns	
Read command set-up time ($\overline{CAS}$)	t_{RCS}	0	–	ns	
Read command hold time ($\overline{CAS}$)	t_{RCH}	0	–	ns	13
Read command hold time ($\overline{RAS}\uparrow$)	t_{RRH}	10	–	ns	13
Transition time (rise and fall)	t_T	3	50	ns	
Refresh time interval	t_{REF}	–	8	ms	

Fast Page Mode Cycle

Parameter	Symbol	MIN.	MAX.	Unit	Note
Fast page mode cycle time	t_{PC}	50	–	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	ns	
$\overline{CAS}$ precharge access time	t_{CACP}	–	45	ns	
Read-write cycle time (page mode)	t_{PRWC}	100	–	ns	12

Write Cycle

Parameter	Symbol	MIN.	MAX.	Unit	Note
(Early Write)					
Write command set-up time ($\overline{CAS}$)	t_{WCS}	0	–	ns	12
Write command hold time ($\overline{CAS}$)	t_{WCH}	15	–	ns	
Data input set-up time	t_{DS}	0	–	ns	
Data input hold time	t_{DH}	15	–	ns	
($\overline{OE}$ Controlled)					
$\overline{CAS}$ set-up time	t_{CWS}	0	–	ns	12
Write command lead time ($\overline{RAS}$)	t_{RWL}	20	–	ns	
Write command lead time ($\overline{CAS}$)	t_{CWL}	20	–	ns	
Write pulse width ($\overline{WE}$)	t_{WP}	10	–	ns	
$\overline{OE}$ hold time ($\overline{WE}$)	t_{OEH}	20	–	ns	

Read-Write Cycle / Read Modify Write Cycle

Parameter	Symbol	MIN.	MAX.	Unit	Note
Read-write cycle time	t_{RWC}	180	–	ns	12
$\overline{WE}$ delay time ($\overline{RAS}$)	t_{RWD}	95	–	ns	12
Column address delay time ($\overline{WE}$)	t_{AWD}	60	–	ns	12
$\overline{WE}$ delay time ($\overline{CAS}$)	t_{CWD}	45	–	ns	12
$\overline{OE}$ delay time	t_{OED}	20	–	ns	

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle / Hidden Refresh Cycle

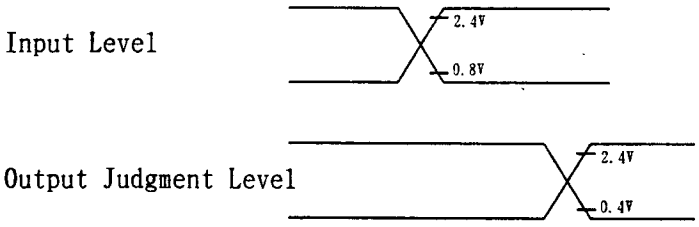
Parameter	Symbol	MIN.	MAX.	Unit	Note
$\overline{CAS}$ set-up time ($\overline{RAS}$)	t_{CSR}	10	–	ns	
$\overline{CAS}$ hold time ($\overline{RAS}$)	t_{CHR}	15	–	ns	
$\overline{RAS}$ · $\overline{CAS}$ precharge time ($\overline{RAS}$ ↑)	t_{RPCP}	10	–	ns	
$\overline{WE}$ precharge time ($\overline{RAS}$)	t_{WRP}	0	–	ns	

Note 6. For properly functioning the memory, it is necessary to pause at least 200μs after power-on and followed by several dummy cycles. When $\overline{RAS}$=V_{IH} is continued for more than 8ms, the above dummy cycles should be given. Usually 8 ordinary refresh cycles should be given.

7. The current consumption (Icc) during power on is dependent on the input level of $\overline{RAS}$. If $\overline{RAS}$ is V_{IL} during power on, the device goes into an active cycle automatically, and Icc exhibits large current transients. It is recommended that $\overline{RAS}$ tracks with Vcc or be held at a valid V_{IH} during power on.

8. AC characteristics assume t_T=5ns.

9. AC characteristics assume the following condition.



10. t_{RAD}(MAX.) is the maximum point for t_{RAD} where t_{RAC}(MAX.) is ensured, and does not represent a limit of operation.
If $t_{RAD} \geqq t_{RAD}$(MAX.), the access time comes under the control of t_{AA}.

11. t_{RCD}(MAX.) is the maximum point for t_{RCD} where t_{RAC}(MAX.) is ensured, and dose not represent a limit of operation.
If $t_{RCD} \geqq t_{RCD}$(MAX.), the access time comes under the control of t_{CAC}.

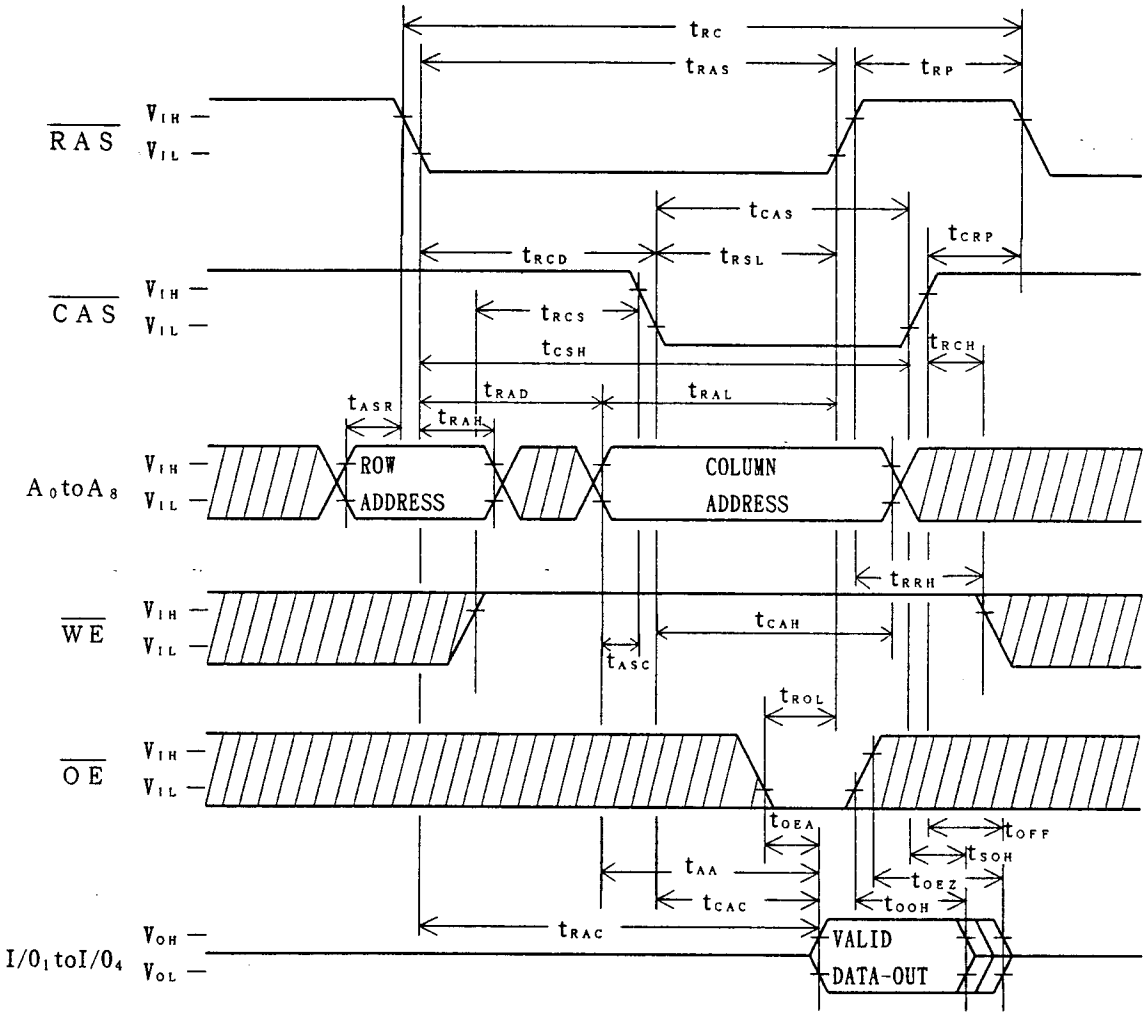
12. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are the restrictive operating parameters and do not represent a limit of operation.
If $t_{WCS} \geqq t_{WCS}$(MIN.), the cycle is the early write cycle and data out buffers remain inactive until $\overline{CAS}$ rises up again.
If $t_{CWD} \geqq t_{CWD}$(MIN.), $t_{RWD} \geqq t_{RWD}$(MIN.) and $t_{AWD} \geqq t_{AWD}$(MIN.), the cycle is the read modify write cycle and the output data will be the information of the selected cell. Except for the above timing, the output data will be indefinite.

13. The operation is ensured when either t_{RRH} or t_{RCH} is satisfied.

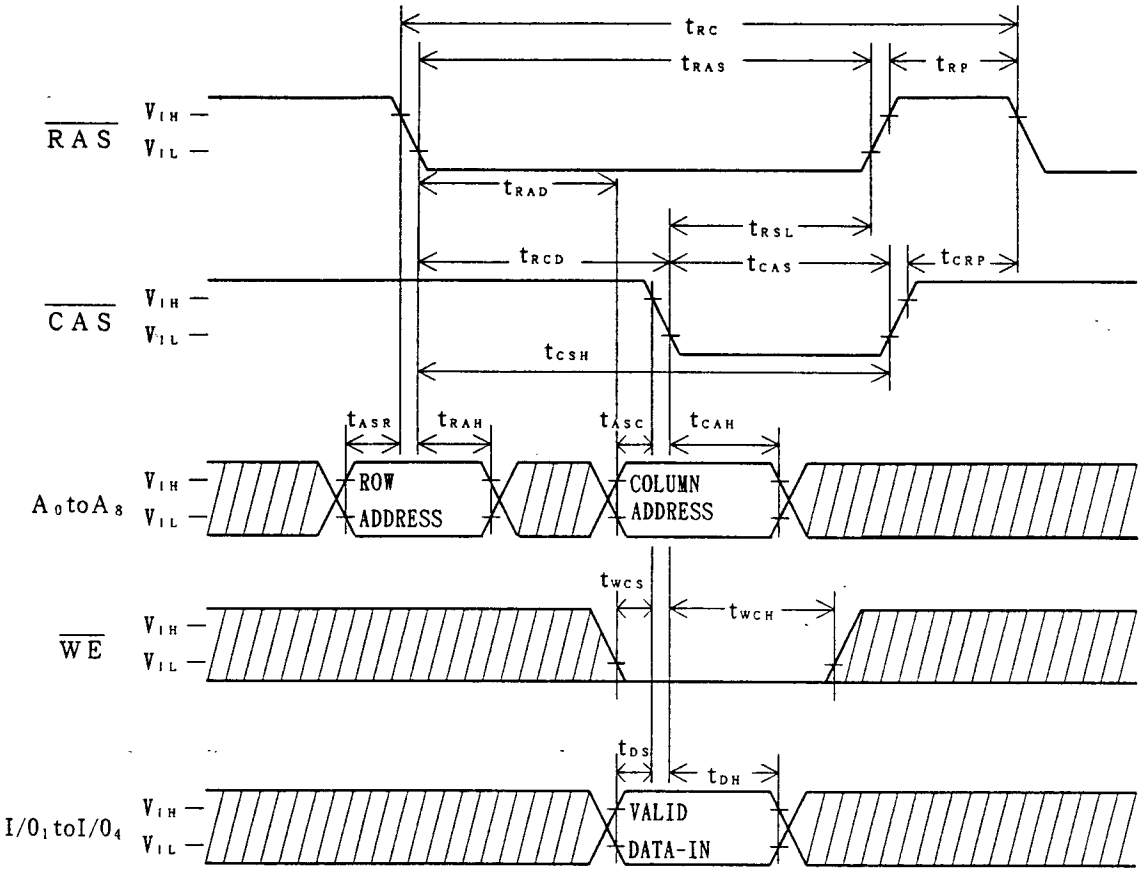
14. Measured with a load equivalent to
2TTL(−1mA, +4mA) + Cload (100pF).
(Including the scope and the jig)

10. Timing Chart

Read Cycle

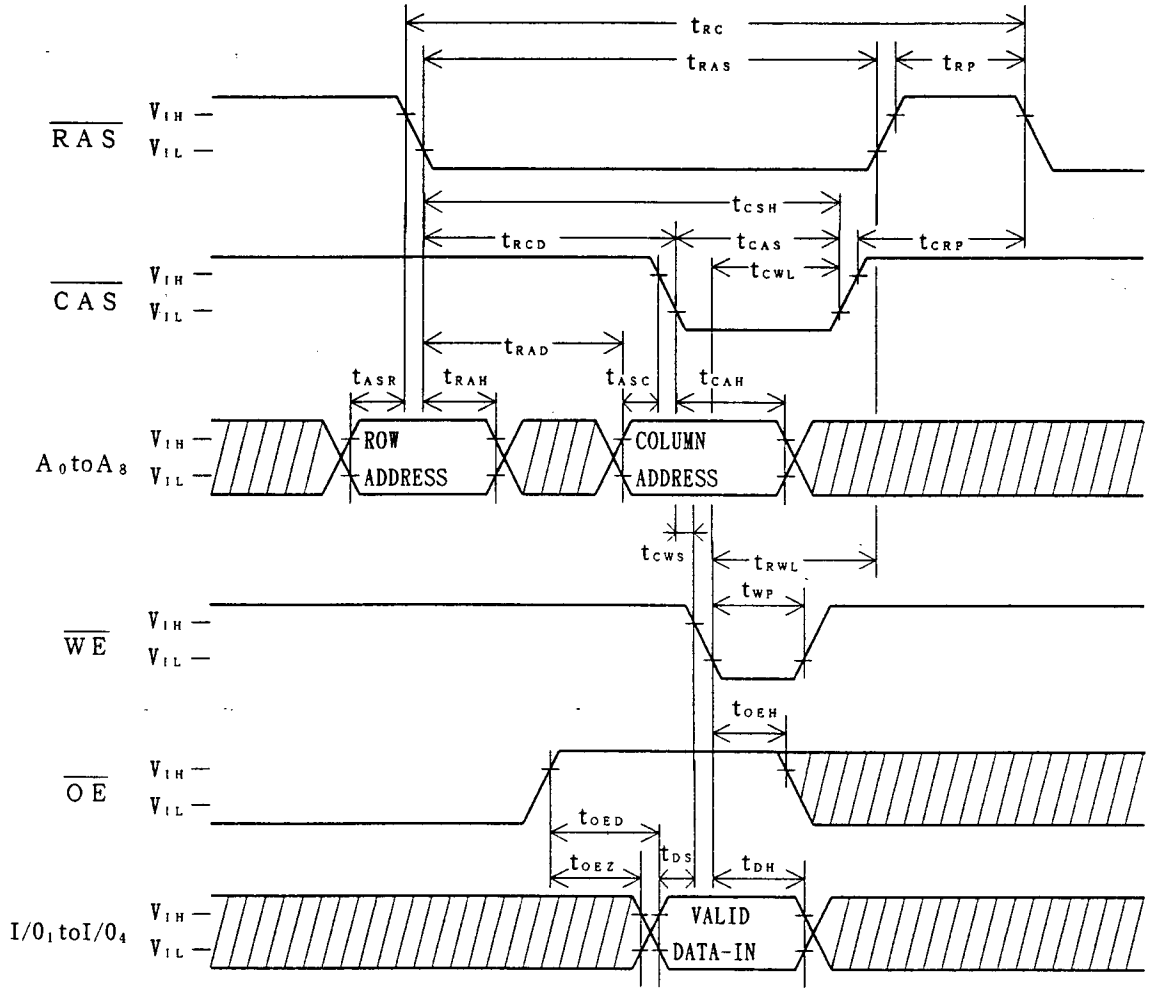


Write Cycle (Early Write)

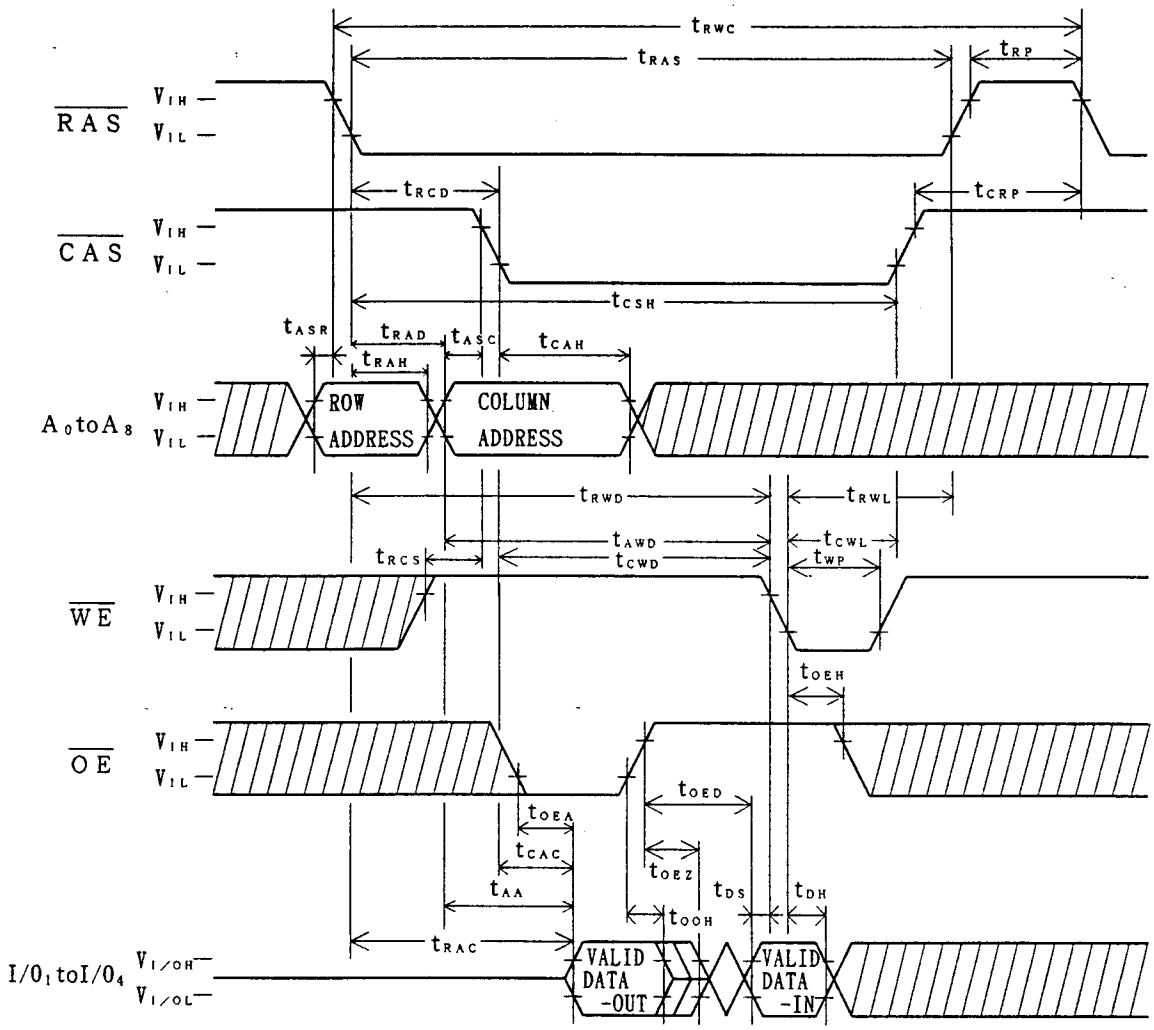


$\overline{OE}$ = Don't Care

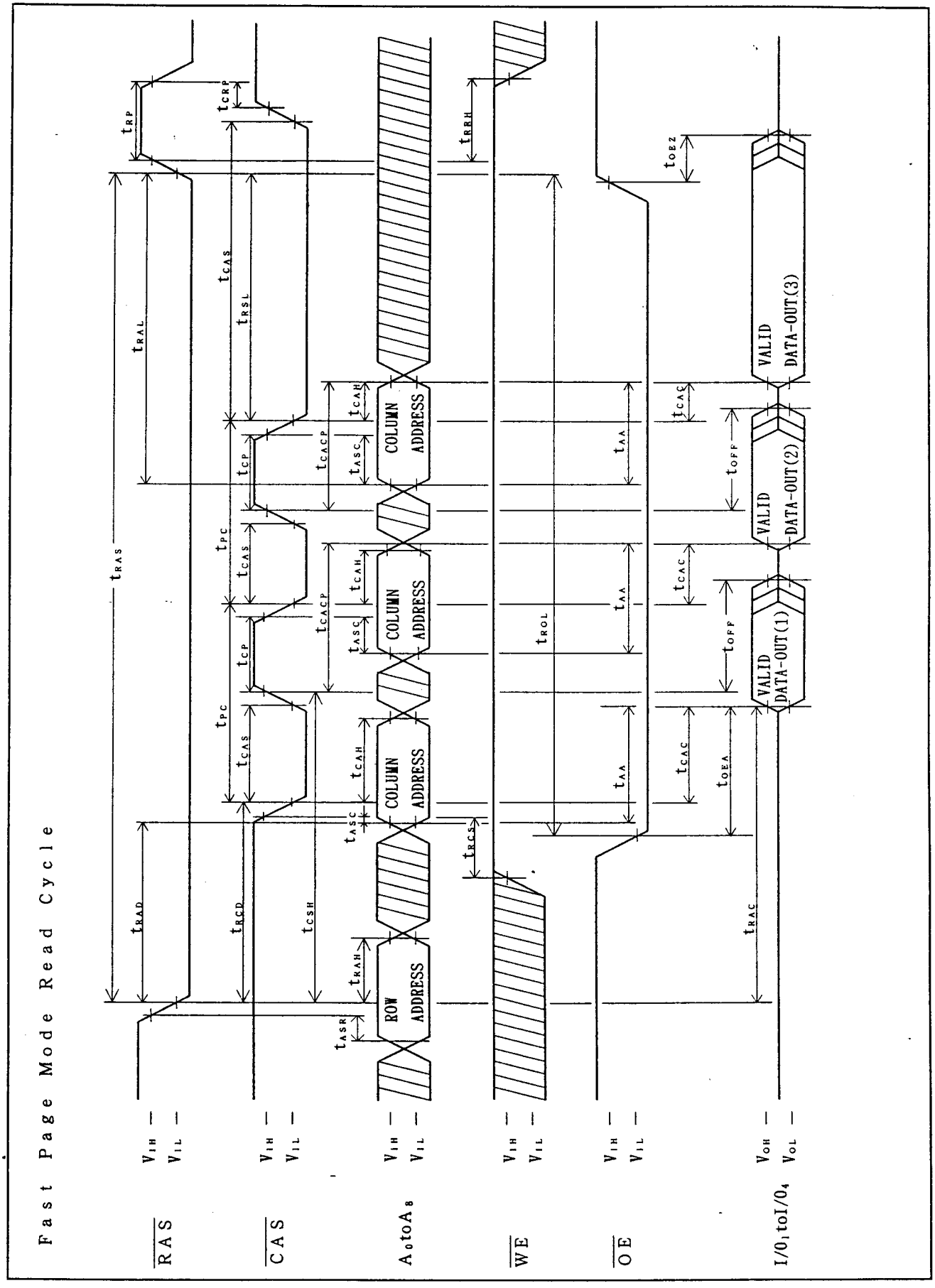
Write Cycle ($\overline{OE}$ Controlled Write)



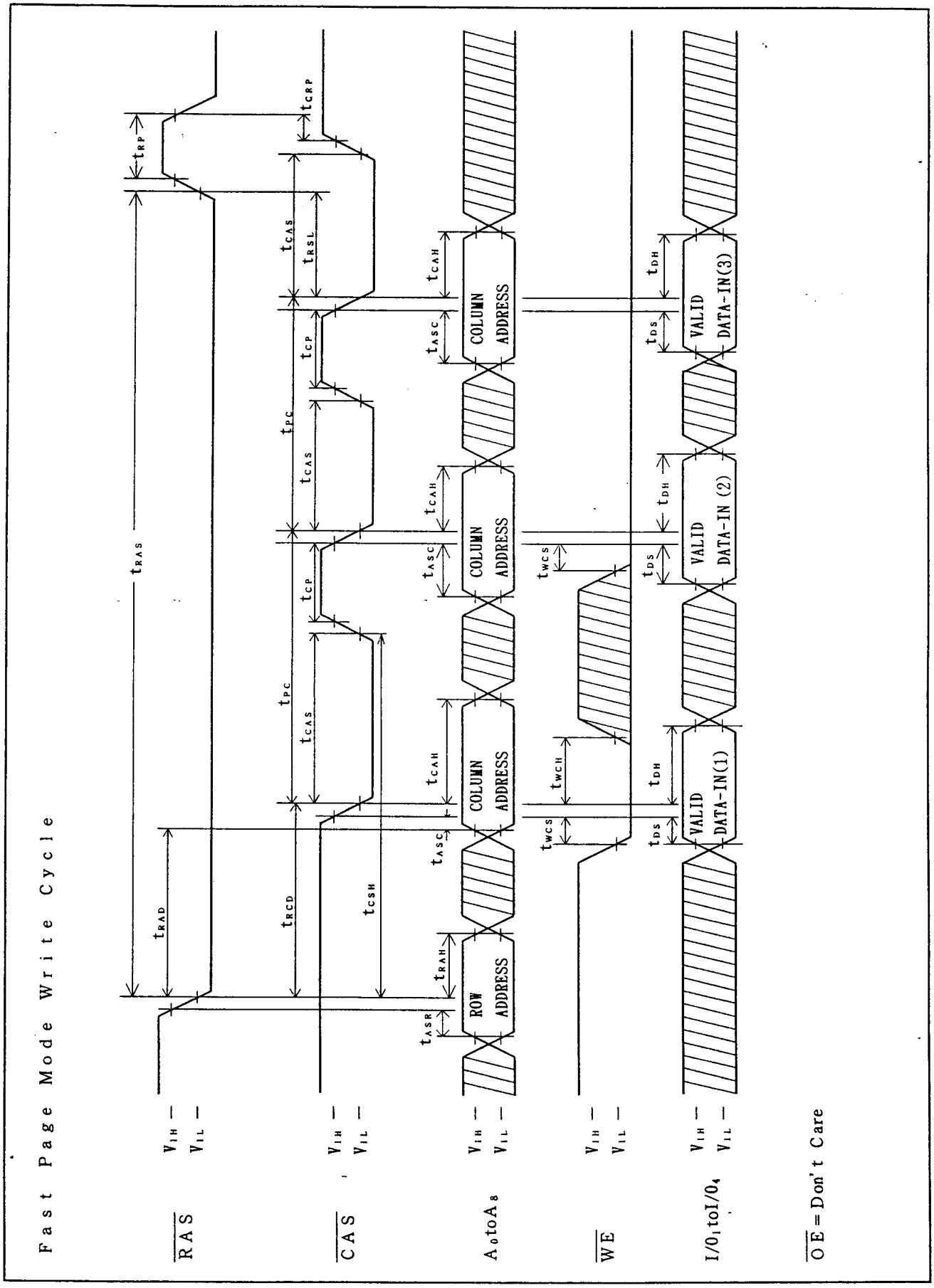
Read/Write Cycle



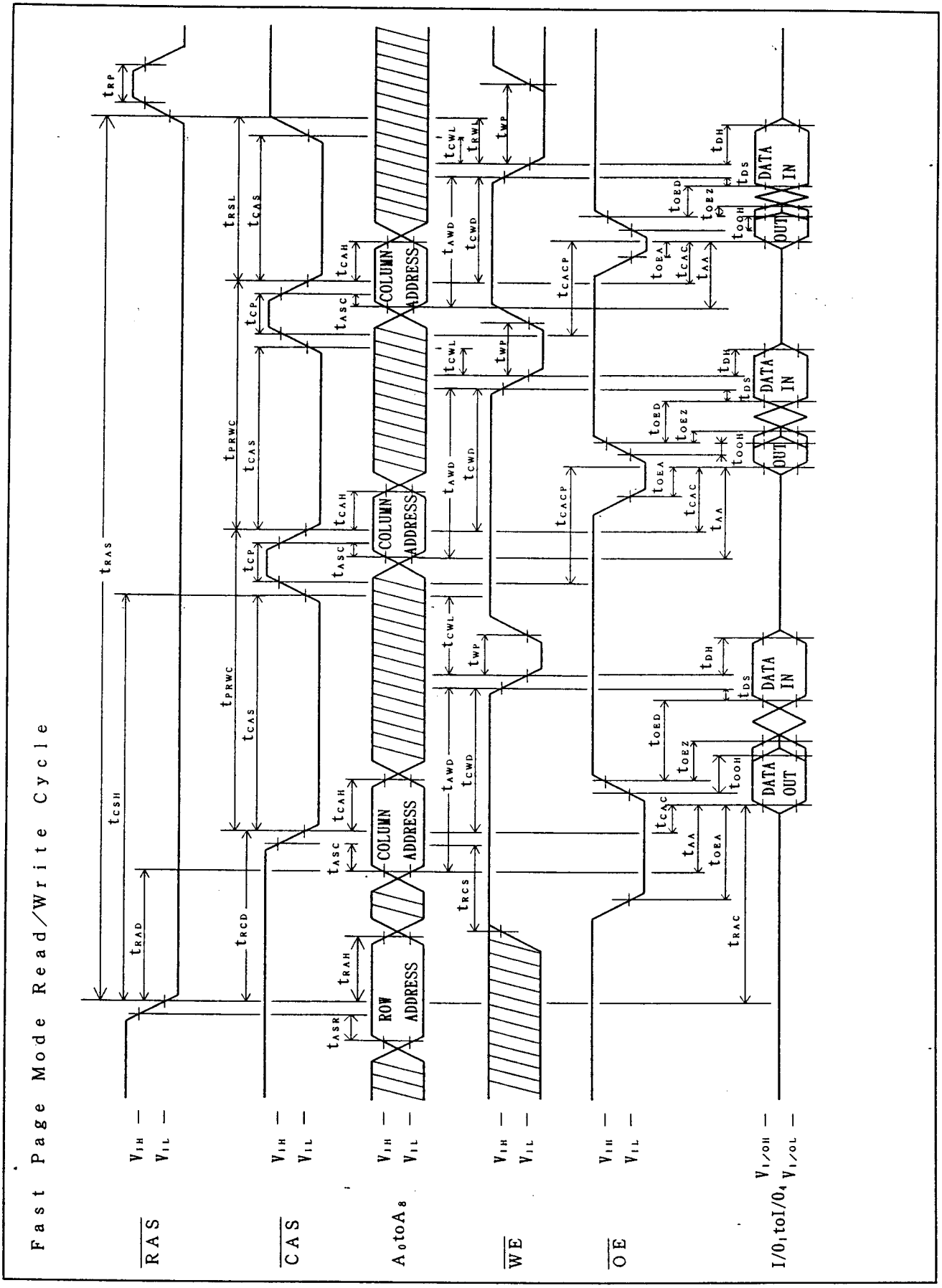
Fast Page Mode Read Cycle



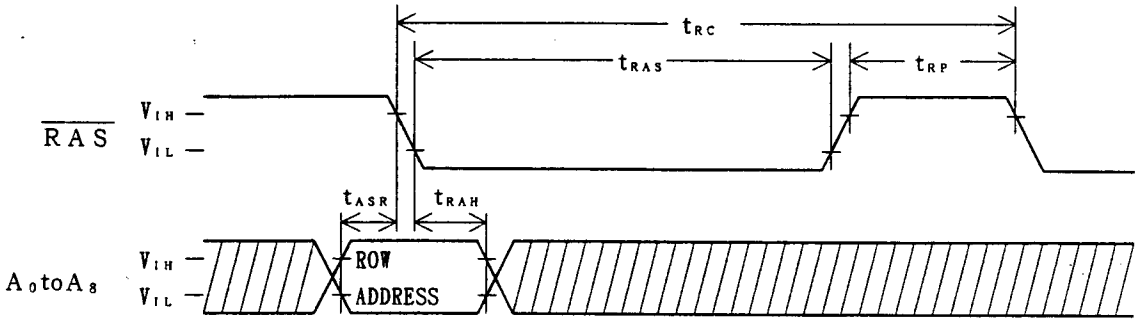
Fast Page Mode Write Cycle



Fast Page Mode Read/Write Cycle

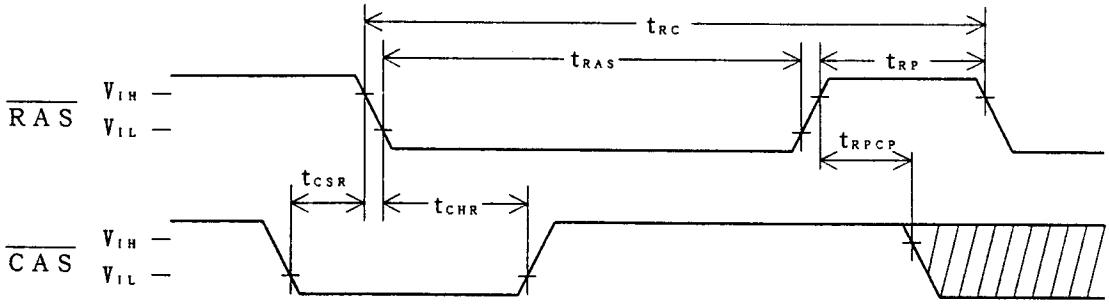


$\overline{RAS}$ Only Refresh Cycle



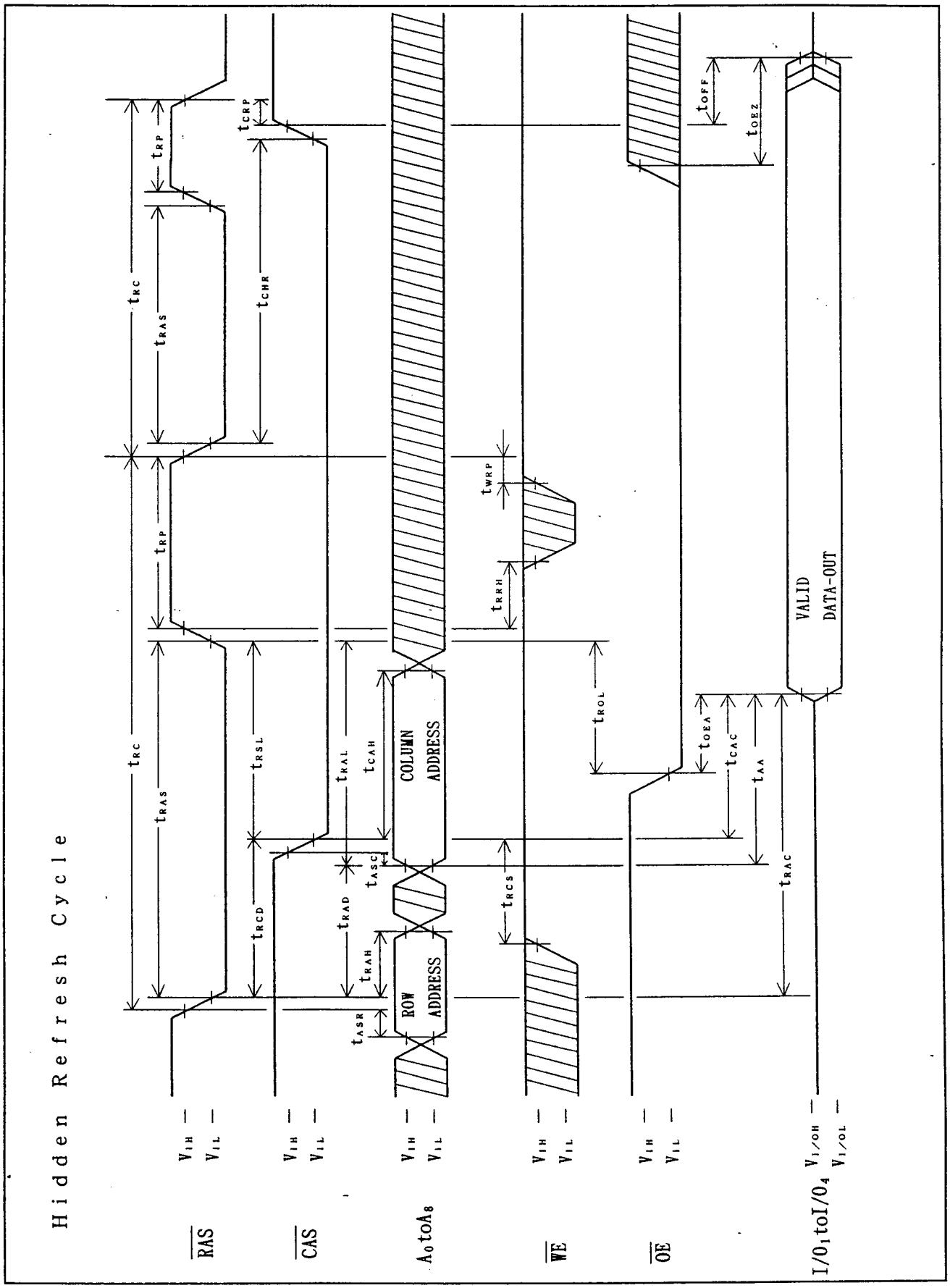
$\overline{CAS}$="H"、$\overline{WE}$, $\overline{OE}$=Don't Care

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



$\overline{WE}$, $\overline{OE}$, A_0~A_8=Don't Care

Hidden Refresh Cycle



11 Package and packing specification

1. Package Outline Specification

Refer to drawing No.AA1009

2. Markings

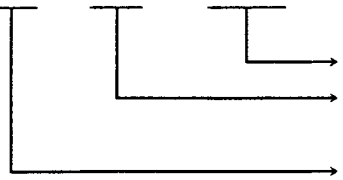
2－1. Marking contents

(1) Product name : LH64256CZ－70

(2) Company name : SHARP

(3) Date code

(Example) YY WW ××× Indicates the product was manufactured in the WWth week of 19YY.



Denotes the production ref.code (1~3)

Denotes the production week. (01,02,03,・・・・・52,53)

Denotes the production year. (Lower two digits of the year.)

(4) The marking of "JAPAN" indicates the country of origin.

2－2. Marking layout

Refer to drawing No.AA1009

(This layout do not define the dimensions of marking character and marking position.)

3. Packing Specification

3－1. Packing materials

Material Name	Material Specification	Purpose
Magazine	Anti-static treated plastic (20devices/magazine)	Packing of device
Stopper	Plastic or rubber	Fixing of device
Label	Paper	Indication of product name, quantity and date of manufacture.
Inner case	Cardboard (1600devices/cace)	Fixing of magazine
Outer case	Cardboard	Outer packing of magazine

(Devices shall be inserted into a magazine (sleeve) in the same direction.)

3－2. Outline dimension of magazine (sleeve)

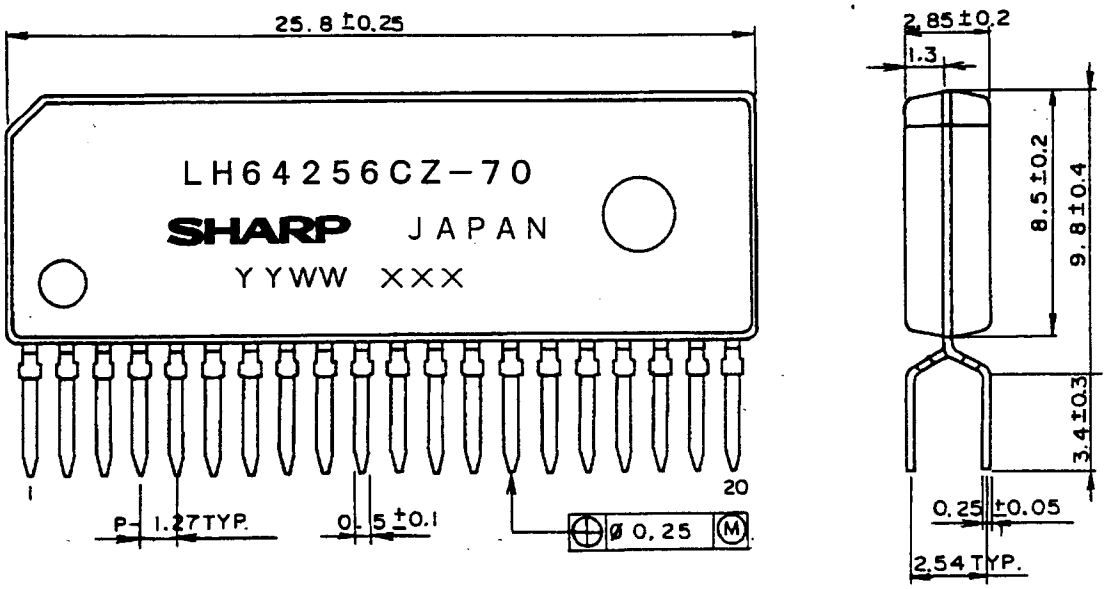
Refer to attached drawing

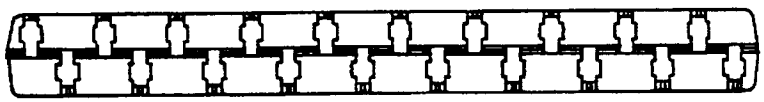
4. Precausion For Unpacking

(1) Unpacking should be done on the stand as well as human body treated with anti-ESD.

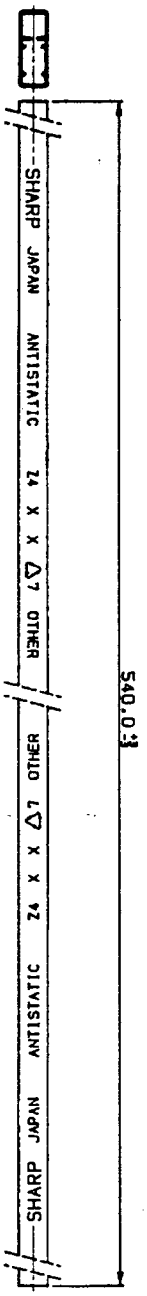
(2) Anti-ESD treatment is given to a magazine.
Use the equivalent magazine , if it is changed to another one.

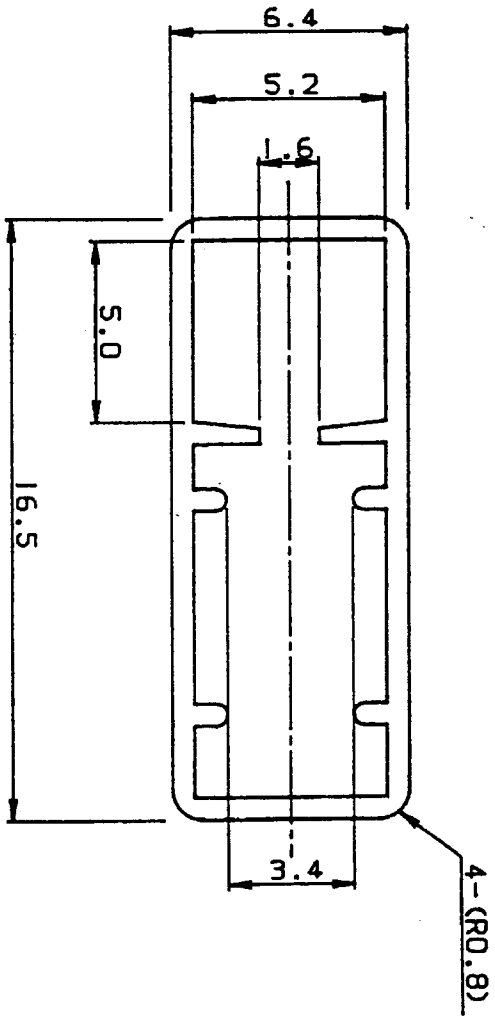
(3) Be sure to fix two stoppers to both ends of a magazine when storage to prevent the devices from slipping.





名称 NAME	ZIP20-P-400	リード仕上 LEAD FINISH	TIN-LEAD PLATING	備考 NOTE プラスチックパッケージ外形寸法は、バリを含まないものとする。 Plastic body dimensions do not include burr of resin.
DRAWING NO.	AA1009	単位 UNIT	mm	





注記 ：マガジン(スリーブ)両側のストッパーは、ゴムストッパーとする。
指示無き寸法公差は全て±０．４mmとする。

NOTES : Stopper which is set at the both ends of magazine (sleeve) is made of rubber.
All tolerances are ±0.4mm unless otherwise specified.

名称 NAME	ZIP20SPN−A2			備考 NOTE
DRAWING NO.	CV666	単位 UNIT	mm	

DRAM Dynamic RAM Random Access Memory ZIP LH64256CZ70 CMOS 1M (256K x 4)