SHARP

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To ;

PRELIMINARY

# S P E C I F I C A T I O N S

Product Type 1M SRAM

## L H 5 1 B V 1 0 0 0 H Y － 7 0 L L

Model No. ( LH51B0HY )

*This specifications contains 11 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

DATE:

BAY:

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● When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.

(1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).

- Office electronics
- Instrumentation and measuring equipment
- Machine tools
- Audiovisual equipment
- Home appliances
- Communication equipment other than for trunk lines

(2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-sale operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.

- Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
- Mainframe computers
- Traffic control systems
- Gas leak detectors and automatic cutoff devices
- Rescue and security equipment
- Other safety devices and safety equipment, etc.

(3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.

- Aerospace equipment
- Communications equipment for trunk lines
- Control equipment for the nuclear power industry
- Medical equipment related to life support, etc.

(4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

● Please direct all queries regarding the products covered herein to a sales representative of the company.

Contents



【Note】

This document contains initial characterization limits that are subject to change upon full characterization of production devices.

1. Description

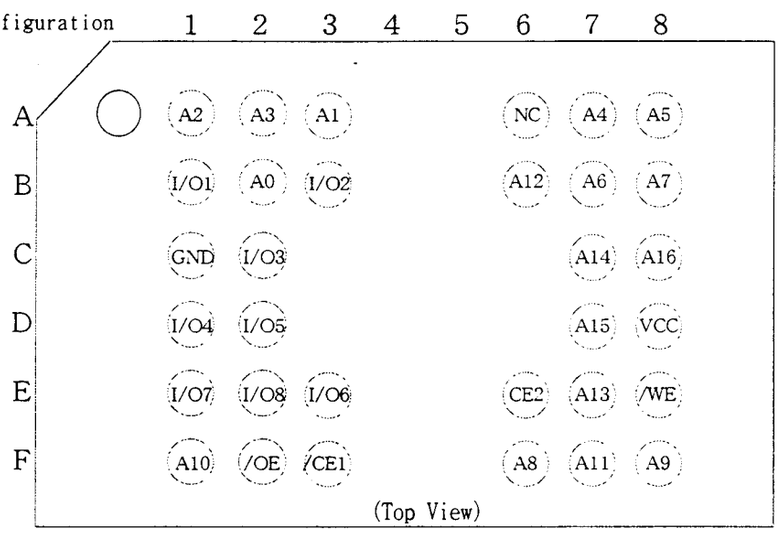
The LH51BV1000HY-70LL is a static RAM organized as 131,072×8 bit with provides low-power standby mode.
It is fabricated using silicon-gate CMOS process technology.

Features

| | | |
|---|---|---|
| ○Access Time | . . . . | 70 ns (Max.) |
| ○Operating current | . . . . | 30 mA (Max.) |
| | . . . . | 5 mA (Max. $t_{RC}$, $t_{WC}$=1 μs) |
| ○Standby current | . . . . | 60 μA (Max.) |
| ○Data retention current | . . . . | 1.0 μA (Max. $V_{CCDR}$=3V, Ta=25℃) |
| ○Single power supply | . . . . | 2.7V to 3.6V |
| ○Operating temperature | . . . . | −40℃ to +85℃ |

○Fully static operation
○Three-state output
○Not designed or rated as radiation hardened
○32 pin CSP (FBGA032-P-0610) plastic package
○P-type bulk silicon

2. Pin Configuration




(Top View)

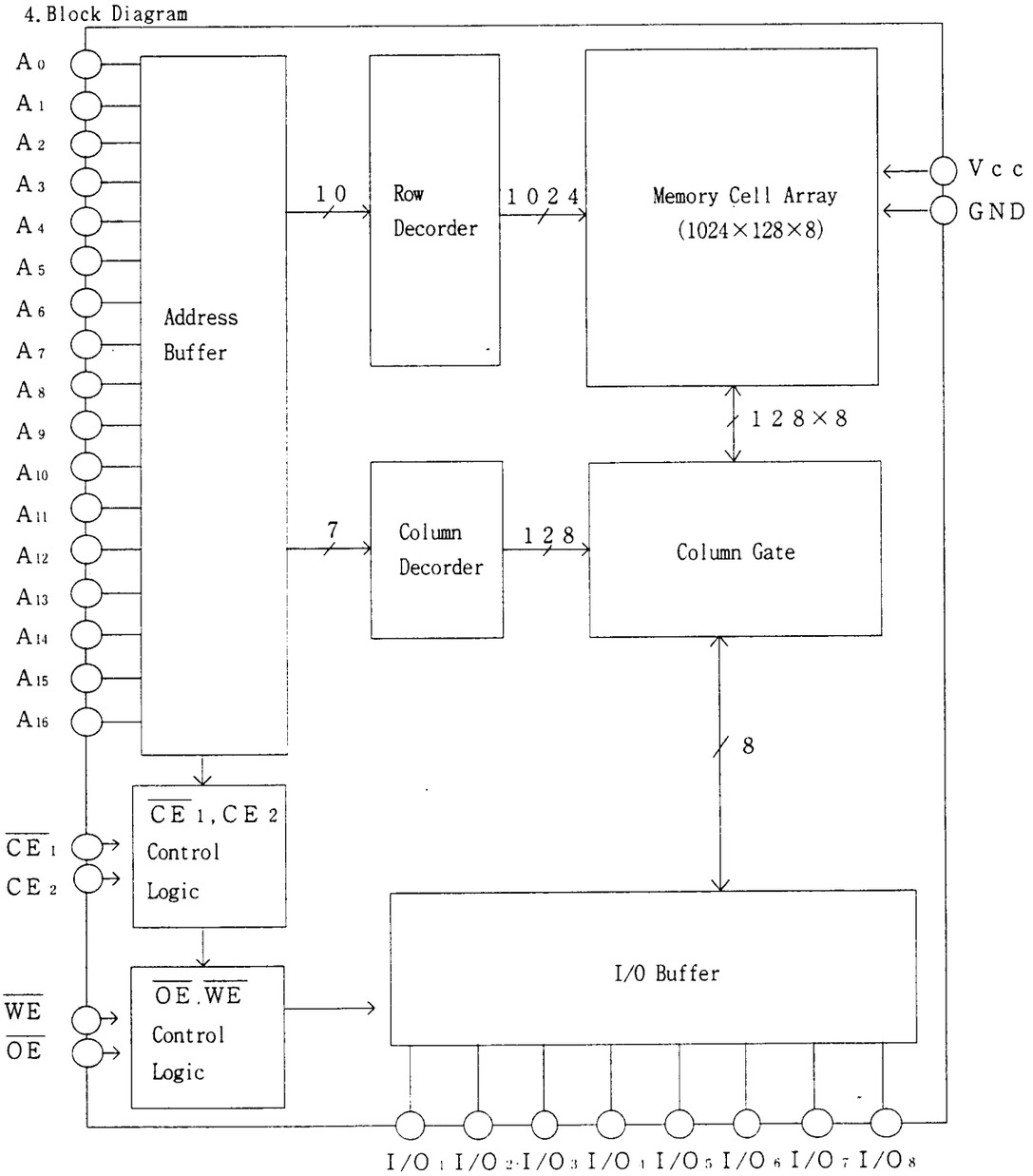
| Pin Name | Function |
|---|---|
| $A_0$ to $A_{16}$ | Address inputs |
| $\overline{CE}_1$ | Chip enable 1 |
| $CE_2$ | Chip enable 2 |
| $\overline{WE}$ | Write enable |
| $\overline{OE}$ | Output enable |
| $I/O_1$ to $I/O_8$ | Data inputs/outputs |
| $V_{CC}$ | Power supply |
| GND | Ground |
| NC | Non connection |

3. Truth Table

| $\overline{CE_1}$ | $CE_2$ | $\overline{WE}$ | $\overline{OE}$ | Mode | $I/O_1$ to $I/O_8$ | Supply current |
|---|---|---|---|---|---|---|
| H | * | * | * | Standby | High impedance | Standby ($I_{SB}$) |
| * | L | * | * | Standby | High impedance | Standby ($I_{SB}$) |
| L | H | L | * | Write | Data input | Active ($I_{CC}$) |
| L | H | H | L | Read | Data output | Active ($I_{CC}$) |
| L | H | H | H | Output disable | High impedance | Active ($I_{CC}$) |

(*=Don't Care, L=Low, H=High)

4. Block Diagram



5. Absolute Maximum Ratings

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage (*1) | $V_{CC}$ | −0.5 to +4.6 | V |
| Input voltage (*1) | $V_{IN}$ | −0.5 (*2) to $V_{CC}$+0.3 | V |
| Operating temperature | $T_{opr}$ | −40 to +85 | ℃ |
| Storage temperature | $T_{stg}$ | −65 to +150 | ℃ |

Note) *1. The maximum applicable voltage on any pin with respect to GND.
*2. Undershoot of −3.0V is allowed width of pulse bellow 50ns.

6. Recommended DC Operating Conditions

(Ta= −40 ℃ to +85℃)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 2.7 | 3.0 | 3.6 | V |
| Input voltage | $V_{IH}$ | 2.2 | | $V_{CC}$+0.3 | V |
| | $V_{IL}$ | −0.3 (*3) | | 0.4 | V |

Note) *3. Undershoot of −3.0V is allowed width of pulse below 50ns.

7. DC Electrical Characteristics

(Ta=−40 ℃ to +85℃, $V_{CC}$= 2.7 V to 3.6 V)

| Parameter | Symbol | Conditions | | Min. | Typ. (*4) | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Input leakage current | $I_{LI}$ | $V_{IN}$=0V to $V_{CC}$ | | −1.0 | | 1.0 | μA |
| Output leakage current | $I_{LO}$ | $\overline{CE_1}$=$V_{IH}$ or $CE_2$=$V_{IL}$ or $\overline{OE}$=$V_{IH}$ or $\overline{WE}$=$V_{IL}$ $V_{I/O}$=0V to $V_{CC}$ | | −1.0 | | 1.0 | μA |
| Operating supply current | $I_{CC1}$ | $\overline{CE_1}$=$V_{IL}$, $V_{IN}$=$V_{IL}$ or $V_{IH}$ $CE_2$=$V_{IH}$, $I_{I/O}$=0mA | $t_{CYCLE}$ =Min | | | 30 | mA |
| | $I_{CC2}$ | $\overline{CE_1}$=$V_{IL}$, $V_{IN}$=$V_{IL}$ or $V_{IH}$ $CE_2$=$V_{IH}$, $I_{I/O}$=0mA | $t_{CYCLE}$ =1.0μS | | | 5 | mA |
| Standby current | $I_{SB}$ | $\overline{CE_1}$, $CE_2$≧$V_{CC}$−0.2V or $CE_2$≦0.2V | | | 0.6 | 60 | μA |
| | $I_{SB1}$ | $\overline{CE_1}$=$V_{IH}$ or $CE_2$=$V_{IL}$ | | | | 1.0 | mA |
| Output voltage | $V_{OL}$ | $I_{OL}$= 2.0 mA, $V_{CC}$≧3V | | | | 0.4 | V |
| | | $I_{OL}$= 0.1 mA | | | | 0.2 | V |
| | $V_{OH}$ | $I_{OH}$=−2.0 mA, $V_{CC}$≧3V | | 2.4 | | | V |
| | | $I_{OH}$=−0.1 mA | | $V_{CC}$−0.2 | - | | V |

Note) *4. Typical values at Vcc=3.0V, Ta=25℃.

8. AC Electrical Characteristics

AC Test Conditions

| | |
|---|---|
| Input pulse level | 0.4V to 2.4V |
| Input rise and fall time | 5ns |
| Input and Output timing Ref. level | 1.5V |
| Output load | 1TTL+$C_L$ (100pF) (*5) |

Note) *5. Including scope and jig capacitance.

Read cycle (Ta=−40℃ to +85℃, Vcc= 2.7V to 3.6V)

| Parameter | Symbol | Min. | Max. | Unit | |
|---|---|---|---|---|---|
| Read cycle time | $t_{RC}$ | 70 | | ns | |
| Address access time | $t_{AA}$ | | 70 | ns | |
| $\overline{CE_1}$ access time | $t_{ACE1}$ | | 70 | ns | |
| $CE_2$ access time | $t_{ACE2}$ | | 70 | ns | |
| Output enable to output valid | $t_{OE}$ | | 40 | ns | |
| Output hold from address change | $t_{OH}$ | 10 | | ns | |
| $\overline{CE_1}$ Low to output active | $t_{LZ1}$ | 5 | | ns | *6 |
| $CE_2$ High to output active | $t_{LZ2}$ | 5 | | ns | *6 |
| $\overline{OE}$ Low to output active | $t_{OLZ}$ | 0 | | ns | *6 |
| $\overline{CE_1}$ High to output in High impedance | $t_{HZ1}$ | | 30 | ns | *6 |
| $CE_2$ Low to output in High impedance | $t_{HZ2}$ | | 30 | ns | *6 |
| $\overline{OE}$ High to output in High impedance | $t_{OHZ}$ | | 30 | ns | *6 |

Write cycle (Ta=−40℃ to +85℃, Vcc= 2.7V to 3.6V)

| Parameter | Symbol | Min. | Max. | Unit | |
|---|---|---|---|---|---|
| Write cycle time | $t_{WC}$ | 70 | | ns | |
| Chip enable to end of write | $t_{CW}$ | 60 | | ns | |
| Address valid to end of write | $t_{AW}$ | 60 | | ns | |
| Address setup time | $t_{AS}$ | 0 | | ns | |
| Write pulse width | $t_{WP}$ | 55 | | ns | |
| Write recovery time | $t_{WR}$ | 0 | | ns | |
| Input data setup time | $t_{DW}$ | 30 | | ns | |
| Input data hold time | $t_{DH}$ | 0 | | ns | |
| $\overline{WE}$ High to output active | $t_{OW}$ | 5 | | ns | *6 |
| $\overline{WE}$ Low to output in High impedance | $t_{WZ}$ | | 30 | ns | *6 |
| $\overline{OE}$ High to output in High impedance | $t_{OHZ}$ | | 30 | ns | *6 |

Note) *6. Active output to High impedance and High impedance to output active tests specified for a ±200mV transition from steady state levels into the test load.

9. Data Retention Characteristics

(Ta= −40℃ to +85℃)

| Parameter | Symbol | Conditions | | Min. | Typ. (*7) | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Data Retention supply voltage | $V_{CCDR}$ | $CE_2 \leqq 0.2V$ or $\overline{CE_1} \geqq V_{CCDR}-0.2V$ (*8) | | 2.0 | | 3.6 | V |
| Data Retention supply current | $I_{CCDR}$ | $V_{CCDR}=3V$ | Ta=25℃ | | 0.5 | 1.0 | μA |
| | | $CE_2 \leqq 0.2$ or | Ta=40℃ | | | 3.0 | μA |
| | | $\overline{CE_1} \geqq V_{CCDR}-0.2V$ (*8) | | | | 50 | μA |
| Chip enable setup time | $t_{CDR}$ | | | 0 | | | ms |
| Chip enable hold time | $t_R$ | | | 5 | | | ms |

Note) *7. Typical values at Ta=25℃.

*8. $CE_2 \geqq V_{CCDR}-0.2V$ or $CE_2 \leqq 0.2V$

10. Pin Capacitance

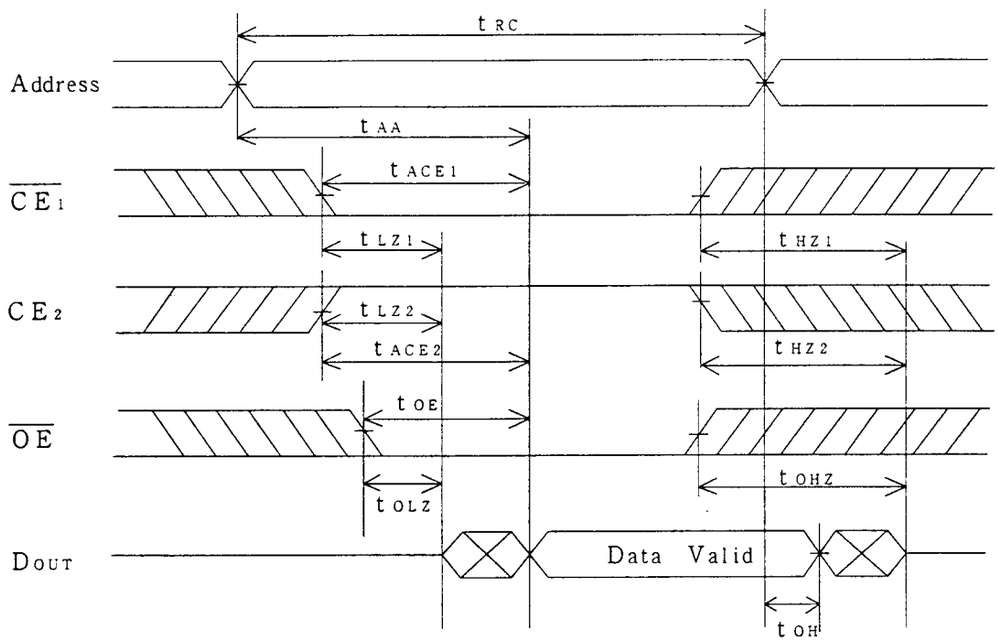
(Ta=25℃, f=1MHz)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit | |
|---|---|---|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | $V_{IN}=0V$ | | | 8 | pF | *9 |
| I/O capacitance | $C_{I/O}$ | $V_{I/O}=0V$ | | | 10 | pF | *9 |

Note) *9. This parameter is sampled and not production tested.

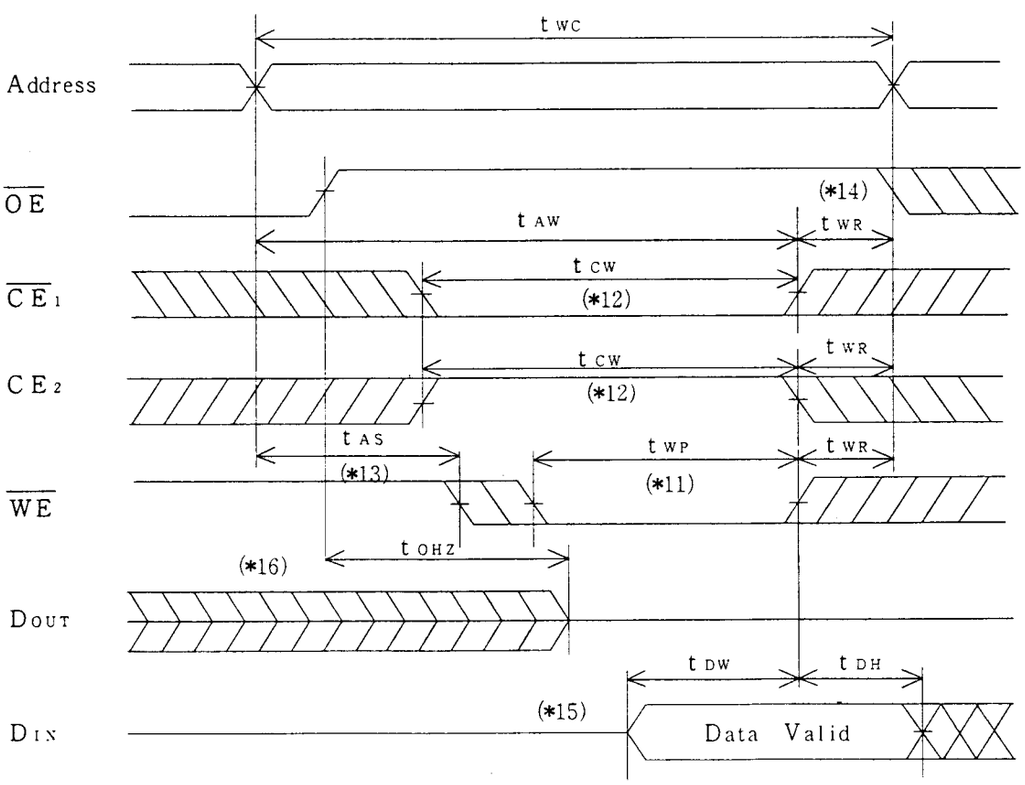
11. Timing Chart

Read cycle timing chart – (*10)

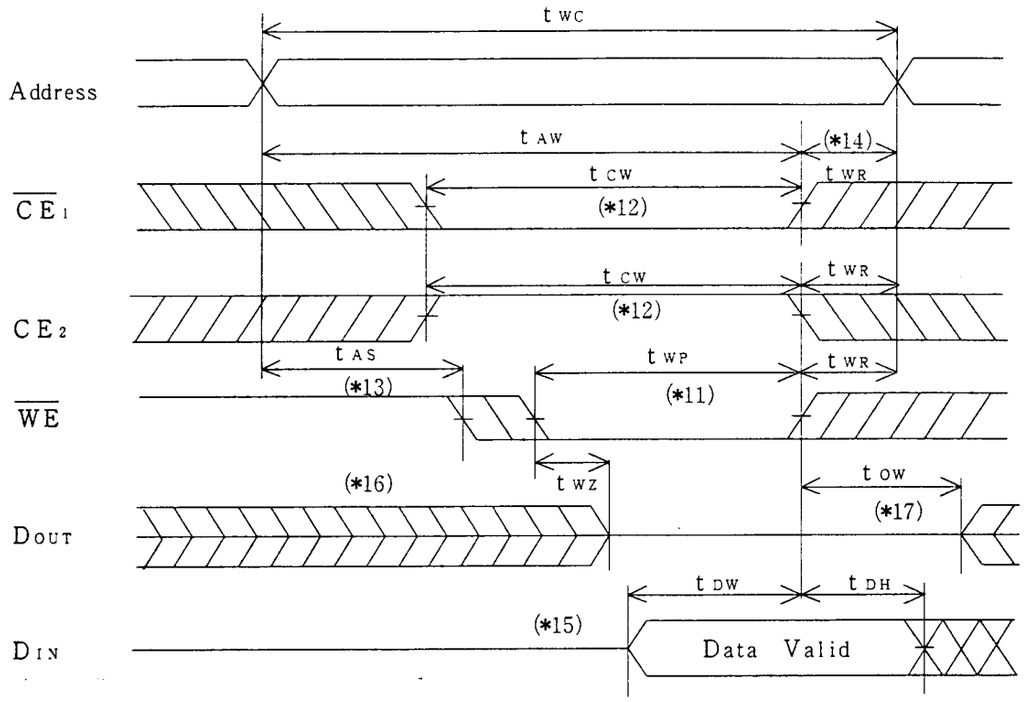



Note) *10. $\overline{WE}$ is high for Read cycle.

Write cycle timing chart – ($\overline{OE}$ Controlled)



Write cycle timing chart — ($\overline{OE}$ Low fixed)




Note) * 11. A write occurs during the overlap of a low $\overline{CE_1}$, a high $CE_2$ and a low $\overline{WE}$.
A write begins at the latest transition among $\overline{CE_1}$ going low, $CE_2$ going high and $\overline{WE}$ going low.
A write ends at the earliest transition among $\overline{CE_1}$ going high, $CE_2$ going low and $\overline{WE}$ going high. $t_{WP}$ is measured from the beginning of write to the end of write.

* 12. $t_{CW}$ is measured from the later of $\overline{CE_1}$ going low or $CE_2$ going high to the end of write.

* 13. $t_{AS}$ is measured from the address valid to the beginning of write.

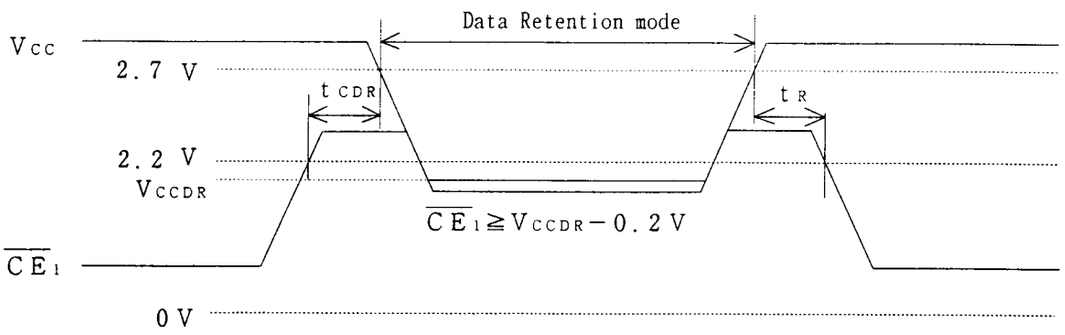
* 14. $t_{WR}$ is measured from the end of write to the address change. $t_{WR1}$ applies in case a write ends at $\overline{CE_1}$ or $\overline{WE}$ going high. $t_{WR2}$ applies in case a write ends at $CE_2$ going low.

* 15. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.

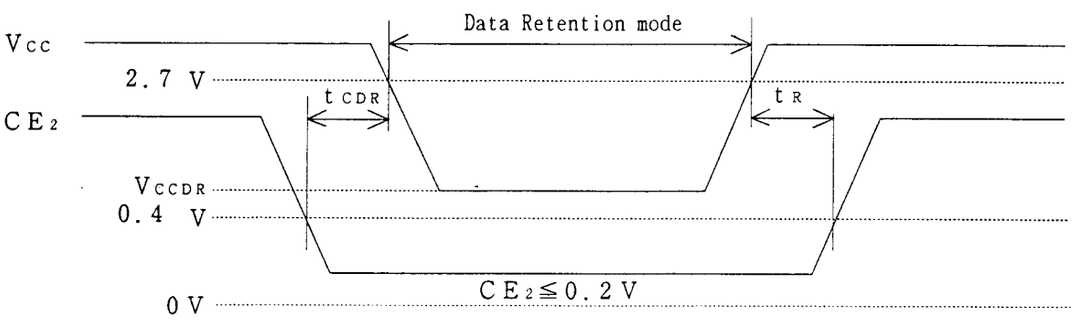
* 16. If $\overline{CE_1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.

* 17. If $\overline{CE_1}$ goes high simultaneously with $\overline{WE}$ going high or before $\overline{WE}$ going high, the outputs remain in high impedance state.

Data Retention timing chart－ ($\overline{CE_1}$ Controlled) (＊18)




Data Retention timing chart－ ($CE_2$ Controlled)




Note) ＊18. To control the data retention mode at $\overline{CE_1}$, fix the input level of $CE_2$ between $V_{CCDR}$ and $V_{CCDR}-0.2V$ or 0V and 0.2V during the data retention mode.

STATIC SRAM RAM Random Access Memory Low Power CSP