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To ;

SPECIFICATIONS

Product Type 8Mbit Flash Memory

LH28F800BGHE-TL85

Model No. (LHF80B25)

※This specifications contains 49 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

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DATE:

BY:

PRESENTED

BY:

T. MIMOTO
Dept. General Manager

SHARP CORPORATION
11. 4'97.
MAIL DATE
IC TENRI GROUP

REVIEWED BY:

PREPARED BY:

T. Akamatsu

Flash Dept. 1
Memory Engineering Center
Tenri Integrated Circuits Group
SHARP CORPORATION

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LH28F800BGHE-TL85
8M-BIT (512KB x 16)
SmartVoltage Flash MEMORY

- **SmartVoltage Technology**
  - 2.7V, 3.3V or 5V V_{CC}
  - 2.7V, 3.3V, 5V or 12V V_{PP}
- **High-Performance Access Time**
  - 85ns(5V±0.25V), 90ns(5V±0.5V), 100ns(3.3V±0.3V), 120ns(2.7V-3.6V)
- **Enhanced Data Protection Features**
  - Absolute Protection with V_{PP}=GND
  - Block Erase/Word Write Lockout during Power Transitions
  - Boot Blocks Protection with WP#=V_{IL}
- **Optimized Array Blocking Architecture**
  - Two 4k-word Boot Blocks
  - Six 4k-word Parameter Blocks
  - Fifteen 32k-word Main Blocks
  - Top Boot Location
- **Automated Word Write and Block Erase**
  - Command User Interface
  - Status Register
- **Extended Cycling Capability**
  - 100,000 Block Erase Cycles
- **Enhanced Automated Suspend Options**
  - Word Write Suspend to Read
  - Block Erase Suspend to Word Write
  - Block Erase Suspend to Read
- **Low Power Management**
  - Deep Power-Down Mode
  - Automatic Power Savings Mode Decreases I_{CC} in Static Mode
- **Industry-Standard Packaging**
  - 48-Lead TSOP
- **SRAM-Compatible Write Interface**
- **ETOX™* V Nonvolatile Flash Technology**
- **Not designed or rated as radiation hardened**

SHARP's LH28F800BGHE-TL85 Flash memory with SmartVoltage technology is a high-density, low-cost, nonvolatile, read/write storage solution for a wide range of applications. LH28F800BGHE-TL85 can operate at V_{CC}=2.7V and V_{PP}=2.7V. Its low voltage operation capability realize battery life and suits for cellular phone application.

Its Boot, Parameter and Main-blocked architecture, flexible voltage and extended cycling provide for highly flexible component suitable for portable terminals and personal computers. Its enhanced suspend capabilities provide for an ideal solution for code + data storage applications. For secure code storage applications, such as networking, where code is either directly executed out of flash or downloaded to DRAM, the LH28F800BGHE-TL85 offers two levels of protection: absolute protection with V_{PP} at GND, selective hardware boot block locking. These alternatives give designers ultimate control of their code security needs.

The LH28F800BGHE-TL85 is manufactured on SHARP's 0.4μm ETOX™ V process technology. It come in industry-standard package: the 48-lead TSOP ideal for board constrained applications.

*ETOX is a trademark of Intel Corporation.

1 INTRODUCTION

This datasheet contains LH28F800BGHE-TL85 specifications. Section 1 provides a flash memory overview. Sections 2, 3, 4 and 5 describe the memory organization and functionality. Section 6 covers electrical specifications.

1.1 New Features

Key enhancements of LH28F800BGHE-TL85 SmartVoltage Flash memory are:

- •SmartVoltage Technology
- •Enhanced Suspend Capabilities
- •Boot Block Architecture

Please note following important differences:

- •V_{PPLK} has been lowered to 1.5V to support 2.7V, 3.3V and 5V block erase and word write operations. Designs that switch V_{PP} off during read operations should make sure that the V_{PP} voltage transitions to GND.
- •To take advantage of SmartVoltage technology, allow V_{PP} connection to 2.7V, 3.3V or 5V.

1.2 Product Overview

The LH28F800BGHE-TL85 is a high-performance 8-Mbit SmartVoltage Flash memory organized as 512K-word of 16 bits. The 512K-word of data is arranged in two 4K-word boot blocks, six 4K-word parameter blocks and fifteen 32K-word main blocks which are individually erasable in-system. The memory map is shown in Figure 3.

SmartVoltage technology provides a choice of V_{CC} and V_{PP} combinations, as shown in Table 1, to meet system performance and power expectations. 2.7V V_{CC} consumes approximately one-fifth the power of 5V V_{CC}. But, 5V V_{CC} provides the highest read performance. V_{PP} at 2.7, 3.3V and 5V eliminates the need for a separate 12V converter, while V_{PP}=12V maximizes block erase and word write performance. In addition to flexible erase and program voltages, the dedicated V_{PP} pin gives complete data protection when $V_{PP} \leq V_{PPLK}$.

Table 1. V_{CC} and V_{PP} Voltage Combinations Offered by SmartVoltage Technology

V_{CC} Voltage	V_{PP} Voltage
2.7V	2.7V, 3.3V, 5V, 12V
3.3V	3.3V, 5V, 12V
5V	5V, 12V

Internal V_{CC} and V_{PP} detection Circuitry automatically configures the device for optimized read and write operations.

A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase and word write operations.

A block erase operation erases one of the device's 32K-word blocks typically within 0.39s (5V V_{CC}, 12V V_{PP}), 4K-word blocks typically within 0.25s (5V V_{CC}, 12V V_{PP}) independent of other blocks. Each block can be independently erased 100,000 times. Block erase suspend mode allows system software to suspend block erase to read or write data from any other block.

Writing memory data is performed in word increments of the device's 32K-word blocks typically within 8.4µs (5V V_{CC}, 12V V_{PP}), 4K-word blocks typically within 17µs (5V V_{CC}, 12V V_{PP}). Word write suspend mode enables the system to read data or execute code from any other flash memory array location.

The boot blocks can be locked for the WP# pin. Block erase or word write for boot block must not be carried out by WP# to Low and RP# to V_{IH}.

The status register indicates when the WSM's block erase or word write operation is finished.

The RY/BY# output gives an additional indicator of WSM activity by providing both a hardware signal of status (versus software polling) and status masking (interrupt masking for background block erase, for example). Status polling using RY/BY# minimizes both CPU overhead and system power consumption. When low, RY/BY# indicates that the WSM is performing a block erase or word write. RY/BY#-high indicates that the WSM is ready for a new command, block erase is suspended (and word write is inactive), word write is suspended, or the device is in deep power-down mode.

The access time is 85 ns (t_{AVQV}) over the commercial temperature range (-40°C to +85°C) and V_{CC} supply voltage range of 4.75V-5.25V. At lower V_{CC} voltages, the access times are 90 ns (4.5V-5.5V), 100 ns (3.0V-3.6V) and 120 ns (2.7V-3.6V).

The Automatic Power Savings (APS) feature substantially reduces active current when the device is in static mode (addresses not switching). In APS mode, the typical I_{CCR} current is 1 mA at 5V V_{CC}.

When CE# and RP# pins are at V_{CC}, the I_{CC} CMOS standby mode is enabled. When the RP# pin is at GND, deep power-down mode is enabled which minimizes power consumption and provides write protection during reset. A reset time (t_{PHQV}) is required from RP# switching high until outputs are valid. Likewise, the device has a wake time (t_{PHEL}) from RP#-high until writes to the CUI are recognized. With RP# at GND, the WSM is reset and the status register is cleared.

The device is available in 48-lead TSOP (Thin Small Outline Package, 1.2 mm thick). Pinout is shown in Figure 2.

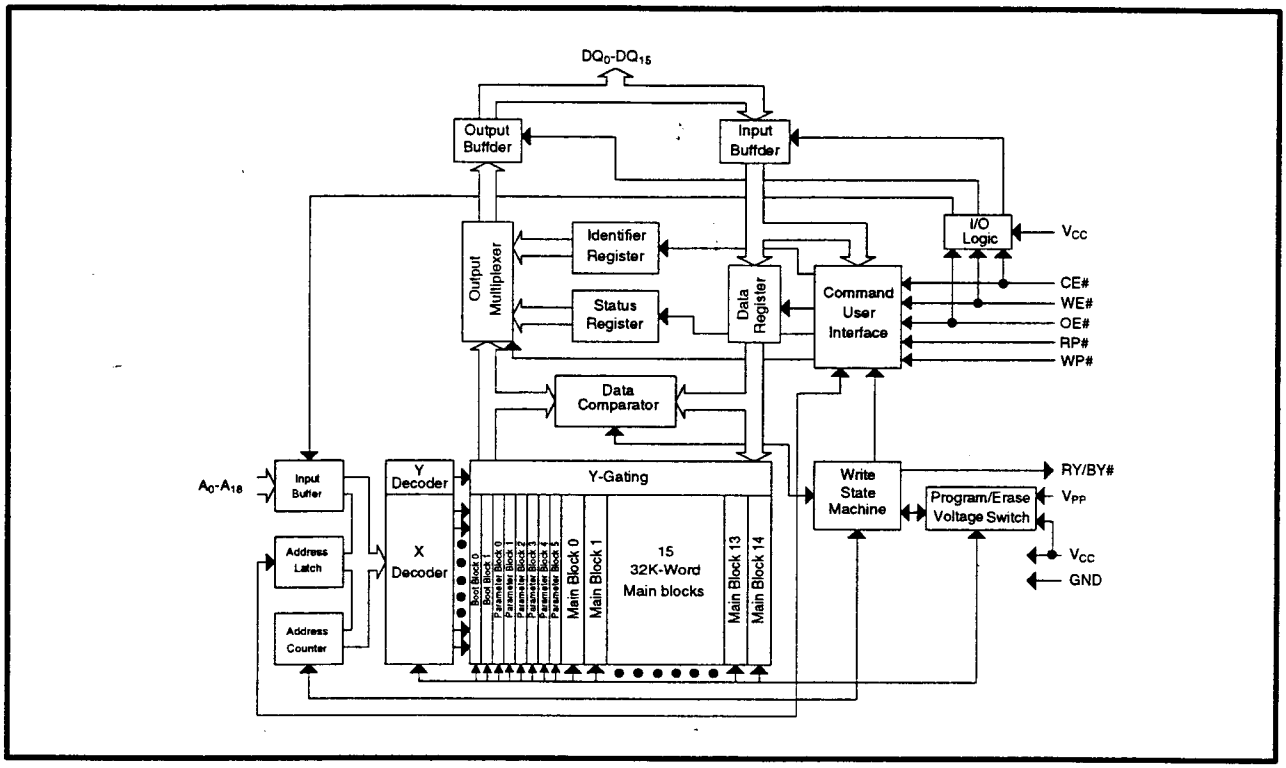


Figure 1. Block Diagram

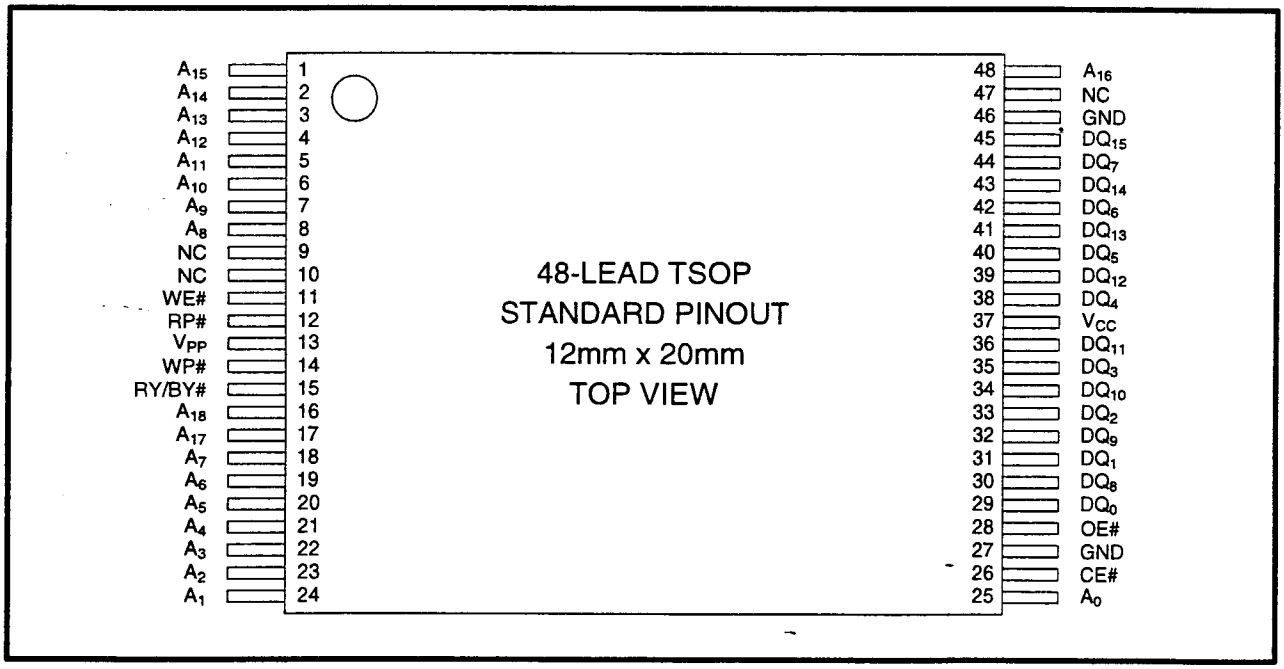


Figure 2. TSOP 48-Lead Pinout

Table 2. Pin Descriptions

Symbol	Type	Name and Function
A_0-A_{18}	INPUT	**ADDRESS INPUTS:** Inputs for addresses during read and write operations. Addresses are internally latched during a write cycle.
DQ_0-DQ_{15}	INPUT/ OUTPUT	**DATA INPUT/OUTPUTS:** Inputs data and commands during CUI write cycles; outputs data during memory array, status register and identifier code read cycles. Data pins float to high-impedance when the chip is deselected or outputs are disabled. Data is internally latched during a write cycle.
CE#	INPUT	**CHIP ENABLE:** Activates the device's control logic, input buffers, decoders and sense amplifiers. CE#-high deselects the device and reduces power consumption to standby levels.
RP#	INPUT	**RESET/DEEP POWER-DOWN:** Puts the device in deep power-down mode and resets internal automation. RP#-high enables normal operation. When driven low, RP# inhibits write operations which provides data protection during power transitions. Exit from deep power-down sets the device to read array mode. With RP#=V_{HH}, block erase or word write can operate to all blocks without WP# state. Block erase or word write with V_{IH}<RP#<V_{HH} produce spurious results and should not be attempted.
OE#	INPUT	**OUTPUT ENABLE:** Gates the device's outputs during a read cycle.
WE#	INPUT	**WRITE ENABLE:** Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of the WE# pulse.
WP#	INPUT	**WRITE PROTECT:** Master control for boot blocks locking. When V_{IL}, locked boot blocks cannot be erased and programmed.
RY/BY#	OUTPUT	**READY/BUSY#:** Indicates the status of the internal WSM. When low, the WSM is performing an internal operation (block erase or word write). RY/BY#-high indicates that the WSM is ready for new commands, block erase is suspended, and word write is inactive, word write is suspended, or the device is in deep power-down mode. RY/BY# is always active and does not float when the chip is deselected or data outputs are disabled.
V_{PP}	SUPPLY	**BLOCK ERASE AND WORD WRITE POWER SUPPLY:** For erasing array blocks or writing words. With $V_{PP} \leq V_{PPLK}$, memory contents cannot be altered. Block erase and word write with an invalid V_{PP} (see DC Characteristics) produce spurious results and should not be attempted.
V_{CC}	SUPPLY	**DEVICE POWER SUPPLY:** Internal detection configures the device for 2.7V, 3.3V or 5V operation. To switch from one voltage to another, ramp V_{CC} down to GND and then ramp V_{CC} to the new voltage. Do not float any power pins. With $V_{CC} \leq V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid V_{CC} voltage (see DC Characteristics) produce spurious results and should not be attempted.
GND	SUPPLY	**GROUND:** Do not float any ground pins.
NC		**NO CONNECT:** Lead is not internal connected; it may be driven or floated.

2 PRINCIPLES OF OPERATION

The LH28F800BGHE-TL85 SmartVoltage Flash memory includes an on-chip WSM to manage block erase and word write functions. It allows for: 100% TTL-level control inputs, fixed power supplies during block erasure and word write, and minimal processor overhead with RAM-like interface timings.

After initial device power-up or return from deep power-down mode (see Bus Operations), the device defaults to read array mode. Manipulation of external memory control pins allow array read, standby and output disable operations.

Status register and identifier codes can be accessed through the CUI independent of the V_{PP} voltage. High voltage on V_{PP} enables successful block erasure and word writing. All functions associated with altering memory contents–block erase, word write, status and identifier codes–are accessed via the CUI and verified through the status register.

Commands are written using standard microprocessor write timings. The CUI contents serve as input to the WSM, which controls the block erase and word write. The internal algorithms are regulated by the WSM, including pulse repetition, internal verification and margining of data. Addresses and data are internally latch during write cycles. Writing the appropriate command outputs array data, accesses the identifier codes or outputs status register data.

Interface software that initiates and polls progress of block erase and word write can be stored in any block. This code is copied to and executed from system RAM during flash memory updates. After successful completion, reads are again possible via the Read Array command. Block erase suspend allows system software to suspend a block erase to read/write data from/to blocks other than that which is suspend. Word write suspend allows system software to suspend a word write to read data from any other flash memory array location.

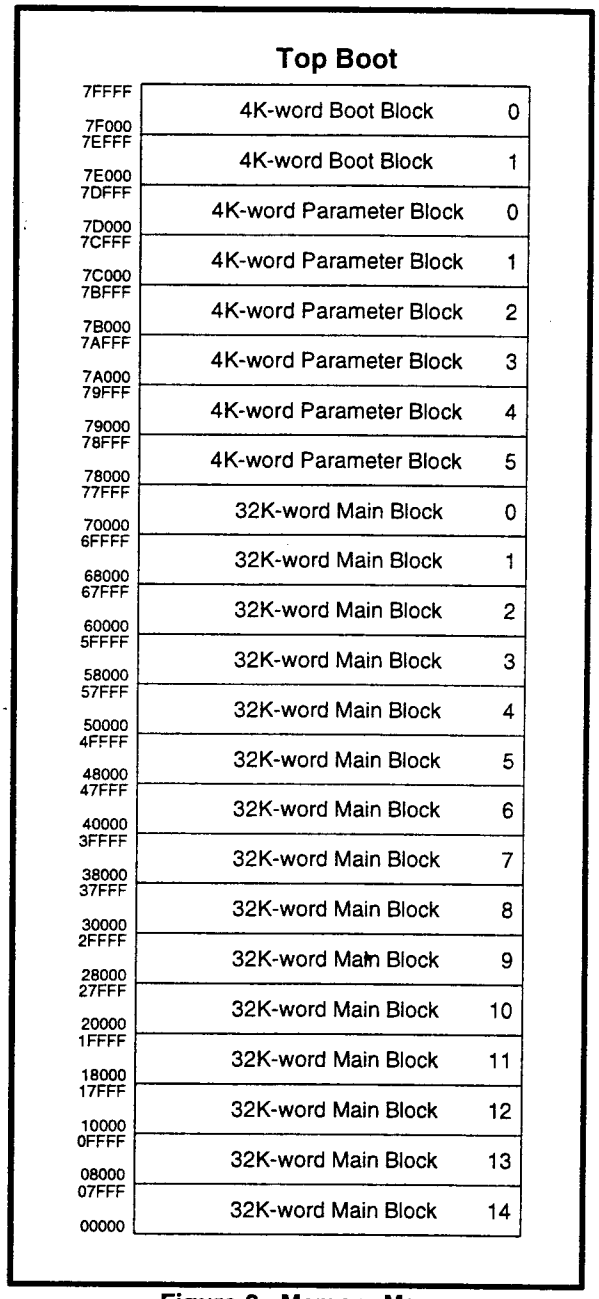


Figure 3. Memory Map

2.1 Data Protection

Depending on the application, the system designer may choose to make the V_{PP} power supply switchable (available only when memory block erases or word writes are required) or hardwired to $V_{PPH1/2/3}$. The device accommodates either design practice and encourages optimization of the processor-memory interface.

When $V_{PP} \leq V_{PPLK}$, memory contents cannot be altered. The CUI, with two-step block erase or word write command sequences, provides protection from unwanted operations even when high voltage is applied to V_{PP}. All write functions are disabled when V_{CC} is below the write lockout voltage V_{LKO} or when RP# is at V_{IL}. The device's boot blocks locking capability for WP# provides additional protection from inadvertent code or data alteration by block erase and word write operations.

3 BUS OPERATION

The local CPU reads and writes flash memory in-system. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

3.1 Read

Information can be read from any block, identifier codes or status register independent of the V_{PP} voltage. RP# can be at either V_{IH} or V_{HH}.

The first task is to write the appropriate read mode command (Read Array, Read Identifier Codes or Read Status Register) to the CUI. Upon initial device power-up or after exit from deep power-down mode, the device automatically resets to read array mode. Five control pins dictate the data flow in and out of the component: CE#, OE#, WE#, RP# and WP#. CE# and OE# must be driven active to obtain data at the outputs. CE# is the device selection control, and when active enables the selected memory device. OE# is the data output (DQ_0-DQ_{15}) control and when active drives the selected memory data onto the I/O bus. WE# must be at V_{IH} and RP# must be at V_{IH} or V_{HH}. Figure 13 illustrates read cycle.

3.2 Output Disable

With OE# at a logic-high level (V_{IH}), the device outputs are disabled. Output pins (DQ_0-DQ_{15}) are placed in a high-impedance state.

3.3 Standby

CE# at a logic-high level (V_{IH}) places the device in standby mode which substantially reduces device power consumption. DQ_0-DQ_{15} outputs are placed in a high-impedance state independent of OE#. If deselected during block erase or word write, the device continues functioning, and consuming active power until the operation completes.

3.4 Deep Power-Down

RP# at V_{IL} initiates the deep power-down mode.

In read modes, RP#-low deselects the memory, places output drivers in a high-impedance state and turns off all internal circuits. RP# must be held low for a minimum of 100 ns. Time t_{PHQV} is required after return from power-down until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI is reset to read array mode and status register is set to 80H.

During block erase or word write modes, RP#-low will abort the operation. RY/BY# remains low until the reset operation is complete. Memory contents being altered are no longer valid; the data may be partially erased or written. Time t_{PHWL} is required after RP# goes to logic-high (V_{IH}) before another command can be written.

As with any automated device, it is important to assert RP# during system reset. When the system comes out of reset, it expects to read from the flash memory. Automated flash memories provide status information when accessed during block erase or word write modes. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. SHARP's flash memories allow proper CPU initialization following a system reset through the use of the RP# input. In this application, RP# is controlled by the same RESET# signal that resets the system CPU.

3.5 Read Identifier Codes Operation

The read identifier codes operation outputs the manufacturer code and device code (see Figure 4). Using the manufacturer and device codes, the system CPU can automatically match the device with its proper algorithms.

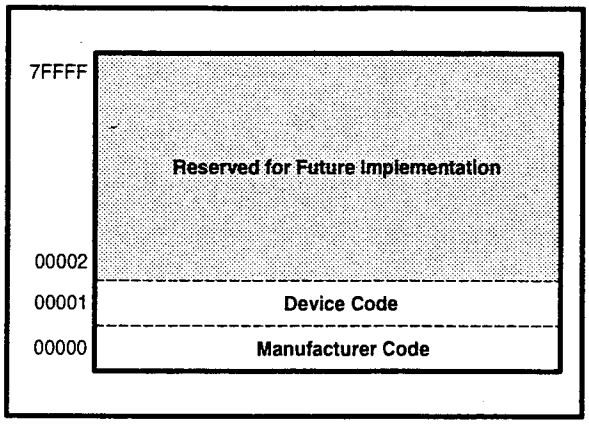


Figure 4. Device Identifier Code Memory Map

3.6 Write

Writing commands to the CUI enable reading of device data and identifier codes. They also control inspection and clearing of the status register. When $V_{CC}=V_{CC1/2/3/4}$ and $V_{PP}=V_{PPH1/2/3}$, the CUI additionally controls block erasure and word write.

The Block Erase command requires appropriate command data and an address within the block to be erased. The Word Write command requires the command and address of the location to be written.

The CUI does not occupy an addressable memory location. It is written when WE# and CE# are active. The address and data needed to execute a command are latched on the rising edge of WE# or CE# (whichever goes high first). Standard microprocessor write timings are used. Figures 14 and 15 illustrate WE# and CE# controlled write operations.

4 COMMAND DEFINITIONS

When the V_{PP} voltage $\leq V_{PPLK}$, Read operations from the status register, identifier codes, or blocks are enabled. Placing $V_{PPH1/2/3}$ on V_{PP} enables successful block erase and word write operations.

Device operations are selected by writing specific commands into the CUI. Table 4 defines these commands.

Table 3. Bus Operations

Mode	Notes	RP#	CE#	OE#	WE#	Address	V_{PP}	DQ_{0-15}	RY/BY#
Read	1,2,3,8	V_{IH} or V_{HH}	V_{IL}	V_{IL}	V_{IH}	X	X	D_{OUT}	X
Output Disable	3	V_{IH} or V_{HH}	V_{IL}	V_{IH}	V_{IH}	X	X	High Z	X
Standby	3	V_{IH} or V_{HH}	V_{IH}	X	X	X	X	High Z	X
Deep Power-Down	4	V_{IL}	X	X	X	X	X	High Z	V_{OH}
Read Identifier Codes	8	V_{IH} or V_{HH}	V_{IL}	V_{IL}	V_{IH}	See Figure 4	X	Note 5	V_{OH}
Write	3,6,7,8	V_{IH} or V_{HH}	V_{IL}	V_{IH}	V_{IL}	X	X	D_{IN}	X

NOTES:

1. Refer to DC Characteristics. When $V_{PP} \leq V_{PPLK}$, memory contents can be read, but not altered.
2. X can be V_{IL} or V_{IH} for control pins and addresses, and V_{PPLK} or $V_{PPH1/2/3}$ for V_{PP}. See DC Characteristics for V_{PPLK} and $V_{PPH1/2/3}$ voltages.
3. RY/BY# is V_{OL} when the WSM is executing internal block erase or word write algorithms. It is V_{OH} during when the WSM is not busy, in block erase suspend mode (with word write inactive), word write suspend mode or deep power-down mode.
4. RP# at GND±0.2V ensures the lowest deep power-down current.
5. See Section 4.2 for read identifier code data.
6. Command writes involving block erase or word write are reliably executed when $V_{PP}=V_{PPH1/2/3}$ and $V_{CC}=V_{CC1/2/3/4}$. Block erase or word write with $V_{IH}<RP\#<V_{HH}$ produce spurious results and should not be attempted.
7. Refer to Table 4 for valid D_{IN} during a write operation.
8. Never hold OE# low and WE# low at the same timing.

Table 4. Command Definitions[7]

Command	Bus Cycles Req'd.	Notes	First Bus Cycle			Second Bus Cycle		
			Oper[1]	Addr[2]	Data[3]	Oper[1]	Addr[2]	Data[3]
Read Array/Reset	1		Write	X	FFH			
Read Identifier Codes	≥2	4	Write	X	90H	Read	IA	ID
Read Status Register	2		Write	X	70H	Read	X	SRD
Clear Status Register	1		Write	X	50H			
Block Erase	2	5	Write	BA	20H	Write	BA	D0H
Word Write	2	5,6	Write	WA	40H or 10H	Write	WA	WD
Block Erase and Word Write Suspend	1	5	Write	X	B0H			
Block Erase and Word Write Resume	1	5	Write	X	D0H			

NOTES:

1. BUS operations are defined in Table 3.
2. X=Any valid address within the device.
   IA=Identifier Code Address: see Figure 4.
   BA=Address within the block being erased.
   WA=Address of memory location to be written.
3. SRD=Data read from status register. See Table 7 for a description of the status register bits.
   WD=Data to be written at location WA. Data is latched on the rising edge of WE# or CE# (whichever goes high first).
   ID=Data read from identifier codes.
4. Following the Read Identifier Codes command, read operations access manufacturer and device codes. See Section 4.2 for read identifier code data.
5. If the block is boot block, WP# must be at V_{IH} or RP# must be at V_{HH} to enable block erase or word write operations. Attempts to issue a block erase or word write to a boot block while WP# is V_{IH} or RP# is V_{IH}.
6. Either 40H or 10H are recognized by the WSM as the word write setup.
7. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

4.1 Read Array Command

Upon initial device power-up and after exit from deep power-down mode, the device defaults to read array mode. This operation is also initiated by writing the Read Array command. The device remains enabled for reads until another command is written. Once the internal WSM has started a block erase or word write, the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via an Erase Suspend or Word Write Suspend command. The Read Array command functions independently of the V_{PP} voltage and RP# can be V_{IH} or V_{HH}.

4.2 Read Identifier Codes Command

The identifier code operation is initiated by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in Figure 4 retrieve the manufacturer and device codes (see Table 5 for identifier code values). To terminate the operation, write another valid command. Like the Read Array command, the Read Identifier Codes command functions independently of the V_{PP} voltage and RP# can be V_{IH} or V_{HH}. Following the Read Identifier Codes command, the following information can be read:

Table 5. Identifier Codes

Code	Address	Data
Manufacture Code	00000H	00B0H
Device Code	00001H	0060H

4.3 Read Status Register Command

The status register may be read to determine when a block erase or word write is complete and whether the operation completed successfully. It may be read at any time by writing the Read Status Register command. After writing this command, all subsequent read operations output data from the status register until another valid command is written. The status register contents are latched on the falling edge of OE# or CE#, whichever occurs. OE# or CE# must toggle to V_{IH} before further reads to update the status register latch. The Read Status Register command functions independently of the V_{PP} voltage. RP# can be V_{IH} or V_{HH}.

4.4 Clear Status Register Command

Status register bits SR.5, SR.4, SR.3 or SR.1 are set to "1"s by the WSM and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see Table 7). By allowing system software to reset these bits, several operations (such as cumulatively erasing multiple blocks or writing several words in sequence) may be performed. The status register may be polled to determine if an error occurred during the sequence.

To clear the status register, the Clear Status Register command (50H) is written. It functions independently of the applied V_{PP} Voltage. RP# can be V_{IH} or V_{HH}. This command is not functional during block erase or word write suspend modes.

4.5 Block Erase Command

Erase is executed one block at a time and initiated by a two-cycle command. A block erase setup is first written, followed by an block erase confirm. This command sequence requires appropriate sequencing and an address within the block to be erased (erase changes all block data to FFFFH). Block preconditioning, erase, and verify are handled internally by the WSM (invisible to the system). After the two-cycle block erase sequence is written, the device automatically outputs status register data when read (see Figure 5). The CPU can detect block erase completion by analyzing the output data of the RY/BY# pin or status register bit SR.7.

When the block erase is complete, status register bit SR.5 should be checked. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1". Also, reliable block erasure can only occur when $V_{CC}=V_{CC1/2/3/4}$ and $V_{PP}=V_{PPH1/2/3}$. In the absence of this high voltage, block contents are protected against erasure. If block erase is attempted while $V_{PP}\leq V_{PPLK}$, SR.3 and SR.5 will be set to "1". Successful block erase for boot blocks requires that the corresponding if set, that WP#=V_{IH} or RP#=V_{HH}. If block erase is attempted to boot block when the corresponding WP#=V_{IL} or RP#=V_{IH}, SR.1 and SR.5 will be set to "1". Block erase operations with $V_{IH}<RP\#<V_{HH}$ produce spurious results and should not be attempted.

4.6 Word Write Command

Word write is executed by a two-cycle command sequence. Word write setup (standard 40H or alternate 10H) is written, followed by a second write that specifies the address and data (latched on the rising edge of WE#). The WSM then takes over, controlling the word write and write verify algorithms internally. After the word write sequence is written, the device automatically outputs status register data when read (see Figure 6). The CPU can detect the completion of the word write event by analyzing the RY/BY# pin or status register bit SR.7.

When word write is complete, status register bit SR.4 should be checked. If word write error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully write to "0"s. The CUI remains in read status register mode until it receives another command.

Reliable word writes can only occur when $V_{CC}=V_{CC1/2/3/4}$ and $V_{PP}=V_{PPH1/2/3}$. In the absence of this high voltage, memory contents are protected against word writes. If word write is attempted while $V_{PP}\leq V_{PPLK}$, status register bits SR.3 and SR.4 will be set to "1". Successful word write for boot blocks requires that the corresponding if set, that WP#=V_{IH} or RP#=V_{HH}. If word write is attempted to boot block when the corresponding WP#=V_{IL} or RP#=V_{IH}, SR.1 and SR.4 will be set to "1". Word write operations with $V_{IH}<RP\#<V_{HH}$ produce spurious results and should not be attempted.

4.7 Block Erase Suspend Command

The Block Erase Suspend command allows block-erase interruption to read or word-write data in another block of memory. Once the block-erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. The device outputs status register data when read after the Block Erase Suspend command is written. Polling status register bits SR.7 and SR.6 can determine when the block erase operation has been suspended (both will be set to "1"). RY/BY# will also transition to V_{OH}. Specification t_{WHRH2} defines the block erase suspend latency.

At this point, a Read Array command can be written to read data from blocks other than that which is suspended. A Word Write command sequence can also be issued during erase suspend to program data in other blocks. Using the Word Write Suspend command (see Section 4.8), a word write operation can also be suspended. During a word write operation with block erase suspended, status register bit SR.7 will return to "0" and the RY/BY# output will transition to V_{OL}. However, SR.6 will remain "1" to indicate block erase suspend status.

The only other valid commands while block erase is suspended are Read Status Register and Block Erase Resume. After a Block Erase Resume command is written to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and RY/BY# will return to V_{OL}. After the Erase Resume command is written, the device automatically outputs status register data when read (see Figure 7). V_{PP} must remain at $V_{PPH1/2/3}$ (the same V_{PP} level used for block erase) while block erase is suspended. RP# must also remain at V_{IH} or V_{HH} (the same RP# level used for block erase). WP# must also remain at V_{IL} or V_{IH} (the same WP# level used for block erase). Block erase cannot resume until word write operations initiated during block erase suspend have completed.

4.8 Word Write Suspend Command

The Word Write Suspend command allows word write interruption to read data in other flash memory locations. Once the word write process starts, writing the Word Write Suspend command requests that the WSM suspend the word write sequence at a predetermined point in the algorithm. The device continues to output status register data when read after the Word Write Suspend command is written. Polling status register bits SR.7 and SR.2 can determine when the word write operation has been suspended (both will be set to "1"). RY/BY# will also transition to V_{OH}. Specification t_{WHRH1} defines the word write suspend latency.

At this point, a Read Array command can be written to read data from locations other than that which is suspended. The only other valid commands while word write is suspended are Read Status Register and Word Write Resume. After Word Write Resume command is written to the flash memory, the WSM will continue the word write process. Status register bits SR.2 and SR.7 will automatically clear and RY/BY# will return to V_{OL}. After the Word Write Resume command is written, the device automatically outputs status register data when read (see Figure 8). V_{PP} must remain at $V_{PPH1/2/3}$ (the same V_{PP} level used for word write) while in word write suspend mode. RP# must also remain at V_{IH} or V_{HH} (the same RP# level used for word write). WP# must also remain at V_{IL} or V_{IH} (the same WP# level used for word write).

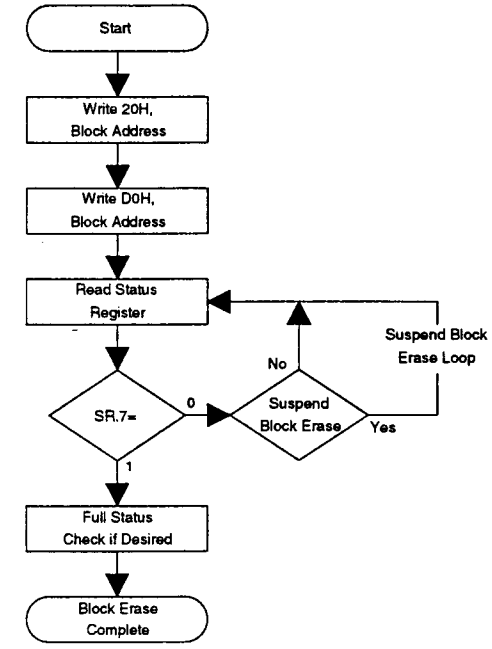
Table 6. Write Protection Alternatives

Operation	V_{PP}	RP#	WP#	Effect
Word Write or Block Erase	V_{IL}	X	X	All Blocks Locked.
	$>V_{PPLK}$	V_{IL}	X	All Blocks Locked.
		V_{HH}	X	All Blocks Unlocked.
		V_{IH}	V_{IL}	2 Boot Blocks Locked.
			V_{IH}	All Blocks Unlocked.

Table 7. Status Register Definition

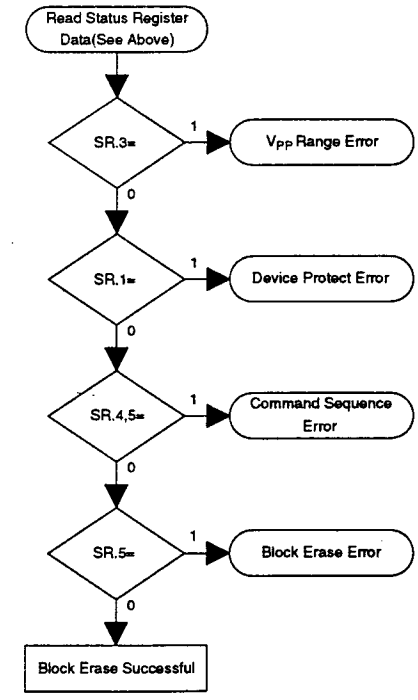
WSMS	ESS	ES	WWS	VPPS	WWSS	DPS	R
7	6	5	4	3	2	1	0

	NOTES:
SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy	Check RY/BY# or SR.7 to determine block erase or word write completion. SR.6-0 are invalid while SR.7="0".
SR.6 = ERASE SUSPEND STATUS (ESS) 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed	
SR.5 = ERASE STATUS (ES) 1 = Error in Block Erasure 0 = Successful Block Erase	If both SR.5 and SR.4 are "1"s after a block erase attempt, an improper command sequence was entered.
SR.4 = WORD WRITE STATUS (WWS) 1 = Error in Word Write 0 = Successful Word Write	
SR.3 = V_{PP} STATUS (VPPS) 1 = V_{PP} Low Detect, Operation Abort 0 = V_{PP} OK	SR.3 does not provide a continuous indication of V_{PP} level. The WSM interrogates and indicates the V_{PP} level only after Block Erase or Word Write command sequences. SR.3 is not guaranteed to reports accurate feedback only when $V_{PP} \neq V_{PPH1/2/3}$.
SR.2 = WORD WRITE SUSPEND STATUS (WWSS) 1 = Word Write Suspended 0 = Word Write in Progress/Completed	
SR.1 = DEVICE PROTECT STATUS (DPS) 1 = WP# or RP# Lock Detected, Operation Abort 0 = Unlock	The WSM interrogates the WP# and RP# only after Block Erase or Word Write command sequences. It informs the system, depending on the attempted operation, if the WP# is not V_{IH}, RP# is not V_{HH}.
SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)	SR.0 is reserved for future use and should be masked out when polling the status register.



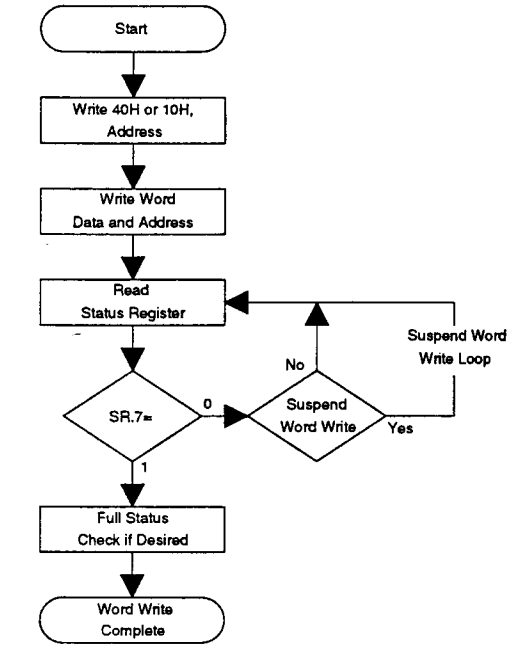
Bus Operation	Command	Comments
Write	Erase Setup	Data=20H Addr=Within Block to be Erased
Write	Erase Confirm	Data=D0H Addr=Within Block to be Erased
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Repeat for subsequent block erasures. Full status check can be done after each block erase or after a sequence of block erasures. Write FFH after the last operation to place device in read array mode.		

FULL STATUS CHECK PROCEDURE



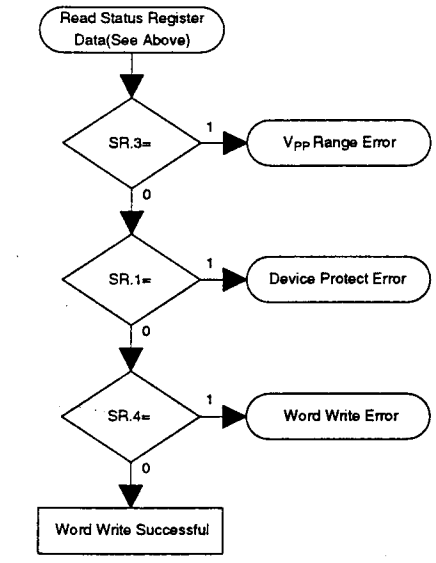
Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{PP} Error Detect
Standby		Check SR.1 1=Device Protect Detect
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.5 1=Block Erase Error
SR.5,SR.4,SR.3 and SR.1 are only cleared by the Clear Status Register Command in cases where multiple blocks are erased before full status is checked. If error is detected, clear the Status Register before attempting retry or other error recovery.		

Figure 5. Automated Block Erase Flowchart



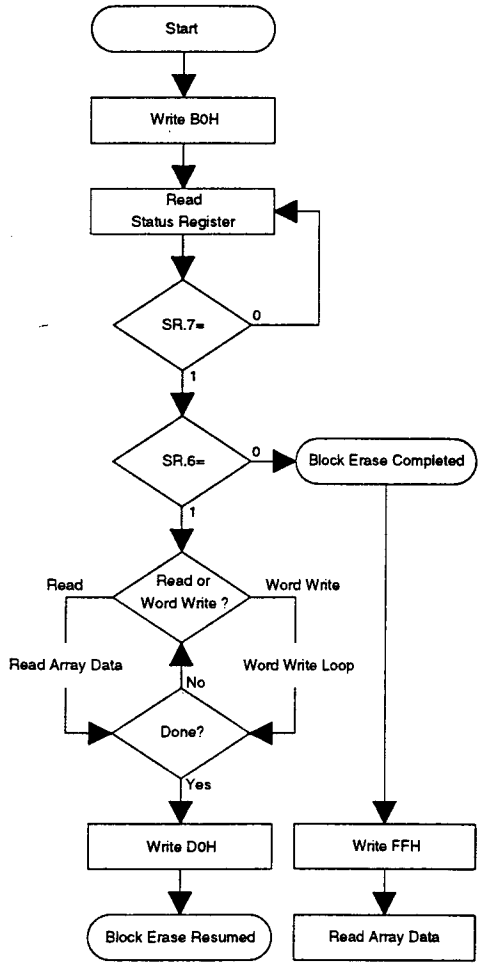
Bus Operation	Command	Comments
Write	Setup Word Write	Data=40H or 10H Addr=Location to Be Written
Write	Word Write	Data=Data to Be Written Addr=Location to Be Written
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Repeat for subsequent byte writes. SR full status check can be done after each word write, or after a sequence of word writes. Write FFH after the last word write operation to place device in read array mode.		

FULL STATUS CHECK PROCEDURE



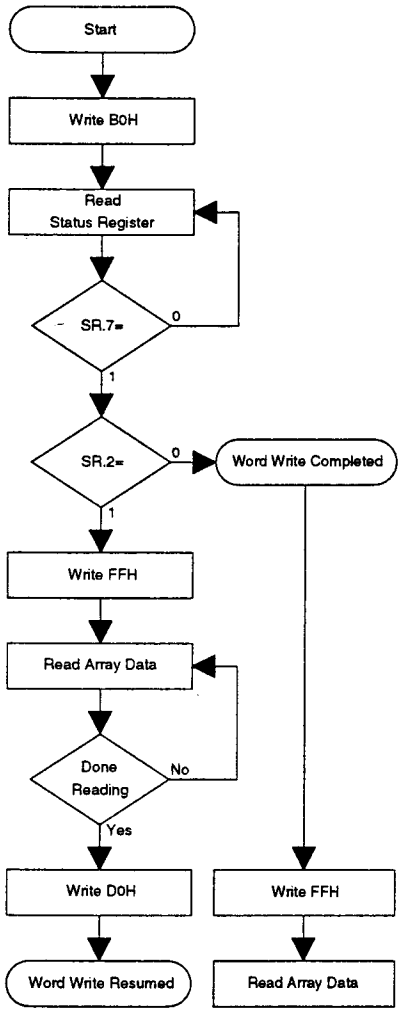
Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{PP} Error Detect
Standby		Check SR.1 1=Device Protect Detect
Standby		Check SR.4 1=Data Write Error
SR.4,SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are written before full status is checked. If error is detected, clear the Status Register before attempting retry or other error recovery.		

Figure 6. Automated Word Write Flowchart



Bus Operation	Command	Comments
Write	Erase Suspend	Data=B0H Addr=X
Read		Status Register Data Addr=X
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.6 1=Block Erase Suspended 0=Block Erase Completed
Write	Erase Resume	Data=D0H Addr=X

Figure 7. Block Erase Suspend/Resume Flowchart



Bus Operation	Command	Comments
Write	Word Write Suspend	Data=B0H Addr=X
Read		Status Register Data Addr=X
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.2 1=Word Write Suspended 0=Word Write Completed
Write	Read Array	Data=FFH Addr=X
Read		Read Array locations other than that being written.
Write	Word Write Resume	Data=D0H Addr=X

Figure 8. Word Write Suspend/Resume Flowchart

5 DESIGN CONSIDERATIONS

5.1 Three-Line Output Control

The device will often be used in large memory arrays. SHARP provides three control inputs to accommodate multiple memory connections. Three-line control provides for:

a. Lowest possible memory power dissipation.
b. Complete assurance that data bus contention will not occur.

To use these control inputs efficiently, an address decoder should enable CE# while OE# should be connected to all memory devices and the system's READ# control line. This assures that only selected memory devices have active outputs while deselected memory devices are in standby mode. RP# should be connected to the system POWERGOOD signal to prevent unintended writes during system power transitions. POWERGOOD should also toggle during system reset.

5.2 RY/BY#, Block Erase and Word Write Polling

RY/BY# is a full CMOS output that provides a hardware method of detecting block erase and word write completion. It transitions low after block erase or word write commands and returns to V_{OH} when the WSM has finished executing the internal algorithm.

RY/BY# can be connected to an interrupt input of the system CPU or controller. It is active at all times. RY/BY# is also V_{OH} when the device is in block erase suspend (with word write inactive), word write suspend or deep power-down modes.

5.3 Power Supply Decoupling

Flash memory power switching characteristics require careful device decoupling. System designers are interested in three supply current issues; standby current levels, active current levels and transient peaks produced by falling and rising edges of CE# and OE#. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 µF ceramic capacitor connected between its V_{CC} and GND and between its V_{PP} and GND. These high-frequency, low inductance capacitors should be placed as close as possible to package leads. Additionally, for every eight devices, a 4.7 µF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductance.

5.4 V_{PP} Trace on Printed Circuit Boards

Updating flash memories that reside in the target system requires that the printed circuit board designer pay attention to the V_{PP} Power supply trace. The V_{PP} pin supplies the memory cell current for word writing and block erasing. Use similar trace widths and layout considerations given to the V_{CC} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

5.5 V_{CC}, V_{PP}, RP# Transitions

Block erase and word write are not guaranteed if V_{PP} falls outside of a valid $V_{PPH1/2/3}$ range, V_{CC} falls outside of a valid $V_{CC1/2/3/4}$ range, or RP#≠V_{IH} or V_{HH}. If V_{PP} error is detected, status register bit SR.3 is set to "1" along with SR.4 or SR.5, depending on the attempted operation. If RP# transitions to V_{IL} during block erase or word write, RY/BY# will remain low until the reset operation is complete. Then, the operation will abort and the device will enter deep power-down. The aborted operation may leave data partially altered. Therefore, the command sequence must be repeated after normal operation is restored. Device power-off or RP# transitions to V_{IL} clear the status register.

The CUI latches commands issued by system software and is not altered by V_{PP} or CE# transitions or WSM actions. Its state is read array mode upon power-up, after exit from deep power-down or after V_{CC} transitions below V_{LKO}.

After block erase or word write, even after V_{PP} transitions down to V_{PPLK}, the CUI must be placed in read array mode via the Read Array command if subsequent access to the memory array is desired.

5.6 Power-Up/Down Protection

The device is designed to offer protection against accidental block erasure or word writing during power transitions. Upon power-up, the device is indifferent as to which power supply (V_{PP} or V_{CC}) powers-up first. Internal circuitry resets the CUI to read array mode at power-up.

A system designer must guard against spurious writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both WE# and CE# must be low for a command write, driving either to V_{IH} will inhibit writes. The CUI's two-step command sequence architecture provides added level of protection against data alteration.

WP# provide additional protection from inadvertent code or data alteration. The device is disabled while RP#=V_{IL} regardless of its control inputs state.

5.7 Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash memory's nonvolatility increases usable battery life because data is retained when system power is removed.

In addition, deep power-down mode ensures extremely low power consumption even when system power is applied. For example, portable computing products and other power sensitive applications that use an array of devices for solid-state storage can consume negligible power by lowering RP# to V_{IL} standby or sleep modes. If access is again needed, the devices can be read following the t_{PHQV} and t_{PHWL} wake-up cycles required after RP# is first raised to V_{IH}. See AC Characteristics– Read Only and Write Operations and Figures 13, 14 and 15 for more information.

6 ELECTRICAL SPECIFICATIONS

6.1 Absolute Maximum Ratings*

Commercial Operating Temperature
During Read, Block Erase and
Word Write .....-40°C to +85°C(1)
Temperature under Bias.....-40°C to +85°C

Storage Temperature.....-65°C to +125°C

Voltage On Any Pin
(except V_{CC}, V_{PP}, and RP#).....-2.0V to +7.0V(2)

V_{CC} Supply Voltage .....-2.0V to +7.0V(2)

V_{PP} Update Voltage during
Block Erase and Word Write . -2.0V to +14.0V(2,3)

RP# Voltage ..... -2.0V to +14.0V(2,3)

Output Short Circuit Current ..... 100mA(4)

NOTICE: This datasheet contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local SHARP Sales office that you have the latest datasheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. All specified voltages are with respect to GND. Minimum DC voltage is -0.5V on input/output pins and -0.2V on V_{CC} and V_{PP} pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins and V_{CC} is V_{CC}+0.5V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
3. Maximum DC voltage on V_{PP} and RP# may overshoot to +14.0V for periods <20ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.

6.2 Operating Conditions

Temperature and V_{CC} Operating Conditions

Symbol	Parameter	Min.	Max.	Unit	Test Condition
T_A	Operating Temperature	-40	+85	°C	Ambient Temperature
V_{CC1}	V_{CC} Supply Voltage (2.7V-3.6V)	2.7	3.6	V	
V_{CC2}	V_{CC} Supply Voltage (3.3V±0.3V)	3.0	3.6	V	
V_{CC3}	V_{CC} Supply Voltage (5V±0.25V)	4.75	5.25	V	
V_{CC4}	V_{CC} Supply Voltage (5V±0.5V)	4.50	5.50	V	

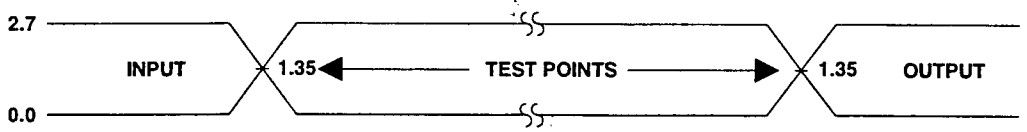
6.2.1 CAPACITANCE(1)

T_A=+25°C, f=1MHz

Symbol	Parameter	Typ.	Max.	Unit	Condition
C_{IN}	Input Capacitance	7	10	pF	V_{IN}=0.0V
C_{OUT}	Output Capacitance	9	12	pF	V_{OUT}=0.0V

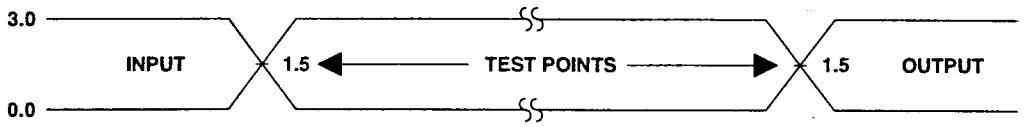
NOTE:
1. Sampled, not 100% tested.

6.2.2 AC INPUT/OUTPUT TEST CONDITIONS



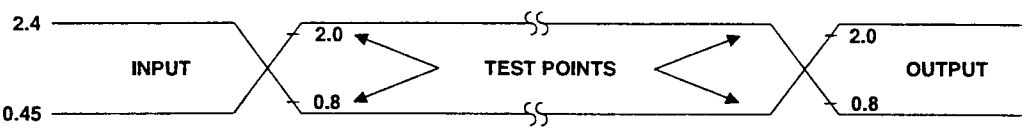
AC test inputs are driven at 2.7V for a Logic "1" and 0.0V for a Logic "0." Input timing begins, and output timing ends, at 1.35V. Input rise and fall times (10% to 90%) <10 ns.

Figure 9. Transient Input/Output Reference Waveform for V_{CC}=2.7V-3.6V



AC test inputs are driven at 3.0V for a Logic "1" and 0.0V for a Logic "0." Input timing begins, and output timing ends, at 1.5V. Input rise and fall times (10% to 90%) <10 ns.

Figure 10. Transient Input/Output Reference Waveform for V_{CC}=3.3V±0.3V and V_{CC}=5V±0.25V (High Speed Testing Configuration)



AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a Logic "1" and V_{OL} (0.45 V_{TTL}) for a Logic "0." Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) <10 ns.

Figure 11. Transient Input/Output Reference Waveform for V_{CC}=5V±0.5V (Standard Testing Configuration)

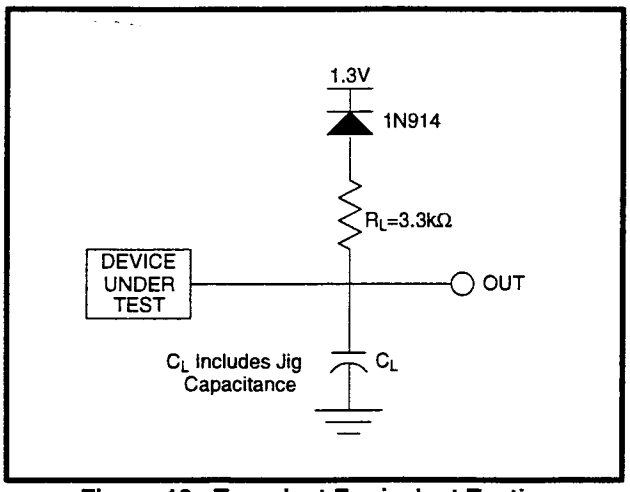


Figure 12. Transient Equivalent Testing Load Circuit

Test Configuration Capacitance Loading Value

Test Configuration	C_L (pF)
V_{CC}=3.3V±0.3V, 2.7V-3.6V	50
V_{CC}=5V±0.25V	30
V_{CC}=5V±0.5V	100

6.2.3 DC CHARACTERISTICS

DC Characteristics

Sym.	Parameter	Notes	V_{CC}=2.7V-3.6V Typ.	V_{CC}=2.7V-3.6V Max.	V_{CC}=5V±0.5V Typ.	V_{CC}=5V±0.5V Max.	Unit	Test Conditions
I_{LI}	Input Load Current	1		±0.5		±1	µA	V_{CC}=V_{CC}Max, V_{IN}=V_{CC} or GND
I_{LO}	Output Leakage Current	1		±0.5		±10	µA	V_{CC}=V_{CC}Max, V_{OUT}=V_{CC} or GND
I_{CCS}	V_{CC} Standby Current	1,3,6	25	50	30	100	µA	CMOS Inputs V_{CC}=V_{CC}Max CE#=RP#=V_{CC}±0.2V
			0.2	2	0.4	2	mA	TTL Inputs V_{CC}=V_{CC}Max CE#=RP#=V_{IH}
I_{CCD}	V_{CC} Deep Power-Down Current	1	4	20		20	µA	RP#=GND±0.2V I_{OUT}(RY/BY#)=0mA
I_{CCR}	V_{CC} Read Current	1,5,6	15	25		50	mA	CMOS Inputs V_{CC}=V_{CC}Max, CE#=GND f=5MHz(3.3V, 2.7V), 8MHz(5V) I_{OUT}=0mA
				30		65	mA	TTL Inputs V_{CC}=V_{CC}Max, CE#=GND f=5MHz(3.3V, 2.7V), 8MHz(5V) I_{OUT}=0mA
I_{CCW}	V_{CC} Word Write Current	1,7	5	17	—	—	mA	V_{PP}=2.7V-3.6V
			5	17		35	mA	V_{PP}=4.5V-5.5V
			5	12		30	mA	V_{PP}=11.4V-12.6V
I_{CCE}	V_{CC} Block Erase Current	1,7	4	17	—	—	mA	V_{PP}=2.7V-3.6V
			4	17		30	mA	V_{PP}=4.5V-5.5V
			4	12		25	mA	V_{PP}=11.4V-12.6V
I_{CCWS} I_{CCES}	V_{CC} Word Write or Block Erase Suspend Current	1,2	1	6	1	10	mA	CE#=V_{IH}
I_{PPS} I_{PPR}	V_{PP} Standby or Read Current	1	±2	±15	±2	±15	µA	V_{PP}≤V_{CC}
			10	200	10	200	µA	V_{PP}>V_{CC}
I_{PPD}	V_{PP} Deep Power-Down Current	1	0.1	5	0.1	5	µA	RP#=GND±0.2V
I_{PPW}	V_{PP} Word Write Current	1,7	12	40	—	—	mA	V_{PP}=2.7V-3.6V
				40		40	mA	V_{PP}=4.5V-5.5V
				30		30	mA	V_{PP}=11.4V-12.6V
I_{PPE}	V_{PP} Block Erase Current	1,7	8	25	—	—	mA	V_{PP}=2.7V-3.6V
				25		25	mA	V_{PP}=4.5V-5.5V
				20		20	mA	V_{PP}=11.4V-12.6V
I_{PPWS} I_{PPES}	V_{PP} Word Write or Block Erase Suspend Current	1	10	200	10	200	µA	V_{PP}=$V_{PPH1/2/3}$

DC Characteristics (Continued)

Sym.	Parameter	Notes	V_{CC}=2.7V-3.6V		V_{CC}=5V±0.5V		Unit	Test Conditions
			Min.	Max.	Min.	Max.		
V_{IL}	Input Low Voltage	7	-0.5	0.8	-0.5	0.8	V	
V_{IH}	Input High Voltage	7	2.0	V_{CC} +0.5	2.0	V_{CC} +0.5	V	
V_{OL}	Output Low Voltage	3,7		0.4		0.45	V	V_{CC}=V_{CC} Min, I_{OL}=5.8mA(5V) I_{OL}=2.0mA(2.7V,3.3V)
V_{OH1}	Output High Voltage (TTL)	3,7	2.4		2.4		V	V_{CC}=V_{CC} Min, I_{OH}=-2.5mA(5V) I_{OH}=-2.0mA(2.7V,3.3V)
V_{OH2}	Output High Voltage (CMOS)	3,7	0.85 V_{CC}		0.85 V_{CC}		V	V_{CC}=V_{CC} Min, I_{OH}=-2.5mA
			V_{CC} -0.4		V_{CC} -0.4		V	V_{CC}=V_{CC} Min, I_{OH}=-100µA
V_{PPLK}	V_{PP} Lockout during Normal Operations	4,7		1.5		1.5	V	
V_{PPH1}	V_{PP} during Word Write or Block Erase Operations		2.7	3.6	—	—	V	
V_{PPH2}	V_{PP} during Word Write or Block Erase Operations		4.5	5.5	4.5	5.5	V	
V_{PPH3}	V_{PP} during Word Write or Block Erase Operations		11.4	12.6	11.4	12.6	V	
V_{LKO}	V_{CC} Lockout Voltage		2.0		2.0		V	
V_{HH}	RP# Unlock Voltage	8,9	11.4	12.6	11.4	12.6	V	Unavailable WP#

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at nominal V_{CC} voltage and T_A=+25°C. These currents are valid for all product versions (packages and speeds).
2. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or word written while in erase suspend mode, the device's current draw is the sum of I_{CCWS} or I_{CCES} and I_{CCR} or I_{CCW}, respectively.
3. Includes RY/BY#.
4. Block erases and word writes are inhibited when $V_{PP} \leq V_{PPLK}$, and not guaranteed in the range between V_{PPLK}(max) and V_{PPH1}(min), between V_{PPH1}(max) and V_{PPH2}(min), between V_{PPH2}(max) and V_{PPH3}(min), and above V_{PPH3}(max).
5. Automatic Power Savings (APS) reduces typical I_{CCR} to 1mA at 5V V_{CC} and 3mA at 2.7V and 3.3V V_{CC} in static operation.
6. CMOS inputs are either V_{CC}±0.2V or GND±0.2V. TTL inputs are either V_{IL} or V_{IH}.
7. Sampled, not 100% tested.
8. Boot block erases and word writes are inhibited when the corresponding RP#=V_{IH} or WP#=V_{IL}. Block erase and word write operations are not guaranteed with V_{CC}<2.7V or V_{IH}<RP#<V_{HH} and should not be attempted.
9. RP# connection to a V_{HH} supply is allowed for a maximum cumulative period of 80 hours.

6.2.4 AC CHARACTERISTICS - READ-ONLY OPERATIONS(1)

V_{CC}=2.7V-3.6V, T_A=-40°C to +85°C

Versions(4)			LH28F800BGH-L120		
Sym.	**Parameter**	**Notes**	**Min.**	**Max.**	**Unit**
t_{AVAV}	Read Cycle Time		120		ns
t_{AVQV}	Address to Output Delay			120	ns
t_{ELQV}	CE# to Output Delay	2		120	ns
t_{PHQV}	RP# High to Output Delay			600	ns
t_{GLQV}	OE# to Output Delay	2		50	ns
t_{ELQX}	CE# to Output in Low Z	3	0		ns
t_{EHQZ}	CE# High to Output in High Z	3		55	ns
t_{GLQX}	OE# to Output in Low Z	3	0		ns
t_{GHQZ}	OE# High to Output in High Z	3		20	ns
t_{OH}	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		ns

NOTE:
See 5.0V V_{CC} Read-Only Operations for notes 1 through 4.

V_{CC}=3.3V±0.3V, T_A=-40°C to +85°C

Versions(4)			LH28F800BGH-L100		
Sym.	**Parameter**	**Notes**	**Min.**	**Max.**	**Unit**
t_{AVAV}	Read Cycle Time		100		ns
t_{AVQV}	Address to Output Delay			100	ns
t_{ELQV}	CE# to Output Delay	2		100	ns
t_{PHQV}	RP# High to Output Delay			600	ns
t_{GLQV}	OE# to Output Delay	2		50	ns
t_{ELQX}	CE# to Output in Low Z	3	0		ns
t_{EHQZ}	CE# High to Output in High Z	3		55	ns
t_{GLQX}	OE# to Output in Low Z	3	0		ns
t_{GHQZ}	OE# High to Output in High Z	3		20	ns
t_{OH}	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		ns

NOTE:
See 5.0V V_{CC} Read-Only Operations for notes 1 through 4.

V_{CC}=5V±0.5V, 5V±0.25V, T_A=-40°C to +85°C

Versions[4]			V_{CC}±0.25V	LH28F800BGH-L85[5]			
			V_{CC}±0.5V		LH28F800BGH-L90[6]		
Sym.	Parameter	Notes	Min.	Max.	Min.	Max.	Unit
t_{AVAV}	Read Cycle Time		85		90		ns
t_{AVQV}	Address to Output Delay			85		90	ns
t_{ELQV}	CE# to Output Delay	2		85		90	ns
t_{PHQV}	RP# High to Output Delay			400		400	ns
t_{GLQV}	OE# to Output Delay	2		40		45	ns
t_{ELQX}	CE# to Output in Low Z	3	0		0		ns
t_{EHQZ}	CE# High to Output in High Z	3		55		55	ns
t_{GLQX}	OE# to Output in Low Z	3	0		0		ns
t_{GHQZ}	OE# High to Output in High Z	3		10		10	ns
t_{OH}	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		0		ns

NOTES:

1. See AC Input/Output Reference Waveform for maximum allowable input slew rate.
2. OE# may be delayed up to t_{ELQV}-t_{GLQV} after the falling edge of CE# without impact on t_{ELQV}.
3. Sampled, not 100% tested.
4. See Ordering Information for device speeds (valid operational combinations).
5. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (High Speed Configuration) for testing characteristics.
6. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (Standard Configuration) for testing characteristics.

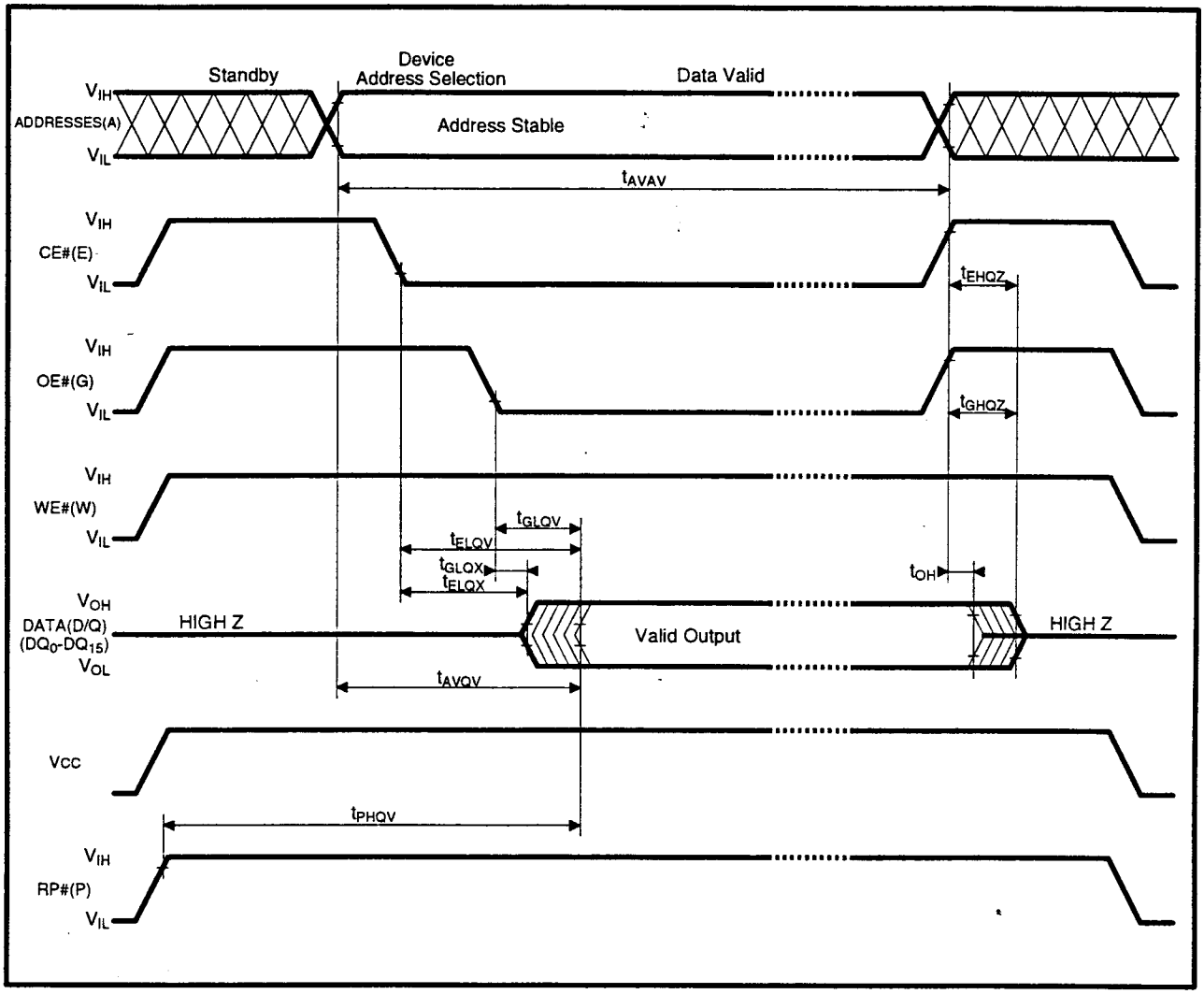


Figure 13. AC Waveform for Read Operations

6.2.5 AC CHARACTERISTICS - WRITE OPERATIONS(1)

V_{CC}=2.7V-3.6V, T_A=-40°C to +85°C

Versions(5)			LH28F800BGH-L120		
Sym.	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Write Cycle Time		120		ns
t_{PHWL}	RP# High Recovery to WE# Going Low	2	1		µs
t_{ELWL}	CE# Setup to WE# Going Low		10		ns
t_{WLWH}	WE# Pulse Width		50		ns
t_{PHHWH}	RP#V_{HH} Setup to WE# Going High	2	100		ns
t_{SHWH}	WP#V_{IH} Setup to WE# Going High	2	100		ns
t_{VPWH}	V_{PP} Setup to WE# Going High	2	100		ns
t_{AVWH}	Address Setup to WE# Going High	3	50		ns
t_{DVWH}	Data Setup to WE# Going High	3	50		ns
t_{WHDX}	Data Hold from WE# High		5		ns
t_{WHAX}	Address Hold from WE# High		5		ns
t_{WHEH}	CE# Hold from WE# High		10		ns
t_{WHWL}	WE# Pulse Width High		30		ns
t_{WHRL}	WE# High to RY/BY# Going Low			100	ns
t_{WHGL}	Write Recovery before Read		0		ns
t_{QVVL}	V_{PP} Hold from Valid SRD, RY/BY# High	2,4	0		ns
t_{QVPH}	RP# V_{HH} Hold from Valid SRD, RY/BY# High	2,4	0		ns
t_{QVSL}	WP# V_{IH} Hold from Valid SRD, RY/BY# High	2,4	0		ns

NOTE:
See 5.0V V_{CC} AC Characteristics - Write Operations for notes 1 through 5.

V_{CC}=3.3V±0.3V, T_A=-40°C to +85°C

Versions(5)			LH28F800BGH-L100		
Sym.	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Write Cycle Time		100		ns
t_{PHWL}	RP# High Recovery to WE# Going Low	2	1		µs
t_{ELWL}	CE# Setup to WE# Going Low		10		ns
t_{WLWH}	WE# Pulse Width		50		ns
t_{PHHWH}	RP# V_{HH} Setup to WE# Going High	2	100		ns
t_{SHWH}	WP#V_{IH} Setup to WE# Going High	2	100		ns
t_{VPWH}	V_{PP} Setup to WE# Going High	2	100		ns
t_{AVWH}	Address Setup to WE# Going High	3	50		ns
t_{DVWH}	Data Setup to WE# Going High	3	50		ns
t_{WHDX}	Data Hold from WE# High		5		ns
t_{WHAX}	Address Hold from WE# High		5		ns
t_{WHEH}	CE# Hold from WE# High		10		ns
t_{WHWL}	WE# Pulse Width High		30		ns
t_{WHRL}	WE# High to RY/BY# Going Low			100	ns
t_{WHGL}	Write Recovery before Read		0		ns
t_{QVVL}	V_{PP} Hold from Valid SRD, RY/BY# High	2,4	0		ns
t_{QVPH}	RP# V_{HH} Hold from Valid SRD, RY/BY# High	2,4	0		ns
t_{QVSL}	WP# V_{IH} Hold from Valid SRD, RY/BY# High	2,4	0		ns

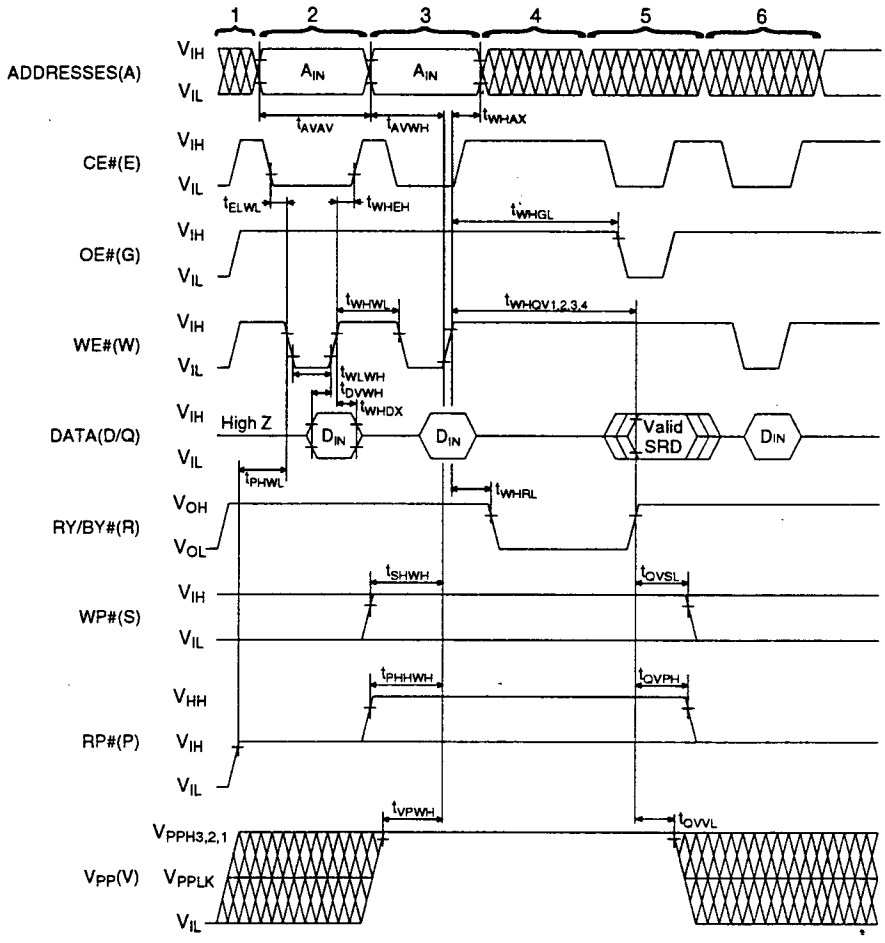
NOTE:
See 5.0V V_{CC} AC Characteristics - Write Operations for notes for notes 1 through 5.

V_{CC}=5V±0.5V, 5V±0.25V, T_A=-40°C to +85°C

Versions[5]		V_{CC}±0.25V / V_{CC}±0.5V	LH28F800BGH-L85[6]		LH28F800BGH-L90[7]		
Sym.	Parameter	Notes	Min.	Max.	Min.	Max.	Unit
t_{AVAV}	Write Cycle Time		85		90		ns
t_{PHWL}	RP# High Recovery to WE# Going Low	2	1		1		µs
t_{ELWL}	CE# Setup to WE# Going Low		10		10		ns
t_{WLWH}	WE# Pulse Width		40		40		ns
t_{PHHWH}	RP# V_{HH} Setup to WE# Going High	2	100		100		ns
t_{SHWH}	WP#V_{IH} Setup to WE# Going High	2	100		100		ns
t_{VPWH}	V_{PP} Setup to WE# Going High	2	100		100		ns
t_{AVWH}	Address Setup to WE# Going High	3	40		40		ns
t_{DVWH}	Data Setup to WE# Going High	3	40		40		ns
t_{WHDX}	Data Hold from WE# High		5		5		ns
t_{WHAX}	Address Hold from WE# High		5		5		ns
t_{WHEH}	CE# Hold from WE# High		10		10		ns
t_{WHWL}	WE# Pulse Width High		30		30		ns
t_{WHRL}	WE# High to RY/BY# Going Low			90		90	ns
t_{WHGL}	Write Recovery before Read		0		0		ns
t_{QVVL}	V_{PP} Hold from Valid SRD, RY/BY# High	2,4	0		0		ns
t_{QVPH}	RP# V_{HH} Hold from Valid SRD, RY/BY# High	2,4	0		0		ns
t_{QVSL}	WP# V_{IH} Hold from Valid SRD, RY/BY# High	2,4	0		0		ns

NOTES:

1. Read timing characteristics during block erase and word write operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
2. Sampled, not 100% tested.
3. Refer to Table 4 for valid A_{IN} and D_{IN} for block erase or word write.
4. V_{PP} should be held at $V_{PPH1/2/3}$ (and if necessary RP# should be held at V_{HH}) until determination of block erase or word write success (SR.1/3/4/5=0).
5. See Ordering Information for device speeds (valid operational combinations).
6. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (High Seed Configuration) for testing characteristics.
7. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (Standard Configuration) for testing characteristics.



NOTES:
1. V_{CC} power-up and standby.
2. Write block erase or word write setup.
3. Write block erase confirm or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

Figure 14. AC Waveform for WE#-Controlled Write Operations

6.2.6 ALTERNATIVE CE#-CONTROLLED WRITES(1)

V_{CC}=2.7V-3.6V, T_A=-40°C to +85°C

Versions(5)			LH28F800BGH-L120		
Sym.	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Write Cycle Time		120		ns
t_{PHEL}	RP# High Recovery to CE# Going Low	2	1		µs
t_{WLEL}	WE# Setup to CE# Going Low		0		ns
t_{ELEH}	CE# Pulse Width		70		ns
t_{PHHEH}	RP#V_{HH} Setup to CE# Going High	2	100		ns
t_{SHEH}	WP#V_{IH} Setup to CE# Going High	2	100		ns
t_{VPEH}	V_{PP} Setup to CE# Going High	2	100		ns
t_{AVEH}	Address Setup to CE# Going High	3	50		ns
t_{DVEH}	Data Setup to CE# Going High	3	50		ns
t_{EHDX}	Data Hold from CE# High		5		ns
t_{EHAX}	Address Hold from CE# High		5		ns
t_{EHWH}	WE# Hold from CE# High		0		ns
t_{EHEL}	CE# Pulse Width High		25		ns
t_{EHRL}	CE# High to RY/BY# Going Low			100	ns
t_{EHGL}	Write Recovery before Read		0		ns
t_{QVVL}	V_{PP} Hold from Valid SRD, RY/BY# High	2,4	0		ns
t_{QVPH}	RP# V_{HH} Hold from Valid SRD, RY/BY# High	2,4	0		ns
t_{QVSL}	WP# V_{IH} Hold from Valid SRD, RY/BY# High	2,4	0		ns

NOTE:
See 5.0V V_{CC} Alternative CE#-Controlled Writes for notes 1 through 5.

V_{CC}=3.3V±0.3V, T_A=-40°C to +85°C

Versions(5)			LH28F800BGH-L100		
Sym.	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Write Cycle Time		100		ns
t_{PHEL}	RP# High Recovery to CE# Going Low	2	1		µs
t_{WLEL}	WE# Setup to CE# Going Low		0		ns
t_{ELEH}	CE# Pulse Width		70		ns
t_{PHHEH}	RP# V_{HH} Setup to CE# Going High	2	100		ns
t_{SHEH}	WP#V_{IH} Setup to CE# Going High	2	100		ns
t_{VPEH}	V_{PP} Setup to CE# Going High	2	100		ns
t_{AVEH}	Address Setup to CE# Going High	3	50		ns
t_{DVEH}	Data Setup to CE# Going High	3	50		ns
t_{EHDX}	Data Hold from CE# High		5		ns
t_{EHAX}	Address Hold from CE# High		5		ns
t_{EHWH}	WE# Hold from CE# High		0		ns
t_{EHEL}	CE# Pulse Width High		25		ns
t_{EHRL}	CE# High to RY/BY# Going Low			100	ns
t_{EHGL}	Write Recovery before Read		0		ns
t_{QVVL}	V_{PP} Hold from Valid SRD, RY/BY# High	2,4	0		ns
t_{QVPH}	RP# V_{HH} Hold from Valid SRD, RY/BY# High	2,4	0		ns
t_{QVSL}	WP# V_{IH} Hold from Valid SRD, RY/BY# High	2,4	0		ns

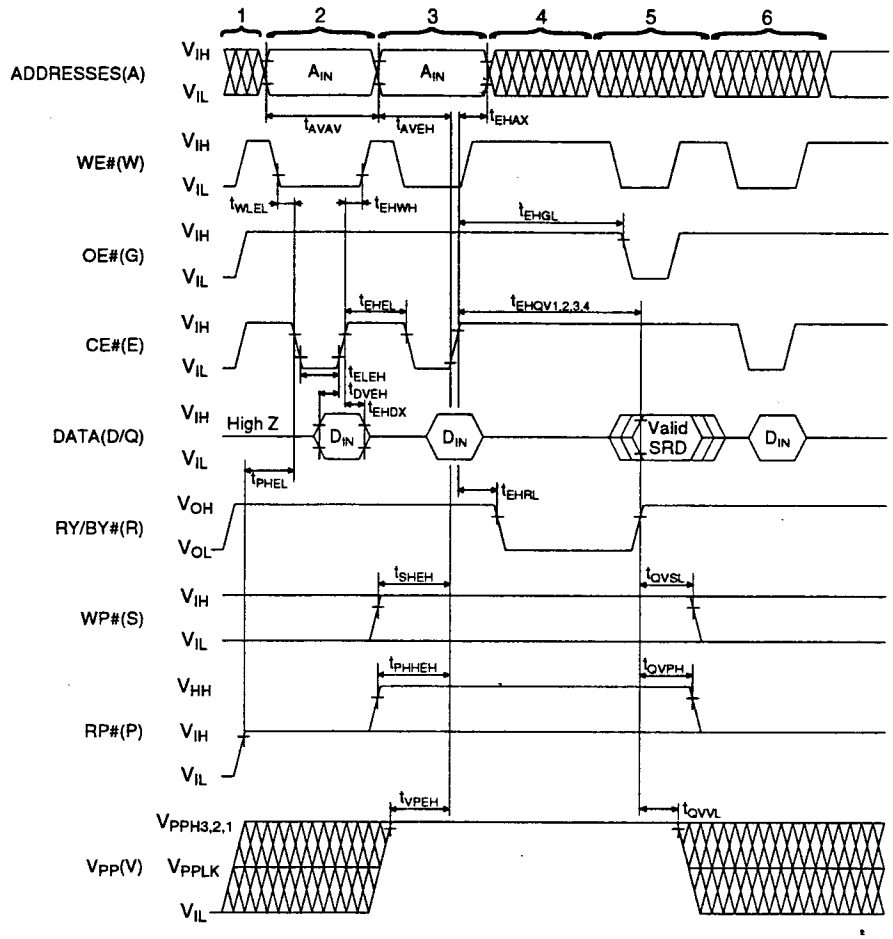
NOTE:
See 5V V_{CC} Alternative CE#-Controlled Writes for Notes 1 through 5.

V_{CC}=5V±0.5V, 5V±0.25V, T_A=-40°C to +85°C

Versions[5]			V_{CC}±0.25V	LH28F800BGH-L85[6]			
			V_{CC}±0.5V		LH28F800BGH-L90[7]		
Sym.	Parameter	Notes	Min.	Max.	Min.	Max.	Unit
t_{AVAV}	Write Cycle Time		85		90		ns
t_{PHEL}	RP# High Recovery to CE# Going Low	2	1		1		µs
t_{WLEL}	WE# Setup to CE# Going Low		0		0		ns
t_{ELEH}	CE# Pulse Width		50		50		ns
t_{PHHEH}	RP# V_{HH} Setup to CE# Going High	2	100		100		ns
t_{SHEH}	WP# V_{IH} Setup to CE# Going High	2	100		100		ns
t_{VPEH}	V_{PP} Setup to CE# Going High	2	100		100		ns
t_{AVEH}	Address Setup to CE# Going High	3	40		40		ns
t_{DVEH}	Data Setup to CE# Going High	3	40		40		ns
t_{EHDX}	Data Hold from CE# High		5		5		ns
t_{EHAX}	Address Hold from CE# High		5		5		ns
t_{EHWH}	WE# Hold from CE# High		0		0		ns
t_{EHEL}	CE# Pulse Width High		25		25		ns
t_{EHRL}	CE# High to RY/BY# Going Low			90		90	ns
t_{EHGL}	Write Recovery before Read		0		0		ns
t_{QVVL}	V_{PP} Hold from Valid SRD, RY/BY# High	2,4	0		0		ns
t_{QVPH}	RP# V_{HH} Hold from Valid SRD, RY/BY# High	2,4	0		0		ns
t_{QVSL}	WP# V_{IH} Hold from Valid SRD, RY/BY# High	2,4	0		0		ns

NOTES:

1. In systems where CE# defines the write pulse width (within a longer WE# timing waveform), all setup, hold, and inactive WE# times should be measured relative to the CE# waveform.
2. Sampled, not 100% tested.
3. Refer to Table 4 for valid A_{IN} and D_{IN} for block erase or word write.
4. V_{PP} should be held at $V_{PPH1/2/3}$ (and if necessary RP# should be held at V_{HH}) until determination of block erase or word write success (SR.1/3/4/5=0).
5. See Ordering Information for device speeds (valid operational combinations).
6. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (High Seed Configuration) for testing characteristics.
7. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (Standard Configuration) for testing characteristics.



NOTES:
1. V_{CC} power-up and standby.
2. Write block erase or word write setup.
3. Write block erase confirm or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

Figure 15. Alternate AC Waveform for CE#-Controlled Write Operations

6.2.7 RESET OPERATIONS

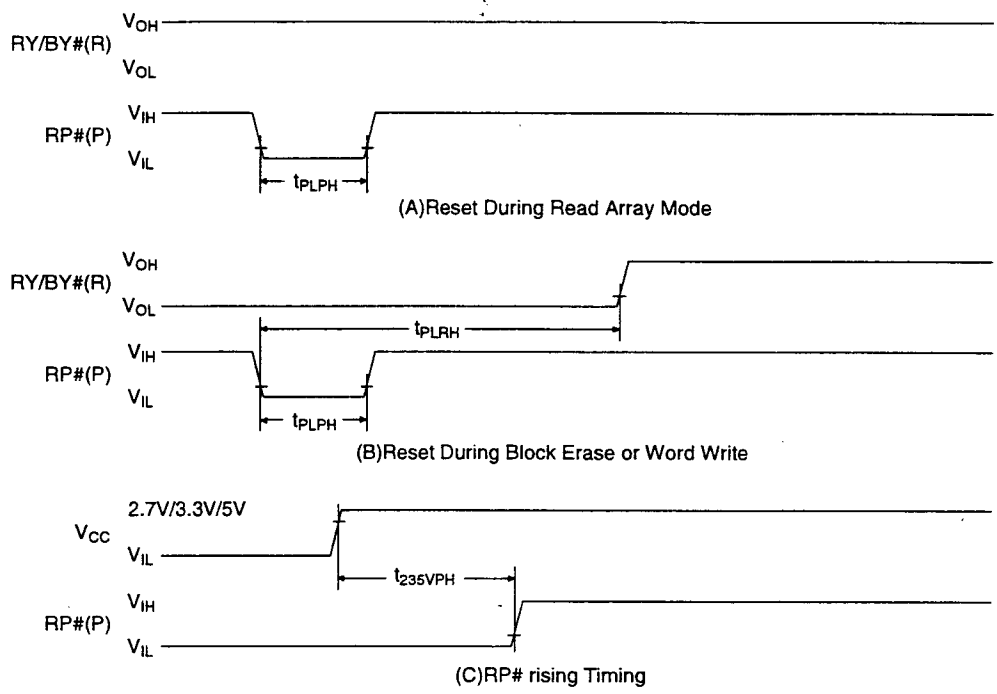


Figure 16. AC Waveform for Reset Operation

Reset AC Specifications(1)

Sym.	Parameter	Notes	V_{CC}=2.7V-3.6V		V_{CC}=3.0V-3.6V		V_{CC}=4.5V-5.5V		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLPH}	RP# Pulse Low Time (If RP# is tied to V_{CC}, this specification is not applicable)		100		100		100		ns
t_{PLRH}	RP# Low to Reset during Block Erase or Word Write	2,3		22		20		12	µs
t_{235VPH}	V_{CC} 2.7V to RP# High V_{CC} 3.0V to RP# High V_{CC} 4.5V to RP# High	4	100		100		100		ns

NOTES:

1. These specifications are valid for all product versions (packages and speeds).
2. If RP# is asserted while a block erase or word write operation is not executing, the reset will complete within 100ns.
3. A reset time, t_{PHQV}, is required from the later of RY/BY# or RP# going high until outputs are valid.
4. When the device power-up, holding RP# low minimum 100ns is required after V_{CC} has been in predefined range and also has been in stable there.

6.2.8 BLOCK ERASE AND WORD WRITE PERFORMANCE(3,4)

V_{CC}=2.7V-3.6V, T_A=-40°C to +85°C

Sym.	Parameter		Notes	V_{PP}=2.7V-3.6V			V_{PP}=4.5V-5.5V			V_{PP}=11.4V-12.6V			Unit
				Min.	Typ.(1)	Max.	Min.	Typ.(1)	Max.	Min.	Typ.(1)	Max.	
t_{WHQV1} t_{EHQV1}	Word Write Time	32K word Block	2		44.6			17.7			12.6		µs
		4K word Block	2		45.9			26.1			24.5		µs
	Block Write Time	32K word Block	2		1.46			0.58			0.42		s
		4K word Block	2		0.19			0.11			0.11		s
t_{WHQV2} t_{EHQV2}	Block Erase Time	32K word Block	2		1.14			0.61			0.51		s
		4K word Block	2		0.38			0.32			0.31		s
t_{WHRH1} t_{EHRH1}	Word Write Suspend Latency Time to Read				7	8		6	8		6	7	µs
t_{WHRH2} t_{EHRH2}	Erase Suspend Latency Time to Read				18	22		11	14		11	14	µs

NOTE:
See 5V V_{CC} Block Erase and Word Write Performance for Notes 1 through 4.

V_{CC}=3.3V±0.3V, T_A=-40°C to +85°C

Sym.	Parameter		Notes	V_{PP}=3.0V-3.6V			V_{PP}=4.5V-5.5V			V_{PP}=11.4V-12.6V			Unit
				Min.	Typ.(1)	Max.	Min.	Typ.(1)	Max.	Min.	Typ.(1)	Max.	
t_{WHQV1} t_{EHQV1}	Word Write Time	32K word Block	2		44			17.3			12.3		µs
		4K word Block	2		45			25.6			24		µs
	Block Write Time	32K word Block	2		1.44			0.57			0.41		s
		4K word Block	2		0.19			0.11			0.1		s
t_{WHQV2} t_{EHQV2}	Block Erase Time	32K word Block	2		1.11			0.59			0.5		s
		4K word Block	2		0.37			0.31			0.3		s
t_{WHRH1} t_{EHRH1}	Word Write Suspend Latency Time to Read				6	7		5	7		5	6	µs
t_{WHRH2} t_{EHRH2}	Erase Suspend Latency Time to Read				16.2	20		9.6	12		9.6	12	µs

NOTE:
See 5V V_{CC} Block Erase and Word Write Performance for Notes 1 through 4.

V_{CC}=5V±0.5V, 5V±0.25V, T_A=-40°C to +85°C

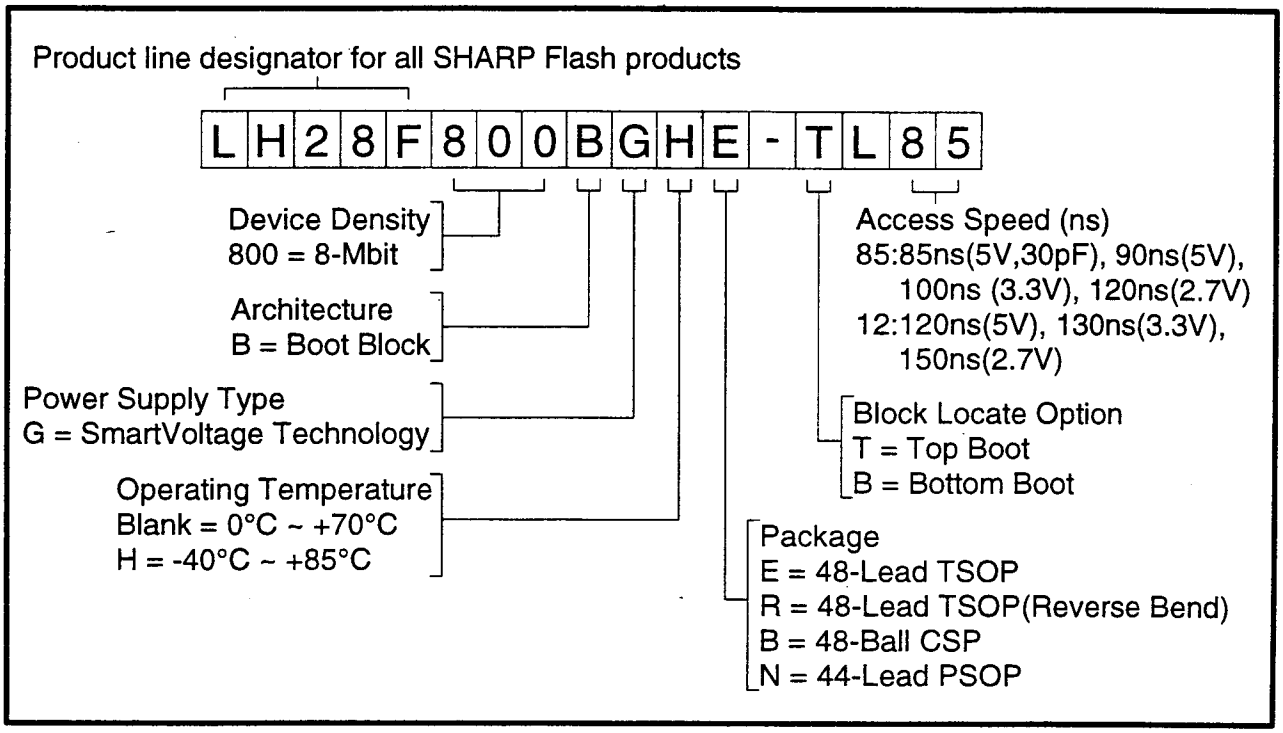
Sym.	Parameter		Notes	V_{PP}=4.5V-5.5V			V_{PP}=11.4V-12.6V			Unit
				Min.	Typ.(1)	Max.	Min.	Typ.(1)	Max.	
t_{WHQV1} t_{EHQV1}	Word Write Time	32K word Block	2		12.2			8.4		µs
		4K word Block	2		18.3			17		µs
	Block Write Time	32K word Block	2		0.4			0.28		s
		4K word Block	2		0.08			0.07		s
t_{WHQV2} t_{EHQV2}	Block Erase Time	32K word Block	2		0.46			0.39		s
		4K word Block	2		0.26			0.25		s
t_{WHRH1} t_{EHRH1}	Word Write Suspend Latency Time to Read				5	6		4	5	µs
t_{WHRH2} t_{EHRH2}	Erase Suspend Latency Time to Read				9.6	12		9.6	12	µs

NOTES:

1. Typical values measured at T_A=+25°C and nominal voltages. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. These performance numbers are valid for all speed versions.
4. Sampled but not 100% tested.

7 ADDITIONAL INFORMATION

7.1 Ordering Information



Option	Order Code	Valid Operational Combinations			
		V_{CC}=2.7V-3.6V 50pF load, 1.35V I/O Levels	V_{CC}=3.3V±0.3V 50pF load, 1.5V I/O Levels	V_{CC}=5V±0.5V 100pF load, TTL I/O Levels	V_{CC}=5V±0.25V 30pF load, 1.5V I/O Levels
1	LH28F800BGHE-TL85	LH28F800BGH-L120	LH28F800BGH-L100	LH28F800BGH-L90	LH28F800BGH-L85

8 Package and packing specification

1. Package Outline Specification

Refer to drawing No.AA1142

2. Markings

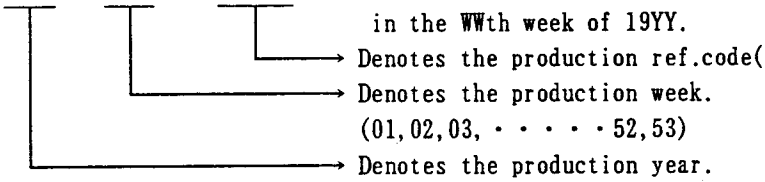
2－1. Marking contents

(1) Product name : LH28F800BGHE－TL85

(2) Company name : SHARP

(3) Date code

(Example) YY WW ×××



Indicates the product was manufactured in the WWth week of 19YY.

Denotes the production ref.code(1~3)

Denotes the production week. (01,02,03,・・・・・52,53)

Denotes the production year. (Lower two digits of the year.)

(4) The marking of "JAPAN" indicates the country of origin.

2－2. Marking layout

Refer drawing No.AA1142

(This layout does not define the dimensions of marking character and marking position.)

3. Surface Mount Conditions

Please perform the following conditions when mounting ICs not to deteriorate IC quality.

3－1.Soldering conditions(The following conditions are valid only for one time soldering.)

Mounting Method	Temperature and Duration	Measurement Point
Reflow soldering (air)	Peak temperature of 230℃ or less, duration of less than 15 seconds. 200℃ or over,duration of less than 40 seconds. Temperature increase rate of 1~4℃/second	IC package surface
Manual soldering (soldering iron)	260℃ or less, duration of less than 10 seconds	IC outer lead surface

3－2. Conditions for removal of residual flux

(1) Ultrasonic washing power : 25 Watts/liter or less

(2) Washing time : Total 1 minute maximum

(3) Solvent temperature : 15~40℃

4. Packing Specification (Embossed Carrier Taping Specification)

This standard apply to the embossed carrier taping specification for ICs to be delivered from SHARP CORPORATION. SHARP's embossed carrier taping specification are generally based on those set forth by the Japanese Industrial Standard JIS C 0806 and the EIA481A.

4－1. Tape Structure

・Embossed carrier tape is made of conductive plastic. The embossed portions of the carrier tape are filled with IC packages and covered with a top covering tape to enclose them.

4－2. Taping Reel and Embossed Carrier Tape Size

・For the taping reel and embossed carrier tape sizes, refer to the attached drawings (NO.CV758 and CV521)

4－3. IC Package Enclosure in Embossed Carrier Tape

・The IC package enclosure direction in the embossed portion as it compares to the direction in which the tape is pulled is indicated by an index mark on package (Index mark indicate the NO.1 pin on package) in the attached drawing (NO. CV522).

4－4. Missing IC Packages inside Embossed Carrier Tape

・The number of missing IC packages inside the embossed carrier tape should not exceed 0.1% of the total enclosed in the tape per reel, or 1, Whichever may be larger.There should never be more than two consecutive missing IC package.

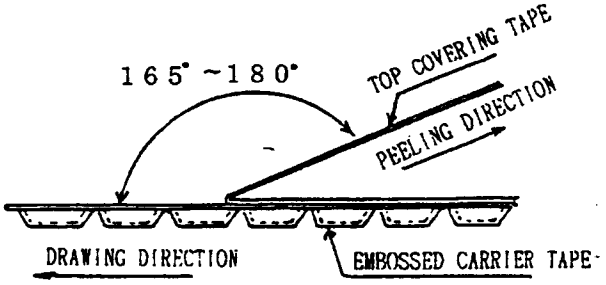
4－5. Tape Joints

・The embossed carrier tape should not have more than one joint per reel.

4－6. Peeling Strength of the Top Covering Tape

・Peeling strength must meet the following conditions.

1) Peeling angle
   at 165° to 180°
2) Peeling speed
   at 300mm/min.
3) Peeling strength
   at 0.2 to 0.7N(20 to 70gf)



4－7. Packing

- The top covering tape (leader side) at the leading edge of the embossed carrier tape, and the trailing edge of the embossed carrier tape, shall be held in place with paper adhesive tape exceeding 30mm in length.
- The leading and trailing edges of the embossed carrier tape shall be left empty (with embossed portions not filled with IC packages), in the attached drawing (NO. CV522).
- The number of IC packages enclosed in the embossed carrier tape per reel shall, in principle, be as listed below.

Package Type	Number of IC Packages/Reel
SOP14-P-225	2,500 pcs
SOP16-P-225	2,500 pcs
SOP24-P-450	1,500 pcs
SOP28-P-450	1,000 pcs
SOP32-P-525	1,000 pcs
SOP44-P-600	750 pcs
TSOP48-P-1220	1,000 pcs

4－8. Indications

- The following shall be indicated on the taping reel and the packing case.
  1) Part Numger (Product Name)
  2) Storage Quantity
  3) Production Date
  4) Manufacture's Name (SHARP)

4－9. Protection While in Transit

Embossed carrier tape should be free from deformed IC leads and deterioration in electrical characteristics.

5. Packing Specification (Dry packing for surface mount packages)

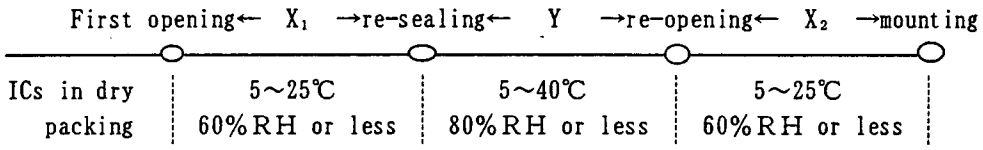
Dry packing is used for the purpose of maintaining IC quality after mounting packages on the PCB (Printed Circuit Board).

When the epoxy resin which is used for plastic packages is stored at high humidity, it may absorb 0.15% or more of its weight in moisture. If the surface mount type package for a relatively large chip absorbs a large amount of moisture between the epoxy resin and insert material (e.g. chip, lead frame) this moisture may suddenly vaporize into steam when the entire package is heated during the soldering process (e.g. VPS). This causes expansion and results in separation between the resin and insert material, and sometimes cracking of the package. This dry packing is designed to prevent the above problem from occurring in surface mount packages. Please conform to the following conditions concerning the storage and opening of dry packing.

5－1. Store under conditions shown below before opening the dry packing
(1) Temperature range : 5～40℃
(2) Humidity : 80% RH or less

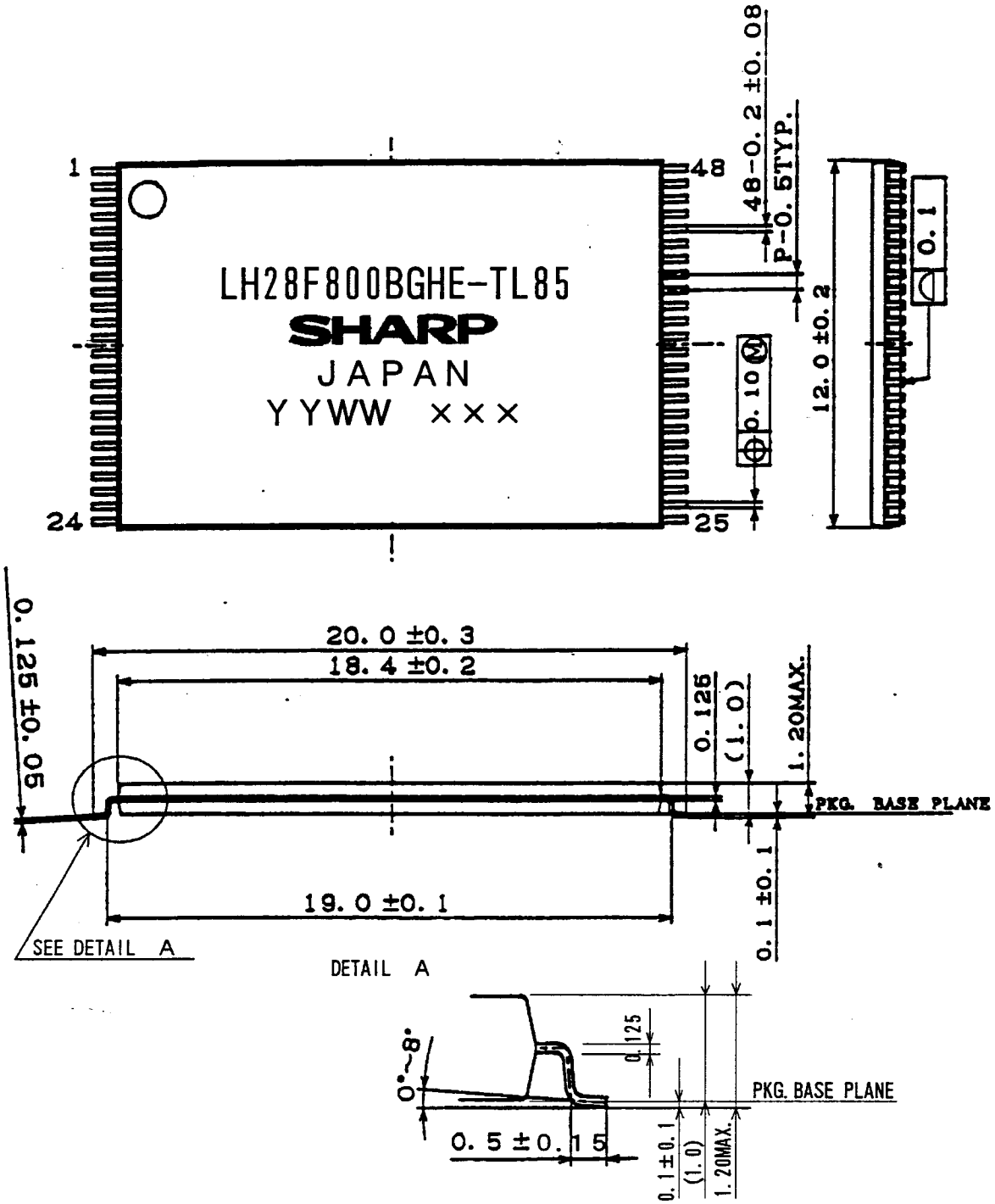
5－2. Notes on opening the dry packing
Before opening the dry packing, prepare a working table which is grounded against ESD and use a grounding strap.

5－3. Storage after opening the dry packing
Perform the following to prevent absorption of moisture after opening.
(1) After opening the dry packing, store the ICs in an environment with a temperature of 5～25℃ and a relative humidity of 60% or less and mount ICs within 3 days after opening dry packing.
(2) To re-store the ICs for an extended period of time within 3 days after opening the dry packing, use a dry box or re-seal the ICs in the dry packing with desiccant (whoes indicater is blue), and store in an environment with a temperature of 5～40℃ and a relative humidity of 80% or less, and mount ICs within 2 weeks.
(3) Total period of storage after first opening and re-opening is within 3 days, and store the ICs in the same environment as section 5-3.(1).



X_1+X_2 : within 3 days
Y : within 2 weeks

5－4. Baking (drying) before mounting
(1) Baking is necessary
(A) If the humidity indicator in the desiccant becomes pink
(B) If the procedure in section 5－3 could not be performed
(2) Recommended baking conditions
If the above conditions (A) and (B) are applicable, bake it before mounting. The recommended conditions are 16～24 hours at 120℃ or 5～10 hours at 150℃. Note that the embossed carrier tape can not be baked at the above temperature. Please transfar ICs to heat resistant carrier.
(3) Storage after baking
After baking ICs, store the ICs in the same environment as section 5-3.(1).

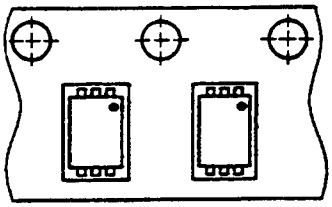


名称 NAME	TSOP48-P-1220	リード仕上 LEAD FINISH	TIN-LEAD PLATING	備考 NOTE プラスチックパッケージ外形寸法は、バリを含まないものとする。 Plastic body dimensions do not include burr of resin.
DRAWING NO.	AA1142	単位 UNIT	mm	

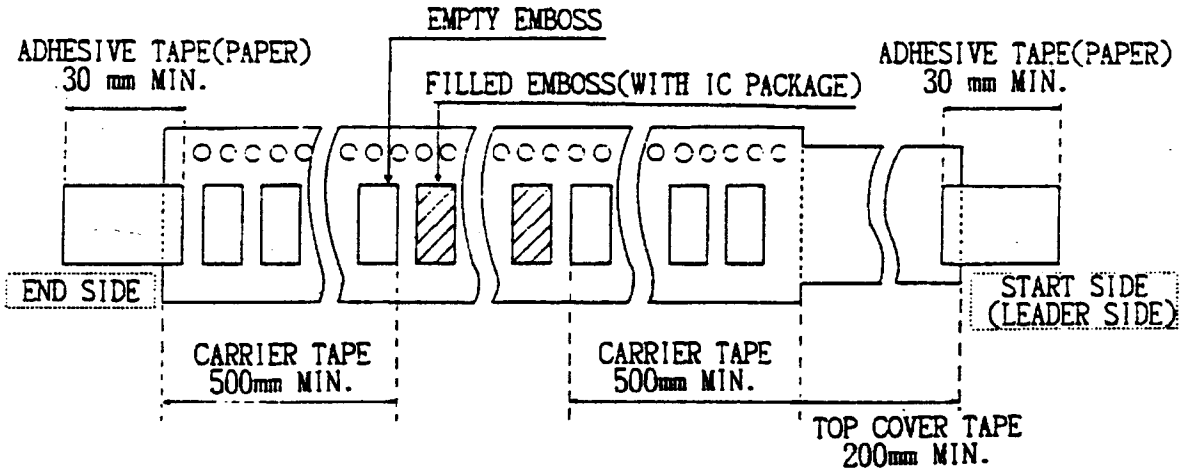
EMBOSS TAPING TYPE

IC TAPING DIRECTION

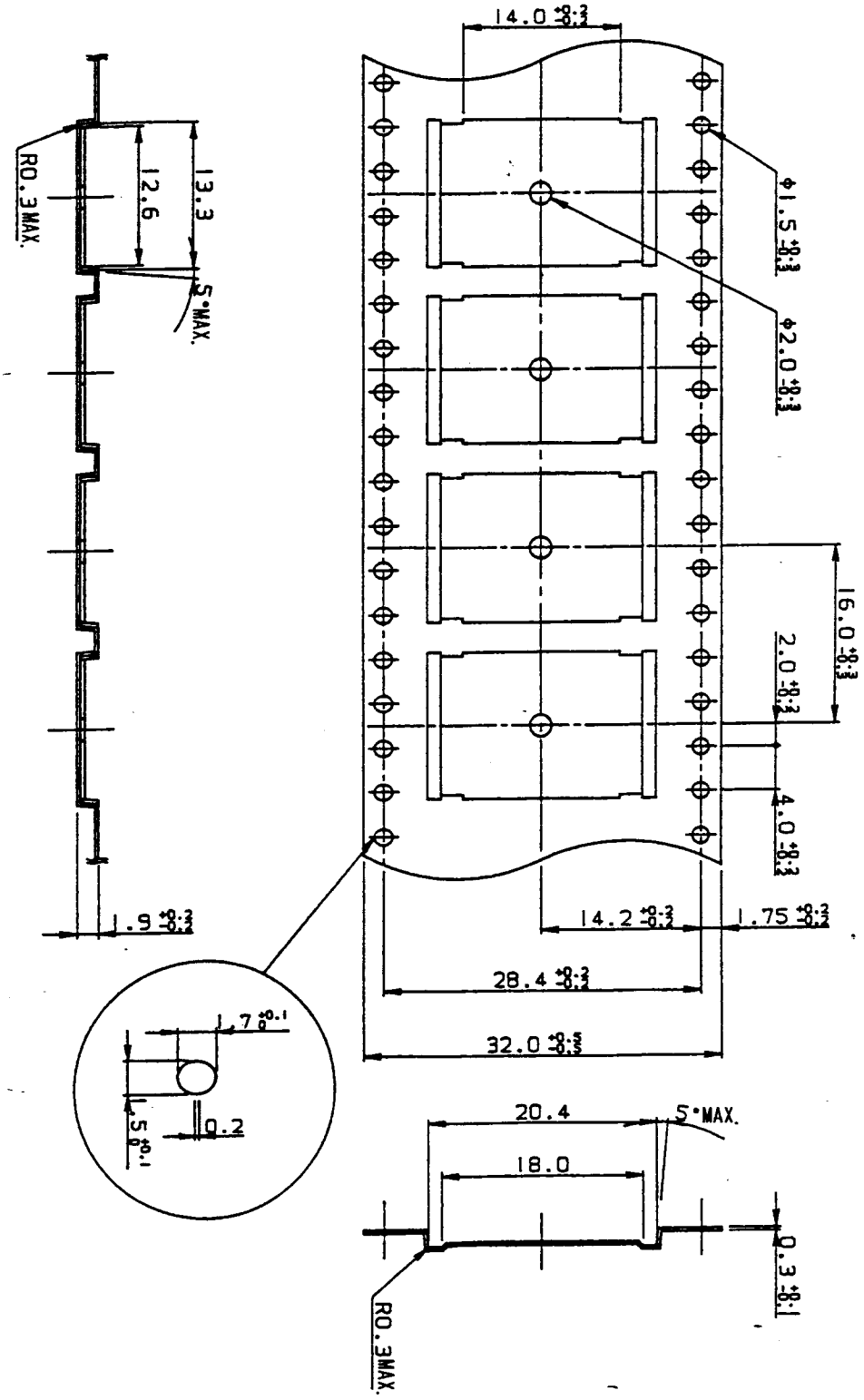
THE DRAWING DIRECTION OF TAPE →



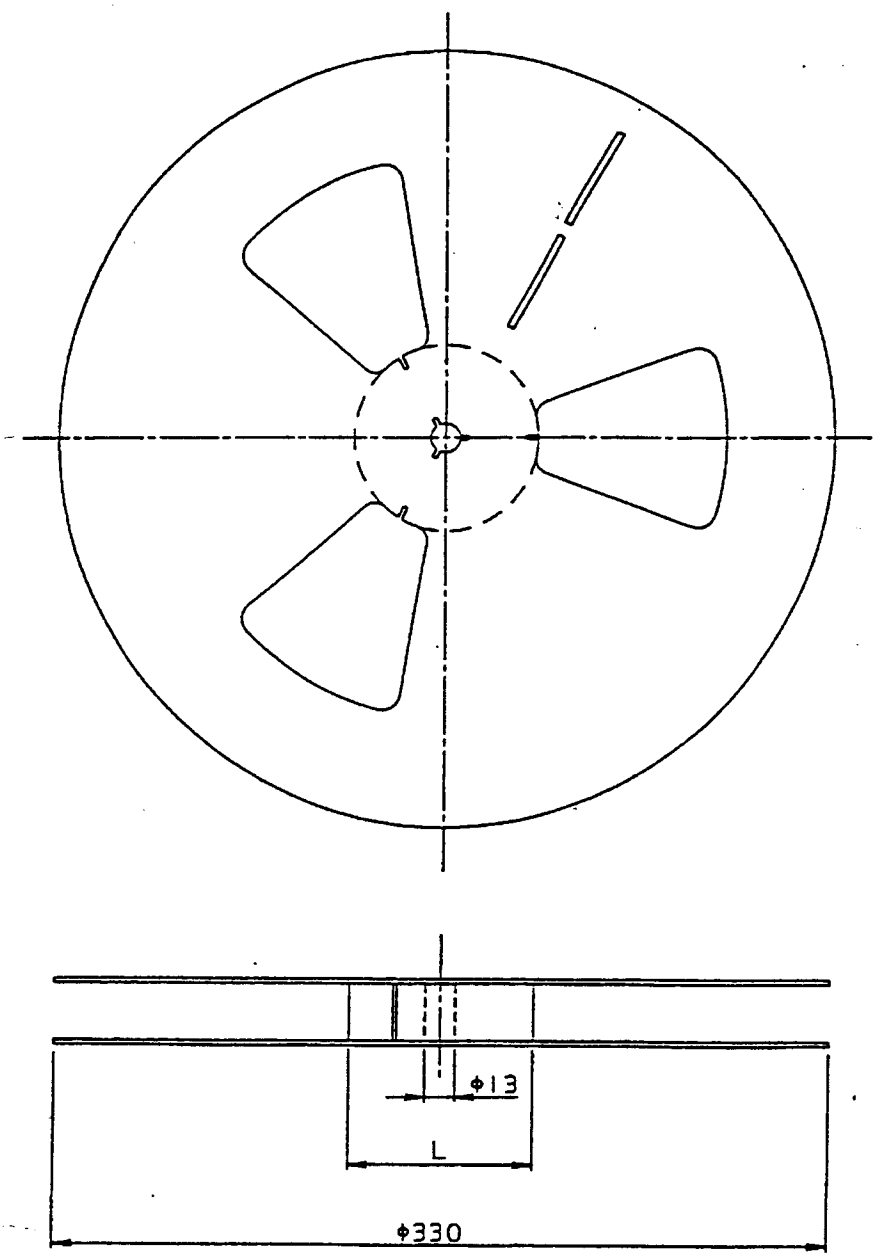
LEADER SIDE AND END SIDE OF TAPE



名称 NAME	EMBOSS TAPING TYPE			備考 NOTE
DRAWING NO.	CV522	単位 UNIT	mm	

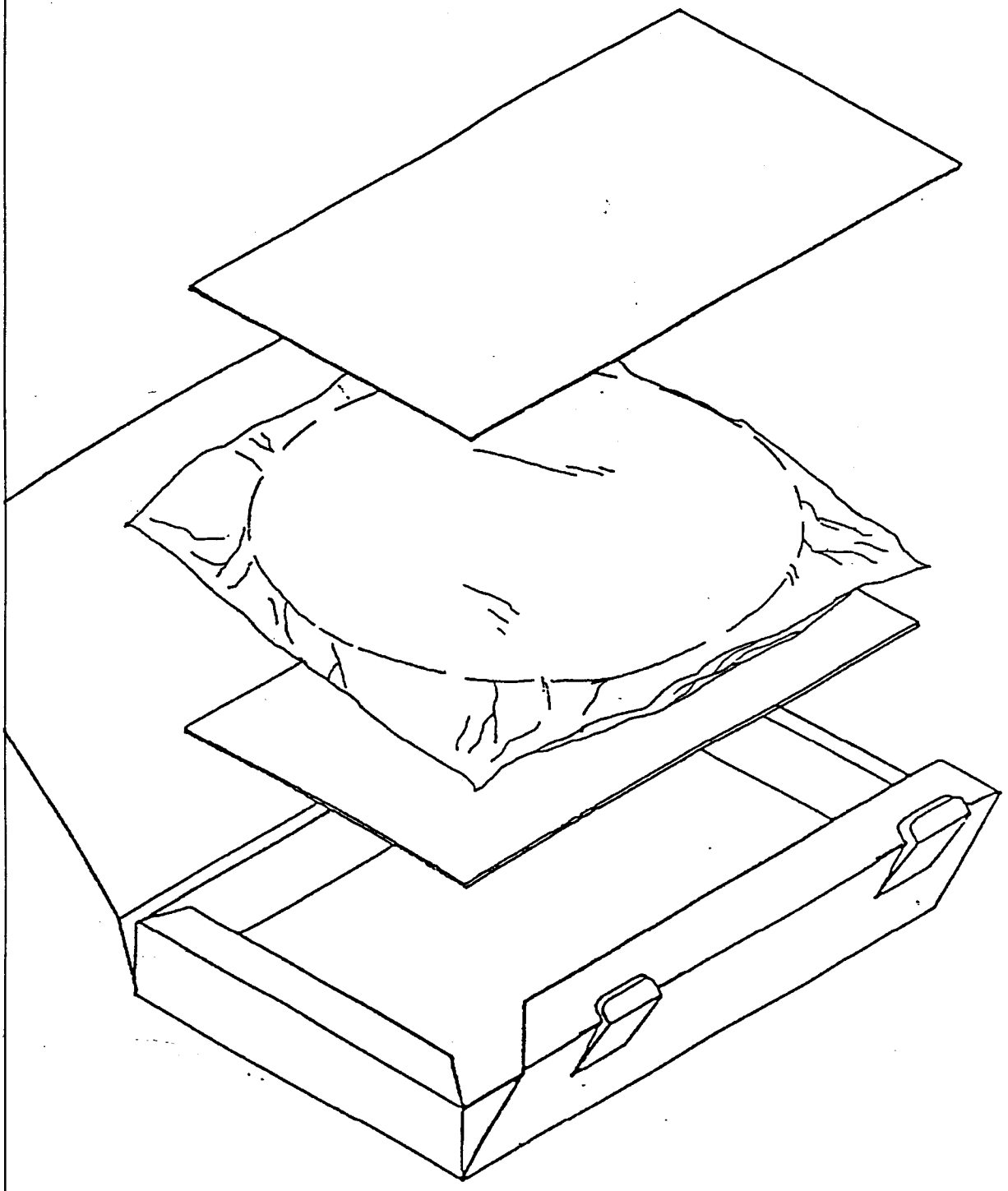


名称 NAME	EC48−1220TSPTS			備考 NOTE
DRAWING NO.	CV758	単位 UNIT	mm	



PKG	L (mm)
TSOP48-P-1220	φ100

名称 NAME	REEL FOR EMBOSS CARRIER TAPING		備考 NOTE
DRAWING NO.	CV521	単位 UNIT	mm



CASE SIZE : 345×345×55 (mm)

名称 NAME	EXTERNAL APPEARANCE OF PACKING CASE FOR EMBOSS CARRIER TAPING			備考 NOTE
DRAWING NO.	BJ279	単位 UNIT	mm	

Flash, Non Volatile, ETOX, Boot Block, Smart Voltage, 8 Mbit, LH28F800BGHE-TL85