SHARP

PRELIMINARY

April 1996

FLASH MEMORY

LH28F400SUT-LC12

SHARP CORPORATION

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LH28F400SUT-LC12
4 Mbit (512 Kbit x 8, 256 Kbit x 16)
3.3V (V_{PP}=5V) Flash Memory

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LH28F400SUT-LC12
4 MBIT (512 KBIT x 8, 256 KBIT x 16)
3.3V (V_{PP}=5V) FLASH MEMORY

FEATURES

- 32 Independently Lockable Blocks
- 100,000 Erase Cycles per Block
- 5V Write/Erase Operation (5V V_{PP}, 3.3V V_{CC})
  - No Requirement for DC/DC Converter to Write/Erase
- User-Configurable x8 or x16 Operation
- 120 ns Maximum Access Time (V_{CC} = 3.3V ± 0.3V)
- Min. 2.7V Read Capability
  - 160 ns Maximum Access Time (V_{CC} = 2.7V)
- Automated Byte Write/Block Erase
  - Command User Interface
  - Status Register
  - RY/BY# Status Output
- 56-Lead, 1.2mm x 14mm x 20mm TSOP Package
- System Performance Enhancement
  - Erase Suspend for Read
  - Two-Byte Write
  - Full Chip Erase
- Data Protection
  - Hardware Erase/Write Lockout during Power Transitions
  - Software Erase/Write Lockout
- Independently Lockable for Write/Erase on Each Block (Lock Block & Protect Set/Reset)
- 4 µA (Typ.) I_{CC} in CMOS Standby
- 0.2 µA (Typ.) Deep Power-Down
- State-of-the-Art 0.55 µm ETOX™* Flash Technology
- Not designed or rated as radiation hardened

Sharp's LH28F400SUT-LC12 4-Mbit Flash Memory is a revolutionary architecture which enables the design of truly mobile, high performance, personal computing and communication products. With innovative capabilities, 3.3V low power operation and very high read/write performance, the LH28F400SUT-LC12 is also the ideal choice for designing embedded mass storage flash memory systems.

The LH28F400SUT-LC12's independently lockable 32 symmetrical blocked architecture (16-Kbyte each) extended cycling, low power operation, very fast write and read performance and selective block locking provide a highly flexible memory component suitable for Cellular phone, Facsimile, Game, PC, Printer and Handy terminal. The LH28F400SUT-LC12's 5.0V/3.3V power supply operation enables the design of memory cards which can be read in 3.3V system and written in 5.0V/3.3V systems. Its x8/x16 architecture allows the optimization of memory to processor interface. The flexible block locking option enables bundling of executable application software in a Resident Flash Array or memory card. Manufactured on Sharp's 0.55 µm ETOX™ process technology, the LH28F400SUT-LC12 is the most cost-effective, high-density 3.3V flash memory.

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* ETOX is a trademark of Intel corporation.

PRELIMINARY

1.0 INTRODUCTION

The data sheet is intended to give an overview of the chip feature-set and of the operating AC/DC specifications.

1.1 Product Overview

The LH28F400SUT-LC12 is a high performance 4-Mbit (4,194,304 bit) block erasable non-volatile random access memory organized as either 256 Kword x 16 or 512 Kbyte x 8. The LH28F400SUT-LC12 includes thirty-two 16 KB (16,384) blocks. A chip memory map is shown in Figure 3.

The implementation of a new architecture, with many enhanced features, will improve the device operating characteristics and results in greater product reliability and ease of use.

Among the significant enhancements of the LH28F400SUT-LC12:

- 3V Read, 5V Write/Erase Operation (5V V_{PP}, 3V V_{CC})
- Low Power Capability (2.7V V_{CC} Read)
- Improved Write Performance
- Dedicated Block Write/Erase Protection
- Command-Controlled Memory Protection Set/Reset Capability

The LH28F400SUT-LC12 will be available in a 56-lead, 1.2mm thick, 14mm x 20mm TSOP type 1 package. This form factor and pinout allow for very high board layout densities.

A Command User Interface (CUI) serves as the system interface between the microprocessor or microcontroller and the internal memory operation.

Internal Algorithm Automation allows Byte Writes and Block Erase operations to be executed using a Two-Write command sequence to the CUI in the same way as the LH28F008SA 8-Mbit Flash memory.

A Superset of commands have been added to the basic LH28F008SA command-set to achieve higher write performance and provide additional capabilities. These new commands and features include:

- Software Locking of Memory Blocks
- Memory Protection Set/Reset Capability
- Two-Byte Serial Writes in 8-bit Systems
- Erase All Unlocked Blocks

Writing of memory data is performed typically within 20 µsec per byte. Writing of memory data is performed typically within 30 µsec per word. A Block Erase operation erases one of the 32 blocks in typically 0.6 sec, independent of the other blocks.

LH28F400SUT-LC12 allows to erase all unlocked blocks. It is desirable in case of which you have to implement Erase operation max. 32 times.

LH28F400SUT-LC12 enables Two-Byte serial Write which is operated by three times command input. Writing of memory data is performed typically within 30 µsec per two-byte. This feature can improve 8-bit system write performance by up to typically 15 µsec per byte.

All operations are started by a sequence of Write commands to the device. Status Register (described in detail later) and a RY/BY# output pin provide information on the progress of the requested operation.

Same as the LH28F008SA, LH28F400SUT-LC12 requires an operation to complete before the next operation can be requested, also it allows to suspend block erase to read data from any other block, and allow to resume erase operation.

The LH28F400SUT-LC12 provides user-selectable block locking to protect code or data such as Device Drivers, PCMCIA card information, ROM-Executable OS or Application Code. Each block has an associated non-volatile lock-bit which determines the lock status of the block. In addition, the LH28F400SUT-LC12 has a software controlled master Write Protect circuit which prevents any modifications to memory blocks whose lock-bits are set.

When the device power-up or RP# turns High, Write Protect Set/Confirm command must be written. Otherwise, all lock bits in the device remain being locked, can't perform the Write to each block and single Block Erase. Write Protect Set/Confirm command must be written to reflect the actual lock status. However, when the device power-on or RP# turns High, Erase All Unlocked Blocks can be used. If used, Erase is performed with reflecting actual lock status, and after that Write and Block Erase can be used.

The LH28F400SUT-LC12 contains a Compatible Status Register (CSR) which is 100% compatible with the LH28F008SA Flash memory's Status Register. This register, when used alone, provides a straightforward upgrade capability to the LH28F400SUT-LC12 from a LH28F008SA-based design.

The LH28F400SUT-LC12 incorporates an open drain RY/BY# output pin. This feature allows the user to OR-tie many RY/BY# pins together in a multiple memory configuration such as a Resident Flash Array.

The LH28F400SUT-LC12 is specified for a maximum access time of 120 nsec (t_{ACC}) at 3.3V operation (3.0 to 3.6V) over the commercial temperature range (0 to +70°C). A corresponding maximum access time of 160 nsec (t_{ACC}) at 2.7V (0 to +70°C) is achieved for reduced power consumption applications.

The LH28F400SUT-LC12 incorporates an Automatic Power Saving (APS) feature which substantially reduces the active current when the device is in static mode of operation (addresses not switching).

In APS mode, the typical I_{CC} current is 1 mA at 3.3V.

A Deep Power-Down mode of operation is invoked when the RP# (called PWD# on the LH28F008SA) pin transitions low, any current operation is aborted and the device is put into the deep power down mode. This mode brings the device power consumption to less than 5 µA, and provides additional write protection by acting as a device reset pin during power transitions. When the power is turned on, RP# pin is turned to low in order to return the device to default configuration. When the power transition is occurred, or at the power on/off, RP# is required to stay low in order to protect data from noise. A recovery time of 620ns is required from RP# switching high until outputs are again valid. In the Deep Power-Down state, the WSM is reset (any current operation will abort) and the CSR register is cleared.

A CMOS Standby mode of operation is enabled when CE# transitions high and RP# stays high with all input control pins at CMOS levels. In this mode, the device draws an I_{CC} standby current of 8 µA.

2.0 DEVICE PINOUT

The LH28F400SUT-LC12 56-Lead TSOP Type I pinout configuration is shown in Figure 2.

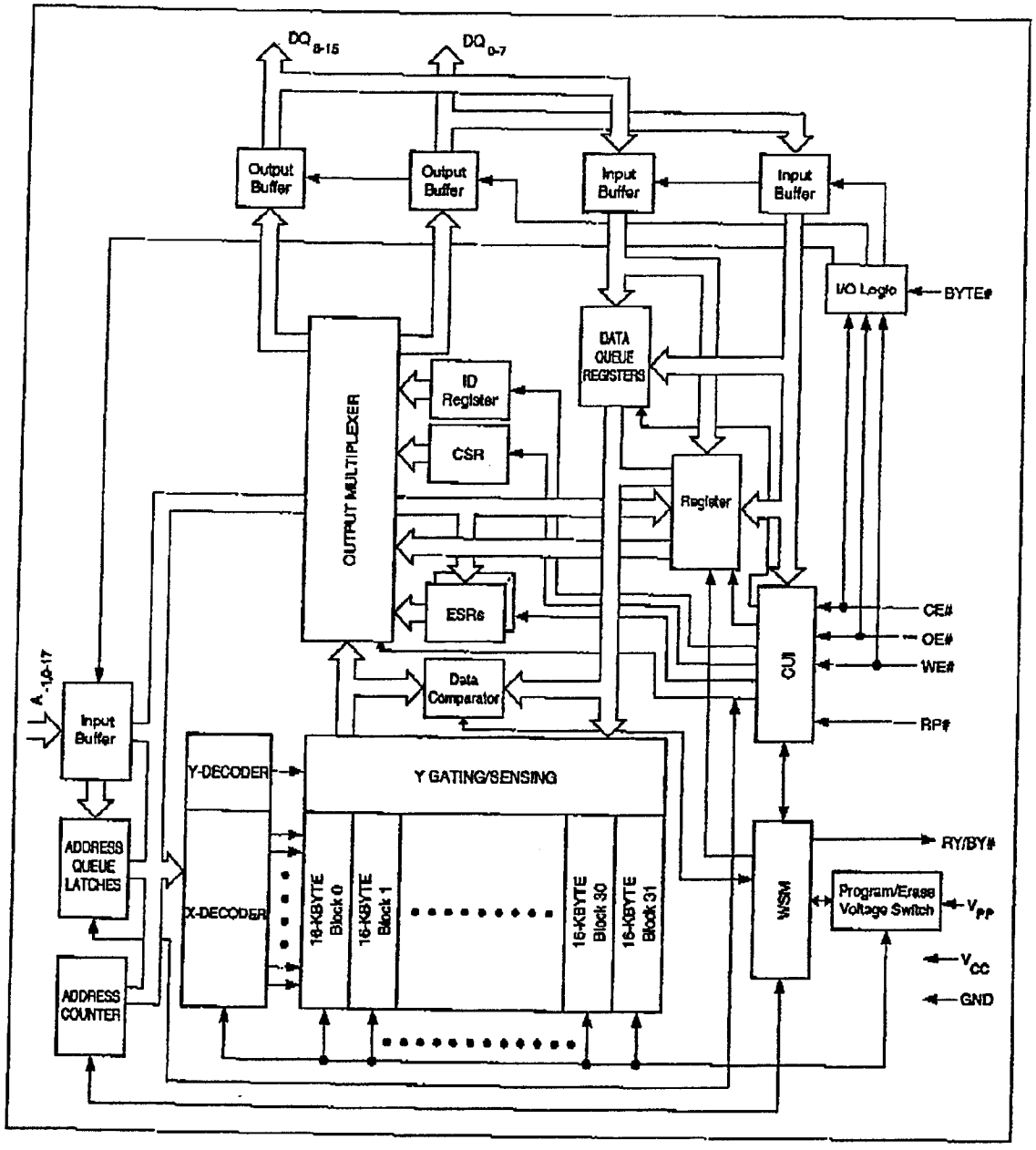

Figure 1. LH28F400SUT-LC12 Block Diagram

2.1 Lead Descriptions

Symbol	Type	Name and Function
DQ_{15}/A_{-1}	INPUT	**BYTE-SELECT ADDRESS:** Selects between high and low byte when device is in x8 mode. This address is latched in x8 Data Writes. Not used in x16 mode (i.e., the DQ_{15}/A_{-1} input buffer is turned off when BYTE# is high).
A_0-A_{12}	INPUT	**WORD-SELECT ADDRESSES:** Select a word within one 16-Kbyte block. These addresses are latched during Data Writes.
A_{13}-A_{17}	INPUT	**BLOCK-SELECT ADDRESSES:** Select 1 of 32 Erase blocks. These addresses are latched during Data Writes, Erase and Lock-Block operations.
DQ_0-DQ_7	INPUT/OUTPUT	**LOW-BYTE DATA BUS:** Inputs data and commands during CUI write cycles. Outputs array, buffer, identifier or status data in the appropriate Read mode. Floated when the chip is de-selected or the outputs are disabled.
DQ_8-DQ_{15}	INPUT/OUTPUT	**HIGH-BYTE DATA BUS:** Inputs data during x16 Data-Write operations. Outputs array, buffer or identifier data in the appropriate Read mode; not used for Status register reads. Floated when the chip is de-selected or the outputs are disabled. DQ_{15}/A_{-1} is address.
CE#	INPUT	**CHIP ENABLE INPUTS:** Activate the device's control logic, input buffers, decoders and sense amplifiers. CE# must be low to select the device.
RP#	INPUT	**RESET/POWER-DOWN:** With RP# low,the device is reset, any current operation is aborted and device is put into the deep power down mode. When the power is turned on, RP# pin is turned to low in order to return the device to default configuration. When the power transition is occurred, or the power on/off, RP# is required to stay low in order to protect data from noise. When returning from Deep Power-Down, a recovery time of 620 ns is required to allow these circuits to power-up. When RP# goes low, any current or pending WSM operation(s) are terminated, and the device is reset. All Status registers return to ready (with all status flags cleared). After returning, the device is in read array mode.
OE#	INPUT	**OUTPUT ENABLE:** Gates device data through the output buffers when low. The outputs float to tri-state off when OE# is high.
WE#	INPUT	**WRITE ENABLE:** Controls access to the CUI, Data Queue Registers and Address Queue Latches. WE# is active low, and latches both address and data (command or array) on its rising edge.
RY/BY#	OPEN DRAIN OUTPUT	**READY/BUSY:** Indicates status of the internal WSM. When low, it indicates that the WSM is busy performing an operation. When the WSM is ready for new operation or Erase is Suspended, or the device is in deep power-down mode RY/BY# pin is floated.
BYTE#	INPUT	**BYTE ENABLE:** BYTE# low places device in x8 mode. All data is then input or output on DQ_{0-7}, and DQ_{8-15} float. Address A_{-1} selects between the high and low byte. BYTE# high places the device in x16 mode, and turns off the A_{-1} input buffer. Address A_0, then becomes the lowest order address.
V_{PP}	SUPPLY	**ERASE/WRITE POWER SUPPLY (5.0V ± 0.5V):** For erasing memory array blocks or writing words/bytes into the flash array.
V_{CC}	SUPPLY	**DEVICE POWER SUPPLY (3.3V ± 0.3V):** Do not leave any power pins floating.
GND	SUPPLY	**GROUND FOR ALL INTERNAL CIRCUITRY:** Do not leave any ground pins floating.
NC		**NO CONNECT:** No internal connection to die, lead may be driven or left floating.

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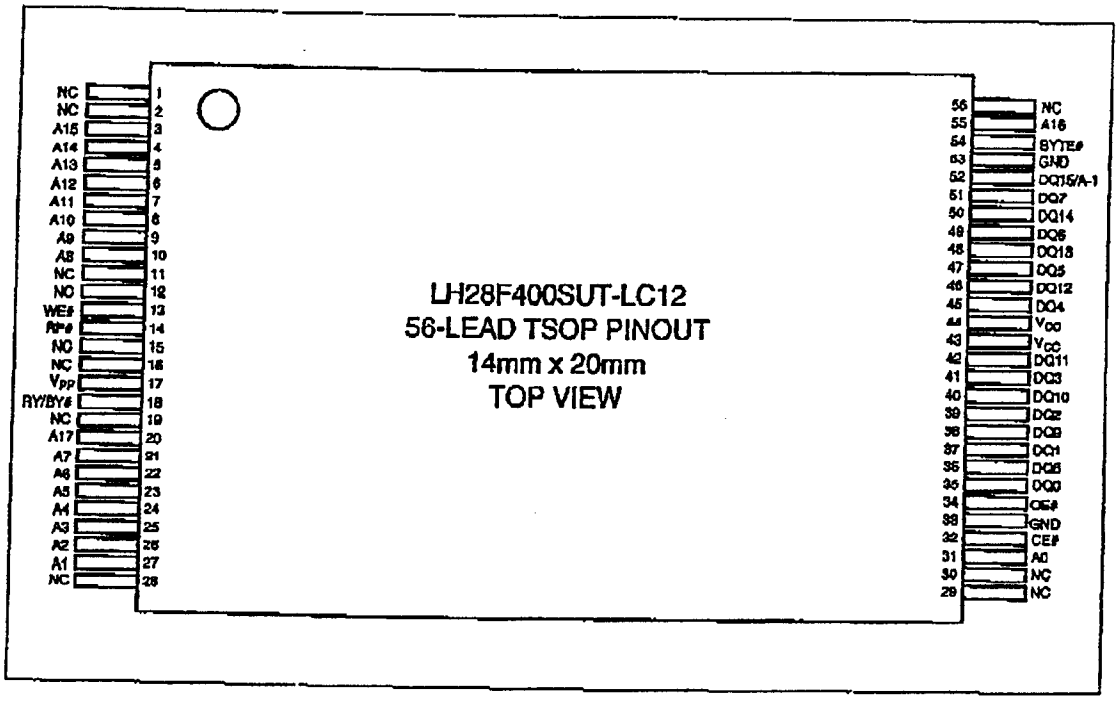

Figure 2. TSOP Configuration

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3.0 MEMORY MAPS

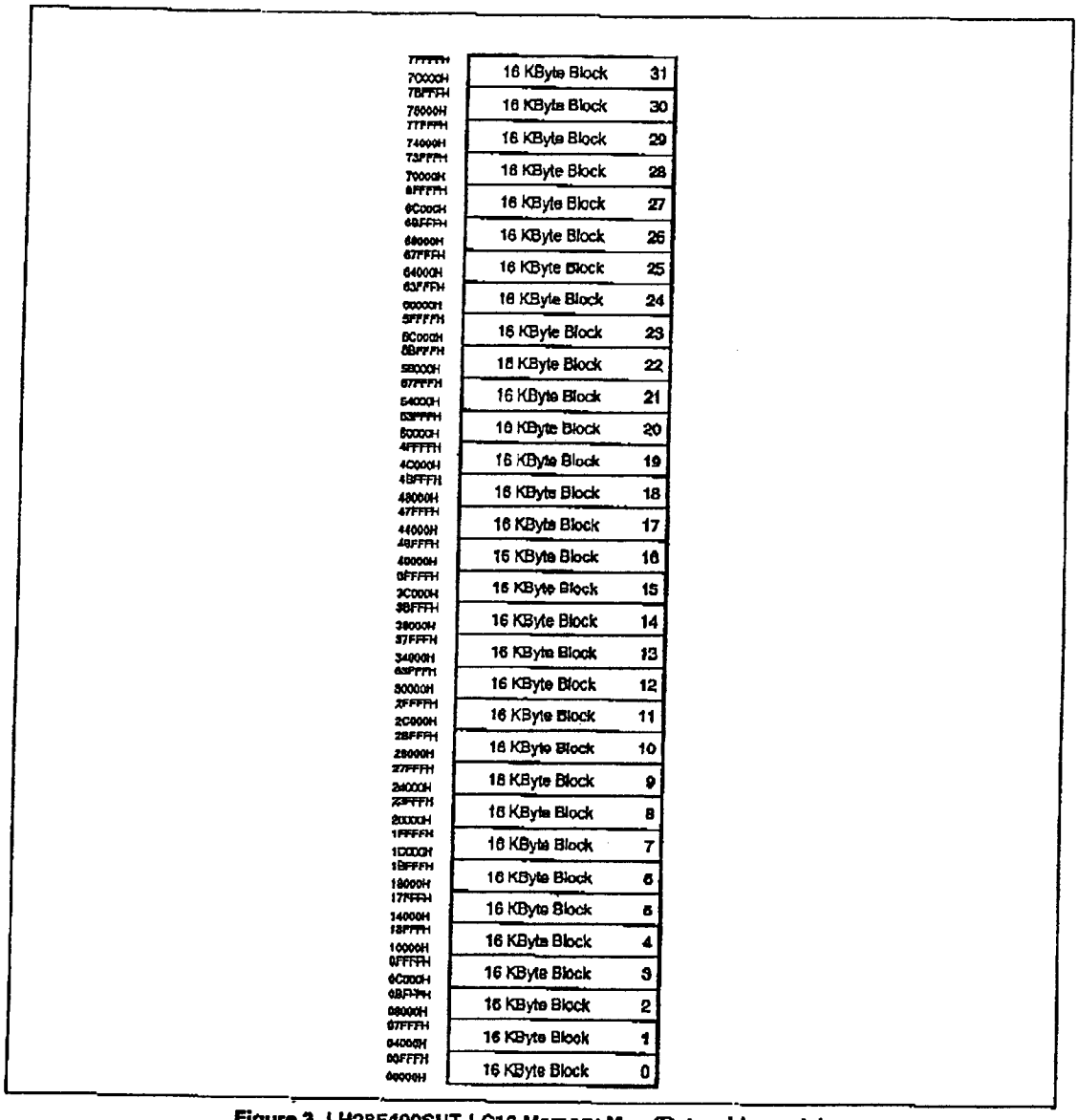


Figure 3. LH28F400SUT-LC12 Memory Map (Byte-wide mode)

*** In Byte-wide (x8) mode A_{-1} is the lowest order address.**
In Word-wide (x16) mode A_{-1} don't care, address values are ignored A_{-1}.

4.0 BUS OPERATIONS, COMMANDS AND STATUS REGISTER DEFINITIONS

4.1 Bus Operations for Word-Wide Mode (Byte#=V_{IH})

Mode	Notes	RP#	CE#	OE#	WE#	A_0	DQ_{0-15}	RY/BY#
Read	1,2,7	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}	X
Output Disable	1,6,7	V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	High Z	X
Standby	1,6,7	V_{IH}	V_{IH}	X	X	X	High Z	X
Deep Power-Down	1,3	V_{IL}	X	X	X	X	High Z	V_{OH}
Manufacturer ID	4	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	00B0H	V_{OH}
Device ID	4	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	ID	V_{OH}
Write	1,5,6	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	D_{IN}	X

4.2 Bus Operations for Byte-Wide Mode (Byte#=V_{IL})

Mode	Notes	RP#	CE#	OE#	WE#	A_0	DQ_{0-7}	RY/BY#
Read	1,2,7	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}	X
Output Disable	1,6,7	V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	High Z	X
Standby	1,6,7	V_{IH}	V_{IH}	X	X	X	High Z	X
Deep Power-Down	1,3	V_{IL}	X	X	X	X	High Z	V_{OH}
Manufacturer ID	4	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	B0H	V_{OH}
Device ID	4	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	ID	V_{OH}
Write	1,5,6	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	D_{IN}	X

NOTES:

1. X can be V_{IH} or V_{IL} for address or control pins except for RY/BY#, which is either V_{OL} or V_{OH}.
2. RY/BY# output is open drain. When the WSM is ready, Erase is suspended or the device is in deep power-down mode, RY/BY# will be at V_{OH} if it is tied to V_{CC} through a resistor. When the RY/BY# at V_{OL} is independent of OE# while a WSM operation is in progress.
3. RP# at GND ± 0.2V ensures the lowest deep power-down current.
4. A_0 at V_{IL} provide manufacturer ID codes.
   A_0 at V_{IH} provide device ID codes. Device ID Code = 23H (x8), Device ID Code = 8823H (x16).
   All other addresses are set to zero.
5. Commands for different Erase operations, Data Write operations, and Lock-Block operations can only be successfully completed when $V_{PP} = V_{PPH}$.
6. While the WSM is running, RY/BY# in Level-Mode (default) stays at V_{OL} until all operations are complete. RY/BY# goes to V_{OH} when the WSM is not busy or in erase suspend mode.
7. RY/BY# may be at V_{OL} while the WSM is busy performing various operations. For example, a status register read during a write operation.

4.3 LH28F008SA-Compatible Mode Command Bus Definitions

Command	Notes	First Bus Cycle			Second Bus Cycle		
		Oper	Addr	Data	Oper	Addr	Data
Read Array		Write	X	FFH	Read	AA	AD
Intelligent Identifier	1	Write	X	90H	Read	IA	ID
Read Compatible Status Register	2	Write	X	70H	Read	X	CSRD
Clear Status Register	3	Write	X	50H			
Word Write		Write	X	40H	Write	WA	WD
Alternate Word Write		Write	X	10H	Write	WA	WD
Block Erase/Confirm	4	Write	X	20H	Write	BA	D0H
Erase Suspend/Resume	4	Write	X	B0H	Write	X	D0H

ADDRESS
AA = Array Address
BA = Block Address
IA = Identifier Address
WA = Write Address
X = Don't Care

DATA
AD = Array Data
CSRD = CSR Data
ID = Identifier Data
WD = Write Data

NOTES:
1. Following the Intelligent identifier command, two Read operations access the manufacturer and device signature codes.
2. The CSR is automatically available after device enters Data Write, Erase, or Suspend operations.
3. Clears CSR.3, CSR.4 and CSR.5. See Status register definitions.
4. While device performs Block Erase, If you issue Erase Suspend command (B0H), be sure to confirm ESS (Erase-Suspend-Status) is set to 1 on compatible status register. In the case, ESS bit was not set to 1, also completed the Erase (ESS=0, WSMS=1), be sure to issue Resume command (D0H) after completed next Erase command. Beside, when the Erase Suspend command is issued, while the device is not in Erase, be sure to issue Resume command (D0H) after the next erase completed.

4.4 LH28F400SUT-LC12-Performance Enhancement Command Bus Definitions

Command	Mode	Notes	First Bus Cycle			Second Bus Cycle			Third Bus Cycle		
			Oper	Addr	Data	Oper	Addr	Data	Oper	Addr	Data
Protect Set/Confirm		1,2	Write	X	57H	Write	0FFH	D0H			
Protect Reset /Confirm		3	Write	X	47H	Write	0FFH	D0H			
Lock Block/Confirm		1,2,4	Write	X	77H	Write	BA	D0H			
Erase All Unlocked Blocks		1,2	Write	X	A7H	Write	X	D0H			
Two-Byte Write	x8	1,2,5	Write	X	FBH	Write	A -1	WD(L,H)	Write	WA	WD(H,L)

ADDRESS
BA = Block Address
WA = Write Address

DATA
AD = Array Data
WD (L,H) = Write Data (Low, High)
WD (H,L) = Write Data (High, Low)

X = Don't Care

NOTES:
1. After initial device power-up, or return from deep power-down mode, the block lock status bits default to the locked state independent of the data in the corresponding lock bits. In order to upload the lock bit status, it requires to write Protect Set/Confirm command.
2. To reflect the actual lock-bit status, the Protect Set/Confirm command must be written after Lock Block/Confirm command.
3. When Protect Reset/Confirm command is written, all blocks can be written and erased regardless of the state of the lock-bits.
4. The Lock Block/Confirm command must be written after Protect Reset/Confirm command was written.
5. A_{-1} is automatically complemented to load second byte of data. A_{-1} value determines which WD is supplied first: A_{-1} = 0 looks at the WDL, A_{-1} = 1 looks at the WDH. In word-wide (x16) mode A_{-1} don't care.
6. Second bus cycle address of Protect Set/Confirm and Protect Reset/Confirm command is 0FFH. Specifically A_0-A_6 = 0, A_7-A_8 = 1, others are don't care.

4.5 Compatible Status Register

WSMS	ESS	ES	DWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

CSR.7 = WRITE STATE MACHINE STATUS (WSMS)
1 = Ready
0 = Busy

CSR.6 = ERASE-SUSPEND STATUS (ESS)
1 = Erase Suspended
0 = Erase in Progress/Completed

CSR.5 = ERASE STATUS (ES)
1 = Error in Block Erasure
0 = Successful Block Erase

CSR.4 = DATA-WRITE STATUS (DWS)
1 = Error in Data Write
0 = Data Write Successful

CSR.3 = V_{PP} STATUS (VPPS)
1 = V_{PP} Low Detect, Operation Abort
0 = V_{PP} OK

NOTES:

RY/BY# output or WSMS bit must be checked to determine completion of an operation (Erase Suspend, Erase or Data Write) before the appropriate Status bit (ESS, ES or DWS) is checked for success.

If DWS and ES are set to "1" during an erase attempt, an improper command sequence was entered. Clear the CSR and attempt the operation again.

The VPPS bit, unlike an A/D converter, does not provide continuous indication of V_{PP} level. The WSM interrogates V_{PP}'s level only after the Data-Write or Erase command sequences have been entered, and informs the system if V_{PP} has not been switched on. VPPS is not guaranteed to report accurate feedback between V_{PPL} and V_{PPH}.

CSR.2-0 = RESERVED FOR FUTURE ENHANCEMENTS
These bits are reserved for future use and should be masked out when polling the CSR.

5.0 4M FLASH MEMORY SOFTWARE ALGORITHMS

5.1 Overview

With the advanced Command User Interface, its Performance Enhancement commands and Status Registers, the software code required to perform a given operation may become more intensive but it will result in much higher write/erase performance compared with current flash memory architectures.

The software flowcharts describing how a given operation proceeds are shown here. Figures 5-1 through 5-3 depict flowcharts using the 2nd generation flash device in the LH28F008SA-compatible mode. Figures 5-4 through 5-9 depict flowcharts using the 2nd generation flash device's performance enhancement commands mode.

When the device power-up or the device is reset by RP# pin, all blocks come up locked. Therefore, Word/Byte Write, Two Byte Serial Write and Block Erase can not be performed in each block. However, at that time, Erase All Unlocked Block is performed normally, if used, and reflect actual lock status, also the unlocked block data is erased. When the device power-up or the device is reset by RP# pin, Set Write Protect command must be written to reflect actual block lock status.

Reset Write Protect command must be written before Write Block Lock command. To reflect actual block lock status, Set Write Protect command is succeeded.

The Compatible Status Register (CSR) is used to determine which blocks are locked. In order to see Lock Status of a certain block, a Word/Byte Write command (WA=Block Address, WD=FFH) is written to the CUI, after issuing Set Write Protect command. If CSR7, CSR5 and CSR4 (WSMS, ES and DWS) are set to "1"s, the block is locked. If CSR7 is set to "1", the block is not locked.

Reset Write Protect command enables Write/Erase operation to each block.

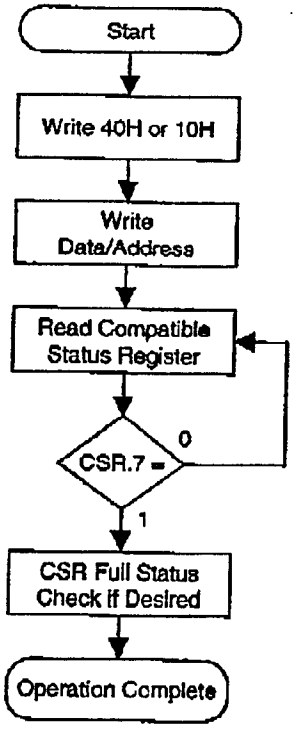
In the case of Block Erase is performed, the block lock information is also erased. Block Lock command and Set Write Protect command must be written to prohibit Write/Erase operation to each block.

There are unassigned commands. It is not recommended that the customer use any command other than the valid commands specified in Chapter 4 "Command Bus Definitions". Sharp reserved the right to redefine these codes for future functions.

5.2 4M Flash Memory Algorithm Flowcharts

The following flowcharts describe the 2nd generation flash device modes of operation:

Figure 5-1	Word/Byte Writes with Compatible Status Register
Figure 5-2	Block Erase with Compatible Status Register
Figure 5-3	Erase Suspend to Read Array with Compatible Status Register
Figure 5-4	Block Locking Scheme
Figure 5-5	Updating Data in a Locked Block
Figure 5-6	Two-Byte Serial Writes with Compatible Status Registers
Figure 5-7	Erase All Unlocked Blocks with Compatible Status Registers
Figure 5-8	Set Write Protect
Figure 5-9	Reset Write Protect



Bus Operation	Command	Comments
Write	Word/Byte Write	D = 40H or 10H A = X
Write		D = WD A = WA
Read		Q = CSRD Toggle CE# or OE# to update CSRD. A = X
Standby		Check CSR.7 1 = WSM Ready 0 = WSM Busy

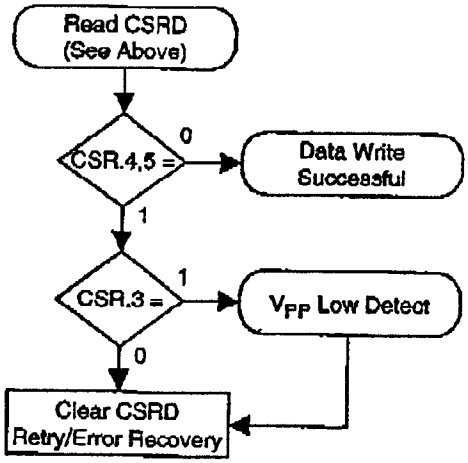
Repeat for subsequent Word/Byte Writes.

CSR Full Status Check can be done after each Word/Byte Write, or after a sequence of Word/Byte Writes.

Write FFH after the last operation to reset device to read array mode.

See Command Bus Cycle notes for description of codes.

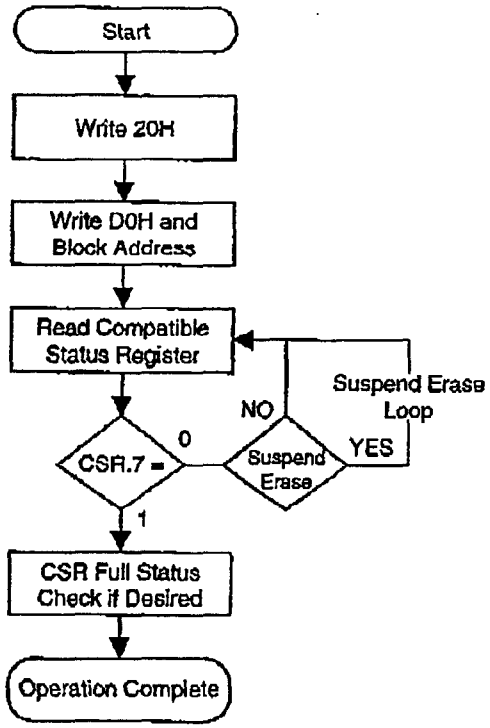
CSR FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check CSR.4,5 1 = Data Write Unsuccessful 0 = Data Write Successful
Standby		Check CSR.3 1 = V_{PP} Low Detect 0 = V_{PP} OK

CSR.3,4,5 SHOULD be cleared, if set, before further attempts are initiated.

Figure 5-1. Word/Byte Writes with Compatible Status Register



Bus Operation	Command	Comments
Write	Block Erase	D = 20H A = X
Write	Confirm	D = D0H A = BA
Read		Q = CSRD Toggle CE# or OE# to update CSRD. A = X
Standby		Check CSR.7 1 = WSM Ready 0 = WSM Busy

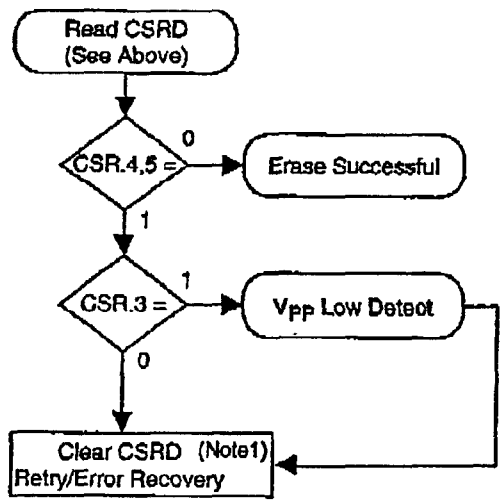
Repeat for subsequent Block Erasures.

CSR Full Status Check can be done after each Block Erase, or after a sequence of Block Erasures.

Write FFH after the last operation to reset device to read array mode.

See Command Bus Cycle notes for description of codes.

CSR FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check CSR.4,5 1 = Erase Error 0 = Erase Successful Both 1 = Command Sequence Error
Standby		Check CSR.3 1 = V_{PP} Low Detect 0 = V_{PP} OK

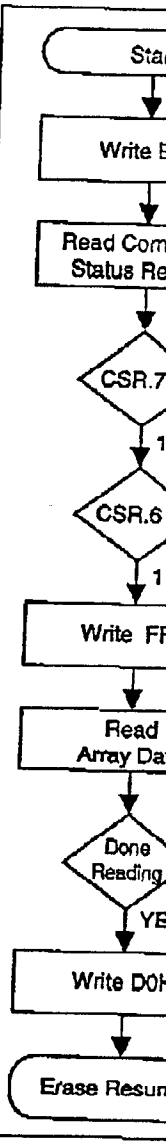
CSR.3,4,5 SHOULD be cleared, if set, before further attempts are initiated.

Note1. If CSR.3 (VPPS) is set to "1", after clearing CSR.3/4/5,
(1). Issue Reset WP command,
(2). Retry Single Block Erase command,
(3). Set WP command is issued, if necessary.

If CSR.3 (VPPS) is set to "0", after clearing CSR.3/4/5,
(1). Retry Single Block Erase command.

If power is off or RP# is set low during erase operation,
(1'). Clear CSR.3/4/5 and issue Reset WP command,
(2'). Retry Single Block Erase command,
(3'). Set WP command is issued, if necessary.

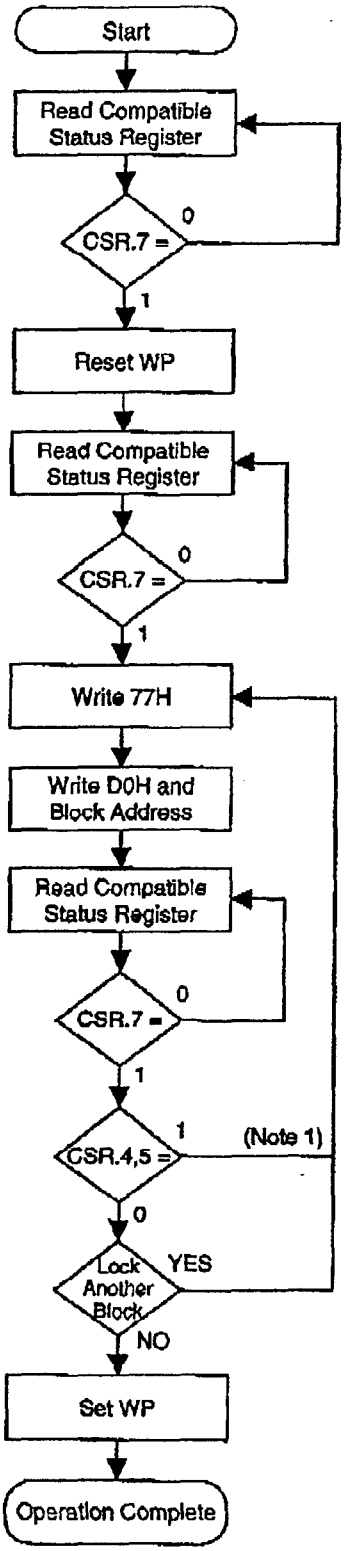
Figure 5-2. Block Erase with Compatible Status Register



Bus Operation	Command	Comments
Write	Erase Suspend	D = B0H A = X
Read		Q = CSRD Toggle CE# or OE# to update CSRD. A = X
Standby		Check CSR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check CSR.6 1 = Erase Suspended 0 = Erase Completed
Write	Read Array	D = FFH A= X
Read		Q = AD Read must be from block other than the one suspended.
Write	Erase Resume	D = D0H A = X

See Command Bus Cycle notes for description of codes.

Figure 5-3. Erase Suspend to Read Array with Compatible Status Register



Bus Operation	Command	Comments
Read		Q = CSRD Toggle CE# or OE# to update CSRD. 1 = WSM Ready 0 = WSM Busy
Write	Reset Write Protect	After Write D = 47H A = X, Write D = D0H A = 0FFH
Read		Q = CSRD Toggle CE# or OE# to update CSRD. 1 = WSM Ready 0 = WSM Busy
Write	Lock Block	D = 77H A = X
Write	Confirm	D = D0H A = BA
Read		Q = CSRD Toggle CE# or OE# to update CSRD. 1 = WSM Ready 0 = WSM Busy
Write	Set Write Protect	After Write D = 57H A = X, Write D = D0H A = 0FFH

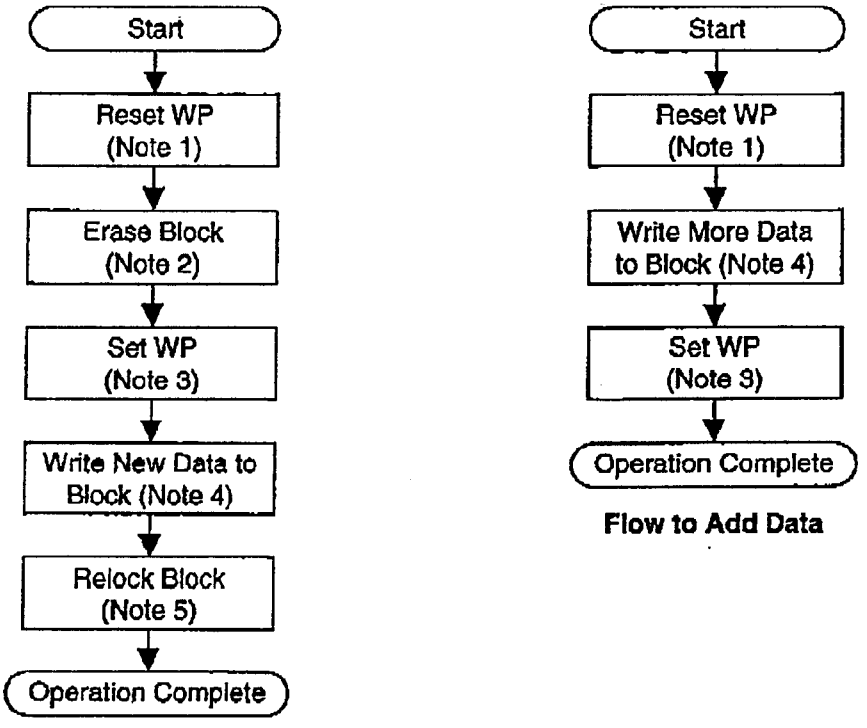
1. See CSR Full Status Check for Data-Write operation.

If CSR.4,5 is set, as it is command sequence error, SHOULD be cleared before further attempts are initiated.

Write FFH after the last operation to reset device to read array mode.

See Command Bus Definitions for description of codes.

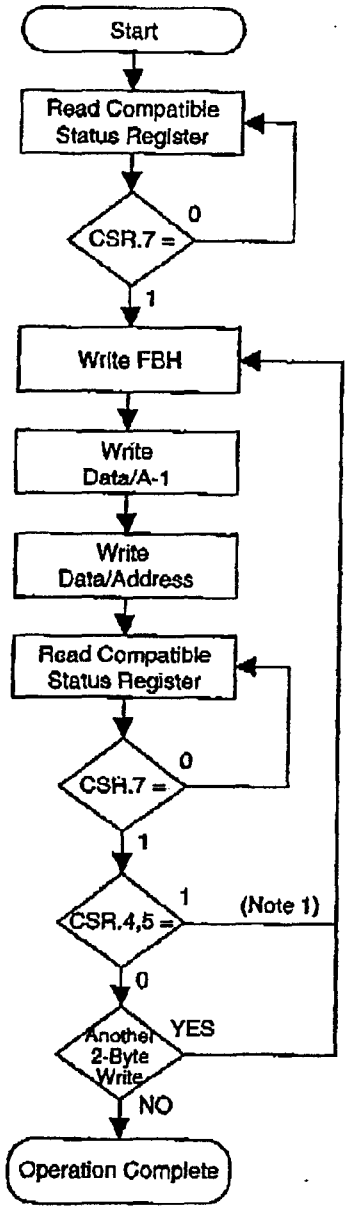
Figure 5-4. Block Locking Scheme



NOTES:

1. Use Reset-Write-Protect flowchart. Enable Write/Erase operation to all blocks.
2. Use Block-Erase flowchart. Erasing a block clears any previously established lockout for that block.
3. Use Set-Write-Protect flowchart. This step re-implements protection to locked blocks.
4. Use Word/Byte-Write or 2-Byte-Write flowchart sequences to write data.
5. Use Block-Lock flowchart to write lock bit if desired.

Figure 5-5. Updating Data in a Locked Block



(Apply to LH28F400SU , x16/x8 , 48TSOP/56TSOP/44SOP)

Bus Operation	Command	Comments
Read		Q = CSRD Toggle CE# or OE# to update CSRD. 1 = WSM Ready 0 = WSM Busy
Write	2-Byte Write	D = FBH A = X
Write		D = WD A-1 = 0 loads low byte of Data Register. A-1 = 1 loads high byte of Data Register. Other Addresses = X
Write		D = WD A = WA Internally, A-1 is automatically complemented to load the alternate byte location of the Data Register.
Read		Q = CSRD Toggle CE# or OE# to update CSRD. 1 = WSM Ready 0 = WSM Busy

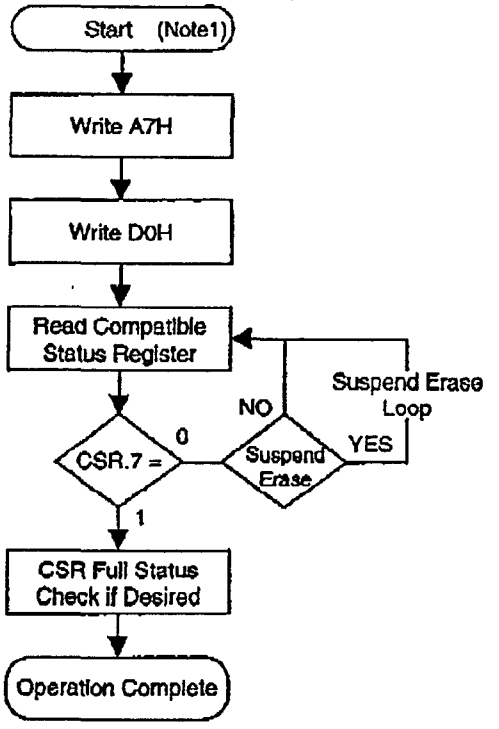
1. If CSR.4,5 is set, as it is command sequence error, SHOULD be cleared before further attempts are initiated.

CSR Full Status Check can be done after each 2-Byte Write, or after a sequence of 2-Byte Writes.

Write FFH after the last operation to reset device to read array mode.

See Command Bus Cycle notes for description of codes.

Figure 5-6. Two-Byte Serial Writes with Compatible Status Registers (LH28F400SU)



Bus Operation	Command	Comments
Write	Erase All Unlocked Block	D = A7H A = X
Write	Confirm	D = D0H A = X
Read		Q = CSRD Toggle CE# or OE# to update CSRD. A = X
Standby		Check CSR.7 1 = WSM Ready 0 = WSM Busy

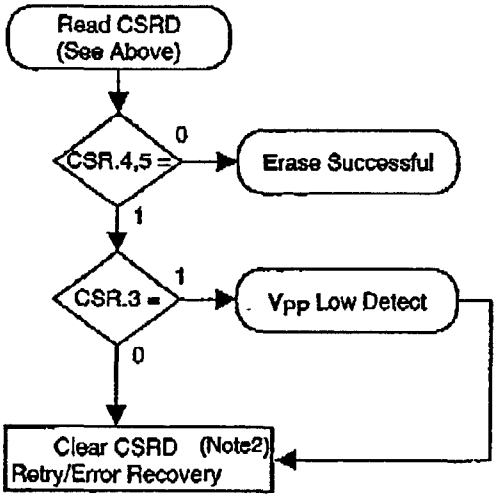
CSR Full Status Check can be done after Erase All Unlocked Block, or after a sequence of Erasures.

Write FFH after the last operation to reset device to read array mode.

See Command Bus Cycle notes for description of codes.

Note1. If power is off or RP# is set low during erase operation,
(1). Clear CSR.3/4/5 and issue Reset WP command,
(2). Retry Erase All Unlocked Block Erase command to erase all blocks, or issue Single Block Erase to erase all of the unlocked blocks in sequence,
(3). Set WP command is issued, if necessary.

CSR FULL STATUS CHECK PROCEDURE



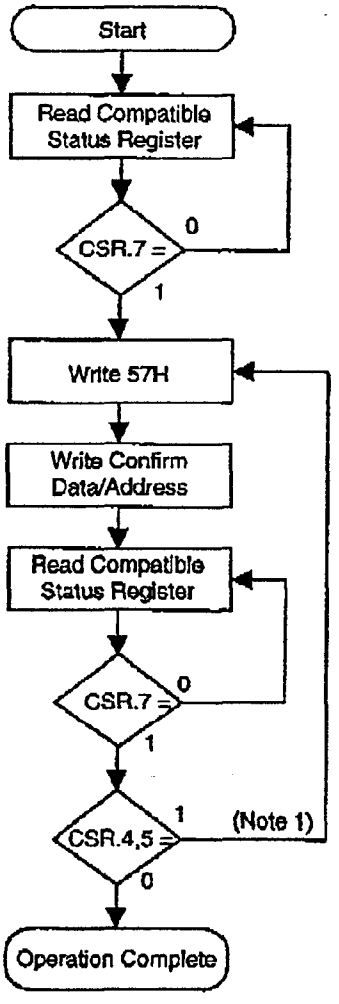
Bus Operation	Command	Comments
Standby		Check CSR.4,5 1 = Erase Error 0 = Erase Successful Both 1 = Command Sequence Error
Standby		Check CSR.3 1 = V_{PP} Low Detect 0 = V_{PP} OK

CSR.3,4,5 SHOULD be cleared, if set, before further attempts are initiated.

Note 2. If CSR.3 (VPPS) is set to "1", after clearing CSR.3/4/5,
(1). Issue Reset WP command,
(2). Retry Erase All Unlocked Block Erase command to erase all blocks, or issue Single Block Erase to erase all of the unlocked blocks in sequence,
(3). Set WP command is issued, if necessary.

If CSR.3 (VPPS) is set to "0", after clearing CSR.3/4/5,
(1). Retry Erase All Unlocked Block Erase command.

Figure 5-7. Erase All Unlocked Blocks with Compatible Status Registers



Bus Operation	Command	Comments
Read		Check CSR.7 1 = WSM Ready 0 = WSM Busy
Write	Set Write Protect	D = 57H A = X
Write	Set Confirm	D = D0H A = 0FFH (A9-A8 = 0, A7-A0 = 1, Others = X)
Read		Check CSR.7 1 = WSM Ready 0 = WSM Busy
Read		Check CSR.4,5 1 = Unsuccessful 0 = Success

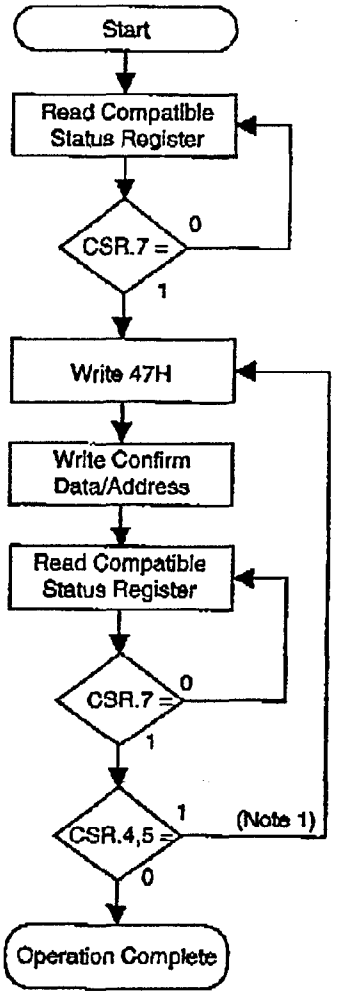
1. If CSR.4,5 is set, as it is command sequence error, SHOULD be cleared before further attempts are initiated.

Upon devicce power-up or toggle RP#, Set Write Protect command must be written to reflect the actual lock-bit status.

Write FFH after the last operation to reset device to Read Array Mode.

See Command Bus Cycle notes for description of codes.

Figure 5-8. Set Write Protect



Bus Operation	Command	Comments
Read		Check CSR.7 1 = WSM Ready 0 = WSM Busy
Write	Reset Write Protect	D = 47H A = X
Write	Reset Confirm	D = D0H A = 0FFH (A9-A8 = 0, A7-A0 = 1, Others = X)
Read		Check CSR.7 1 = WSM Ready 0 = WSM Busy
Read		Check CSR.4,5 1 = Unsuccessful 0 = Success

1. If CSR.4,5 is set, as it is command sequence error, SHOULD be cleared before further attempts are initiated.

Reset Write Protect command enables Write/Erase operation to all blocks.

Write FFH after the last operation to reset device to Read Array Mode.

See Command Bus Cycle notes for description of codes.

Figure 5-9. Reset Write Protect

6.0 ELECTRICAL SPECIFICATIONS(1)

Note: 1. Vcc supply range during read is 2.7 to 3.6V.

6.1 Absolute Maximum Ratings*

Temperature Under Bias ..... 0°C to + 80°C
Storage Temperature ..... - 65°C to + 125°C

WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

V_{CC} = 3.3V ± 0.3V Systems

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
T_A	Operating Temperature, Commercial	1	0	70	°C	Ambient Temperature
V_{CC}	V_{CC} with Respect to GND	2	- 0.2	7.0	V	
V_{PP}	V_{PP} Supply Voltage with Respect to GND	2	- 0.2	7.0	V	
V	Voltage on any Pin (except V_{CC}, V_{PP}) with Respect to GND	2	- 0.5	V_{CC} +0.5	V	
I	Current into any Non-Supply Pin			± 30	mA	
I_{OUT}	Output Short Circuit Current	3		100	mA	

NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC voltage is - 0.5V on input/output pins. During transitions, this level may undershoot to - 2.0V for periods < 20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5V which, during transitions, may overshoot to V_{CC} + 2.0V for periods < 20 ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.

6.2 Capacitance

For a 3.3V System:

Symbol	Parameter	Note	Typ	Max	Units	Test Conditions
C_{IN}	Capacitance Looking into an Address/Control Pin	1	7	10	pF	T_A = 25°C, f = 1.0 MHz
	Capacitance Looking into an Address/Control Pin A-1	1	9	12	pF	T_A = 25°C, f = 1.0 MHz
C_{OUT}	Capacitance Looking into an Output Pin	1	9	12	pF	T_A = 25°C, f = 1.0 MHz
C_{LOAD}	Load Capacitance Driven by Outputs for Timing Specifications	1		50	pF	For V_{CC} = 3.3V ± 0.3V
	Equivalent Testing Load Circuit Voc ± 10%			2.5	ns	50Ω transmission line delay

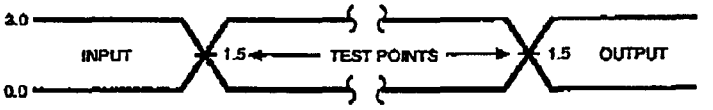
NOTE:
1. Sampled, not 100% tested.

6.3 Timing Nomenclature

For 3.3V systems use 1.5V cross point definitions.
Each timing parameter consists of 5 characters. Some common examples are defined below:

- t_{CE} t_{ELQV} time(t) from CE# (E) going low (L) to the outputs (Q) becoming valid (V)
- t_{OE} t_{GLQV} time(t) from OE# (G) going low (L) to the outputs (Q) becoming valid (V)
- t_{ACC} t_{AVQV} time(t) from address (A) valid (V) to the outputs (Q) becoming valid (V)
- t_{AS} t_{AVWH} time(t) from address (A) valid (V) to WE# (W) going high (H)
- t_{DH} t_{WHDX} time(t) from WE# (W) going high (H) to when the data (D) can become undefined (X)

	Pin Characters		Pin States
A	Address Inputs	H	High
D	Data Inputs	L	Low
Q	Data Outputs	V	Valid
E	CE# (Chip Enable)	X	Driven, but not necessarily valid
G	OE# (Output Enable)	Z	High Impedance
W	WE# (Write Enable)		
P	RP# (Deep Power-Down Pin)		
R	RY/BY# (Ready/Busy#)		
V	Any Voltage Level		
3V	V_{CC} at 3.0V Minimum		



AC test inputs are driven at 3.0V for a Logic "1" and 0.0V for a Logic "0." Input timing begins, and output timing ends, at 1.5V. Input rise and fall times (10% to 90%) < 10 ns.

Figure 4. Transient Input/Output Reference Waveform (V_{CC} = 3.3V)

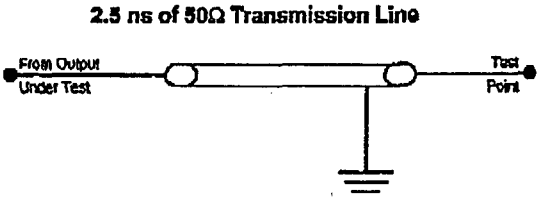


Figure 5. Transient Equivalent Testing Load Circuit (V_{CC} = 3.3V)

6.4 DC Characteristics

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to + 70°C

Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Conditions
I_{IL}	Input Load Current	1			± 1	µA	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or GND
I_{LO}	Output Leakage Current	1			± 10	µA	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or GND
I_{CCS}	V_{CC} Standby Current	1,4		4	8	µA	V_{CC} = V_{CC} Max, CE#, RP# = V_{CC} ± 0.2V BYTE# = V_{CC} ± 0.2V or GND ± 0.2V
				0.3	4	mA	V_{CC} = V_{CC} Max, CE#, RP# = V_{IH} BYTE# = V_{IH} or V_{IL}
I_{CCD}	V_{CC} Deep Power-Down Current	1		0.2	5	µA	RP# = GND ± 0.2V
I_{CCR1}	V_{CC} Read Current	1,3,4			35	mA	V_{CC} = V_{CC} Max, CMOS: CE# = GND ± 0.2V BYTE# = GND ± 0.2V or V_{CC} ± 0.2V Inputs = GND ± 0.2V or V_{CC} ± 0.2V, TTL: CE# = V_{IL}, BYTE# = V_{IL} or V_{IH} Inputs = V_{IL} or V_{IH}, f = 8 MHz, I_{OUT} = 0 mA
I_{CCR2}	V_{CC} Read Current	1,3,4		10	20	mA	V_{CC} = V_{CC} Max, CMOS: CE# = GND ± 0.2V, BYTE# = V_{CC} ± 0.2V or GND ± 0.2V Inputs = GND ± 0.2V or V_{CC} ± 0.2V, TTL: CE# = V_{IL} BYTE# = V_{IH} or V_{IL} Inputs = V_{IL} or V_{IH}, f = 4 MHz, I_{OUT} = 0 mA
I_{CCW}	V_{CC} Write Current	1		8	12	mA	Word/Byte Write in Progress
I_{CCE}	V_{CC} Block Erase Current	1		6	12	mA	Block Erase In Progress
I_{CCES}	V_{CC} Erase Suspend Current	1,2		3	6	mA	CE# = V_{IH} Block Erase Suspended
I_{PPS}	V_{PP} Standby Current	1		± 1	± 10	µA	V_{PP} ≤ V_{CC}
I_{PPD}	V_{PP} Deep Power-Down Current	1		0.2	5	µA	RP# = GND ± 0.2V

DC Characteristics (Continued)

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to + 70°C

Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Conditions
I_{PPR}	V_{PP} Read Current	1			200	µA	$V_{PP} > V_{CC}$
I_{PPW}	V_{PP} Write Current	1		15	35	mA	$V_{PP} = V_{PPH}$, Word/Byte Write in Progress
I_{PPE}	V_{PP} Erase Current	1		20	40	mA	$V_{PP} = V_{PPH}$, Block Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current	1			200	µA	$V_{PP} = V_{PPH}$, Block Erase Suspended
V_{IL}	Input Low Voltage	5	- 0.3		0.8	V	
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage				0.4	V	$V_{CC} = V_{CC}$ Min and I_{OL} = 4 mA
V_{OH1}	Output High Voltage		2.4			V	I_{OH} = - 2 mA $V_{CC} = V_{CC}$ Min
V_{OH2}			V_{CC} - 0.2			V	I_{OH} = - 100 µA $V_{CC} = V_{CC}$ Min
V_{PPL}	V_{PP} during Normal Operations	6	0.0		5.5	V	
V_{PPH}	V_{PP} during Write/ Erase Operations		4.5	5.0	5.5	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage		1.4			V	

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 3.3V, V_{PP} = 5.0V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. I_{CCS} is specified with the device de-selected. If the device is read while in erase suspend mode, current draw is the sum of I_{CCS} and I_{CCR}.
3. Automatic Power Saving (APS) reduces I_{CCR} to less than 1 mA in Static operation.
4. CMOS inputs are either V_{CC} ± 0.2V or GND ± 0.2V. TTL inputs are either V_{IL} or V_{IH}.
5. In 2.7V < V_{CC} < 3.0V operation, TTL-level input of RP# is V_{IL} (Max.) = 0.6V.
6. V_{PPL} in read is V_{CC} - 0.2V < V_{PPL} < 5.5V or GND < V_{PPL} < GND + 0.2V.

6.5 AC Characteristics - Read Only Operations[1]

V_{CC} = 3.3V ± 0.3V, T_A =0°C to +70°C

Symbol	Parameter	Notes	Min	Max	Units
t_{AVAV}	Read Cycle Time		120		ns
t_{AVGL}	Address Setup to OE# Going Low	3	0		ns
t_{AVQV}	Address to Output Delay			120	ns
t_{ELQV}	CE# to Output Delay	2		120	ns
t_{PHQV}	RP# High to Output Delay			620	ns
t_{GLQV}	OE# to Output Delay	2		45	ns
t_{ELQX}	CE# to Output in Low Z	3	0		ns
t_{EHQZ}	CE# to Output in High Z	3		50	ns
t_{GLQX}	OE# to Output in Low Z	3	0		ns
t_{GHQZ}	OE# to Output in High Z	3		30	ns
t_{OH}	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		ns
t_{FLQZ}	BYTE# Low to Output in High Z	3		50	ns
t_{FLEL} t_{FHEL}	BYTE# High or Low to CE# Low	3	20		ns

NOTES:

1. See AC Input/Output Reference Waveforms for timing measurements, Figure 4.
2. OE# may be delayed up to $t_{ELQV} - t_{GLQV}$ after the falling edge of CE# without impact on t_{ELQV}.
3. Sampled, not 100% tested.

AC Characteristics - Read Only Operations[1] (Continued)

V_{CC} = 2.85V ± 0.15V, T_A =0°C to +70°C

Symbol	Parameter	Notes	Min	Max	Units
t_{AVAV}	Read Cycle Time		160		ns
t_{AVGL}	Address Setup to OE# Going Low	3	0		ns
t_{AVQV}	Address to Output Delay			160	ns
t_{ELQV}	CE# to Output Delay	2		160	ns
t_{PHQV}	RP# High to Output Delay			800	ns
t_{GLQV}	OE# to Output Delay	2		55	ns
t_{ELQX}	CE# to Output in Low Z	3	0		ns
t_{EHQZ}	CE# to Output in High Z	3		60	ns
t_{GLQX}	OE# to Output in Low Z	3	0		ns
t_{GHQZ}	OE# to Output in High Z	3		50	ns
t_{OH}	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		ns
t_{FLGZ}	BYTE# Low to Output in High Z	3		75	ns
t_{FLEL} t_{FHEL}	BYTE# High or Low to CE# Low	3	25		ns

NOTES:
1. See AC Input/Output Reference Waveforms for timing measurements, Figure 4.
2. OE# may be delayed up to $t_{ELQV} - t_{GLQV}$ after the falling edge of CE# without impact on t_{ELQV}.
3. Sampled, not 100% tested.

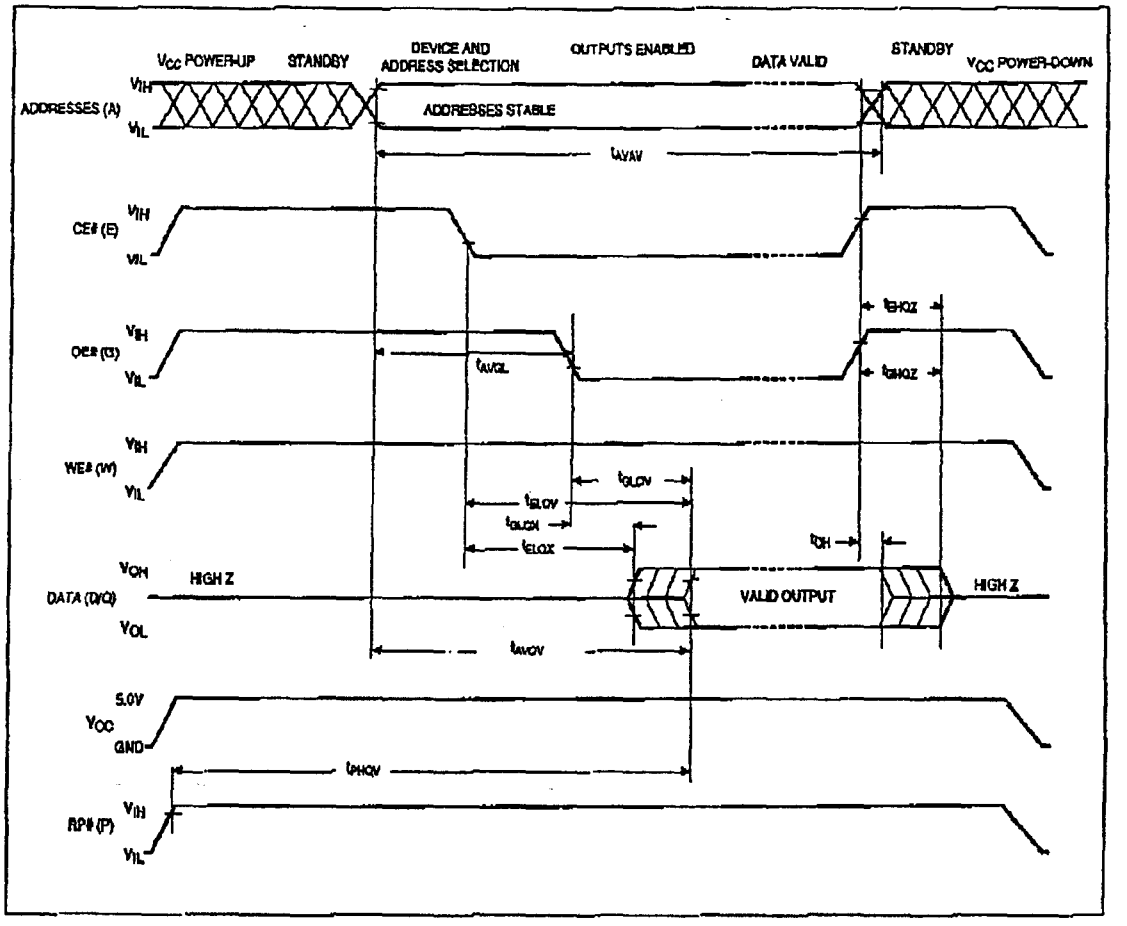


Figure 6. Read Timing Waveforms

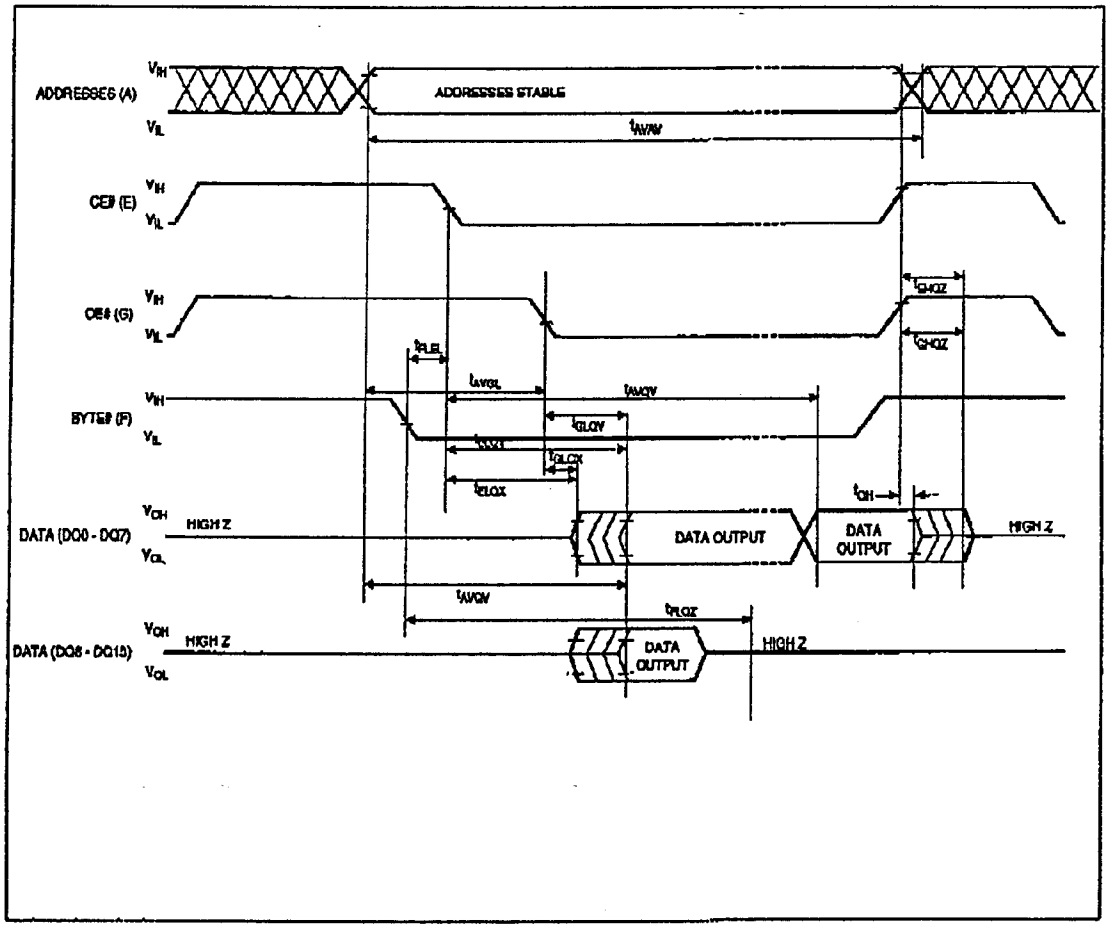


Figure 7. BYTE# Timing Waveforms

6.6 Power-Up and Reset Timings

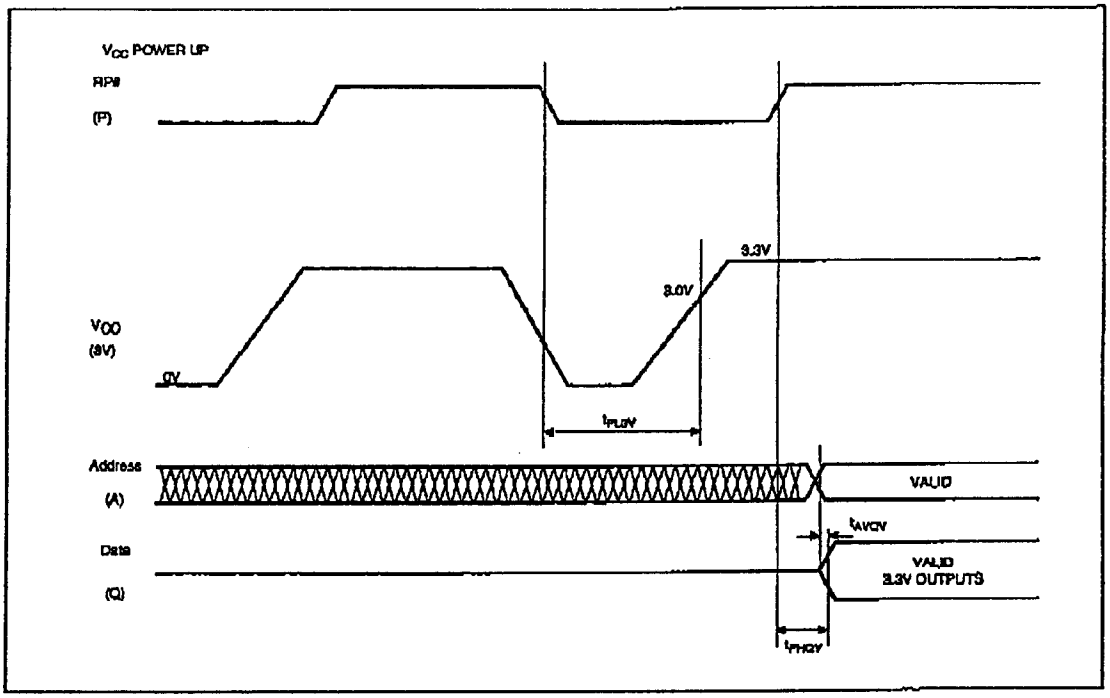


Figure 8. V_{cc} Power-Up and RP# Reset Waveforms

Symbol	Parameter	Note	Min	Max	Unit
t_{PL3V}	RP# Low to V_{CC} at 3.0V Minimum	1	0		µs
t_{AVQV}	Address Valid to Data Valid for $V_{CC} = 3.3V \pm 0.3V$	2		120	ns
t_{PHQV}	RP# High to Data Valid for $V_{CC} = 3.3V \pm 0.3V$	2		620	ns

NOTES:
CE# and OE# are switched low after Power-Up.

1. The power supply may start to switch concurrently with RP# going Low. RP# is required to stay low, until Vcc stays at recommended operating voltage.
2. The address access time and RP# high to data valid time are shown for 3.3V V_{cc} operation. Refer to the AC Characteristics Read Only Operations also.

6.7 AC Characteristics for WE# - Controlled Command Write Operations[1]

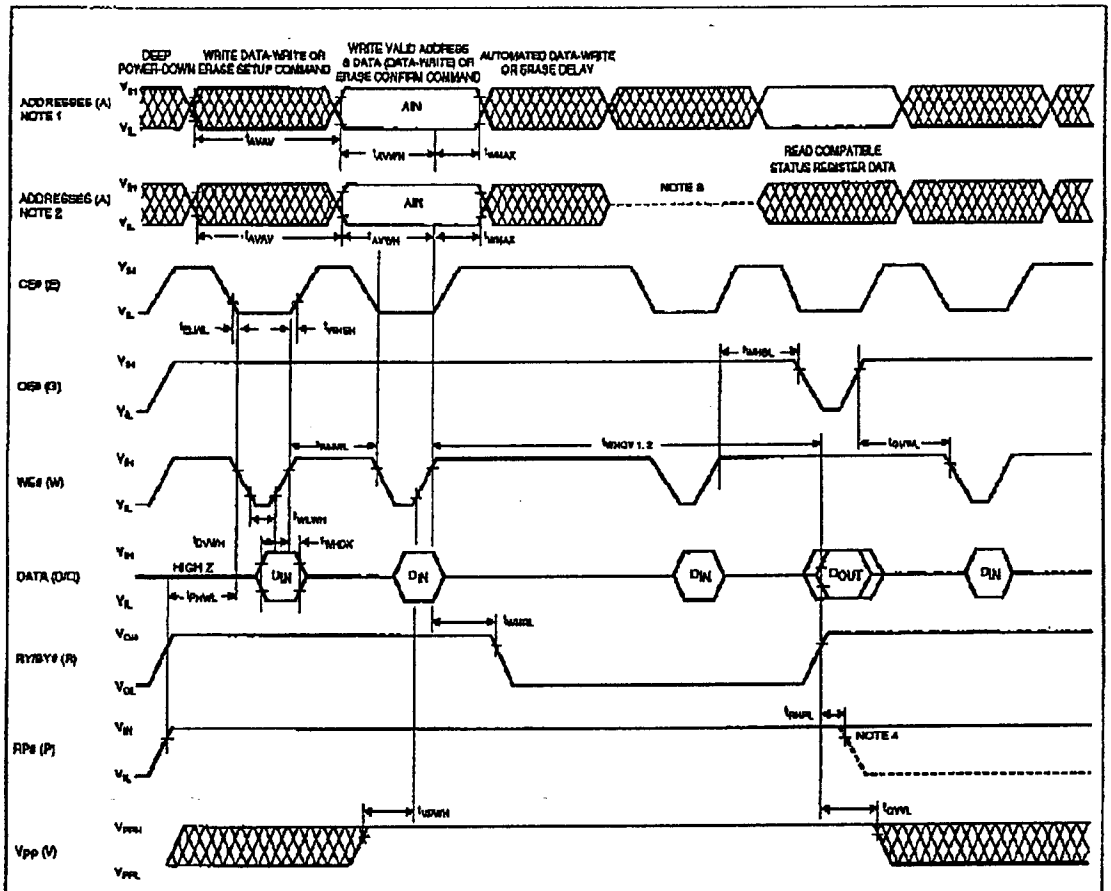
V_{CC} = 3.3 ± 0.3V, T_A = 0°C to + 70°C

Symbol	Parameter	Notes	Min	Typ	Max	Unit
t_{AVAV}	Write Cycle Time		120			ns
t_{VPWH}	V_{PP} Setup to WE# Going High	3	100			ns
t_{PHEL}	RP# Setup to CE# Going Low		480			ns
t_{ELWL}	CE# Setup to WE# Going Low		10			ns
t_{AVWH}	Address Setup to WE# Going High	2,6	110			ns
t_{DVWH}	Data Setup to WE# Going High	2,6	110			ns
t_{WLWH}	WE# Pulse Width		110			ns
t_{WHDX}	Data Hold from WE# High	2	5			ns
t_{WHAX}	Address Hold from WE# High	2	5			ns
t_{WHEH}	CE# Hold from WE# High		5			ns
t_{WHWL}	WE# Pulse Width High		60			ns
t_{GHWL}	Read Recovery before Write		0			ns
t_{WHRL}	WE# High to RY/BY# Going Low				100	ns
t_{RHPL}	RP# Hold from Valid Status Register Data and RY/BY# High	3	0			ns
t_{PHWL}	RP# High Recovery to WE# Going Low		1			µs
t_{WHGL}	Write Recovery before Read		95			ns
t_{QVVL}	V_{PP} Hold from Valid Status Register Data and RY/BY# High		0			µs
t_{WHQV1}	Duration of Byte Write Operation	4,5	8	20		µs
t_{WHQV2}	Duration of Block Erase Operation	4	0.3			s

NOTES:

1. Read timing during write and erase are the same as for normal read.
2. Refer to command definition tables for valid address and data values.
3. Sampled, but not 100% tested.
4. Write/Erase durations are measured to valid Status Register (CSR) Data.
5. Byte write operations are typically performed with 1 Programming Pulse.
6. Address and Data are latched on the rising edge of WE# for all Command Write operations.

PRELIMINARY



NOTES:

1. This address string depicts Data-Write/Erase cycles with corresponding verification via ESRD.
2. This address string depicts Data-Write/Erase cycles with corresponding verification via CSRD.
3. This cycle is invalid when using CSRD for verification during Data-Write/Erase operations
4. RP# low transition is only to show t_{PHPL}; not valid for above Read and Writs cycles.

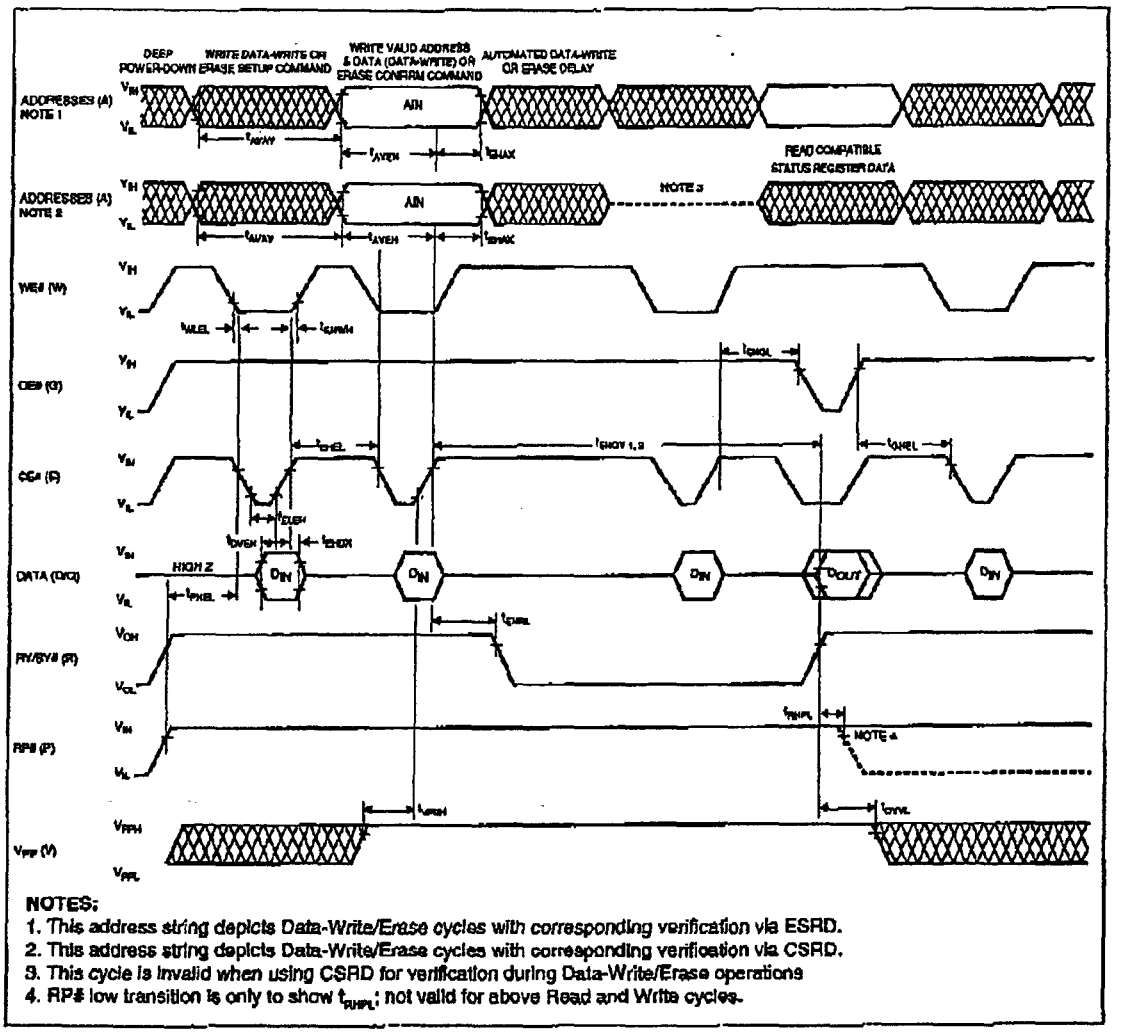
Figure 9. AC Waveforms for Command Write Operations

6.8 AC Characteristics for CE# - Controlled Command Write Operations[1]

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to + 70°C

Symbol	Parameter	Notes	Min	Typ	Max	Unit
t_{AVAV}	Write Cycle Time		120			ns
t_{PHWL}	RP# Setup to WE# Going Low	3	480			ns
t_{VPEH}	V_{PP} Setup to CE# Going High	3	100			ns
t_{WLEL}	WE# Setup to CE# Going Low		0			ns
t_{AVEH}	Address Setup to CE# Going High	2,6	110			ns
t_{DVEH}	Data Setup to CE# Going High	2,6	110			ns
t_{ELEH}	CE# Pulse Width		110			ns
t_{EHDX}	Data Hold from CE# High	2	5			ns
t_{EHAX}	Address Hold from CE# High	2	5			ns
t_{EHWH}	WE# Hold from CE# High		5			ns
t_{EHEL}	CE# Pulse Width High		60			ns
t_{QHEL}	Read Recovery before Write		0			ns
t_{EHRL}	CE# High to RY/BY# Going Low				100	ns
t_{RHPL}	RP# Hold from Valid Status Register Data and RY/BY# High	3	0			ns
t_{PHEL}	RP# High Recovery to CE# Going Low		1			µs
t_{EHGL}	Write Recovery before Read		95			ns
t_{QVVL}	Vpp Hold from Valid Status Register Data and RY/BY# High		0			µs
t_{EHQV1}	Duration of Byte Write Operation	4,5	8	20		µs
t_{EHQV2}	Duration of Block Erase Operation	4	0.3			s

NOTES:
1. Read timing during write and erase are the same as for normal read.
2. Refer to command definition tables for valid address and data values.
3. Sampled, but not 100% tested.
4. Write/Erase durations are measured to valid Status Register (OSR) Data.
5. Byte write operations are typically performed with 1 Programming Pulse.
6. Address and Data are latched on the rising edge of CE# for all Command Write Operations.



NOTES:
1. This address string depicts Data-Write/Erase cycles with corresponding verification via ESRD.
2. This address string depicts Data-Write/Erase cycles with corresponding verification via CSRD.
3. This cycle is invalid when using CSRD for verification during Data-Write/Erase operations
4. RP# low transition is only to show t_{PHPL}; not valid for above Read and Write cycles.

Figure 10. Alternate AC Waveforms for Command Write Operations

6.9 Erase and Word/Byte Write Performance

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to + 70°C

Symbol	Parameter	Notes	Min	Typ(1)	Max	Units	Test Conditions
$t_{WHRH}1$	Byte Write Time	2		20		µs	
$t_{WHRH}2$	Two-Byte Serial Write Time	2,3		30		µs	
$t_{WHRH}3$	Word Write Time	2,4		30		µs	
$t_{WHRH}4$	16KB Block Write Time	2		0.33	1.3	s	Byte Write Mode
$t_{WHRH}5$	16KB Block Write Time	2,3		0.26	1.0	s	Two-Byte Serial Write Mode
$t_{WHRH}6$	16KB Block Write Time	2,4		0.26	1.0	s	Word Write Mode
	Block Erase Time (16KB)	2		0.8	10	s	
	Full Chip Erase Time	2,5		12-19.2		s	

NOTES:
1. 25°C, V_{PP} = 5.0V.
2. Excludes System-Level Overhead.
3. Two-Byte Serial Write mode is valid at x8-bit configuration only.
4. Word Write mode is valid at x16-bit configuration only.
5. Depends on the number of protected blocks.

LH28Fxxx FLASH MEMORY FLASH NON-VOLATILE MEMORY FLASH E2ROM FLASH ROM READ ONLY MEMORY ETOX SINGLE VOLTAGE LH28F400SUT-LC12 4M (512Kx8/256Kx16)