SHARP

NEW PRODUCT INFORMATION

LH28F040SU

4M-bit Dual Work Flash Memory

■ Description

Sharp's LH28F040SUTD 4M-bit flash memory is a revolutionary architecture which enables the design of truly mobile, high performance, personal computing and communication products. With innovative capabilities, 3.3 V low power operation and very high read/write performance, the LH28F040SUTD is also the ideal choice for designing embedded mass storage flash memory systems.

The LH28F040SUTD is a very high density, highest performance non-volatile read/write solution for solid-state storage applications. Its independently lockable 32 symmetrical blocked architecture (16k-byte each) extended cycling, low power operation, very fast write and read performance and selective block locking provide a highly flexible memory component suitable for high density memory cards, Resident Flash Arrays and PCMCIA-ATA Flash Drives. The LH28F040SUTD's 5.0 V/3.3 V power supply operation enables the design of memory cards which can be read in 3.3 V system and written in 5.0 V/3.3 V systems. Its ×8 architecture allows the optimization of memory to processor interface. The flexible block locking option enables bundling of executable application software in a Resident Flash Array or memory card. Manufactured on Sharp's 0.55 μm ETOX™ process technology, the LH28F040SUTD is the most cost-effective, high-density 3.3 V flash memory.

LH28F040SUTD divides 4M-bit into two areas. Each area can read/write/erase independently. For example, while you write and erase on one area, you can simultaneously read the data from the other area. This enables users to reduce the number of components in their system.

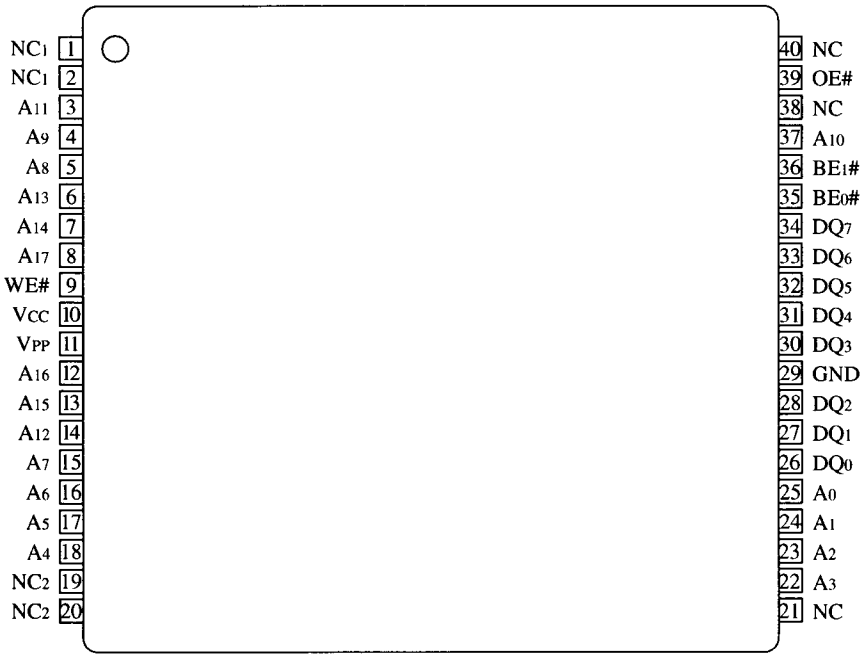
*ETOX is a trademark of Intel Corporation.

IC

■ Features

1. 262 144 word×8 bit×2 organization
2. Maximum access time 150 ns (V_{CC}=3.3±0.3 V)
   190 ns (V_{CC}=2.7 V)
3. Maximum supply current
   Standby 20 μA (Low-power consumption type)
   160 μA (Normal power consumption type)
4. 2 banks enable the simultaneous Read/Write/Erase operation
5. 32 independently lockable blocks
6. 100 000 erase cycles per block
7. 5 V Write/Erase operation (5 V V_{PP}, 3.3 V V_{CC})
   - V_{CC} for Write/Erase at as low as 2.9 V
8. Automated Byte write/Block erase
   - Command user interface
   - Stafus register
9. System performance enhancement
   - Erase suspend for read
   - Two-byte write
   - Bank erase
10. Data protection
    - Hardware Erase/Write lockout during power transitions
    - Software Erase/Write lockout
11. Independently lockable for Write/Erase on each block (Lock Block & Protect Set/Reset)
12. Package
    40-pin TSOP (I) normal bend (TSOP040-P-1020)

Pin Connections

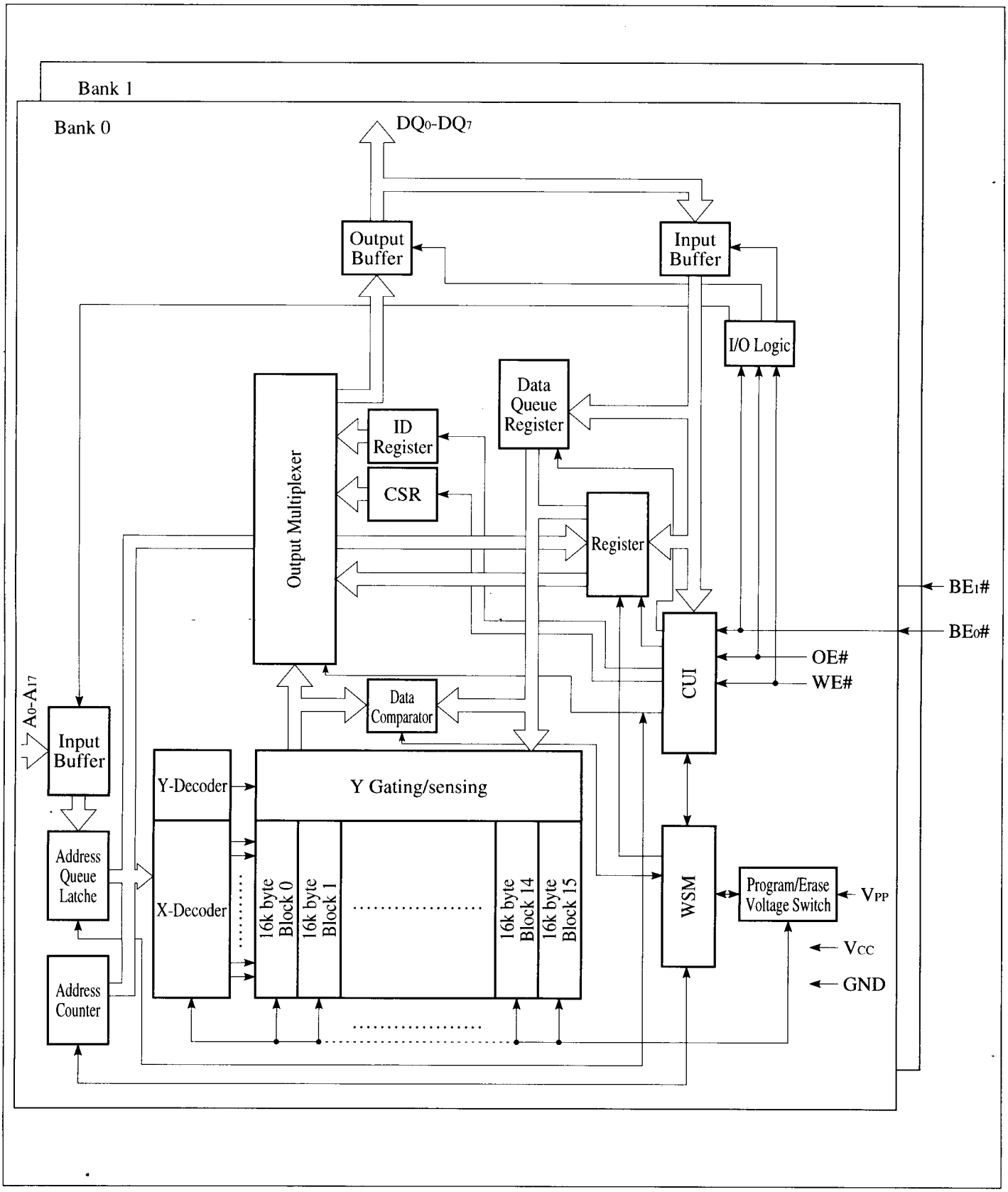


Top View

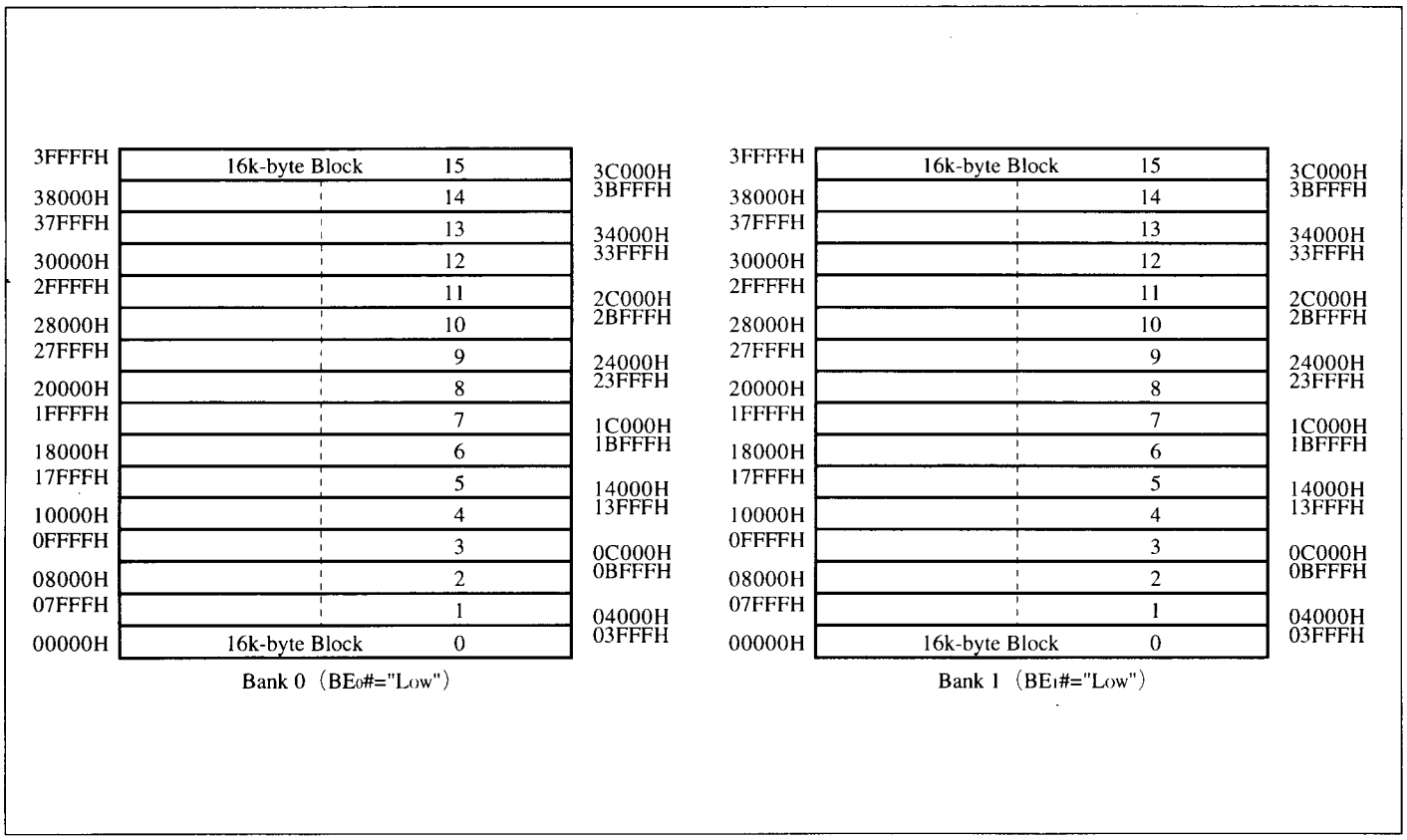
Pin Description

Symbol	I/O	Name and Function
A_0-A_{13}	I	Byte-select addresses: Select a byte within one 16k-byte block. These addresses are latched during Data Writes.
A_{14}-A_{17}	I	Block-select addresses : Select 1 of 16k-byte Erase block. These addresses are latched during Data Writes, Erase and Lock-Block operations.
DQ_0-DQ_7	I/O	Data input/output: Inputs data and commands during CUI write cycles. Outputs array, buffer, identifier or status data in the appropriate Read mode. Floated when the chip is de-selected or the outputs are disabled.
BE_0#, BE_1#	I	Bank enable inputs: Activate the device's control logic, input buffers, decoders and sense amplifiers. CE# must be low to select the device. When BE_0# is low, bank0 is active. When BE_1# is low, bank1 is active. Both BE_0# and BE_1# must not be low at the same time.
OE#	I	Output enable : Gates device data through the output buffers when low. The outputs float to tri-state off when OE# is high.
WE#	I	Write enable: Controls access to the CUI, Page Buffers, Data Queue Registers and Address Queue Latches. WE# is active low, and latches both address and data (command or array) on its rising edge.
V_{PP}	—	Erase/write power supply (5.0 V$\pm$0.5 V): For erasing memory array blocks or writing bytes into the flash array.
V_{CC}	—	Device power supply (3.3 V$\pm$0.3 V): Do not leave any power pins floating.
GND	—	Ground for all internal circuitry: Do not leave any ground pins floating.
NC	—	No connection
NC_1, NC_2	—	Open pin: But NC_1 (between pin1 and pin2) and also NC_2 (pin19 and pin20) are connected inside package.

Block Diagram



Memory Map



Bus Operations

Operation		BE0#	BE1#	OE#	WE#	A0	DQ0-DQ7	Note
Read	Bank 0	VIL	VIH	VIL	VIH	X	DOUT	1
	Bank 1	VIH	VIL					
Output disable		X	X	VIH	VIH	X	High-Z	1
Standby		VIH	VIH	X	X	X	High-Z	1
Manufacturer ID	Bank 0	VIL	VIH	VIL	VIH	VIL	B0H	2
	Bank 1	VIH	VIL					
Device ID	Bank 0	VIL	VIH	VIL	VIH	VIH	31H	2
	Bank 1	VIH	VIL					
Write	Bank 0	VIL	VIH	VIH	VIL	X	DIN	1, 3
	Bank 1	VIH	VIL					

Note 1. X can be VIH or VIL for address or control pins, which is either VOL or VOH.

Note 2. A0 at VIL provide manufacturer ID codes. A0 at VIH provide device ID codes. All other addresses are set to zero.

Note 3. Commands for different Erase operations, Data write operations or Lock-block operations can only be successfully completed when VPP = VPPH.

Note 4. Both BE0# and BE1# must not be low at the same time.

■ Command Definitions

(1) LH28F008SA-Compatible mode command bus definitions

Following is the commands to be applied to each bank.

Command	First bus cycle			Second bus cycle			Note
	Operation	Address	Data	Operation	Address	Data	
Read array	Write	X	FFH	Read	AA	AD	
Intelligent identifier	Write	X	90H	Read	IA	ID	1
Read compatible status register	Write	X	70H	Read	X	CSRD	2
Clear status register	Write	X	50H				3
Byte write	Write	X	40H	Write	WA	WD	
Alternate byte write	Write	X	10H	Write	WA	WD	
Block erase/Confirm	Write	X	20H	Write	BA	D0H	4
Erase suspend/Resume	Write	X	B0H	Write	X	D0H	4

- Address
  - AA : Array Address
  - BA : Block Address
  - IA : Identifier Address
  - WA : Write Address
  - X : Don't care
- Data
  - AD : Array Data
  - CSRD : CSR Data
  - ID : Identifier Data
  - WD : Write Data

Note 1. Following the intelligent identifier command, two Read operations access the manufacturer and device signature codes.

Note 2. The CSR is automatically available after device enters Data write, erase, or suspend operations.

Note 3. Clears CSR.3, CSR.4 and CSR.5. See Status register definitions.

Note 4. While device performs Block erase, if you issue Erase suspend command (B0H), be sure to confirm ESS (Erase-Suspend-Status) is set to 1 on compatible status register. In the case, ESS bit was not set to 1, also completed the Erase(ESS = 0, WSMS = 1), be sure to issue Resume command (D0H) after completed next Erase command. Beside, when the Erase suspend command is issued, while the device is not in Erase, be sure to issue Resume command (D0H) after the next erase completed.

(2) LH28F040SU-Performance enhancement command bus definitions

Following is the commands to be applied to each bank.

Command	First bus cycle			Second bus cycle			Third bus cycle			Note
	Operation	Address	Data	Operation	Address	Data	Operation	Address	Data	
Protect set/Confirm	Write	X	57H	Write	0FFH	D0H				1, 2, 6
Protect reset/Confirm	Write	X	47H	Write	0FFH	D0H				3, 6
Lock block/Confirm	Write	X	77H	Write	BA	D0H				1, 2, 4
Bank erase all unlocked blocks	Write	X	A7H	Write	X	D0H				1, 2
Two-byte write	Write	X	FBH	Write	A0	WD (L, H)	Write	WA	WD (L, H)	1, 2, 5

· Address
BA : Block Address
WA : Write Address
X : Don't care

· Data
AD : Array Data
WD (L, H) : Write Data (Low, High)
WD (H, L) : Write Data (High, Low)

Note 1. After initial device power-up, or reset is completed, the block lock status bits default to the locked state independent of the data in the corresponding lock bits. In order to upload the lock bit status, it requires to write Protect set/Confirm command.

Note 2. To reflect the actual lock-bit status, the Protect set/Confirm command must be written after Lock Block/confirm command.

Note 3. When Protect reset/Confirm command is written, all blocks can be written and erased regardless of the state of the lock-bits.

Note 4. The Lock block/Confirm command must be written after Protect reset/Confirm command was written.

Note 5. A_0 is automatically complemented to load second byte of data. A_0 value determines which WD is supplied first: $A_0 = 0$ looks at the WDL, $A_0 = 1$ looks at the WDH.

Note 6. Second bus cycle address of Protect set/Confirm and Protect reset/Confirm command is 0FFH. Specifically A_9-$A_8 = 0$, A_7-$A_0 = 1$, others are don't care.

■ Status Register

Each bank has its own status register.

〈Compatible status register (CSR)〉

WSMS	ESS	ES	DWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

CSR.7= WRITE STATE MACHINE STATUS (WSMS)
1=Ready
0=Busy

CSR.6= ERASE-SUSPEND STATUS (ESS)
1=Erase Suspended
0=Erase in Progress/Completed

CSR.5= ERASE STATUS (ES)
1=Error In Block Erasure
0=Successful Block Erase

CSR.4= DATA-WRITE STATUS (DWS)
1=Error in Data Write
0=Data Write Successful

CSR.3= V_{PP} STATUS (VPPS)
1=V_{PP} Low Detect, Operation Abort
0=V_{PP} OK

Notes

- WSMS bit must be checked to determine completion of an operation (Erase suspend, Erase or Data write) before the appropriate Status bit (ESS, ES or DWS) is checked for success.
- If DWS and ES are set to "1" during an erase attempt, an improper command sequence was entered. Clear the CSR and attempt the operation again.
- The VPPS bit, unlike an A/D converter, does not provide continuous indication of V_{PP} level. The WSM interrogates V_{PP} level only after the Data-write or Erase command sequences have been entered, and informs the system if V_{PP} has not been switched on. VPPS is not guaranteed to report accurate feedback between V_{PPL} and V_{PPH}.

※ CSR.2-0 = Reserved for future enhancements
These bits are reserved for future use and should be masked out when polling the CSR.

■ Absolute Maximum Ratings

Temperature under bias ·····−20 to +80 ℃
Storage temperature ·····−65 to +125 ℃

WARNING Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
V_{CC} with respect to GND	V_{CC}		−0.2		7.0	V	1
V_{PP} supply voltage with respect to GND	V_{PP}		−0.2		7.0	V	
Voltage on any pin (except V_{CC}, V_{PP}) with respect to GND	V		−0.5		V_{CC}+0.5	V	
Current into any non-supply pin	I				±30	mA	
Output short circuit current	I_{OUT}				100	mA	2
Operating temperature, commercial	Ta	Ambient temperature	−20		70	℃	3

Note 1. Minimum DC voltage is −0.5 V on input/output pins. During transitions, this level may undershoot to −2.0 V for periods < 20 ns. Maximum DC voltage on input/output pins is V_{CC}+0.5 V which, during transitions, may overshoot to V_{CC}+2.0 V for periods < 20 ns.
Note 2. Output shorted for no more than one second. No more than one output shorted at a time.
Note 3. Operating temperature is for commercial product defined by this specification.

■ Capacitance

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Capacitance looking into an Address/Control pin	C_{IN}	Ta=25 ℃, f=1.0 MHz		14	20	pF	1, 2
Capacitance looking into an output pin	C_{OUT}	Ta=25 ℃, f=1.0 MHz		18	24	pF	1
Load capacitance driven by outputs for timing specifications	C_{LOAD}	V_{CC}=3.3 ±0.3 V			50	pF	1
Equivalent testing load circuit V_{CC}±10%		50 Ω transmission line delay			2.5	ns	

Note 1. Sampled, not 100% tested.
Note 2. BE_0#, and BE_1# have half the value of this.

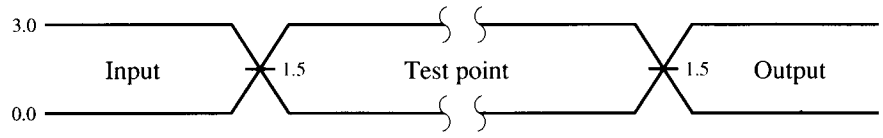
■ DC Characteristics (Note 1)

(V_{CC}=3.3±0.3 V, Ta=−20 to +70 ℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input load current	I_{IL}	V_{CC}=V_{CC} MAX. V_{IN}=V_{CC} or GND			±2.0	μA	2
Output leakage current	I_{LO}	V_{CC}=V_{CC} MAX. V_{IN}=V_{CC} or GND			±20	μA	2
V_{CC} Standby current	I_{CCS}	V_{CC}=V_{CC} MAX. BE_0#,BE_1#=V_{CC}±0.2 V		5.0	10	μA	2, 5, 6
		V_{CC}=V_{CC} MAX. BE_0#,BE_1#=V_{IH}		0.3	4.0	mA	
V_{CC} read current (10 MHz operation)	I_{CCR1}	V_{CC}=V_{CC} MAX. CMOS: BE_0#, BE_1#=GND±0.2 V Inputs=GND±0.2 V or V_{CC}±0.2 V TTL: BE_0#, BE_1#=V_{IL} Inputs=V_{IL} or V_{IH} f=10 MHz, I_{OUT}=0 mA			35	mA	2,4,5,6
V_{CC} read current (5.0 MHz operation)	I_{CCR2}	V_{CC}=V_{CC} MAX. CMOS: BE_0#, BE_1#=GND±0.2 V Inputs=GND±0.2 V or V_{CC}±0.2 V TTL: BE_0#, BE_1#=V_{IL} Inputs=V_{IL} or V_{IH} f=5.0 MHz, I_{OUT}=0 mA		10	20	mA	2,4,5,6
V_{CC} write current	I_{CCW}	Byte/Two-byte serial write in progress		8.0	12	mA	2, 6
V_{CC} block erase current	I_{CCE}	Block erase in progress		6.0	12	mA	2, 6
V_{CC} erase suspend current	I_{CCES}	BE_0#, BE_1#=V_{IH} Block erase suspended		3.0	6.0	mA	2, 3, 6
V_{PP} standby current	I_{PPS}	V_{PP}≦V_{CC}		±1.0	±10	μA	2, 6
V_{PP} read current	I_{PPR}	V_{PP}>V_{CC}		65	200	μA	2, 6
V_{PP} write current	I_{PPW}	V_{PP}=V_{PPH} byte/two-byte serial write in progress		15	35	mA	2, 6
V_{PP} erase current	I_{PPE}	V_{PP}=V_{PPH} block erase in progress		20	40	mA	2, 6
V_{PP} erase suspend current	I_{PPES}	V_{PP}=V_{PPH} block erase suspended		65	200	μA	2, 6
Input "Low" voltage	V_{IL}		−0.3		0.8	V	
Input "High" voltage	V_{IH}		2.0		V_{CC}+0.3	V	
Output "Low" voltage	V_{OL}	V_{CC}=V_{CC} MIN. and I_{OL}=4.0 mA			0.4	V	
Output "High" voltage	V_{OH1}	I_{OH}=−2.0 mA V_{CC}=V_{CC} MIN.	2.4			V	
	V_{OH2}	I_{OH}=−100 μA V_{CC}=V_{CC} MIN.	V_{CC}−0.2			V	
V_{PP} during normal operations	V_{PPL}		0		5.5	V	
V_{PP} during Write/Erase operations	V_{PPH}		4.5	5.0	5.5	V	
V_{CC} Erase/Write lock voltage	V_{LKO}		1.4			V	

Note 1. Following is the current consumption of one bank. For the current consumption of one device total, please refer to the Note 6.
Note 2. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 3.3 V, V_{PP} = 5.0 V, Ta = 25℃.
Note 3. I_{CCES} is specified with the device de-selected. If the device is read while in erase suspend mode, current draw is the sum of I_{CCES} and I_{CCR}.
Note 4. Automatic Power Saving (APS) reduces I_{CCR} to less than 2 mA in Static operation.
Note 5. CMOS Inputs are either V_{CC} ±0.2 V or GND ±0.2V. TTL Inputs are either V_{IL} or V_{IH}.
Note 6. These are the values of the current which is consumed within one bank area. The value for the bank0 and bank1 should added in order to calculate the value for the whole chip. If the bank0 is in write state and bank1 is in read state,the I_{CC} = I_{CCW} + I_{CCR}. If both bank are in standby mode, the value for the device is 2 times the value in the above table.

■ AC Characteristics



AC test inputs are driven at 3.0 V for a Logic "1" and 0.0 V for a Logic "0." Input timing begins, and output timing ends, at 1.5 V. Input rise and fall times (10% to 90%) < 10ns.

Figure 1. Transient input/output reference waveform (V_{CC} = 3.3 V)

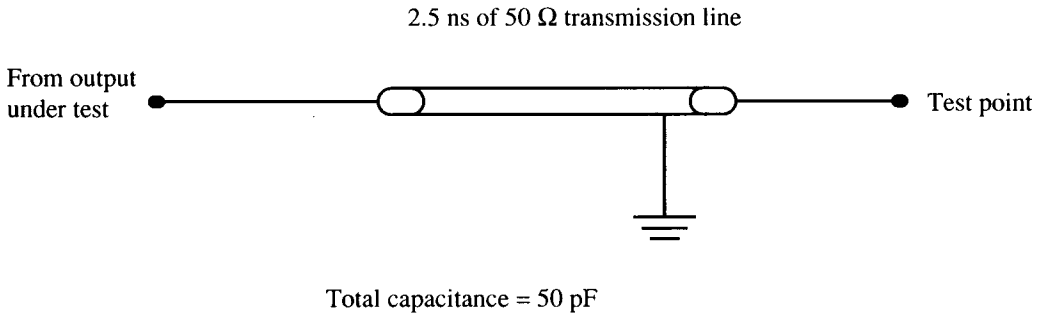


Figure 2. Transient equivalent testing load circuit (V_{CC} = 3.3 V)

〈Read only operations〉 Note 1

(V_{CC}=3.3±0.3 V, Ta=−20 to +70 ℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Read cycle time	t_{AVAV}	150			ns	
Address setup to OE# going low	t_{AVGL}	0			ns	3
Address to output delay	t_{AVQV}			150	ns	
BE_0#, BE_1# to output delay	t_{ELQV}			150	ns	2
OE# to output delay	t_{GLQV}			50	ns	2
BE_0#, BE_1# to output in Low-Z	t_{ELQX}	0			ns	3
BE_0#, BE_1# to output in High-Z	t_{EHQZ}			55	ns	3
OE# to output in Low-Z	t_{GLQX}	0			ns	3
OE# to output in High-Z	t_{GHQZ}			40	ns	3
Output hold from address, BE_0#, BE_1# or OE# change, whichever occurs first	t_{OH}	0			ns	3

(V_{CC}=2.85±0.15 V, Ta=−20 to +70 ℃)

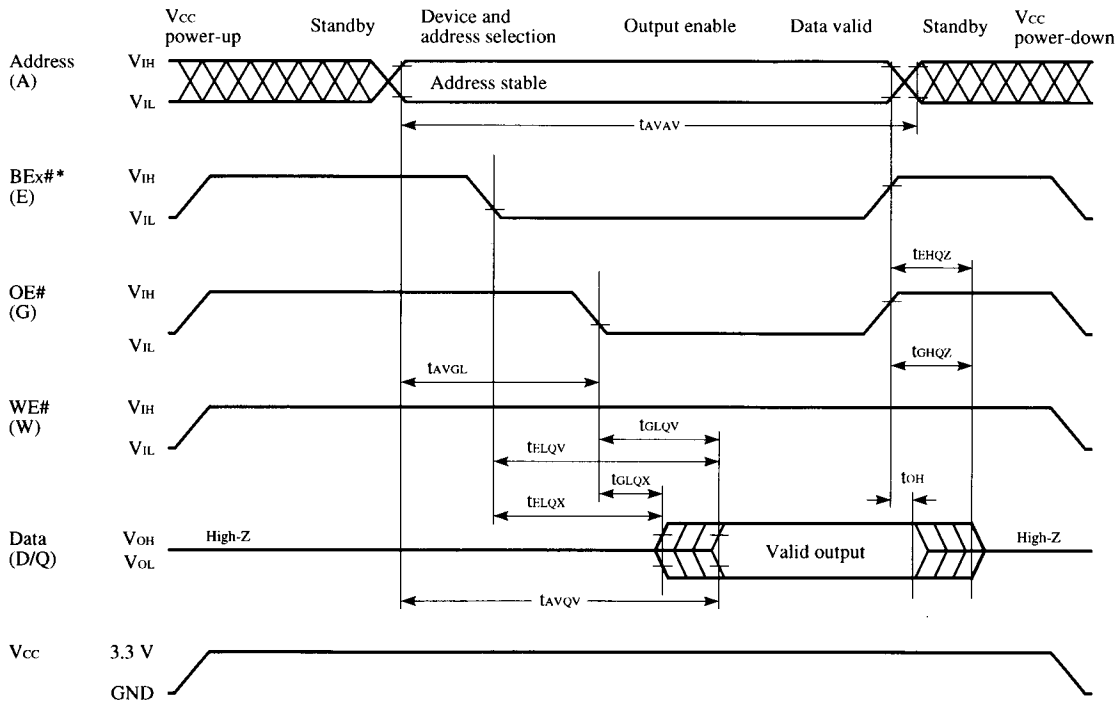
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Read cycle time	t_{AVAV}	190			ns	
Address setup to OE# going low	t_{AVGL}	0			ns	3
Address to output delay	t_{AVQV}			190	ns	
BE_0#, BE_1# to output delay	t_{ELQV}			190	ns	2
OE# to output delay	t_{GLQV}			65	ns	2
BE_0#, BE_1# to output in Low-Z	t_{ELQX}	0			ns	3
BE_0#, BE_1# to output in High-Z	t_{EHQZ}			70	ns	3
OE# to output in Low-Z	t_{GLQX}	0			ns	3
OE# to output in High-Z	t_{GHQZ}			55	ns	3
Output hold from address, BE_0#, BE_1# or OE# change, whichever occurs first	t_{OH}	0			ns	3

Note 1. See AC Input/Output reference waveforms for timing measurements, Figure 1.

Note 2. OE# may be delayed up to t_{ELQV}-t_{GLQV} after the falling edge of BE_0# or BE_1# without impact on t_{ELQV}.

Note 3. Sampled, not 100% tested.

○ Read timing Waveforms



* BEx# means either BE0# or BE1#.

〈Vcc Power-up and reset timing〉 Note 1

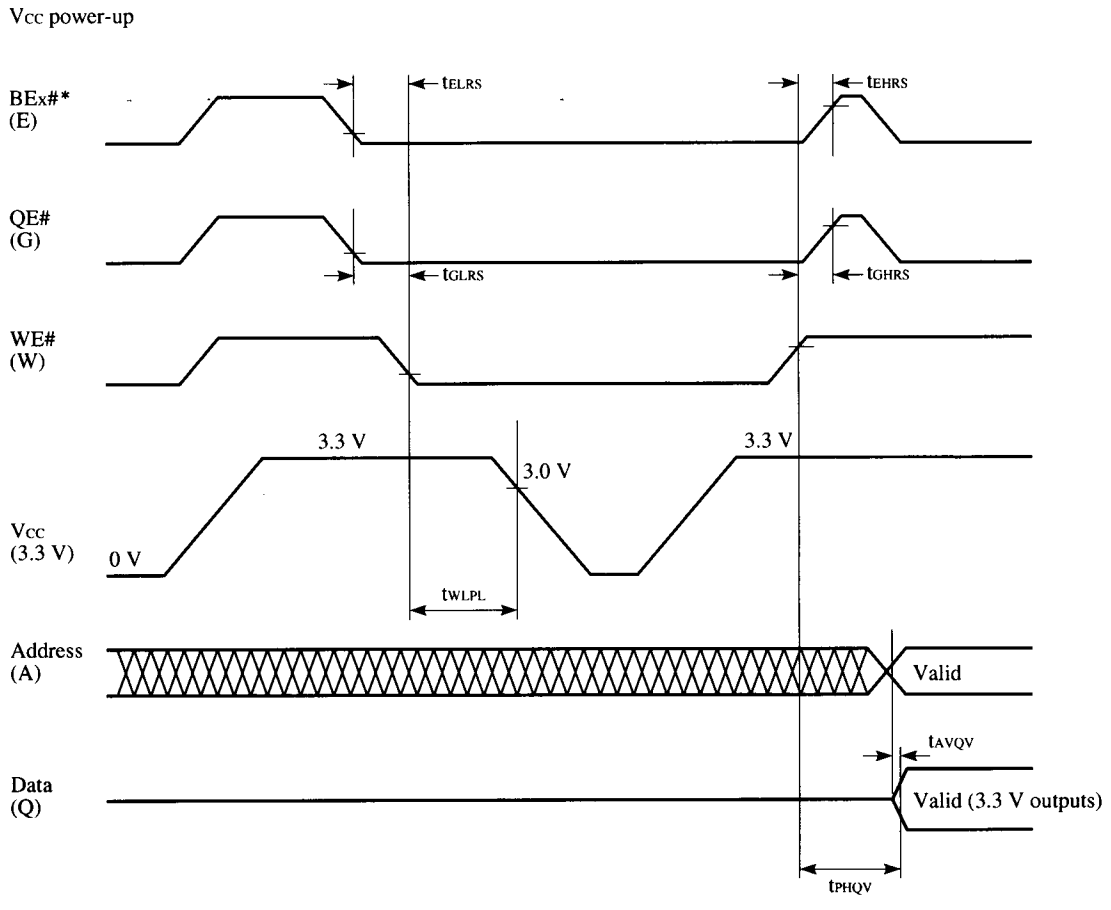
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
WE# low to Vcc at 3.0 V minimum	t_{WLPL}	5.0			μs	2
Address valid to data valid for Vcc = 3.3±0.3 V	t_{AVQV}			150	ns	3
WE# high to data valid for Vcc = 3.3±0.3 V	t_{PHQV}			500	ns	3
BE0# and BE1# setup to WE# going low	t_{ELRS}	100			ns	
OE# setup to WE# going low	t_{GLRS}	100			ns	
BE0# and BE1# hold from WE# going high	t_{EHRS}	100			ns	
OE# hold from WE# going High	t_{GHRS}	100			ns	

Note 1. BE0#, BE1# and OE# must be set high once after power-up. BE0# and BE1# must not be set low at the same time.

Note 2. Chip reset is enabled when the low state of all BE0# (or BE1#), OE# and WE# exceeds 5 μs. Especially when you will power on the chip, execute an above chip reset sequence for a protection from noise. All BE0# (or BE1#), OE# and WE# must not be low, except of the purpose for chip reset.

Note 3. These values are shown for 3.3 V Vcc operation. Refer to the AC Characteristics read only operations also.

○ Power-up and reset timing waveforms



* BEx# means either BE0# or BE1#.

〈WE# controlled command write operation〉 Note 1

(V_{CC}=3.25±0.35 V, Ta=−20 to +70 ℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Write cycle time	t_{AVAV}	150			ns	
V_{PP} setup to WE# going high	t_{VPWH}	100			ns	3
BE_0# and BE_1# setup to WE# going low	t_{ELWL}	0			ns	
Address setup to WE# going high	t_{AVWH}	110			ns	2, 6
Data setup to WE# going high	t_{DVWH}	110			ns	2, 6
WE# pulse width	t_{WLWH}	110			ns	
Data hold from WE# high	t_{WHDX}	10			ns	2
Address hold from WE# high	t_{WHAX}	10			ns	2
BE_0# and BE_1# hold from WE# high	t_{WHEH}	10			ns	
WE# pulse width high	t_{WHWL}	75			ns	
Read recovery before write	t_{GHWL}	0			ns	
Write recovery before read	t_{WHGL}	120			ns	
V_{PP} hold from valid status register data	t_{QVVL}	0			μs	
Duration of byte write operation	t_{WHQV1}	8.0	20	250	μs	4, 5, 7
Duration of block erase operation	t_{WHQV2}	0.3			s	4

Note 1. Read timing during write and erase are the same as for normal read.

Note 2. Refer to command definition tables for valid address and data values.

Note 3. Sampled, but not 100% tested.

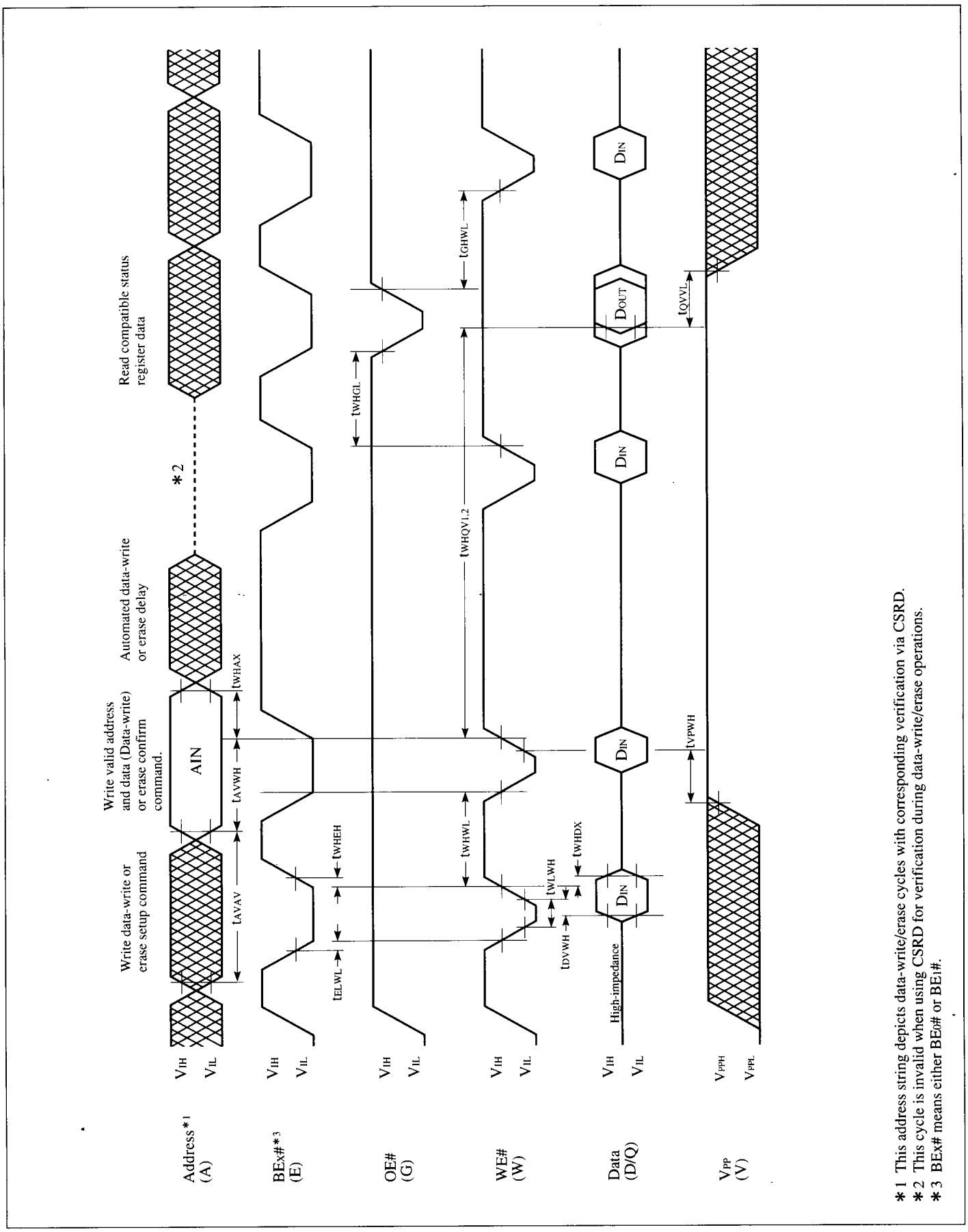
Note 4. Write/Erase durations are measured to valid Status Register (CSR) Data.

Note 5. Byte write operations are typically performed with 1 Programming pulse.

Note 6. Address and Data are latched on the rising edge of WE# for all Command write operations.

Note 7. The max value of byte write time is the maximum write time inside the chip. It is not the time until the whole writing procedure is completed properly. It is necessary to check CSR to see if the writing procedure is properly completed.

○ Command write operation waveforms (1)



*1 This address string depicts data-write/erase cycles with corresponding verification via CSRD.
*2 This cycle is invalid when using CSRD for verification during data-write/erase operations.
*3 BEx# means either BE0# or BE1#.

〈BE# controlled command write operation〉 Note 1

(V_{CC}=3.25±0.35 V, Ta=−20 to +70 ℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Write cycle time	t_{AVAV}	150			ns	
V_{PP} setup to BE_0# or BE_1# going high	t_{VPEH}	100			ns	3
WE# setup to BE_0# or BE_1# going low	t_{WLEL}	0			ns	
Address setup to BE_0# or BE_1# going high	t_{AVEH}	110			ns	2, 6
Data setup to BE_0# or BE_1# going high	t_{DVEH}	110			ns	2, 6
BE_0# or BE_1# pulse width	t_{ELEH}	110			ns	
Data hold from BE_0# or BE_1# high	t_{EHDX}	10			ns	2
Address hold from BE_0# or BE_1# high	t_{WHAX}	10			ns	2
WE# hold from BE_0# or BE_1# high	t_{EHWH}	10			ns	
BE_0# or BE_1# pulse width high	t_{EHEL}	75			ns	
Read recovery before write	t_{GHWL}	0			ns	
Write recovery before read	t_{EHGL}	120			ns	
V_{PP} hold from valid status register data	t_{QVVL}	0			μs	
Duration of byte write operation	t_{EHQV1}	8.0	20	250	μs	4, 5, 7
Duration of block erase operation	t_{EHQV2}	0.3			s	4

Note 1. Read timing during write and erase are the same as for normal read.

Note 2. Refer to command definition tables for valid address and data values.

Note 3. Sampled, but not 100% tested.

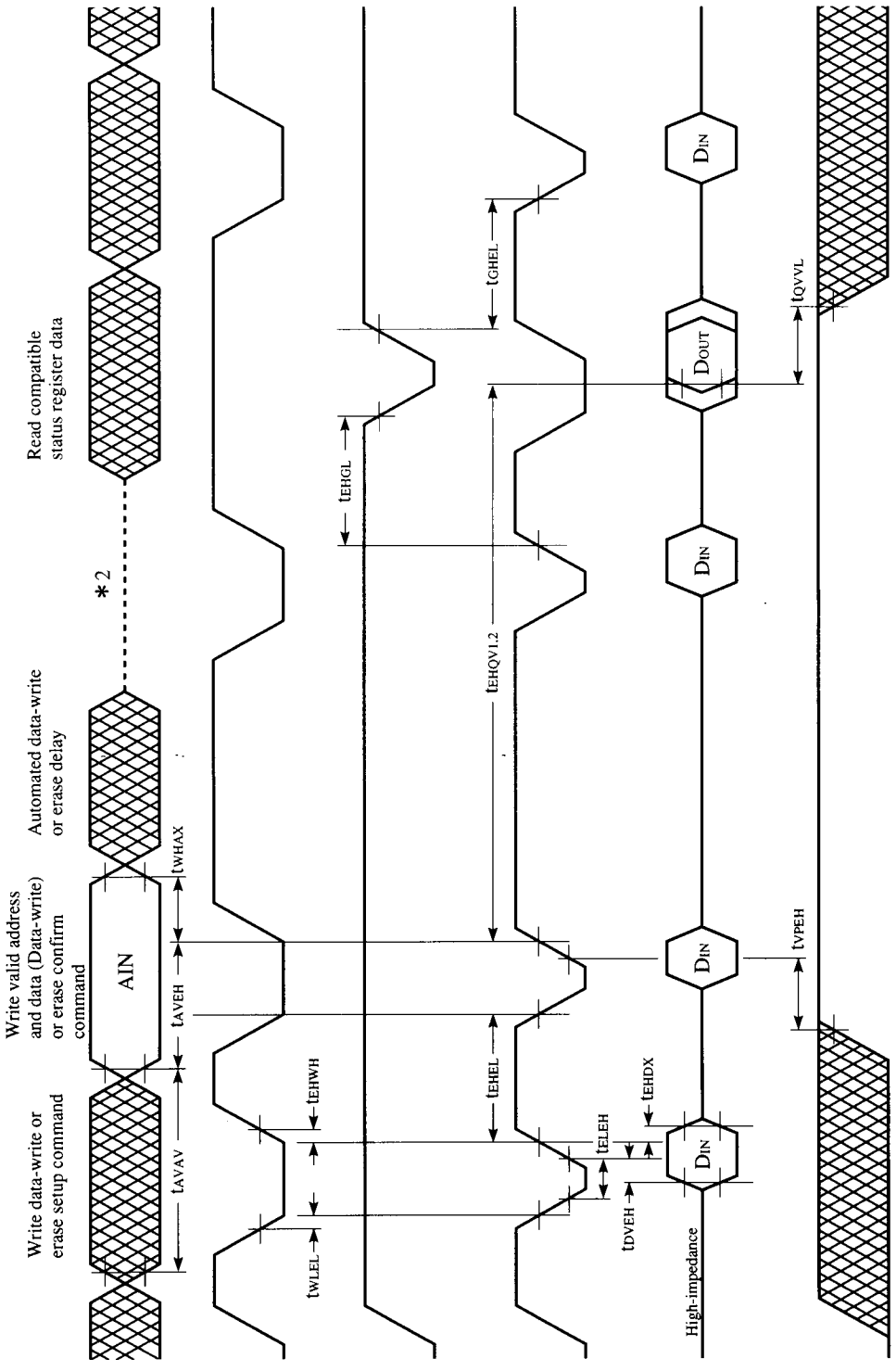
Note 4. Write/Erase durations are measured to valid Status Register (CSR) Data.

Note 5. Byte write operations are typically performed with 1 Programming Pulse.

Note 6. Address and Data are latched on the rising edge of BE_0# or BE_1# for all Command write operations.

Note 7. The max value of byte write time is the maximum write time inside the chip. It is not the time until the whole writing procedure is completed properly. It is necessary to check CSR to see if the writing procedure is properly completed.

○ Command write operation waveforms (2)



*1 This address string depicts Data-Write/Erase cycles with corresponding verification via CSRD.
*2 This cycle is invalid when using CSRD for verification during Data-Write/Erase operations.
*3 BEx# means either BE0# or BE1#.

〈Erase and byte write performance〉

(V_{CC}=3.25±0.35 V, Ta=−20 to +70 ℃)

Parameter	Symbol	Conditions	MIN.	TYP.*	MAX.	Unit	Note
Byte write time	t_{WHRH1}			20	250	μs	1, 2
Two-byte serial write time	t_{WHRH2}			34		μs	1
16kB block write time	t_{WHRH3}	Byte write mode		0.33	1.0	s	1
16kB block write time	t_{WHRH4}	Two-byte serial write mode		0.28	1.0	s	1
Block erase time (16kB)				0.8		s	1
2M-bit bank erase time				9 to 15		s	1, 3

* 25 ℃, V_{PP}=5.0 V

Note 1. Excludes System-Level Overhead. It actually indicates the time from input write/erase command until bit7 of status register becomes ready (WSMS = 0).

Note 2. The max value of byte write time is the maximum write time inside the chip. It is not the time until the whole writing procedure is completed properly. It is necessary to check CSR to see if the writing procedure is properly completed.

Note 3. Depends on the number of protected blocks.

SHARP

SHARP CORPORATION Japan

HEAD OFFICE
INTERNATIONAL SALES & MARKETING GROUP
-IC/ELECTRONIC COMPONENTS
22-22, NAGAIKE-CHO, ABENO-KU, OSAKA 545, JAPAN
PHONE: (06) 621-1221
FAX: 6117-725300, 6117-725301, 6117-725302

IC SALES DEPARTMENT
INTERNATIONAL SALES & MARKETING GROUP
-IC/ELECTRONIC COMPONENTS
2613-1 ICHINOMOTO-CHO TENRI-CITY NARA 632, JAPAN
PHONE: (07436) 5-1321
FAX: (07436) 5-1532

U.S.A.

SHARP ELECTRONICS CORPORATION
Microelectronics Group

North American Head Quarters
5700 Northwest Pacific Rim Blvd. #20,
Camas, WA 98607
PHONE: (1)360-834-2500
FAX : (1)360-834-8903

West
1980 Zanker Road, San Jose, CA 95112
PHONE: (1)408-436-4900
FAX : (1)408-436-0924

16841 Armstrong Avenue,
Irvine, CA 92714
PHONE: (1)714-25-0225
FAX : (1)714-250-0438

Central
1025 Royal Lane,
DFW Airport, TX 75261-9035
PHONE: (1)972-574-5205
FAX : (1)972-574-9870

10222 Scull Creek, Austin, TX 78730
PHONE: (1)512-349-7262
FAX : (1)512-349-7002

9950 Cypresswood, Suite 350,
Houston, TX 77070
PHONE: (1)713-955-9909
FAX : (1)713-955-9910

East
1300 Napervill Road, Romeoville, IL 60441
PHONE: (1)630-226-2400
FAX : (1)630-759-8572

691 N. Squirrel Road, Suite 110,
Auburn Hills, MI 48326
PHONE: (1)810-377-9220
FAX : (1)810-377-9222

14A Second Avenue, Burlington, MA 01803
PHONE: (1)617-270-7979
FAX : (1)617-229-9117

Canterbury Hall, 4815 Emperor Blvd.
Suite 140, Durham, NC 27703
PHONE: (1)919-941-0065
FAX : (1)919-941-0066

EUROPE

SHARP ELECTRONICS (EUROPE) GmbH

Head Office
Microelectronics Division, (MED)
Sonninstrasse 3, 20097 Hamburg, Germany
PHONE: (49)40-23 76 22 86
FAX : (49)40-23 76 22 32

Germany MED Stuttgart Office
Zettachring 8, 70567, Stuttgart, Germany
PHONE: (49)711-90076-3
FAX : (49)711-90076-50

Germany MED Nürnberg Office
Donaustrasse 69, 90451 Nürnberg, Germany
PHONE: (49)911-642 70 51
FAX : (49)911-642 66 69

France MED Paris Office
Immeuble Rosny 2, Avénue du
Général de Gaulle 93110
Rosny Sous Bois Cédex, France
PHONE: (33)1-48 12 19 00
FAX : (33)1-48 55 46 78

Italy MED Milano Office
Centro Direzionale Colleoni
Palazzo Taurus Ingresso 2
20041 Agrate Brianza, Milano, Italy
PHONE: (39)39-68 99 946
FAX : (39)39-68 99 948

U.K. MED London Office
Centennial Court, Easthampstead
Road Bracknell, Berks RG12 1YQ,
United Kingdom
PHONE: (44)1344-86 99 22
FAX : (44)1344-36 09 03

U.K. MED Scotland Office
Unit 48 Grovewood Business Centre,
Strathclyde Business Park,
Bellshill ML43NQ,
Scotland, United Kingdom
PHONE: (44)1698-84 34 42
FAX : (44)1698-84 28 99

Ireland MED Dublin Office
First Floor, Block 1, St. Johns Court
Santry, Dublin 9, Ireland
PHONE: (353)1-842 87 05
FAX : (353)1-842 84 55

ASIA

SHARP-ROXY (HONG KONG) LTD.
3rd Business Division,
17/F, Admiralty Centre,
Tower 1, 18 Harcourt Road, Hong Kong
PHONE : (852)28229311
FAX : (852)28660779

SHARP ELECTRONICS (SINGAPORE) PTE., LTD.
Electronic Components Division,
100, Beach Road #32-07 to 13,
Shaw Towers, Singapore 189702
PHONE : (65)295-0566
FAX : (65)295-0977

SHARP ELECTRONIC COMPONENTS (TAIWAN) CORPORATION
8Fl., No. 16, Sec. 4, Nanking E. Rd.,
Taipei, Taiwan, Republic of China
PHONE : (886)2-577-7341
FAX : (886)2-577-7326, (886)2-577-7328

SHARP ELECTRONIC COMPONENTS (KOREA) CORPORATION
RM 501 Geosung B/D, 541,
Dohwa-dong, Mapo-ku, Seoul, Korea
PHONE : (82)2-711-5813 to 5818
FAX : (82)2-711-5819

The circuit application examples in this publication are provided to explain representative applications of SHARP devices and are not intended to guarantee any circuit design or license any intellectual property rights. SHARP takes no responsibility for any problems related to any intellectual property right of a third party resulting from the use SHARP devices.

In the absence of confirmation by device specification sheets, SHARP takes no responsibility for any defects that occur in equipment using any of SHARP devices shown in catalogs, data books, etc.

SHARP reserves the right to make changes in the specifications, characteristics, data, materials, structures and other contents described herein at any time without notice in order to improve design or reliability. Contact SHARP in order to obtain the latest specification sheets before using any SHARP device. Manufacturing locations are also subject to change without notice.

Observe the following points when using any device in this publication. SHARP takes no responsibility for change caused by improper use of the devices, which does not meet the conditions and absolute maximum ratings for use specified in the relevant specification sheet nor meet the following conditions :

■ The devices in this publication are designed for use in general electronic equipment designs, such as :
- Personal computers
- Office automation equipment
- Telecommunication equipment (except for trunk lines)
- Test and measurement equipment
- Industrial control
- Audio visual equipment
- Consumer electronics

■ Measures such as Fail-safe function and redandant desigh should be taken to ensure reliability and safety when SHARP devices are used for or in connection with equipment that requires higher reliability such as :
- Main frame computers
- Transportation control and safety equipment (i.e., aircraft, trains, automobiles, etc.)
- Traffic signals
- Gas leakage sensor breakers
- Alarm equipment
- Various safety devices etc.

■ SHARP devices shall not be used for or in connection with equipment that requires an extremely high level of reliability and safety such as :
- Space applications
- Telecommunication equipment (trunk lines)
- Nuclear power control equipment
- Medical and other life suport equipment (e.g scuba)

Contact a SHARP representative in advance when intending to use SHARP devices for any "specific" applications other than those recommended by SHARP or when it is unclear which category mentioned above controls the intended use.

If the SHARP devices listed in this publication fall in the scope of strategic products described in the Foreign Exchange and Foreign Trade Control Law, it is necessary to obtain export permission or approval under the law in order to export such SHARP devices.

Contact and consult with a SHARP representative if there are any questions about the contents of this publication.

Ref. No. NP 161C

LH28Fxxx FLASH MEMORY FLASH NON-VOLATILE MEMORY FLASH E2ROM FLASH ROM READ ONLY MEMORY ETOX DUAL VOLTAGELH28F040SU 4M-bit Dual Work