SHARP

No: RD-96Y16

RELIABILITY TEST REPORT

Dual power operation

Product Type : 16M bit flash memory

Model No. : LH28F016SAT

Package : 56Pin TSOP (TSOP056-P-1420)

Date : NOV. 28, 1996

GENERAL MANAGER M. NAKAJIMA

QUALITY & RELIABILITY CONTROL CENTER
TENRI INTEGRATED CIRCUITS GROUP
SHARP CORPORATION

1. Quality Assurance And Reliability Testing During New Product Development

New product development begins with establishing reliability targets during the planning stage. During this stage the end applications functions and requirements are also considered in addition to the reliability targets.

Quality and reliability are built into the product from the start by having design and reliability review sessions in the development and design stages. This insures that quality and reliability levels are maintained at the preproduction and mass production stages.

2. Reliability Test Methods

Reliability tests should always have good reproducibility. Thus, reliability tests for IC devices are based upon standardized test methods. Such uniform testing standards include those established by JIS(Japanese Industrial Standard), MIL-STD(U.S. MILitary Standard), EIAJ(Electronic Industries Association of Japan) and IEC(International Electrotechnical Commission). Sharp has based its own testing methods on these standards.

3. Evaluation Results

The results attached show that Sharp has met the high quality and reliability targets which are required by the above standards.

Note: This evaluation has been performed upon a representative product which is selected from a series of related products with the same basic design, all packaged in the same package type. Therefore, these evaluation results are applicable for the following Sharp models :

LH28F016SAT, LH28F016SAR

4. Other Considerations

Please confirm that the specifications of this product meet the requirements of the application.

1-1. ENDURANCE TEST-1

No.	Test	Conditions	Reference Standards	Number of Samples	Number of Failures / Test Time			LTPD
					240h	500h	1 000h	
1	High Temperature Operation	Ta=125℃ V_{CC}/V_{PP}=6.5V 1 000h	JIS C 7022:B-1 MIL-STD-883C 1005.6	153	0	0	0	1.5%
					240h	500h	1 000h	
2	High Temp. Storage	Ta=140℃ 1 000h	JIS C 7022:B-3 MIL-STD-883C 1008.2	45	0	0	0	5%
					240h	500h	1 000h	
3	Low Temp. Storage	Ta=-65℃ 1 000h	JIS C 7022:B-4	11	0	0	0	20%
					240h	500h	1 000h	
4	High Temp. High Humi. Storage	Ta=60℃, 90%RH 1 000h	JIS C 7022:B-5	22	0	0	0	10%
					240h	500h	1 000h	
5	High Temp. High Humi. Bias	Ta=85℃, 85%RH V_{CC}/V_{PP}=5.5V 1 000h	JIS C 7022:B-5	76	0	0	0	3%

1-2. ENDURANCE TEST-2

No.	Test	Conditions	Reference Standards	Number of Samples	Number of Failures	LTPD
6	Thermal Shock	Ta=-65℃(5min)~150℃(5min) 100cyc	JIS C 7022:A-3 MIL-STD-883C 1011.7	45	0	5%
7	Temp. Cycling	Ta=-65℃(30min)~150℃(30min) 500cyc	JIS C 7022:A-4 MIL-STD-883C 1010.7	76	0	3%
8	Temp. & Humi. Cycling	Ta=-10℃~65℃, 90~96%RH 1cyc/24h 10cyc	JIS C 7022:A-5 MIL-STD-883C 1004.7	22	0	10%
9	Solt Atmosphere	Solt Concentration=5wt% Solt Fog Temp.=35℃ Spray Rate=10~50g/m²/d 24h	JIS C 7022:A-12 MIL-STD-883C 1009.7	22	0	10%

CRITERIA

No. 1 ~ 8 : To maintain electrical characteristics within the limits established in the specifications of each device.

No. 9 : To maintain electrical characteristics within the limits established in the specifications of each device.
There is no evidence of damage to the body material or lead finish of each device. All package marking is remain visible to the naked eye.

1-3. ENDURANCE TEST-3

No.	Test	Conditions	Reference Standards	Number of Samples	Number of Failures	LTPD
10	[Series Test] Baking	Ta=150℃ 20h	EIAJ ED-4701:B-101	22		10%
	↓ Moisture Absorption	Ta=30℃, 70% 96h				
	↓ I.R Soldering	Highest Temp.=240℃, 230℃~240℃. 15s			0	
	↓ PCT	Ta=121℃, 100%RH, No Bias 2×10^5 Pa{2atm}, 100h			0	

CRITERIA

No. 10 : To maintain electrical characteristics within the limits established in the specifications of each device.
There is no evidence of damage to the body material(i.e. Package cracking)

2. ERASE/WRITE CYCLING TEST

No.	Test	Conditions	Number of Cycles	Number of Samples	Number of Failures	Failure Rate	Note
1	Erase/ Write Cycling	Ta=0, 70℃	10k	1890	0	15 DPM/Block	Confidence Level=60%
			100k		0	243 DPM/Block	

CRITERIA

No. 1 : To maintain electrical characteristics within the limits established in the specifications of each device.

3. MECHANICAL TEST

No.	Test	Conditions	Reference Standards	Number of Samples	Number of Failures	LTPD
1	Vibration	100~2 000~100Hz. 4min 200m/s² {20G} X. Y. Z each 4times. total 48min	JIS C 7022:A-10 MIL-STD-883C 2007. 1	11	0	20%
2	Shock	15 000m/s² {1 500G} 0. 5ms. ±X. ±Y. ±Z each 3 times	JIS C 7022:A-7 MIL-STD-883C 2002. 3	11	0	20%
3	Acceleration	200 000m/s² {20 000G} ±X. ±Y. ±Z each 1 min	JIS C 7022:A-9 MIL-STD-883C 2001. 2	11	0	20%
4	Terminal Strength (Bending)	A specified load ※ is applied to the tip of each lead is bent once through a 90° arc and back. 0. 25・~~0. 5~~・~~1. 25~~ N 1 time	JIS C 7022:A-11 MIL-STD-883C 2004. 5	5	0	50%
5	Terminal Strength (Tension)	A specified load ※ is applied in a direction parallel to the lead axis. 0. 5・~~1. 0~~・~~2. 5~~ N 10s	JIS C 7022:A-11 MIL-STD-883C 2004. 5	5	0	50%
6	Solderability	230℃ 5s Used with rosin flux	JIS C 7022:A-2 MIL-STD-883C 2003. 5	11	0	20%

※ The specified load is determined by nominal cross section.

CRITERIA

No. 1, 2, 3 : To maintain electrical characteristics within the limits established in the specifications of each device.

No. 4, 5 : There is no evidence of damage to the body. There is no broken or cracked lead (terminals).

No. 6 : Lead coverage of at least 95% with a continuous solder coating. Pinholes and voids are not concentrated in one area and exceed 5% of the total area.

3. MISCELLANEOUS

No.	Test	Conditions	Reference Standards	Number Of Samples	Number Of Failures	LTPD
1	Permanence Of Marking	20~25℃, Brushing 5 times after dipping 10 minutes	EIAJ ED-4701:C-121 (Solvent):Acetone, Butyl acetate, Isopropyl alcohol, Ethyl alcohol	11(each)	0	20%

No.	Test	Conditions	Reference Standards	Number Of Samples	Condition	ESD/Latch-up Strength				
						≧0.4kV	≧0.6kV	≧0.8kV	≧1.0kV	
2	Electro-static discharges	C=100pF R=1.5kΩ	MIL-STD 883C Method 3015	3(each)	GND, +				○	
					GND, -				○	
					VCC, +				○	
					VCC, -				○	
3	Latch-up	Current application test Tp=10ms, Toff=500ms, VccMAX	EIAJ ED-4701-1 C-113	3(each)		≧40mA	≧60mA	≧80mA	≧100mA	
					+				○	
					-				○	

"○" Pass, "×" NG, "—" No measurement

CRITERIA

No. 1 : There is no evidence of damage to the device and package marking which are no missing in whole or in part.

No. 2 : To maintain electrical characteristics within the limits established in the specifications of each device.

No. 3 : No latch-up occurs.

SHARP

No: RD-96Y18

RELIABILITY TEST REPORT

Dual power operation

Product Type : 16M bit flash memory

Model No. : LH28F016SAT(New device)

Package : 56Pin TSOP (TSOP056-P-1420)

Date: NOV. 28. 1996

GENERAL MANAGER M. NAKAJIMA

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					240h	500h	1 000h	
3	Low Temp. Storage	Ta=-65℃ 1 000h	JIS C 7022:B-4	11	0	0	0	20%
					240h	500h	1 000h	
4	High Temp. High Humi. Storage	Ta=60℃, 90%RH 1 000h	JIS C 7022:B-5	22	0	0	0	10%
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No.	Test	Conditions	Reference Standards	Number of Samples	Number of Failures	LTPD
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	Moisture Absorption	Ta=30℃, 70% 96h				
	I.R Soldering	Highest Temp.=240℃, 230℃~240℃. 15s			0	
	PCT	Ta=121℃, 100%RH, No Bias 2×10^5 Pa{2atm}. 100h			0	

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No.	Test	Conditions	Number of Cycles	Number of Samples	Number of Failures	Failure Rate	Note
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Overview of Alteration to Flash Manufacturing process

Purpose

(1) Yield improvement

(2) Allow to manufacture with completely compatible process to that of Current device

(3) Device(5V-single power operation 16M Flash Memory) has same or partially improved performance.

Equalize memory cell performance and transistor performance

Key concept

(1) Adoption of most advanced manufacturing process

(2) 1.71 μm x 1.9 μm Memory cell size(1.8 μm x 2.0 μm : Current device)
The size of X, Y have been 95% short, end, cell area been 90.25% of current device.

Character of shrink process

(1) We have redesigned memory cell

- We have not changed memory cell performance in order to assure the equality of device performance

  Memory cell gate length : has not been changed

  Memory cell gate width : has not been changed

  Active space : has been shrunk to 0.66 μm form0.75 μm

  1 space of poli : has been shrunk to 0.5 μm from 0.6 μm

  Contact size : has been shrunk to 0.64 μm from 0.7 μm

(2) peripheral

The gate length of N/P transistor has not been changed

(3) Requirement for Photo

Same alignment margin

Same line width control ability

Sharp Corporation
Tenri Integrated Circuit Group
Flash memory Development Center

IC structure analysis note

structure and manufacturing place

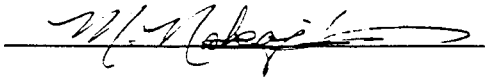
Model name	: LH28F016SAT/SAR (New device)
Article	Content
Package	56 Pin TSOP (Type 1)
Package material	Plastic
Chip size	11.02 mm x 10.15mm
Process	CMOS
Minimum design rule	0.55 μ m
Wiring layer	Al = 2 layer Poli-si = 2 layer
Chip cost material	Nothing
Passivation	SiON/low density BPSG
Integration scale	VLSI(more than 100000 transistor)
Lead frame material	42 alloy
Surface cost	Solder plating
Mount material	Solver paste
Wire material	AU

Manufacturing Place

Wafer	: Sharp corporation Fukuyama No.1, 2, 3 Group
Assembly	: San-Es corporation / Sharp Takaya electronic industry corporation
Test	: The same place the above

Signature : 1996 .Nov 28

Sharp Corporation
IC Tenri Group
Quality & Reliability Control Center Tel 07436-5-4038
Masayuki Nakajima



IC structure analysis note

structure and manufacturing place

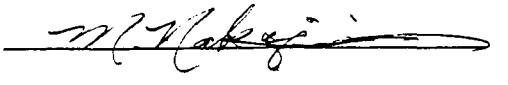
Model name	: LH28F016SAT/SAR (Current device)
Article	Content
Package	56 Pin TSOP (Type 1)
Package material	Plastic
Chip size	11.66 mm x 10.69mm
Process	CMOS
Minimum design rule	0.6 μ m
Wiring layer	Al = 2 layer Poli-si = 2 layer
Chip cost material	Nothing
Passivation	SiON/low density BPSG
Integration scale	VLSI(more than 100000 transistor)
Lead frame material	42 alloy
Surface cost	Solder plating
Mount material	Solver paste
Wire material	AU

Manufacturing Place

Wafer	: Sharp corporation Fukuyama No.1, 2, 3 Group
Assembly	: San-Es corporation / Sharp Takaya electronic industry corporation
Test	: The same place the above

Signature :

1996 .Nov 28
Sharp Corporation
IC Tenri Group
Quality & Reliability Control Center Tel 07436-5-4038
Masayuki Nakajima



D.R. P827 vs P827D

Memory cell

Equal size of gate width and length after alteration of process
Equal memory cell character

	Current device			New device
	LSL	Target	USL	
Gate width	0.88	1.00	1.12	1.00
Gate length	0.79	0.87	0.95	0.87

Peripheral Transistor

Equal minimum gate after shrink
Transistor performance and reliability not been changed
Although the 95% shrink of gate width has decreased the drive performance, the 10% less of parasitic capacitance has prevented it form AC characteristics fail.

	Current device			New device
	LSL	Target	USL	
Gate length	0.72	0.84	0.96	0.845

Contact, VIA

Although shrink has increased the resistance, it is within a tolerance of design.

Wiring resistance

Due to the constant L/W ratio, has not been affected by shrink

Sharp Corporation
Flash Memory Development Center

E-test P827 vs P827D

Current device

New device

	P827			P827D
	LSL	Target	USL	Target
Cell drain contact chain	6400	7285	10200	7800
poli contact chain	140000	180960	36000	183960
P+ contact chain	6000	13950	22325	19153
N+ contact chain	370	672	1075	672
poli2 contact chain	550	672	1075	684
VIA chain	20	35	70	40

	P827			P827D
	LSL	Target	USL	Target
Cell drain contact chain	-12.1%	7285	40.0%	7.1%
poli contact chain	-22.6%	180960	98.9%	1.7%
P+ contact chain	-57.0%	13950	60.0%	37.3%
N+ contact chain	-28.3%	672	59.9%	30.2%
poli2 contact chain	-18.2%	672	60.0%	1.8%
VIA chain	-42.9%	35	100%	14.3%

Sharp Corporation
Flash Memory Development Center

SHARP

TO _____

LHF16S01 (Current device) ／LHF16S17 (New device)

Characteristic Data Comparison

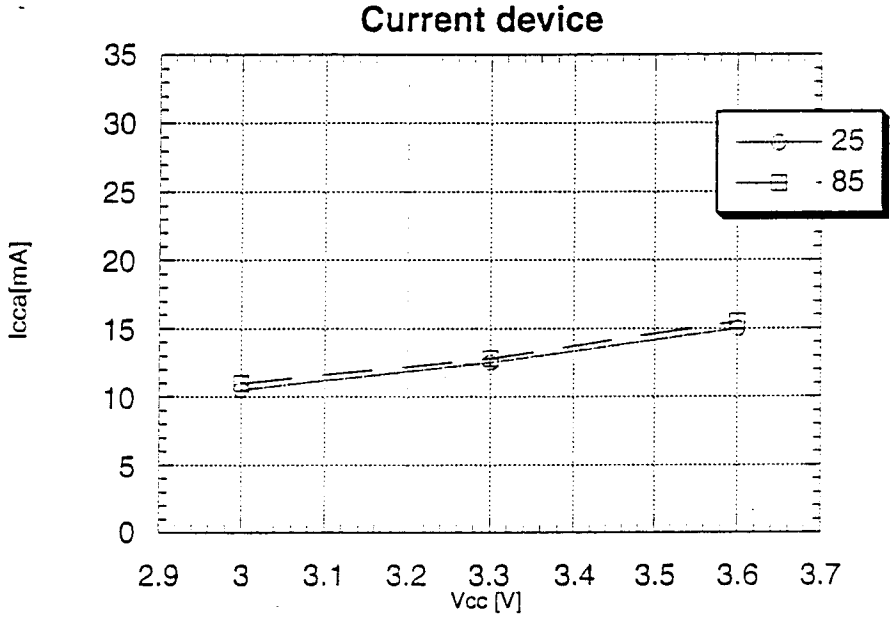
Sharp Corporation
IC Tenri Group
FLash Memory Development Center

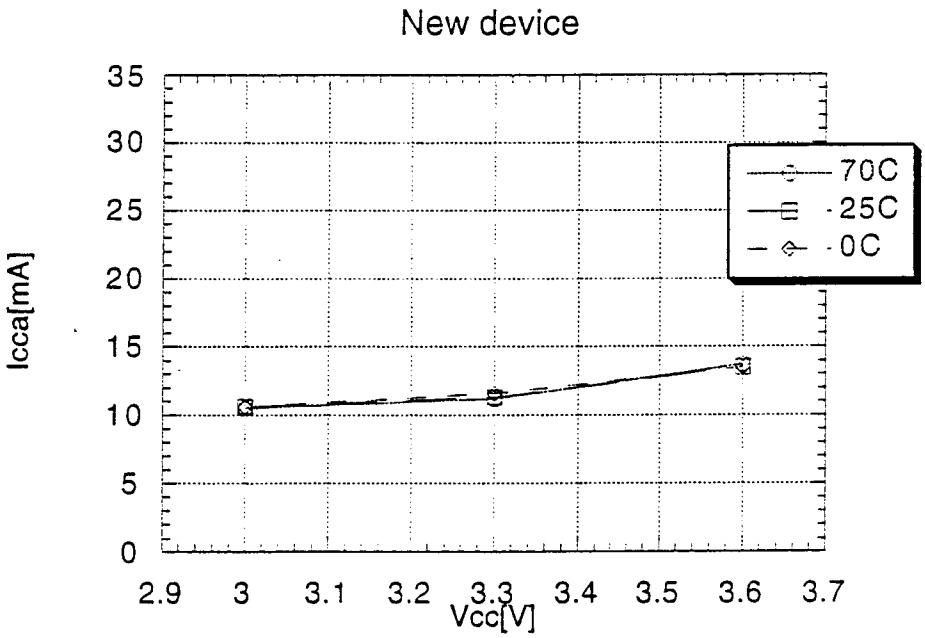
LH28F016SA Series
LHF16S01/LHF16S17

SHARP

Icc Active TTL

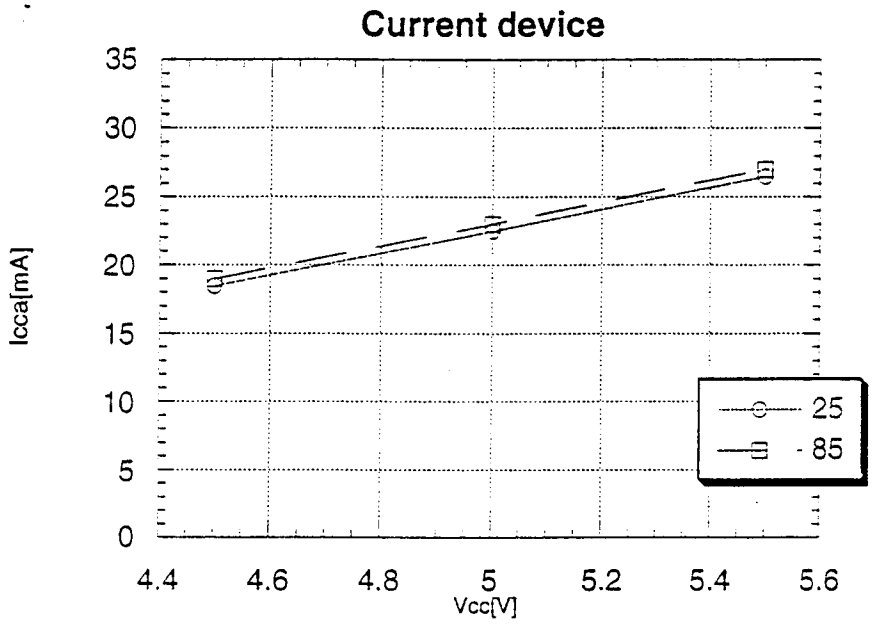
Addr=0.4/2.4[V], f=4MHz,Iout=0[mA] Spec=20[mA] Max

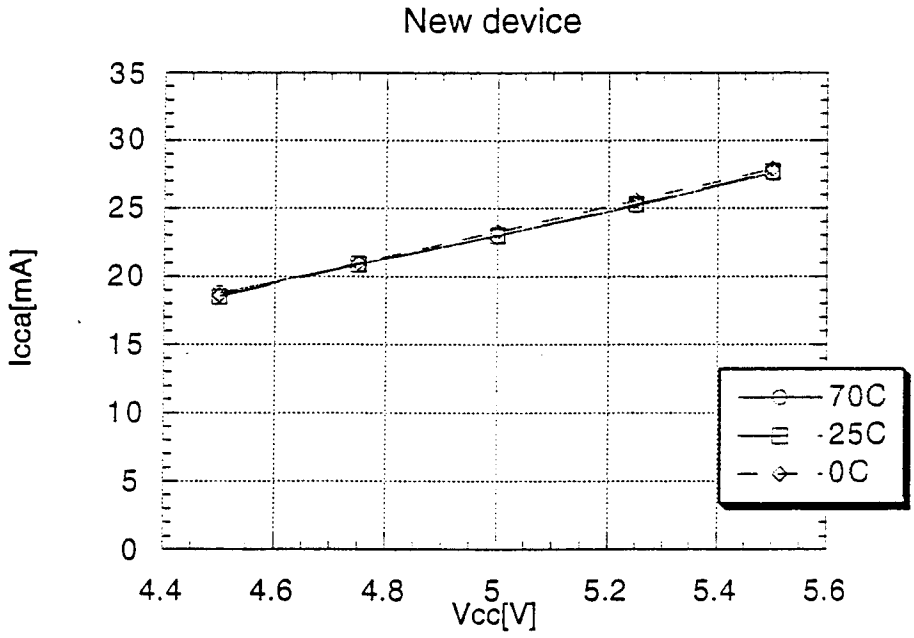




Icc Active TTL

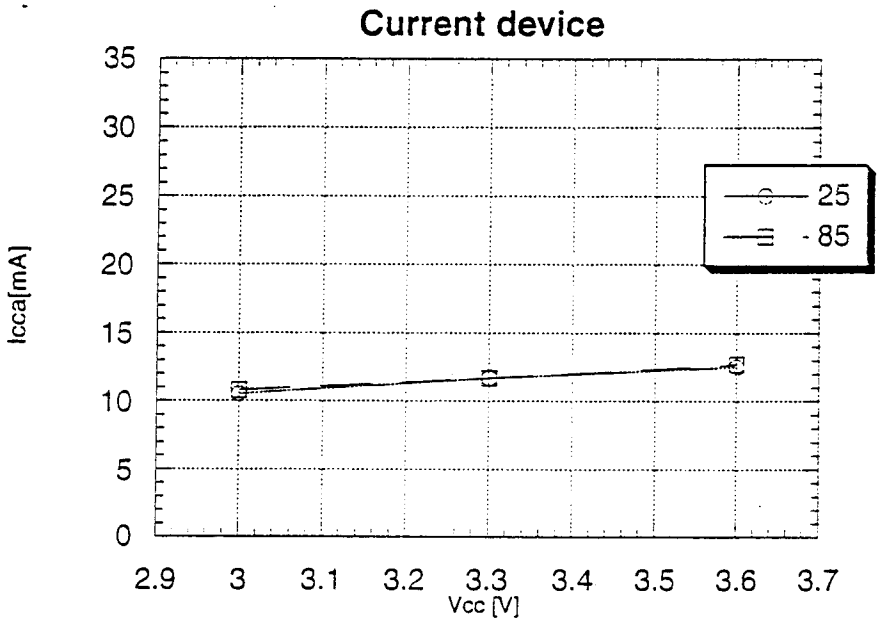
Addr=0.4/2.4[V], f=5MHz, Iout=0[mA] Spec=35[mA] Max

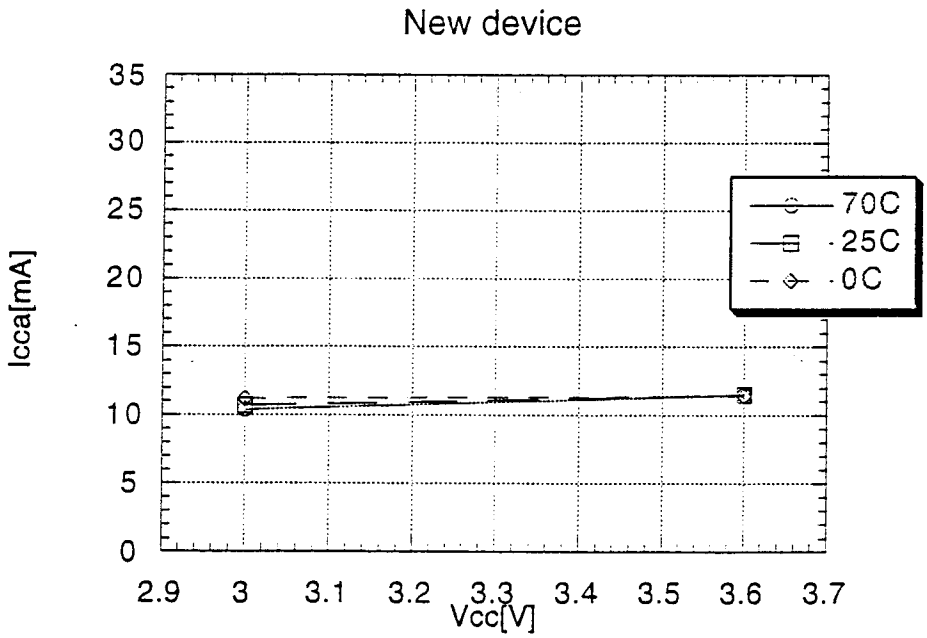




Icc Active CMOS

Addr=0.4/2.4[V], f=4MHz, Iout=0[mA] Spec=20[mA] Max

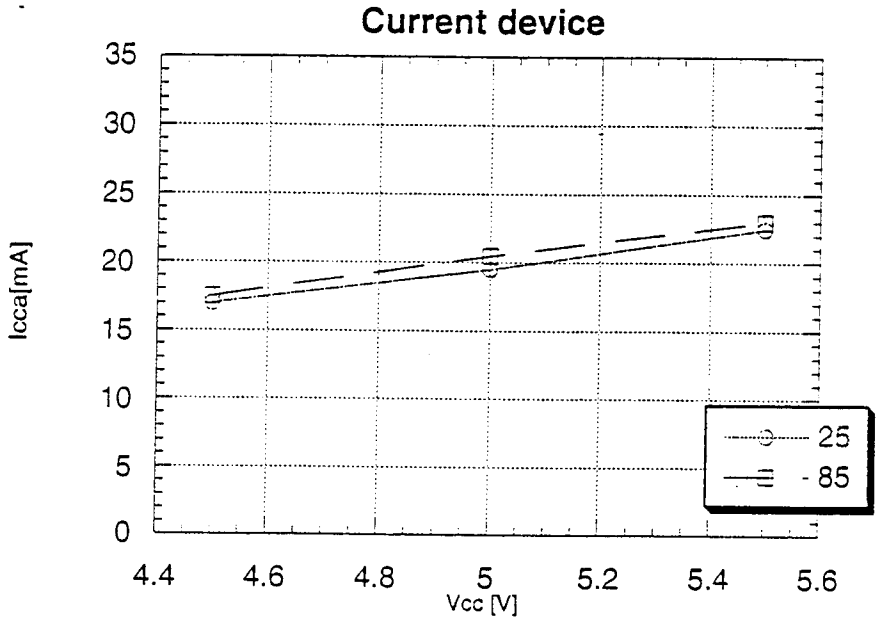


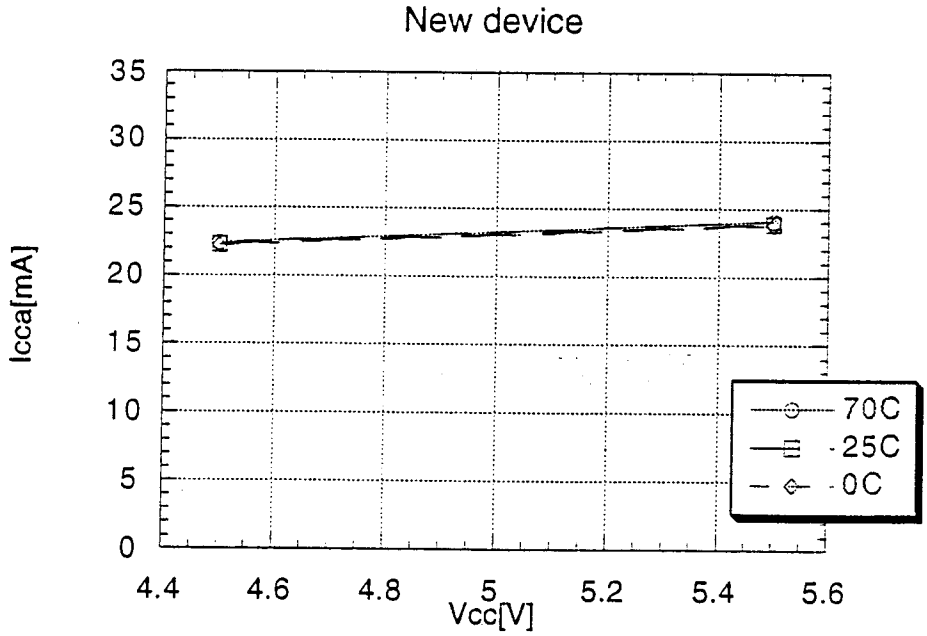


SHARP

Icc Active CMOS

Addr=0.4/2.4[V], f=5MHz, Iout=0[mA] Spec=35[mA] Max

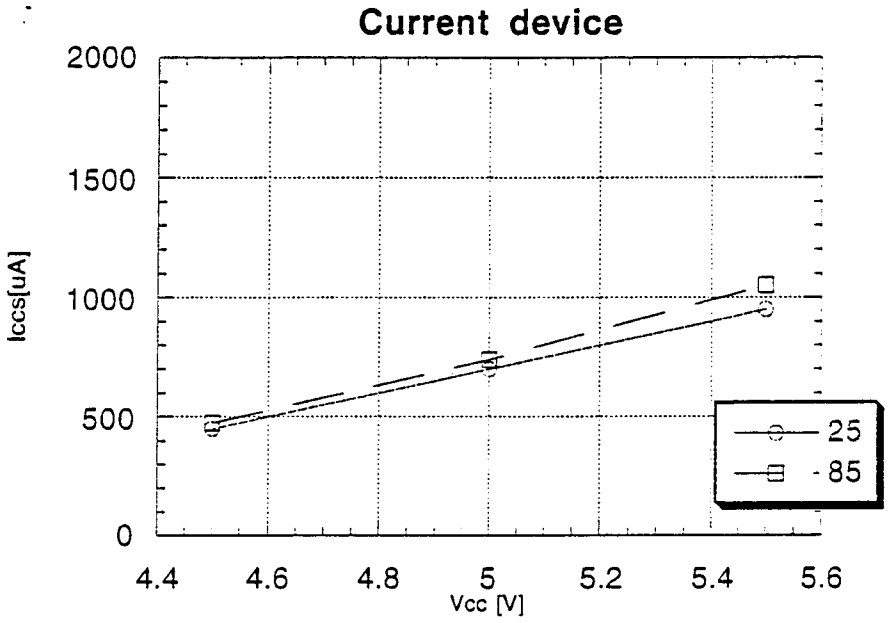


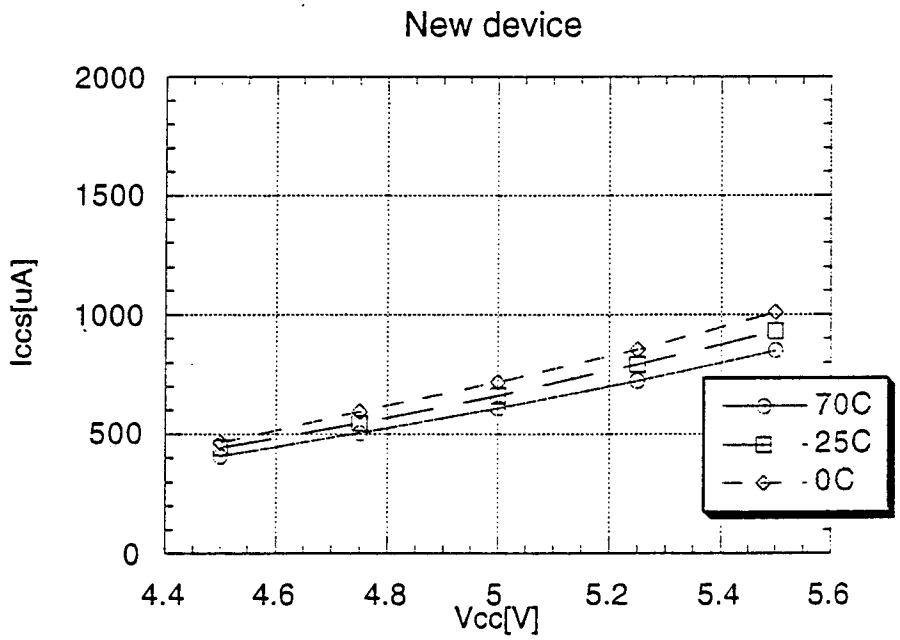


SHARP

Icc Standby TTL

CE#,RP#=Vih,BYTE#,WP#,3/5#=Vih orVil ,Spec=4[mA] Max





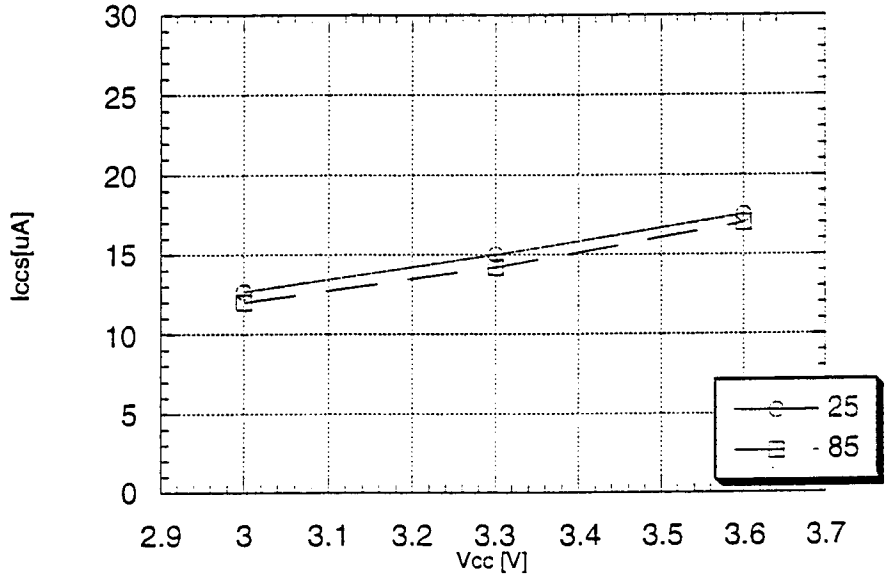
SHARP

Icc Standby CMOS

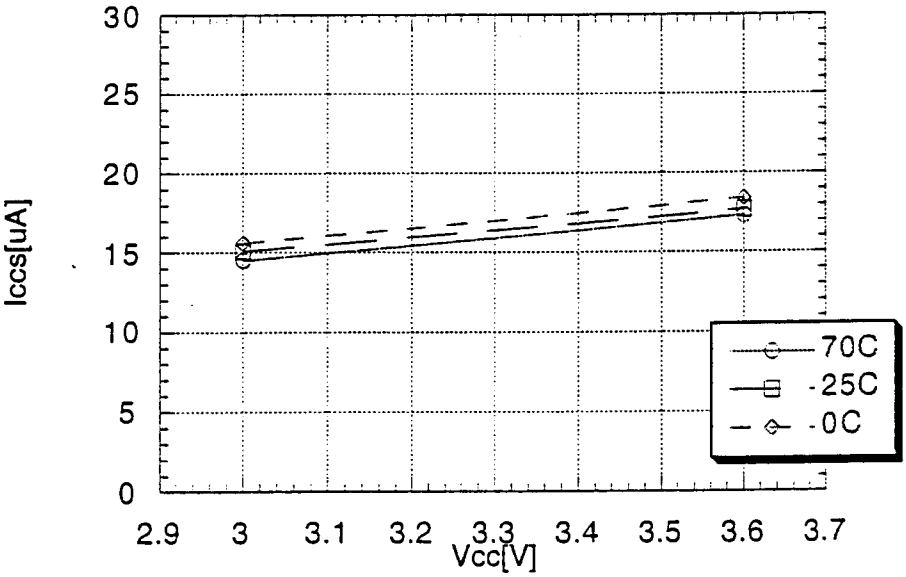
CE#,RP#=Vcc ± 0.2[V],BYTE#,WP#,3/5#=Vcc ± 0.2[V]

Spec=8[uA] Max

Current device



New device

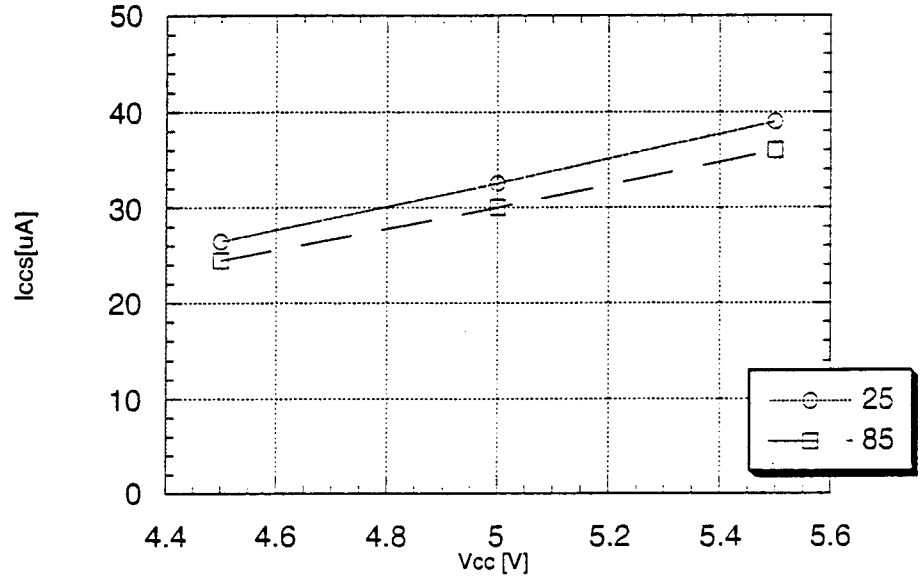


Icc Standby CMOS

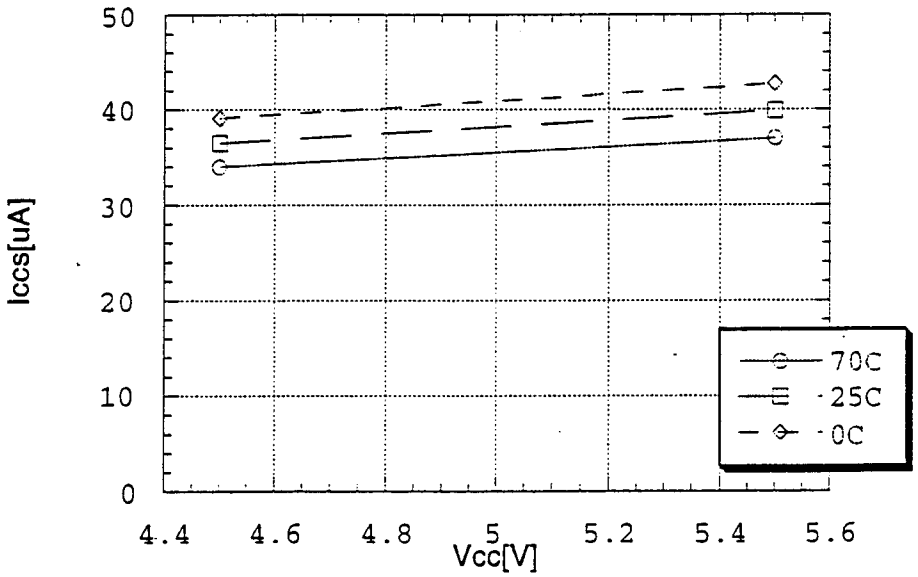
CE#,RP#=Vcc ± 0.2[V],BYTE#,WP#,3/5#=GND ± 0.2[V]

Spec=10[uA] Max

Current device



New device

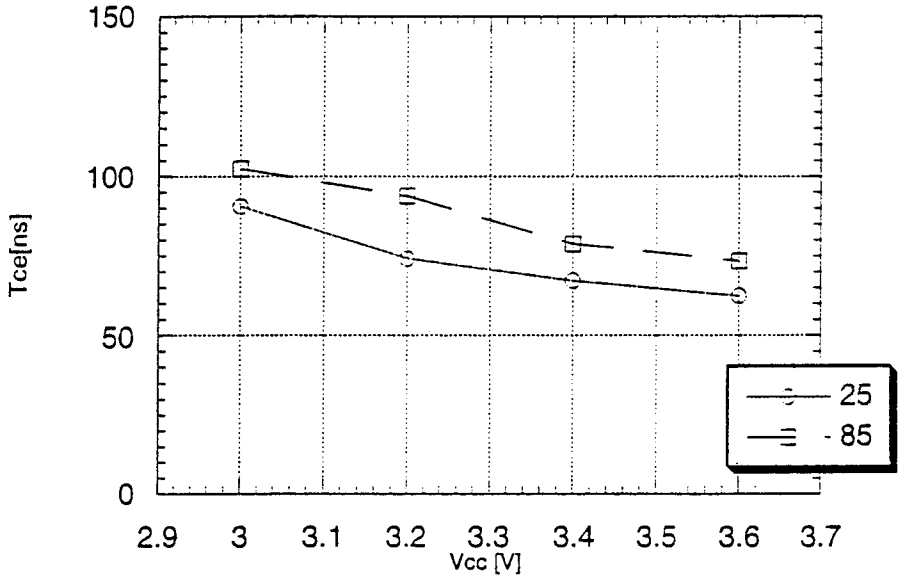


SHARP

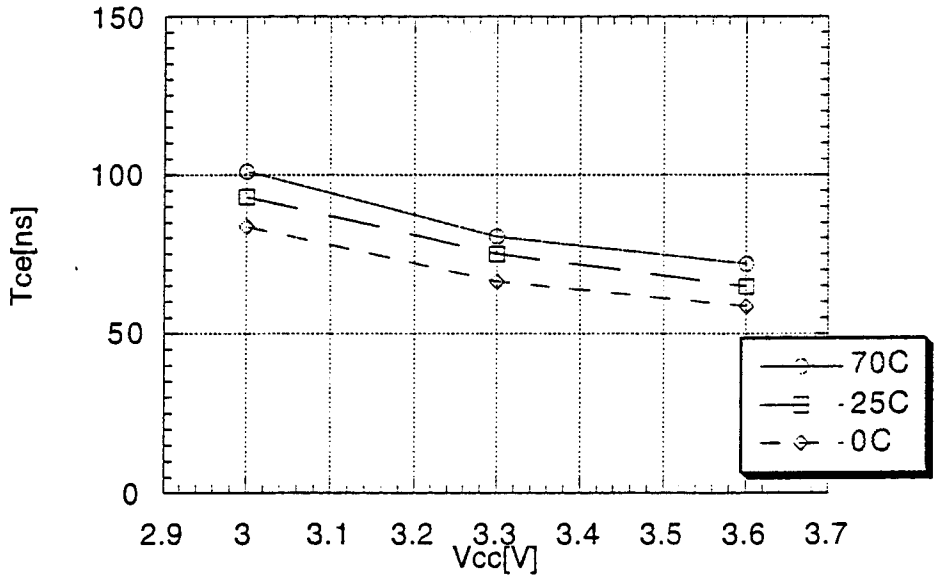
Array Speed Tce

Spec.= 120[ns]Max

Current device



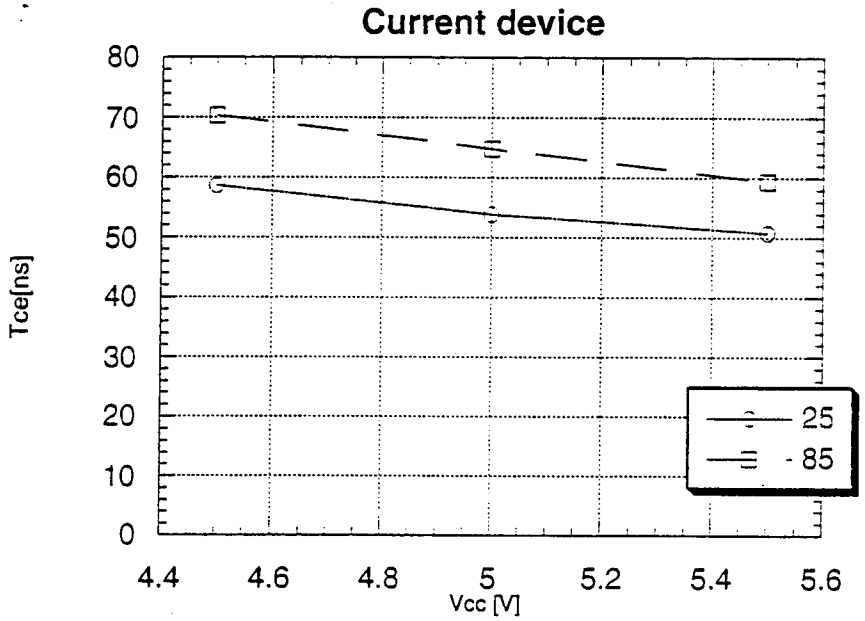
New device

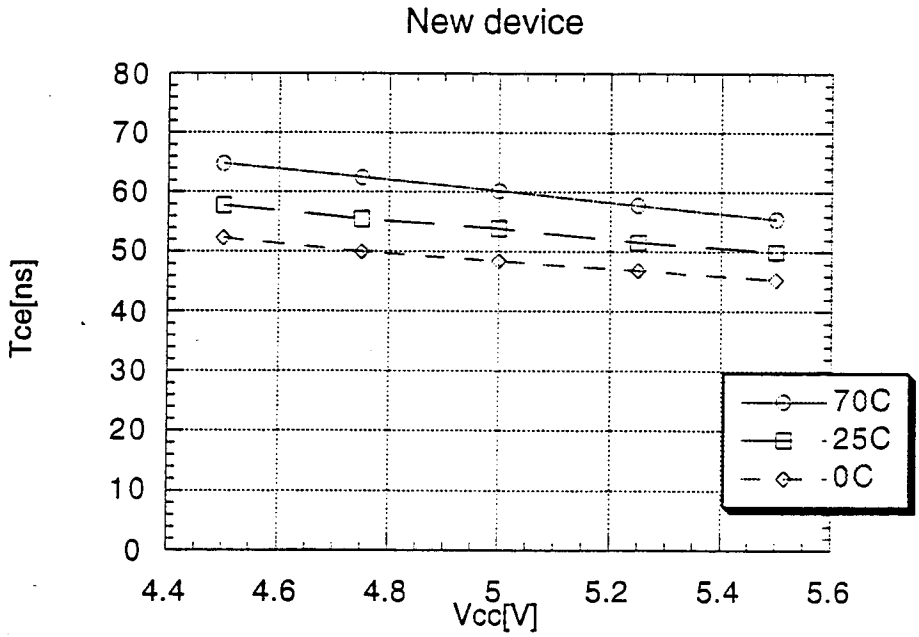


SHARP

Array Speed Tce

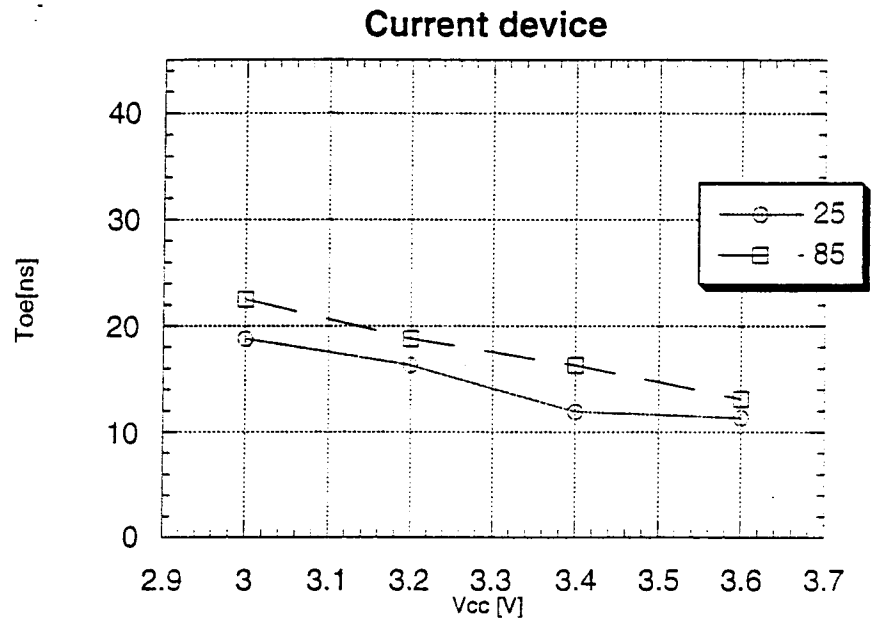
Spec.=70[ns]Max

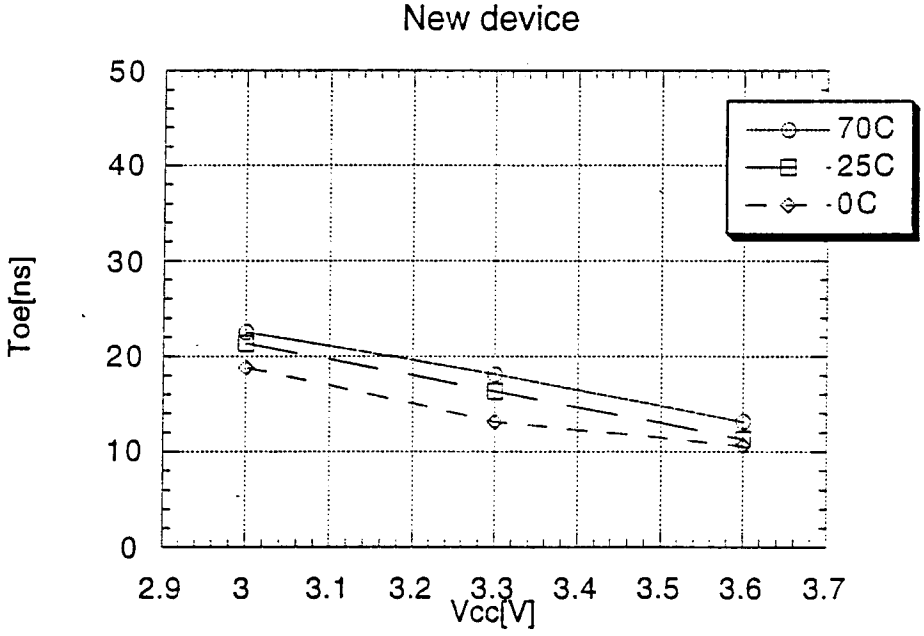




Array Speed Toe

Spec.= 45[ns]Max

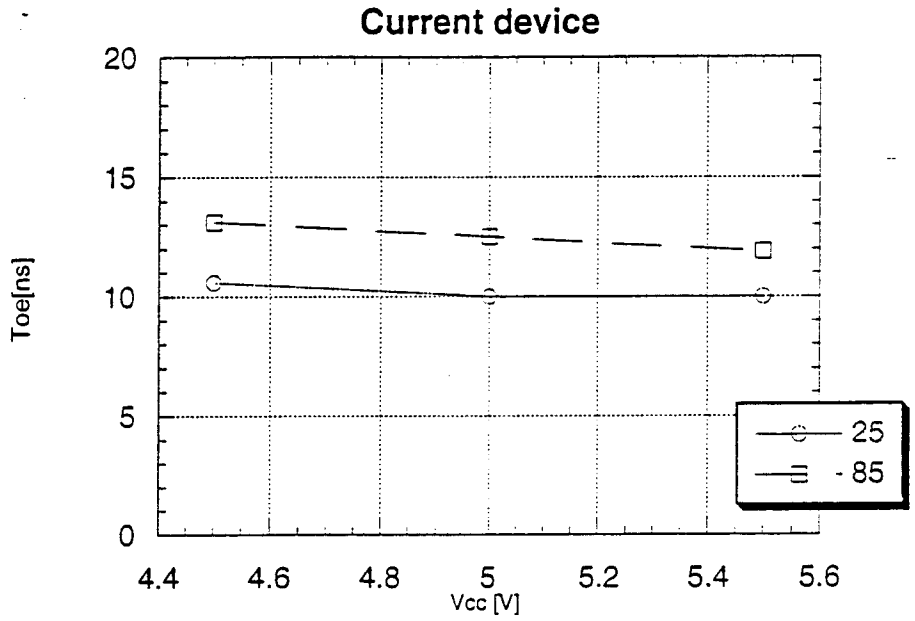


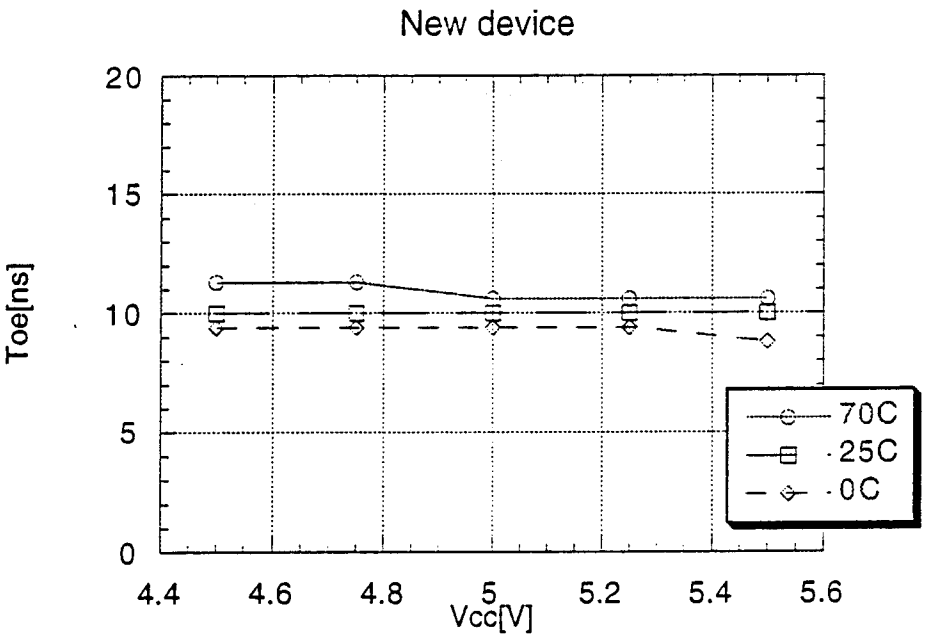


SHARP

Array Speed Toe

Spec.= 30[ns]Max



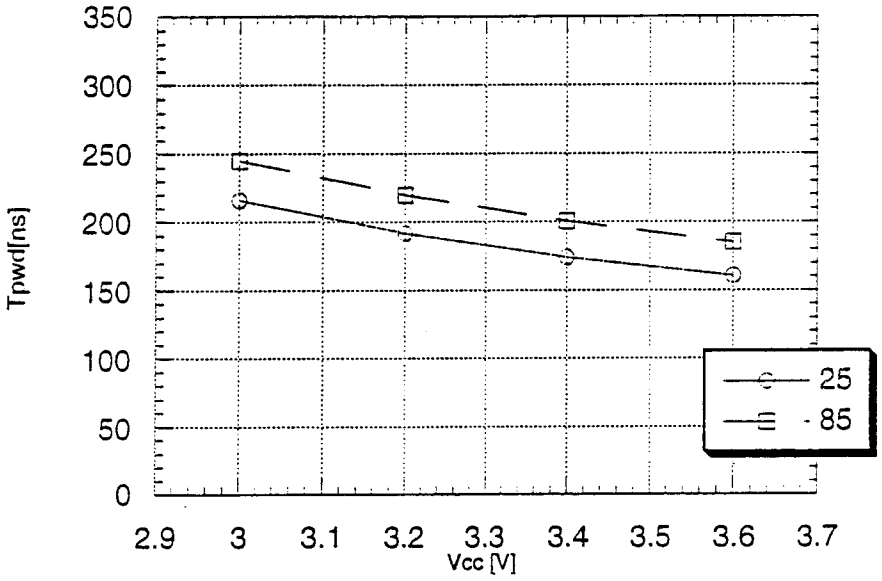


SHARP

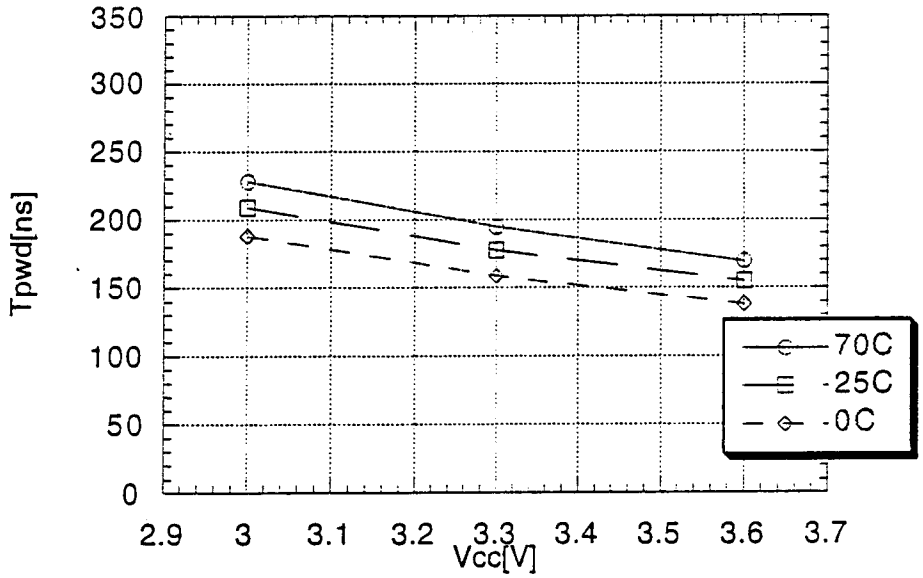
Array Speed Tpwd

Spec.= 620[ns]Max

Current device

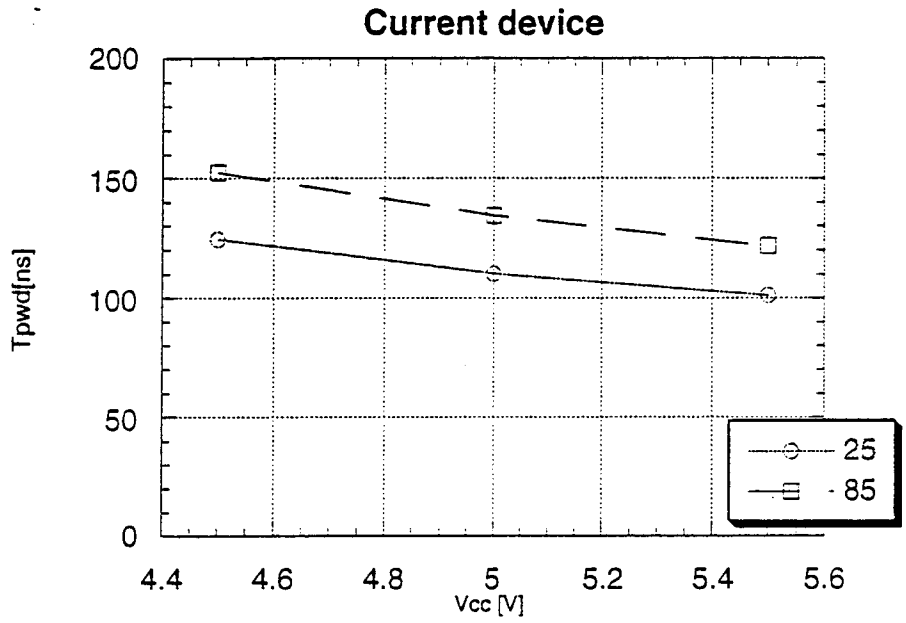


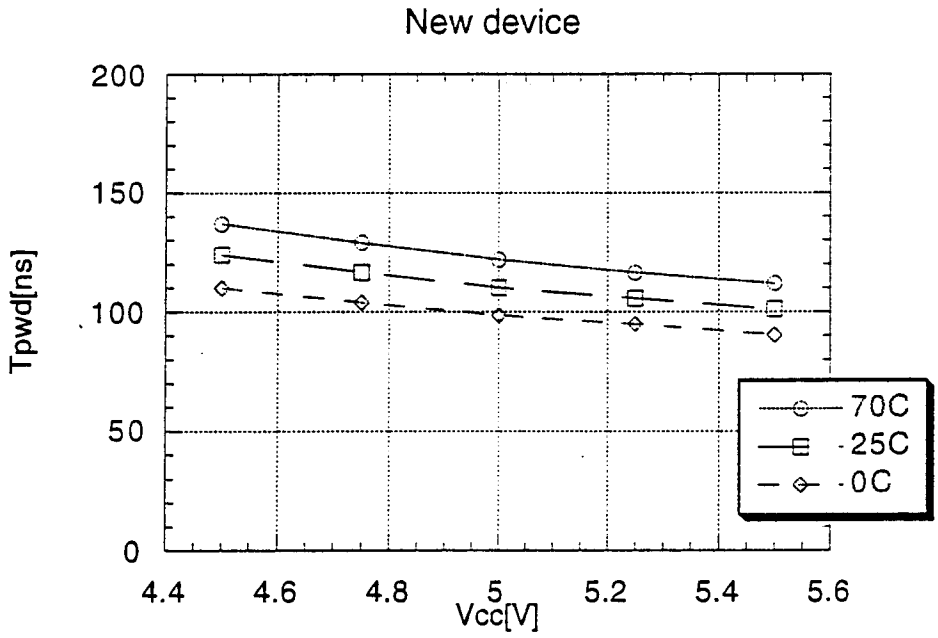
New device



Array Speed Tpwd

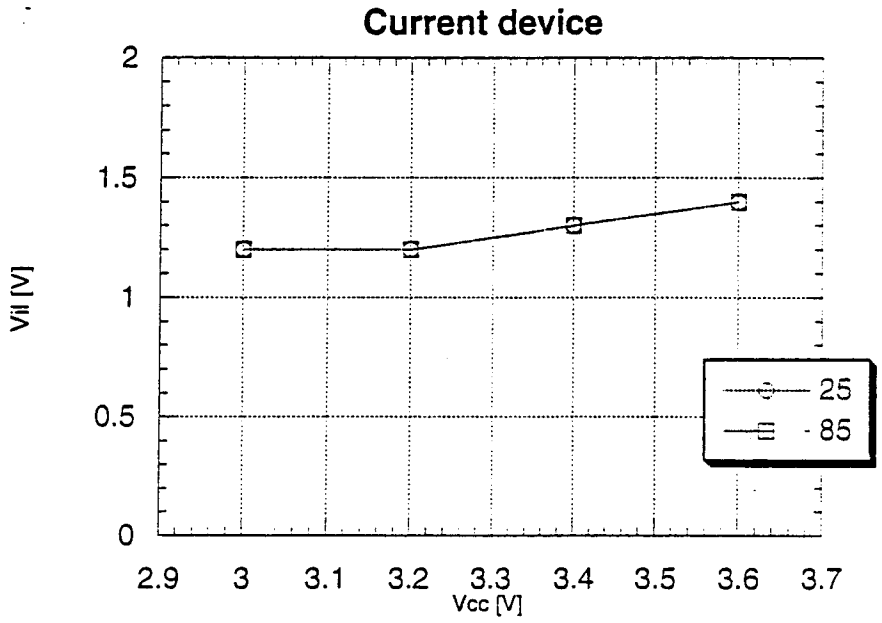
Spec.= 400[ns]Max

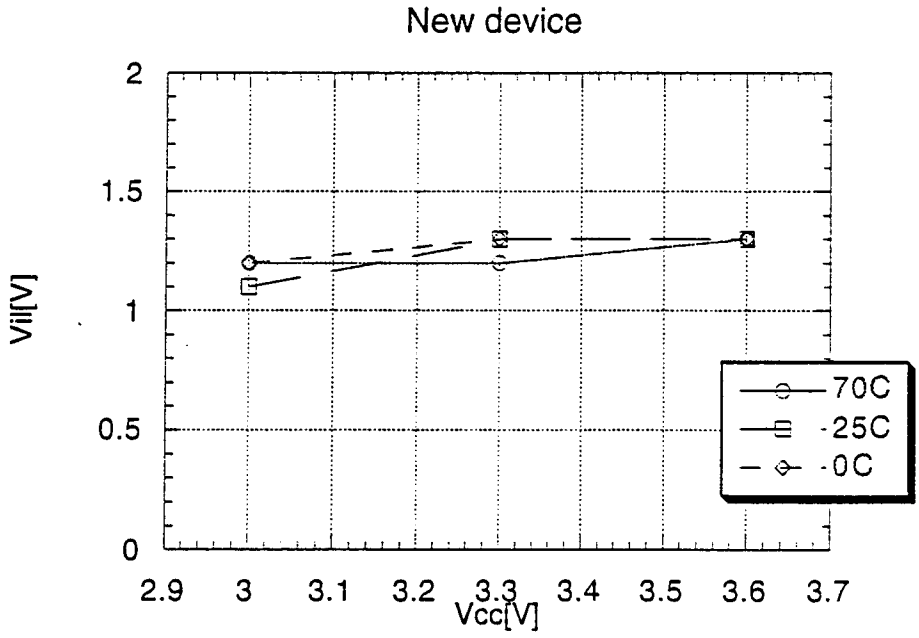




Vil W_Strobe Static

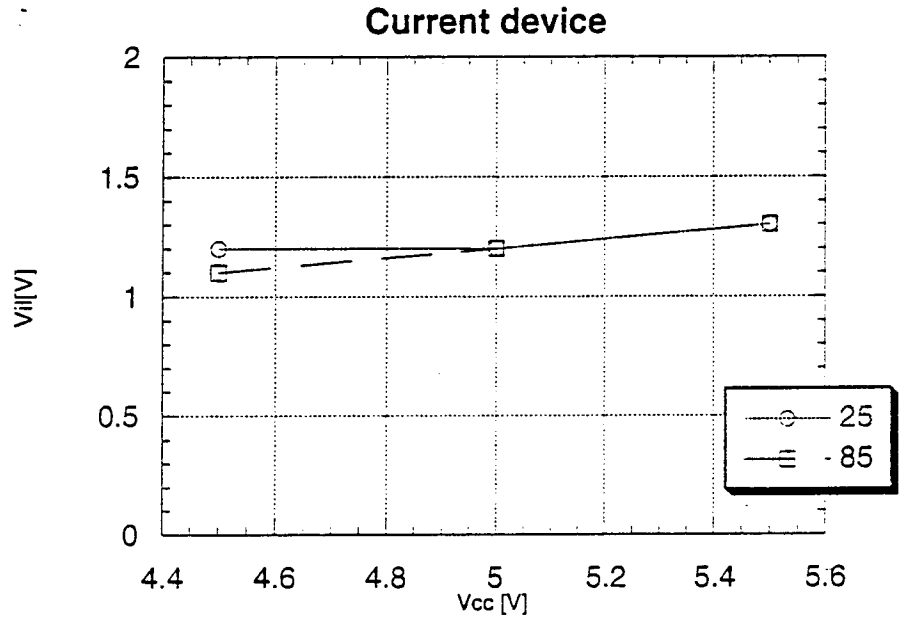
Spec=0.8[V] min.

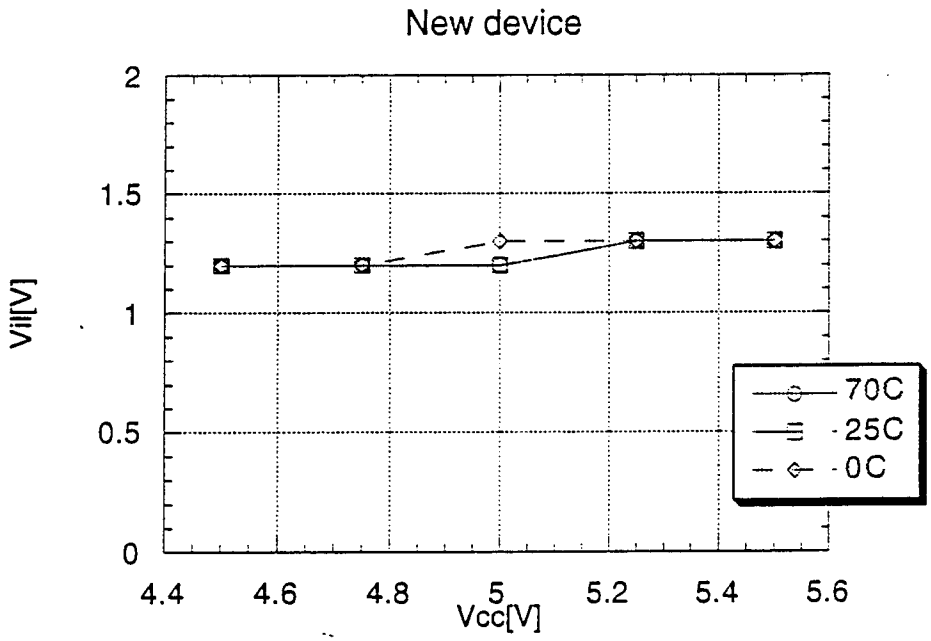




Vil W_Strobe Static

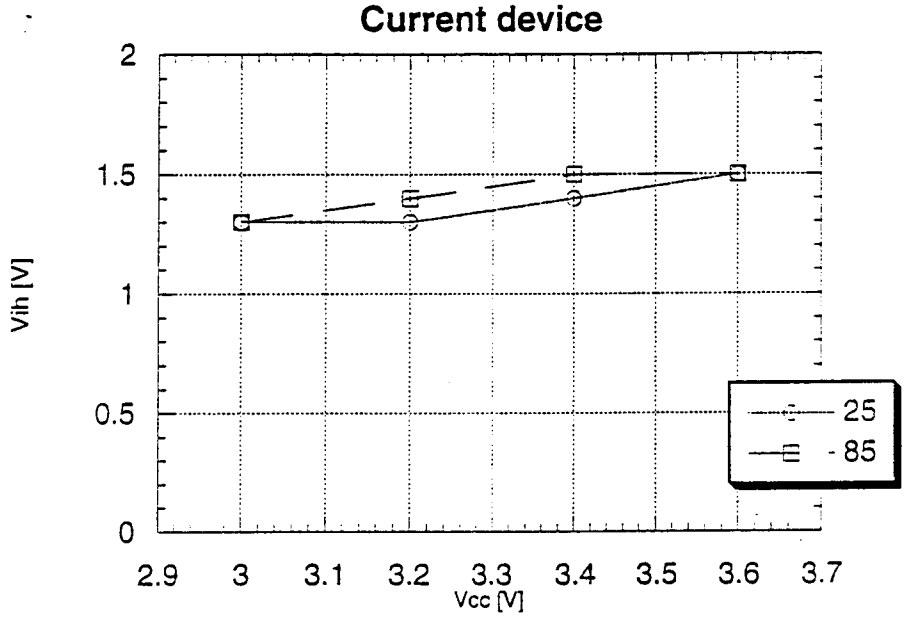
Spec=0.8[V] min.

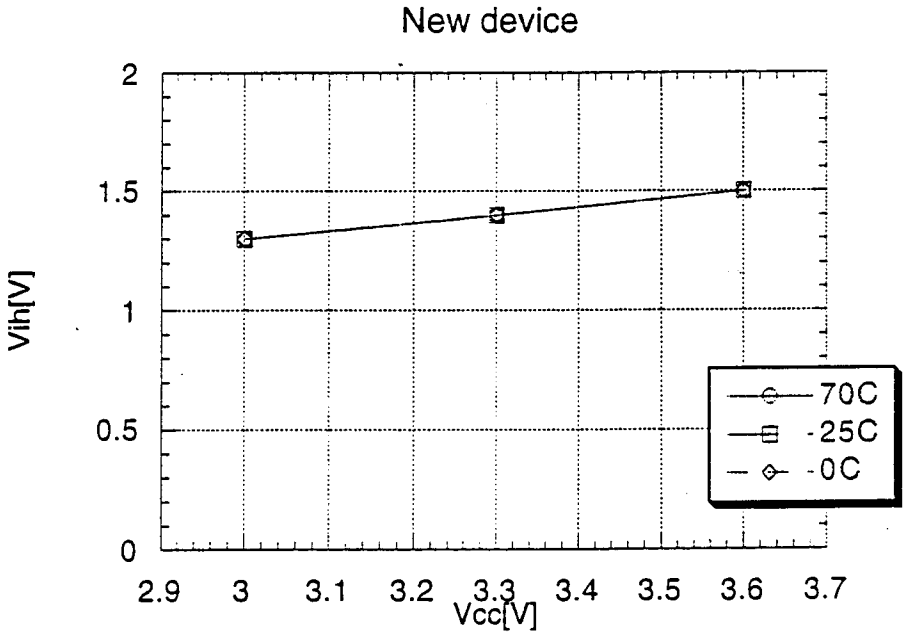




Vih W/Strobe Static

Spec=2.0[V] max.

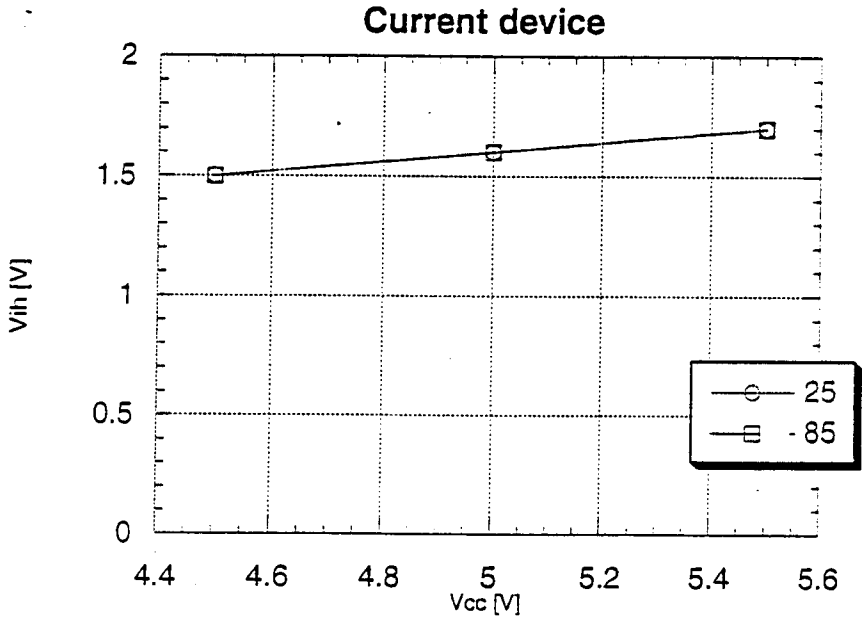


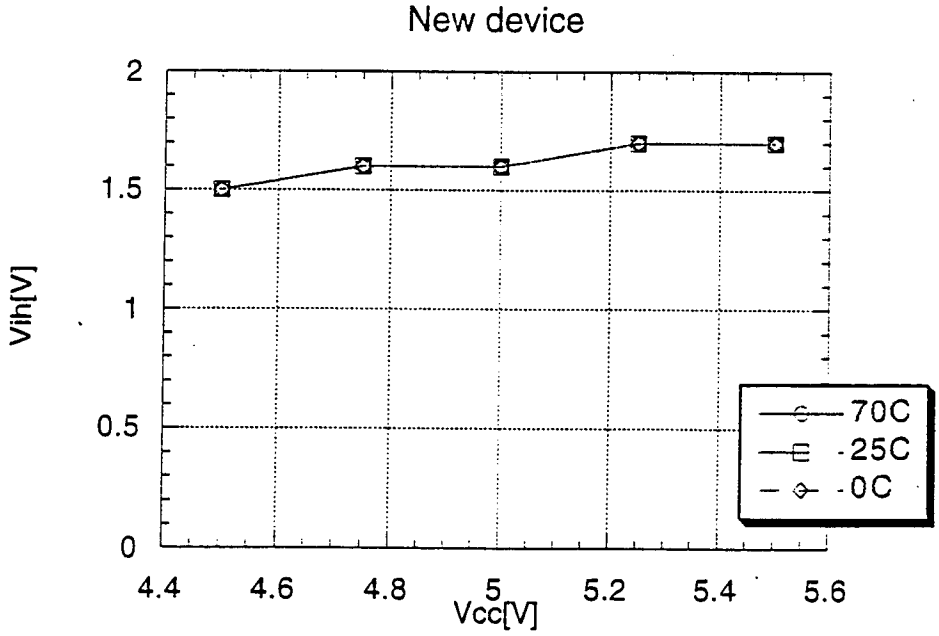


SHARP

Vih W/Strobe Static

Spec=2.0[V] max.

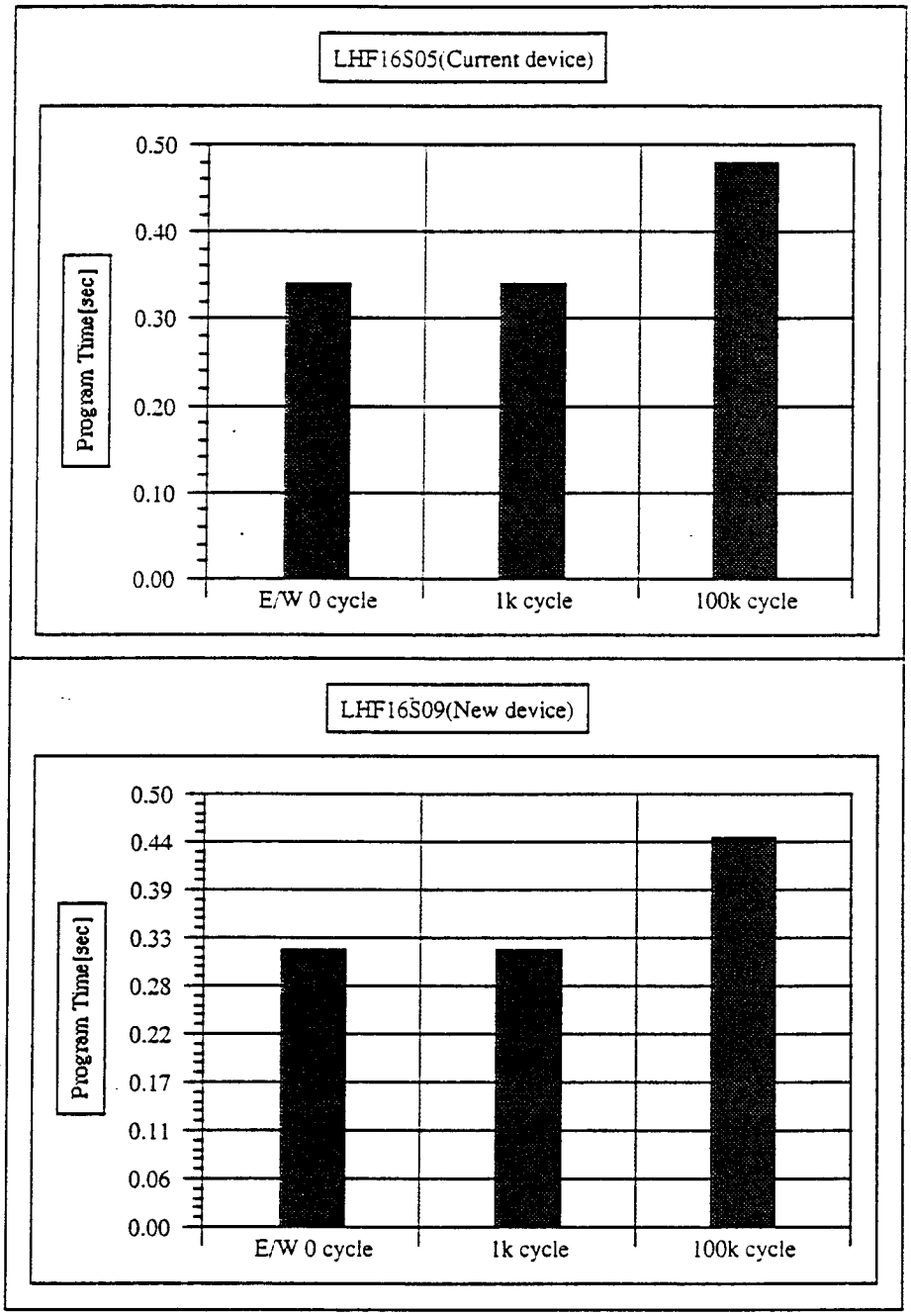




SHARP

Block Program Time

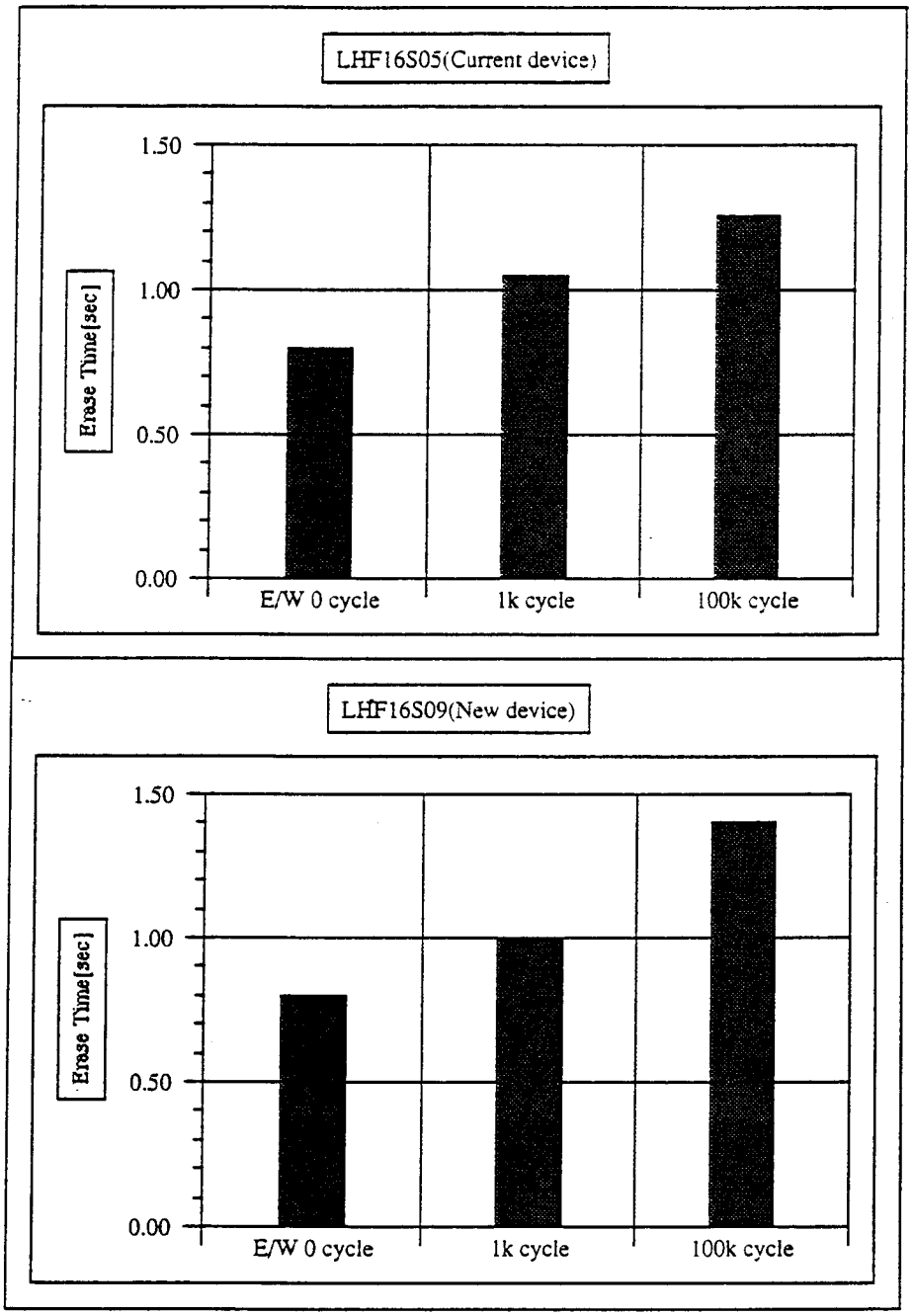
Ta=25°C, Vcc=Vpp=5V



SHARP

Block Erase Time

Ta=25°C, Vcc=Vpp=5V



LH28Fxxx FLASH MEMORY FLASH NON-VOLATILE MEMORY FLASH E2ROM FLASH ROM READ ONLY MEMORY ETOX LH28F016SAT