

FCD5N60 / FCU5N60
600V N-Channel MOSFET

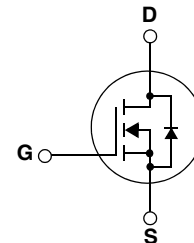
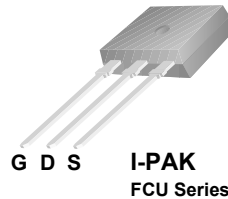
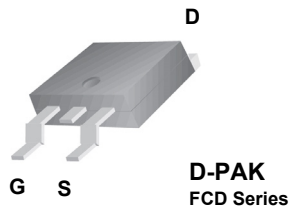
Features

- 650V @T_J = 150°C
- Typ. R_{ds(on)}=0.81Ω
- Ultra low gate charge (typ. Q_g=16nC)
- Low effective output capacitance (typ. C_{oss,eff}=32pF)
- 100% avalanche tested

Description

SuperFET™ is, Fairchild's proprietary, new generation of high voltage MOSFET family that is utilizing an advanced charge balance mechanism for outstanding low on-resistance and lower gate charge performance.

This advanced technology has been tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. Consequently, SuperFET is very suitable for various AC/DC power conversion in switching mode operation for system miniaturization and higher efficiency.



Absolute Maximum Ratings

Symbol	Parameter	FCD5N60 / FCU5N60	Unit
V _{DSS}	Drain-Source Voltage	600	V
I _D	Drain Current - Continuous (T _C = 25°C) - Continuous (T _C = 100°C)	4.6 2.9	A
I _{DM}	Drain Current - Pulsed (Note 1)	13.8	A
V _{GSS}	Gate-Source voltage	± 30	V
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	2.9	mJ
I _{AR}	Avalanche Current (Note 1)	4.6	A
E _{AR}	Repetitive Avalanche Energy (Note 1)	5.4	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	20	V/ns
P _D	Power Dissipation (T _C = 25°C) - Derate above 25°C	54 0.43	W W/°C
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C
T _L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	°C

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	FCD5N60/FCU5N60	Unit
R _{θJC}	Thermal Resistance, Junction-to-Case	2.3	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient	83	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCD5N60	FCD5N60TM	D-PAK	380mm	16mm	2500
FCD5N60	FCD5N60TF	D-PAK	380mm	16mm	2000
FCU5N60	FCU5N60	I-PAK	--	--	70

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA, T _J = 25°C	600	--	--	V
		V _{GS} = 0V, I _D = 250μA, T _J = 150°C	--	650	--	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250μA, Referenced to 25°C	--	0.6	--	V/°C
BV _{DS}	Drain-Source Avalanche Breakdown Voltage	V _{GS} = 0V, I _D = 4.6A	--	700	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 600V, V _{GS} = 0V	--	--	1	μA
		V _{DS} = 480V, T _C = 125°C	--	--	10	μA
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30V, V _{DS} = 0V	--	--	100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -30V, V _{DS} = 0V	--	--	-100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	3.0	--	5.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10V, I _D = 2.3A	--	0.81	0.95	Ω
g _{FS}	Forward Transconductance	V _{DS} = 40V, I _D = 2.3A (Note 4)	--	3.8	--	S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = 25V, V _{GS} = 0V, f = 1.0MHz	--	470	600	pF
C _{oss}	Output Capacitance		--	250	320	pF
C _{rss}	Reverse Transfer Capacitance		--	22	--	pF
C _{oss}	Output Capacitance	V _{DS} = 480V, V _{GS} = 0V, f = 1.0MHz	--	12	--	pF
C _{oss eff.}	Effective Output Capacitance	V _{DS} = 0V to 400V, V _{GS} = 0V	--	32	--	pF
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{DD} = 300V, I _D = 4.6A R _G = 25Ω (Note 4, 5)	--	12	30	ns
t _r	Turn-On Rise Time		--	40	90	ns
t _{d(off)}	Turn-Off Delay Time		--	47	95	ns
t _f	Turn-Off Fall Time		--	22	55	ns
Q _g	Total Gate Charge	V _{DS} = 480V, I _D = 4.6A V _{GS} = 10V (Note 4, 5)	--	16	--	nC
Q _{gs}	Gate-Source Charge		--	2.8	--	nC
Q _{gd}	Gate-Drain Charge		--	7	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	4.6	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	13.8	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0V, I _S = 4.6A	--	--	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0V, I _S = 4.6A dI _F /dt = 100A/μs (Note 4)	--	295	--	ns
Q _{rr}	Reverse Recovery Charge		--	2.7	--	μC

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. I_{AS} = 2.3A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
3. I_{SD} ≤ 4.6A, di/dt ≤ 1200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

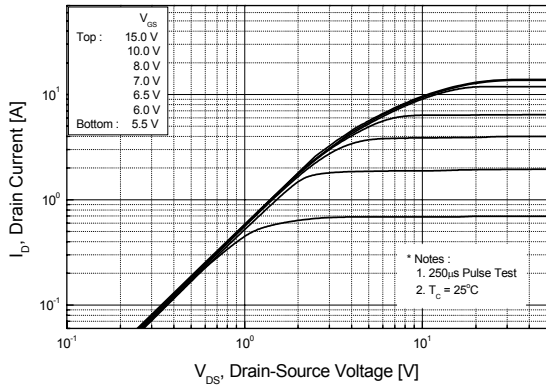


Figure 2. Transfer Characteristics

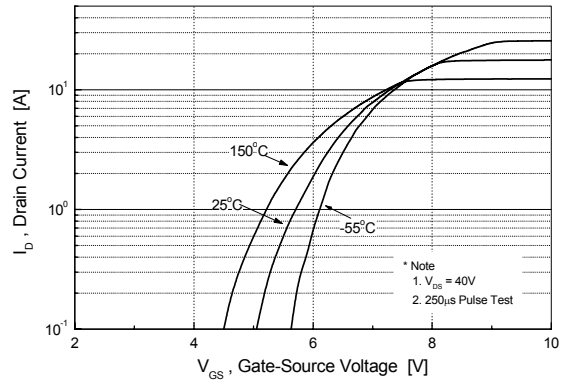


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

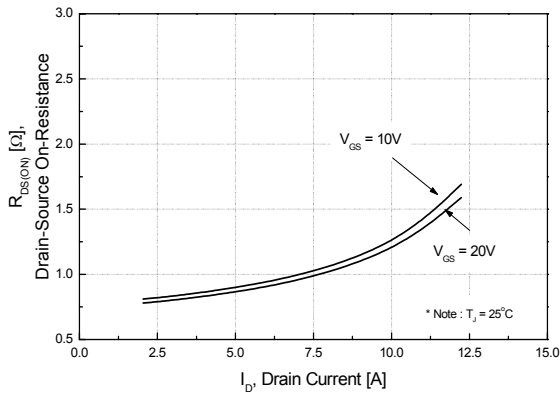


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

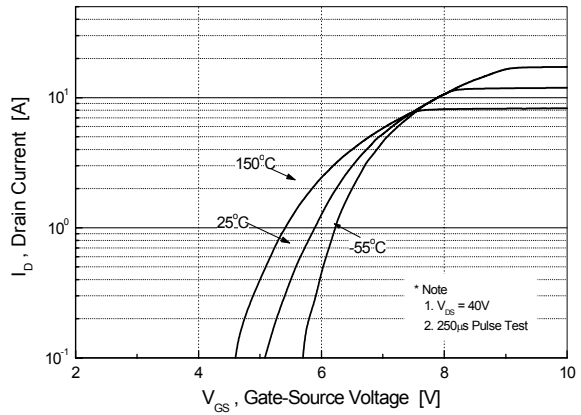


Figure 5. Capacitance Characteristics

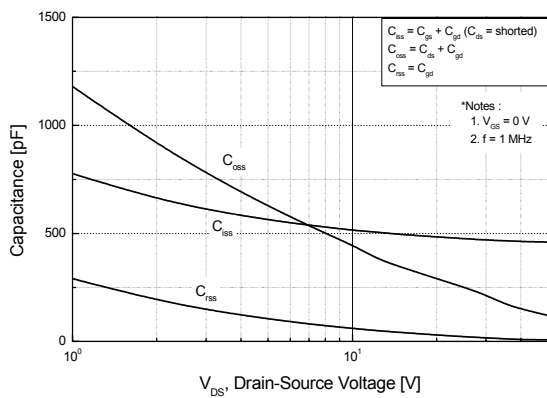
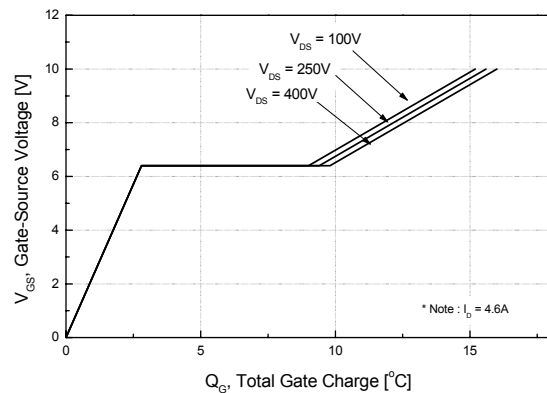


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

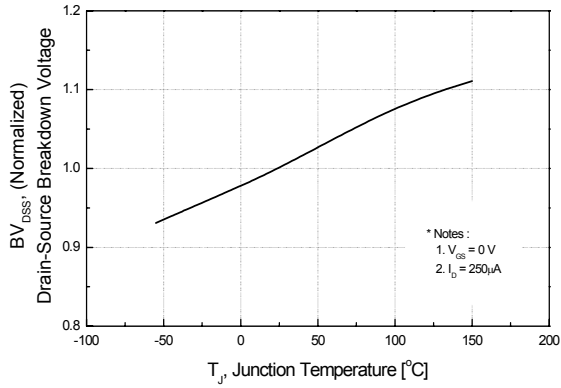


Figure 8. On-Resistance Variation vs. Temperature

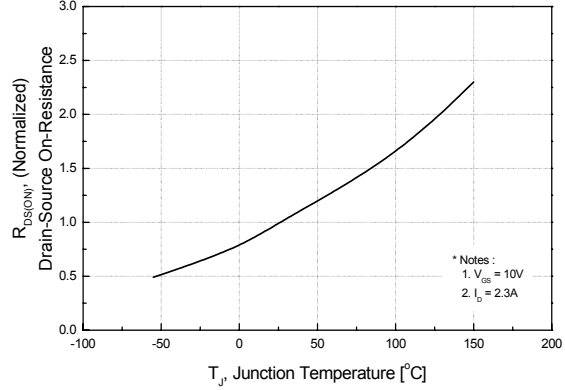


Figure 9. Maximum Safe Operating Area

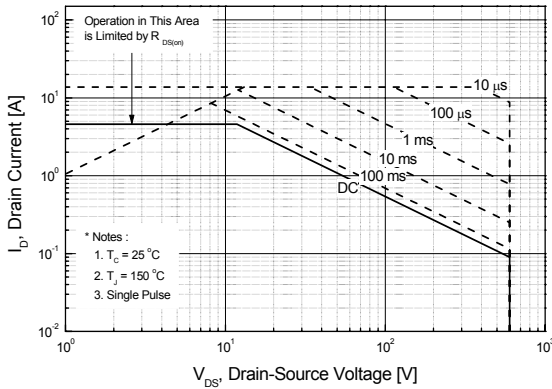


Figure 10. Maximum Drain Current vs. Case Temperature

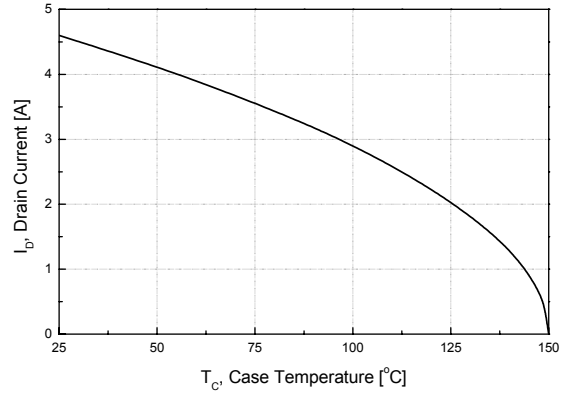
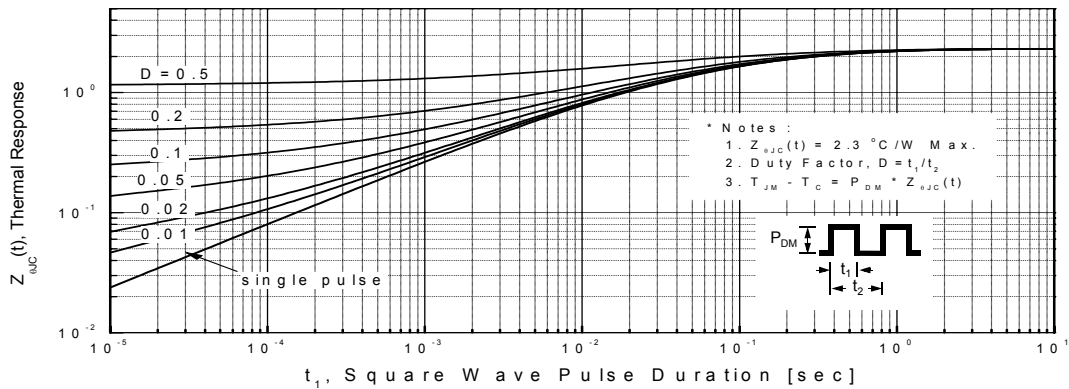


Figure 11. Transient Thermal Response Curve



Gate Charge Test Circuit & Waveform



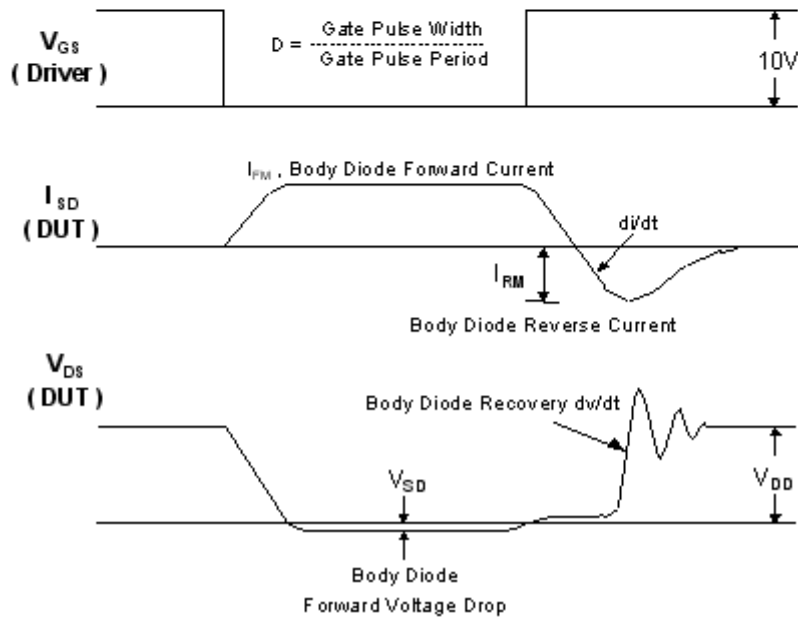
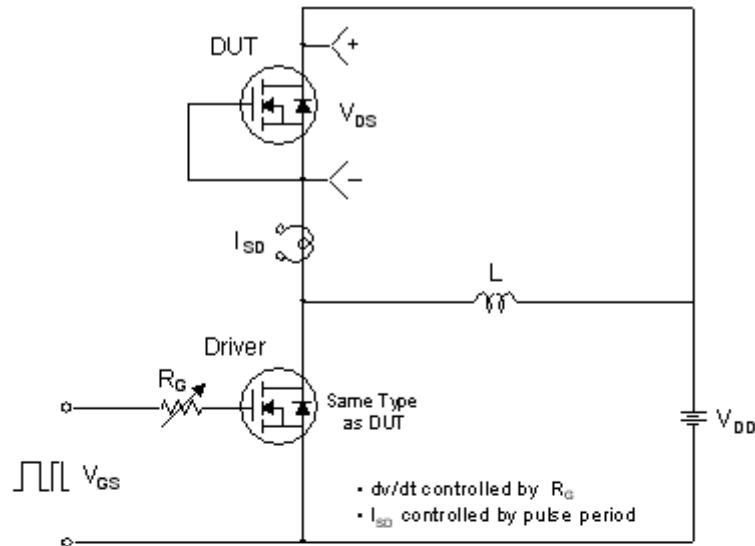
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

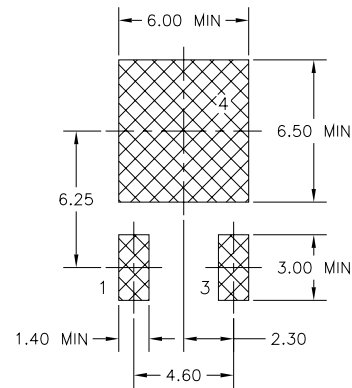
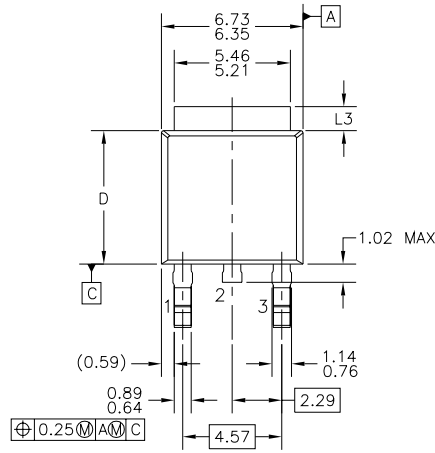


Peak Diode Recovery dv/dt Test Circuit & Waveforms

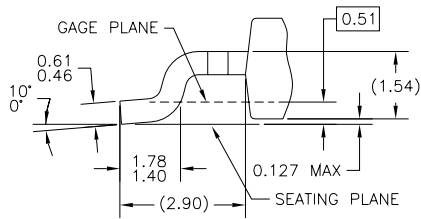
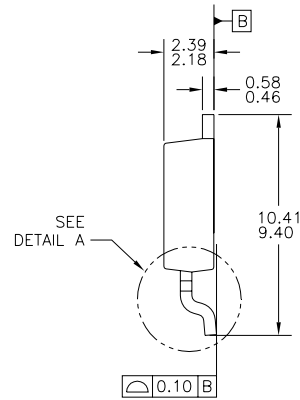
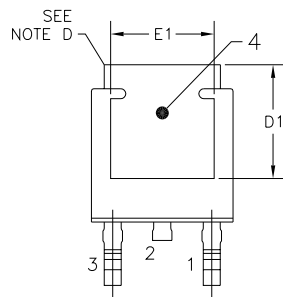


Mechanical Dimensions

D-PAK



LAND PATTERN RECOMMENDATION



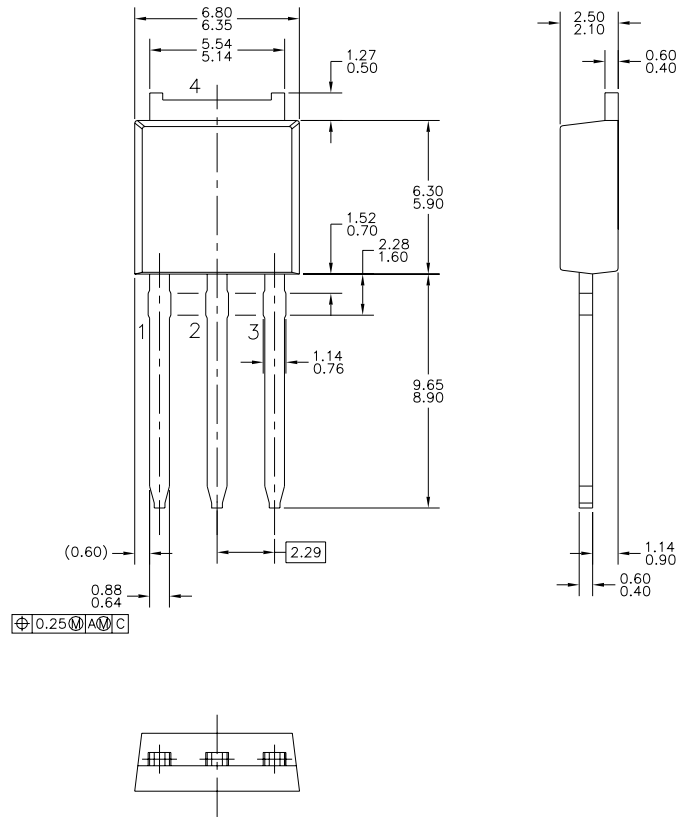
DETAIL A
(ROTATED -90°)
SCALE: 12X

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
 - B) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) DIMENSIONS L3,D,E1&D1 TABLE:
- | | OPTION AA | OPTION AB |
|----|-----------|-----------|
| L3 | 0.89-1.27 | 1.52-2.03 |
| D | 5.97-6.22 | 5.33-5.59 |
| E1 | 4.32 MIN | 3.81 MIN |
| D1 | 5.21 MIN | 4.57 MIN |
- F) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

Dimensions in Millimeters

Package Dimensions (Continued)

I-PAK



Dimensions in Millimeters

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Build it Now™	HiSeC™	OPTOPLANAR™	Stealth™	Wire™
CoolFET™	I ² C™	PACMAN™	SuperFET™	
CROSSVOLT™	i-Lo™	POP™	SuperSOT™-3	
DOME™	ImpliedDisconnect™	Power247™	SuperSOT™-6	
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E ² CMOS™	ISOPLANAR™	PowerSaver™	SyncFET™	
EnSigna™	LittleFET™	PowerTrench®	TCM™	
FACT™	MICROCOUPLER™	QFET®	TinyBoost™	
FAST®	MicroFET™	QS™	TinyBuck™	
FASTr™	MicroPak™	QT Optoelectronics™	TinyPWM™	
FPS™	MICROWIRE™	Quiet Series™	TinyPower™	
FRFET™	MSX™	RapidConfigure™	TinyLogic®	
	MSXPro™	RapidConnect™	TINYOPTO™	
Across the board. Around the world.™		µSerDes™	TruTranslation™	
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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Datasheet Identification	Product Status	Definition
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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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