# DATA SHEET

## 74ALS646/74ALS646–1
## 74ALS648/74ALS648–1
Transceiver/register

Product specification
IC05 Data Handbook

1991 Feb 08

Philips
Semiconductors

PHILIPS

# Transceiver/register

# 74ALS646/74ALS646-1
# 74ALS648/74ALS648-1

*74ALS646/646-1 Octal transceiver/register, non-inverting (3-State)*
*74ALS648/648-1 Octal transceiver/register, inverting (3-State)*

## FEATURES

- Combines 74ALS245 and two 74ALS374 type functions in one chip
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Choice of non-inverting and inverting data paths
- 3-State outputs
- The -1 version sink 48mA $I_{OL}$ within the ±5% $V_{CC}$ range

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74ALS646/646-1 | 140MHz | 48mA |
| 74ALS648/648-1 | 140MHz | 54mA |

## DESCRIPTION

The 74ALS646/74ALS646-1 and 74ALS648/74ALS648-1 transceivers/registers consist of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output enable ($\overline{OE}$) and direction (DIR) and select (SAB, SBA) pins are provided for bus management.

The 74ALS646-1 and 74ALS648-1 will sink 48mA if the $V_{CC}$ is limited to 5.0V ±0.25V.

## ORDERING INFORMATION

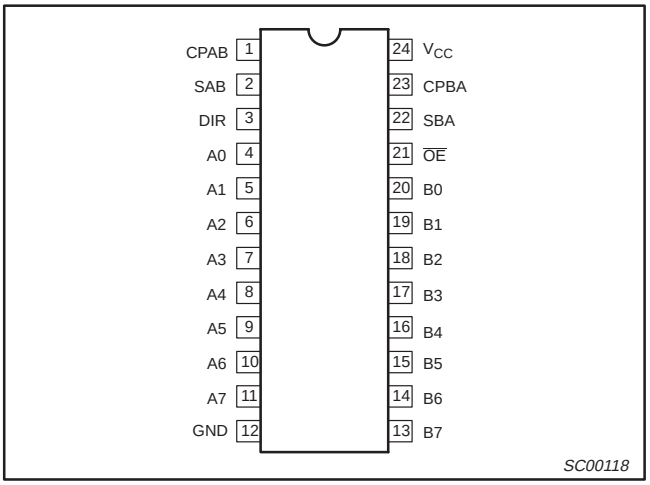
| DESCRIPTION | ORDER CODE: COMMERCIAL RANGE $V_{CC}$ = 5V ±10%, $T_{amb}$ = 0°C to +70°C | DRAWING NUMBER |
|---|---|---|
| 24-pin plastic DIP | 74ALS646N, 74ALS646-1N, 74ALS648N, 74ALS648-1N | SOT222-1 |
| 24-pin plastic SOL | 74ALS646D, 74ALS646-1D, 74ALS648D, 74ALS648-1D | SOT137-1 |

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

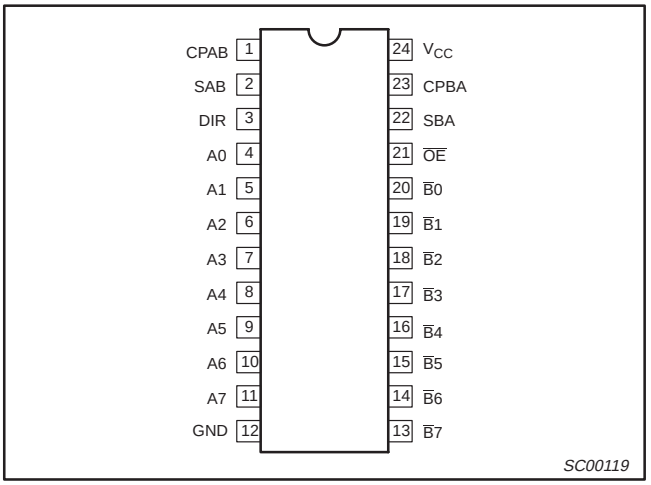
| PINS | DESCRIPTION | 74ALS (U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|---|---|---|---|
| A0 – A7 | A inputs | 1.0/1.0 | 20µA/0.1mA |
| B0 – B7 | B inputs | 1.0/1.0 | 20µA/0.1mA |
| $\overline{CPAB}$ | A-to-B clock input | 1.0/1.0 | 20µA/0.1mA |
| CPBA | B-to-A clock input | 1.0/1.0 | 20µA/0.1mA |
| SAB | A-to-B select input | 1.0/1.0 | 20µA/0.1mA |
| SBA | B-to-A select input | 1.0/1.0 | 20µA/0.1mA |
| DIR | Data flow directional control input | 1.0/1.0 | 20µA/0.1mA |
| $\overline{OE}$ | Output enable input | 1.0/1.0 | 20µA/0.1mA |
| A0 – A7, B0 – B7 | Data outputs | 750/240 | 15mA/24mA |
| A0 – A7, B0 – B7 | Data outputs (-1 version) | 750/480 | 15mA/48mA |

**NOTE:** One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

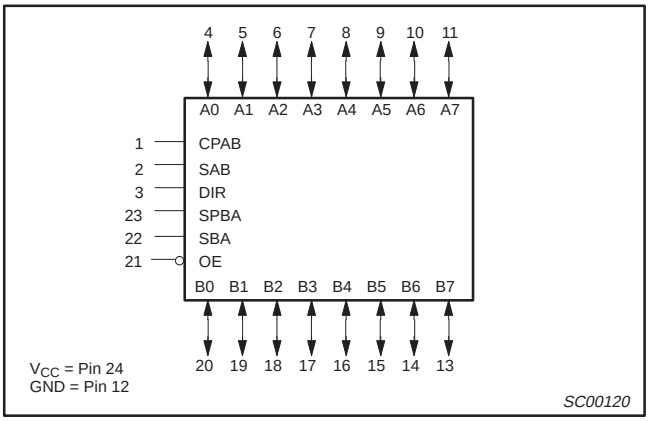
## PIN CONFIGURATION – 74ALS646/646-1



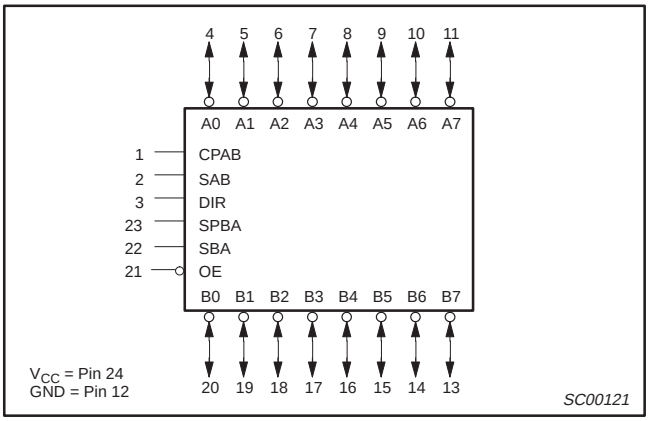

## PIN CONFIGURATION – 74ALS648/648-1



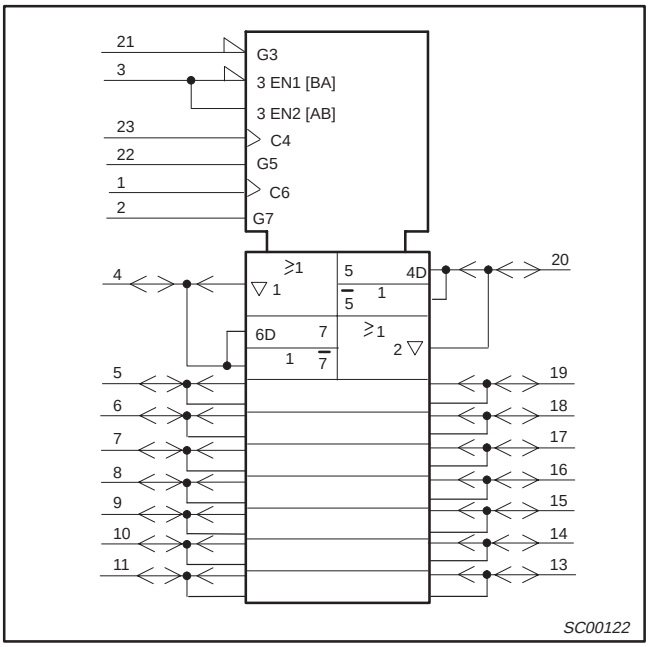

## LOGIC SYMBOL – 74ALS646/646-1



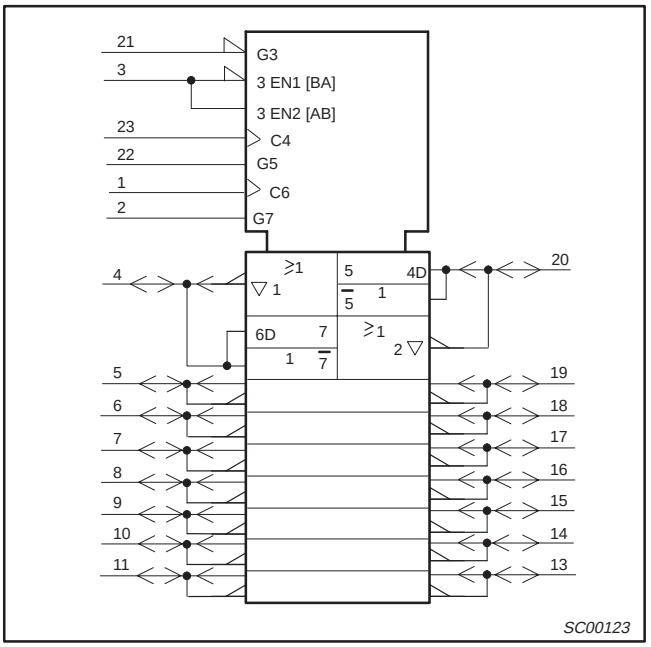

## LOGIC SYMBOL – 74ALS648/648-1




## IEC/IEEE SYMBOL – 74ALS646/646-1




## IEC/IEEE SYMBOL – 74ALS648/648-1

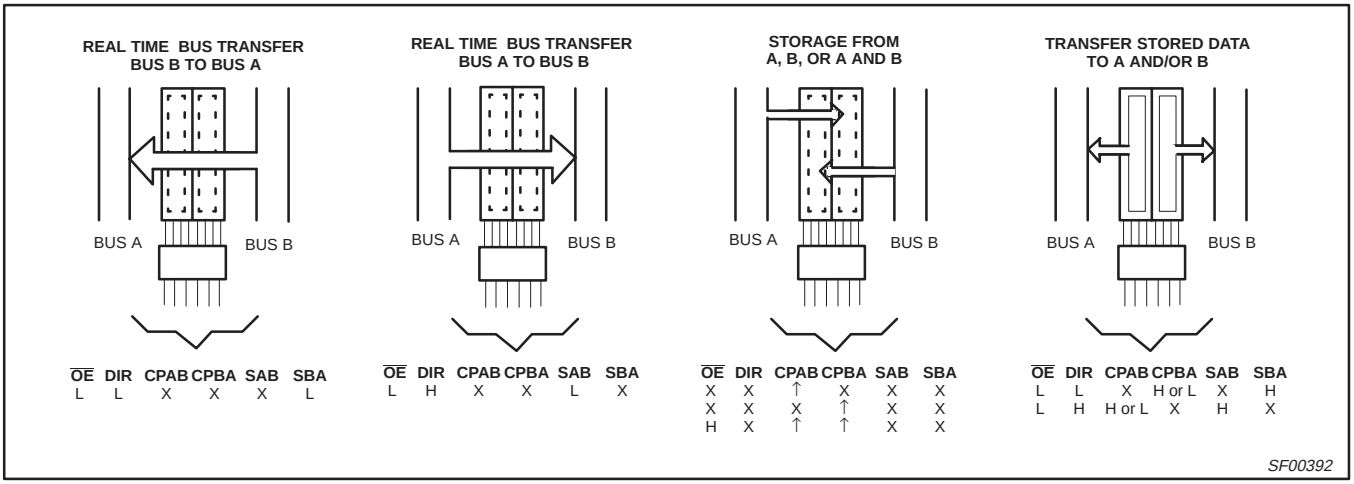


## BUS MANAGEMENT FUNCTIONS

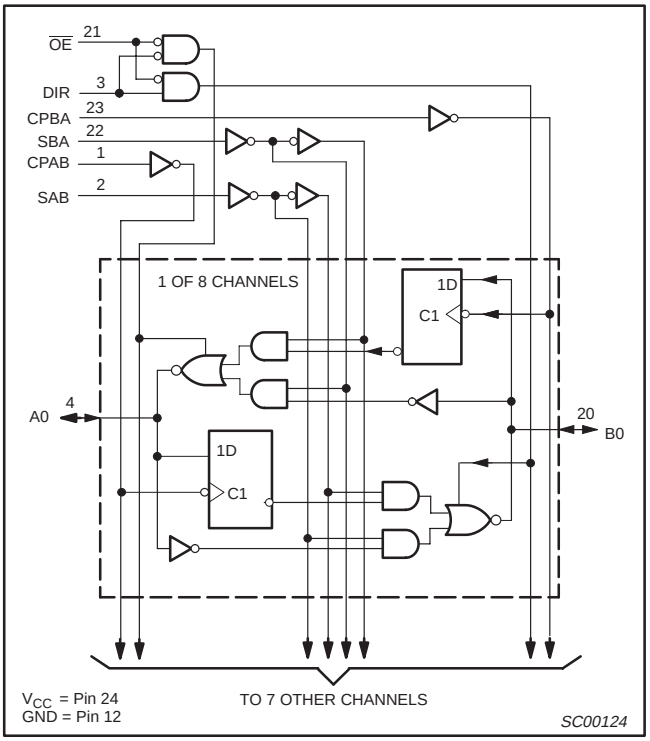
The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74ALS646/646-1 and 74ALS648/648-1.

The select pins determine whether data is stored or transferred through the device in real time.

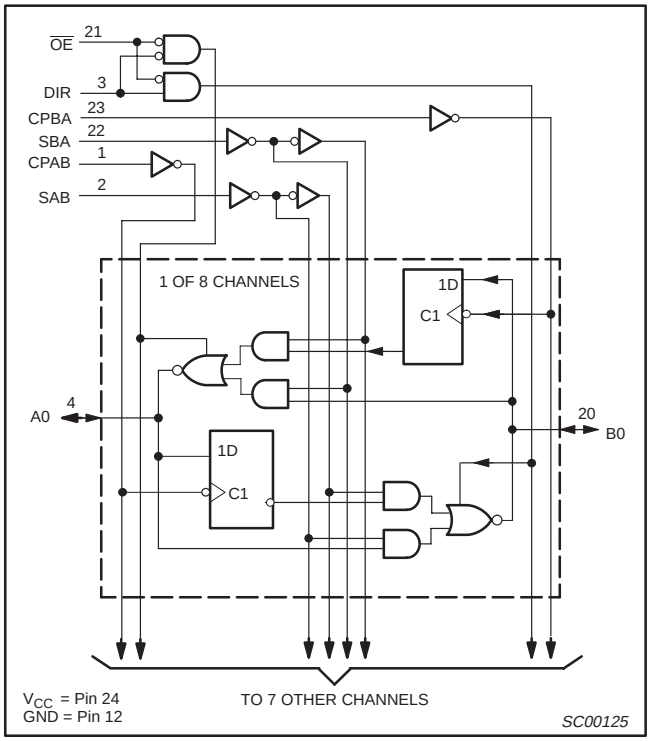
The DIR determines which bus will receive data when the OE pin is Low.



## LOGIC SYMBOL – 74ALS646/646-1




## LOGIC SYMBOL – 74ALS648/648-1




## FUNCTION TABLE

| INPUTS | | | | | | DATA I/O | | OPERATING MODE | |
|---|---|---|---|---|---|---|---|---|---|
| $\overline{OE}$ | DIR | CPAB | CPBA | SAB | SBA | An | Bn | 74ALS646/74ALS646-1 | 74ALS648/74ALS648-1 |
| X | X | ↑ | X | X | X | Input | Unspecified* | Store A, B unspecified* | Store A, B unspecified* |
| X | X | X | ↑ | X | X | Unspecified* | Input | Store B, A unspecified* | Store B, A unspecified* |
| H | X | ↑ | ↑ | X | X | Input | Input | Store A and B data | Store A and B data |
| H | X | H or L | H or L | X | X | Input | Input | Isolation, hold storage | Isolation, hold storage |
| L | L | X | X | X | L | Output | Input | Real time B data to A bus | Real time $\overline{B}$ data to A bus |
| L | L | X | H or L | X | H | Output | Input | Stored B data to A bus | Stored $\overline{B}$ data to A bus |
| L | H | X | X | L | X | Input | Output | Real time A data to B bus | Real time $\overline{A}$ data to B bus |
| L | H | H or L | X | H | X | Input | Output | Stored A data to B bus | Stored $\overline{A}$ data to B bus |

**NOTES:**
H = High voltage level
L = Low voltage level
X = Don't care
* = The data output function may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.
↑ = Low-to-High clock transition

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

| SYMBOL | PARAMETER | | RATING | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 to +7.0 | V |
| $V_{IN}$ | Input voltage | | –0.5 to +7.0 | V |
| $I_{IN}$ | Input current | | –30 to +5 | mA |
| $V_{OUT}$ | Voltage applied to output in High output state | | –0.5 to $V_{CC}$ | V |
| $I_{OUT}$ | Current applied to output in Low output state | All versions | 48 | mA |
| | | -1 version | 96 | mA |
| $T_{amb}$ | Operating free-air temperature range | | 0 to +70 | °C |
| $T_{stg}$ | Storage temperature range | | –65 to +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2.0 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | | –18 | mA |
| $I_{OH}$ | High-level output current | | | | –15 | mA |
| $I_{OL}$ | Low-level output current | All versions | | | 24 | mA |
| | | -1 version | | | 48 [1] | mA |
| $T_{amb}$ | Operating free-air temperature range | | 0 | | +70 | °C |

**NOTE:**
1. The 48mA limit applies only under the condition of $V_{CC}$ = 5.0V ±5%.

## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER | | TEST CONDITIONS[1] | | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP[2] | MAX | |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$±10%, $V_{IL}$ = MAX, $V_{IH}$ = MIN | $I_{OH}$ = –0.4mA | $V_{CC}$ – 2 | | | V |
| | | | | $I_{OH}$ = –3mA | 2.4 | 3.2 | | V |
| | | | $V_{CC}$ = MIN, $V_{IL}$ = MAX, $V_{IH}$ = MIN | $I_{OH}$ = –15mA | 2.0 | | | V |
| $V_{OL}$ | Low-level output voltage | All versions | $V_{CC}$ = MIN, $V_{IL}$ = MAX, $V_{IH}$ = MIN | $I_{OL}$ = 12mA | | 0.25 | 0.40 | V |
| | | | | $I_{OL}$ = 24mA | | 0.35 | 0.50 | V |
| | | -1 versions | $V_{CC}$ = 4.75V, $V_{IL}$ = MAX, $V_{IH}$ = MIN | $I_{OL}$ = 48mA | | 0.35 | 0.50 | V |
| $V_{IK}$ | Input clamp voltage | | $V_{CC}$ = MIN, $I_I$ = $I_{IK}$ | | | –0.73 | –1.5 | V |
| $I_I$ | Input current at maximum input voltage | control inputs | $V_{CC}$ = MAX, $V_I$ = 7.0V | | | | 0.1 | mA |
| | | A or B ports | $V_{CC}$ = MAX, $V_I$ = 5.5V | | | | 0.1 | mA |
| $I_{IH}$ | High-level input current[3] | | $V_{CC}$ = MAX, $V_I$ = 2.7V | | | | 20 | µA |
| $I_{IL}$ | Low-level input current[3] | | $V_{CC}$ = MAX, $V_I$ = 0.4V | | | | –0.1 | mA |
| $I_O$ | Output current[4] | | $V_{CC}$ = MAX, $V_O$ = 2.25V | | –30 | | –112 | mA |
| $I_{CC}$ | Supply current (total) | $I_{CCH}$ | $V_{CC}$ = MAX | | | 40 | 57 | mA |
| | | $I_{CCL}$ | | | | 53 | 78 | mA |
| | | $I_{CCZ}$ | | | | 51 | 72 | mA |

**NOTES:**
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at $V_{CC}$ = 5V, $T_{amb}$ = 25°C.
3. For I/O ports, the parameter $I_{IH}$ and $I_{IL}$ include the off-state current.
4. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.

## AC ELECTRICAL CHARACTERISTICS FOR 74ALS646/74ALS646-1

| SYMBOL | PARAMETER | TEST CONDITION | LIMITS $T_{amb}$ = 0°C to +70°C, $V_{CC}$ = +5.0V ± 10%, $C_L$ = 50pF, $R_L$ = 500Ω | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $f_{max}$ | Maximum clock frequency | Waveform 1 | 100 | | MHz |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>CPBA to An, CPAB to Bn | Waveform 1 | 5.0<br>6.0 | 13.0<br>13.0 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>An to Bn or Bn to An | Waveform 2, 3 | 2.0<br>3.0 | 8.0<br>9.0 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>SBA to An or SAB to Bn (A or B Low) | Waveform 2, 3 | 5.0<br>5.0 | 13.0<br>11.0 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>SBA to An or SAB to Bn (A or B High) | Waveform 2, 3 | 5.0<br>5.0 | 11.0<br>11.0 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output enable time<br>$\overline{OE}$ to An or Bn | Waveform 5<br>Waveform 6 | 3.0<br>5.0 | 9.0<br>11.0 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output disable time<br>$\overline{OE}$ to An or Bn | Waveform 5<br>Waveform 6 | 2.0<br>3.0 | 8.0<br>10.0 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output enable time<br>DIR to An or Bn | Waveform 5<br>Waveform 6 | 2.0<br>5.0 | 10.0<br>12.0 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output disable time<br>DIR to An or Bn | Waveform 5<br>Waveform 6 | 2.0<br>3.0 | 10.0<br>13.0 | ns |

## AC ELECTRICAL CHARACTERISTICS FOR 74ALS648/74ALS648-1

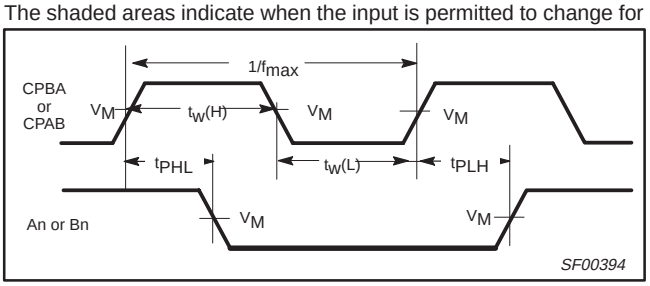
| SYMBOL | PARAMETER | TEST CONDITION | LIMITS | | UNIT |
|---|---|---|---|---|---|
| | | | $T_{amb}$ = 0°C to +70°C<br>$V_{CC}$ = +5.0V ± 10%<br>$C_L$ = 50pF, $R_L$ = 500Ω | | |
| | | | MIN | MAX | |
| $f_{max}$ | Maximum clock frequency | Waveform 1 | 100 | | MHz |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>CPBA to An, CPAB to Bn | Waveform 1 | 5.0<br>6.0 | 13.0<br>13.0 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>An to Bn or Bn to An | Waveform 2, 3 | 1.0<br>3.0 | 7.0<br>9.0 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>SBA to An or SAB to Bn (A or B Low) | Waveform 2, 3 | 5.0<br>5.0 | 13.0<br>11.0 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>SBA to An or SAB to Bn (A or B High) | Waveform 2, 3 | 4.0<br>5.0 | 11.0<br>11.0 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output enable time<br>$\overline{OE}$ to An or Bn | Waveform 5<br>Waveform 6 | 2.0<br>4.0 | 8.0<br>13.0 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output disable time<br>$\overline{OE}$ to An or Bn | Waveform 5<br>Waveform 6 | 1.0<br>2.0 | 8.0<br>10.0 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output enable time<br>DIR to An or Bn | Waveform 5<br>Waveform 6 | 3.0<br>5.0 | 10.0<br>12.0 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output disable time<br>DIR to An or Bn | Waveform 5<br>Waveform 6 | 2.0<br>2.0 | 11.0<br>11.0 | ns |

## AC SETUP REQUIREMENTS

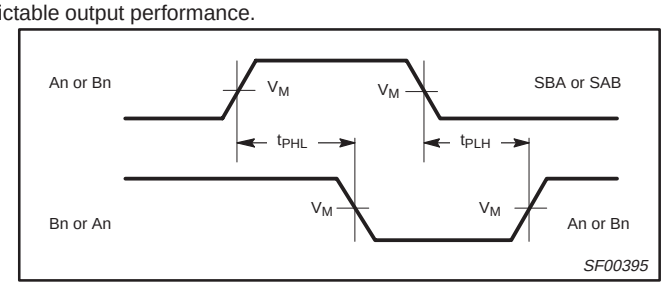
| SYMBOL | PARAMETER | TEST CONDITION | LIMITS | | UNIT |
|---|---|---|---|---|---|
| | | | $T_{amb}$ = 0°C to +70°C<br>$V_{CC}$ = +5.0V ± 10%<br>$C_L$ = 50pF, $R_L$ = 500Ω | | |
| $t_{su}$ (H)<br>$t_{su}$ (L) | Setup time, High or Low<br>An or Bn to CPAB or CPBA | Waveform 4 | 5.0<br>5.0 | | ns |
| $t_h$ (H)<br>$t_h$ (L) | Hold time, High or Low<br>An or Bn to CPAB or CPBA | Waveform 4 | 0.0<br>1.0 | | ns |
| $t_w$ (H)<br>$t_w$ (L) | Pulse width, High or Low<br>CPAB or CPBA | Waveform 1 | 6.0<br>4.0 | | ns |

## AC WAVEFORMS

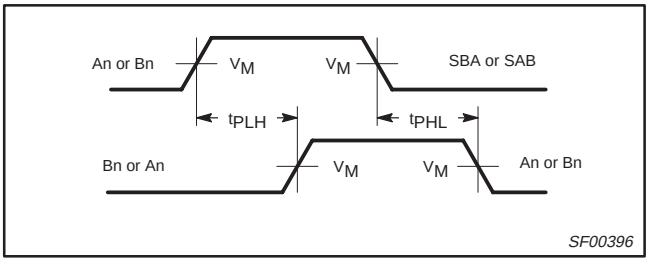
For all waveforms, $V_M$ = 1.3V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



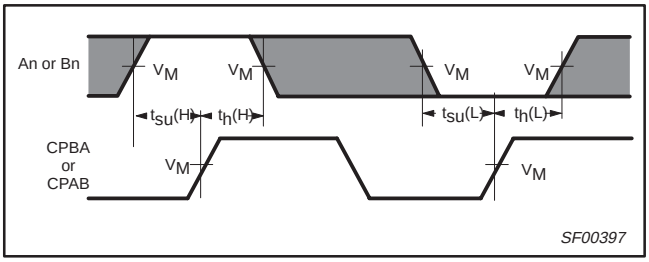

**Waveform 1. Propagation Delay for Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency**



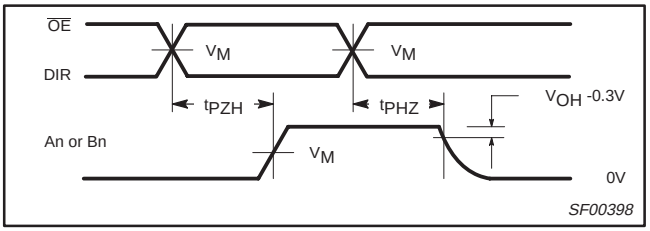

**Waveform 2. Propagation Delay for An to Bn or Bn to An and SAB or SBA to An or Bn**



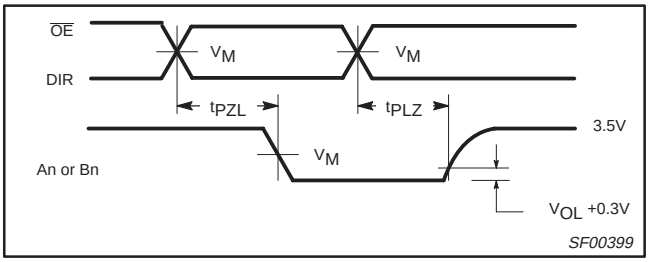

**Waveform 3. Propagation Delay for An to Bn or Bn to An and SAB or SBA to An or Bn**




**Waveform 4. Data Setup Time and Hold Times**

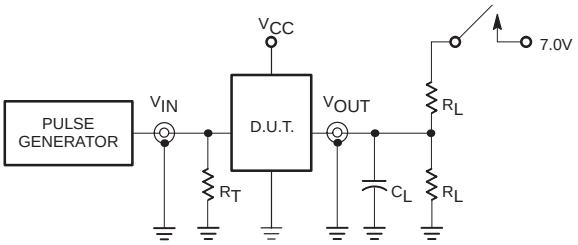



**Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level**




**Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level**

## TEST CIRCUIT AND WAVEFORMS




**Test Circuit for 3-State and Open Collector Outputs**

**SWITCH POSITION**

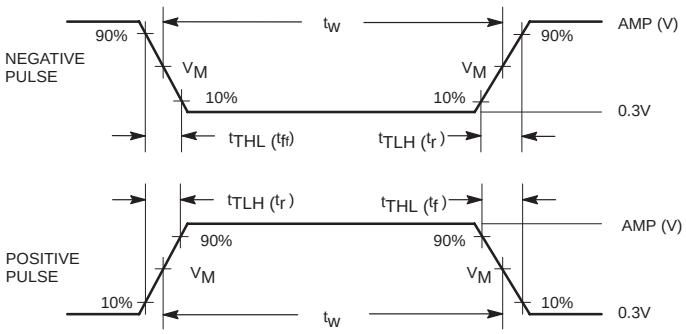
| TEST | SWITCH |
|---|---|
| $t_{PLZ}$, $t_{PZL}$ | closed |
| open collector | closed |
| All other | open |

**DEFINITIONS:**

$R_L$ = Load resistor; see AC electrical characteristics for value.

$C_L$ = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

$R_T$ = Termination resistance should be equal to $Z_{OUT}$ of pulse generators.

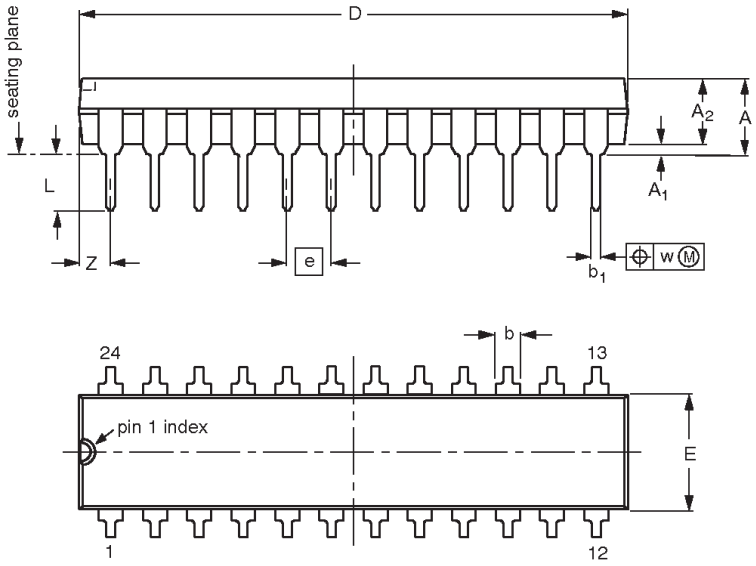


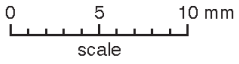

**Input Pulse Definition**

| Family | INPUT PULSE REQUIREMENTS | | | | | |
|---|---|---|---|---|---|---|
| | Amplitude | $V_M$ | Rep.Rate | $t_w$ | $t_{TLH}$ | $t_{THL}$ |
| 74ALS | 3.5V | 1.3V | 1MHz | 500ns | 2.0ns | 2.0ns |

SC00126

**DIP24: plastic dual in-line package; 24 leads (300 mil)** **SOT222-1**




**DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)**

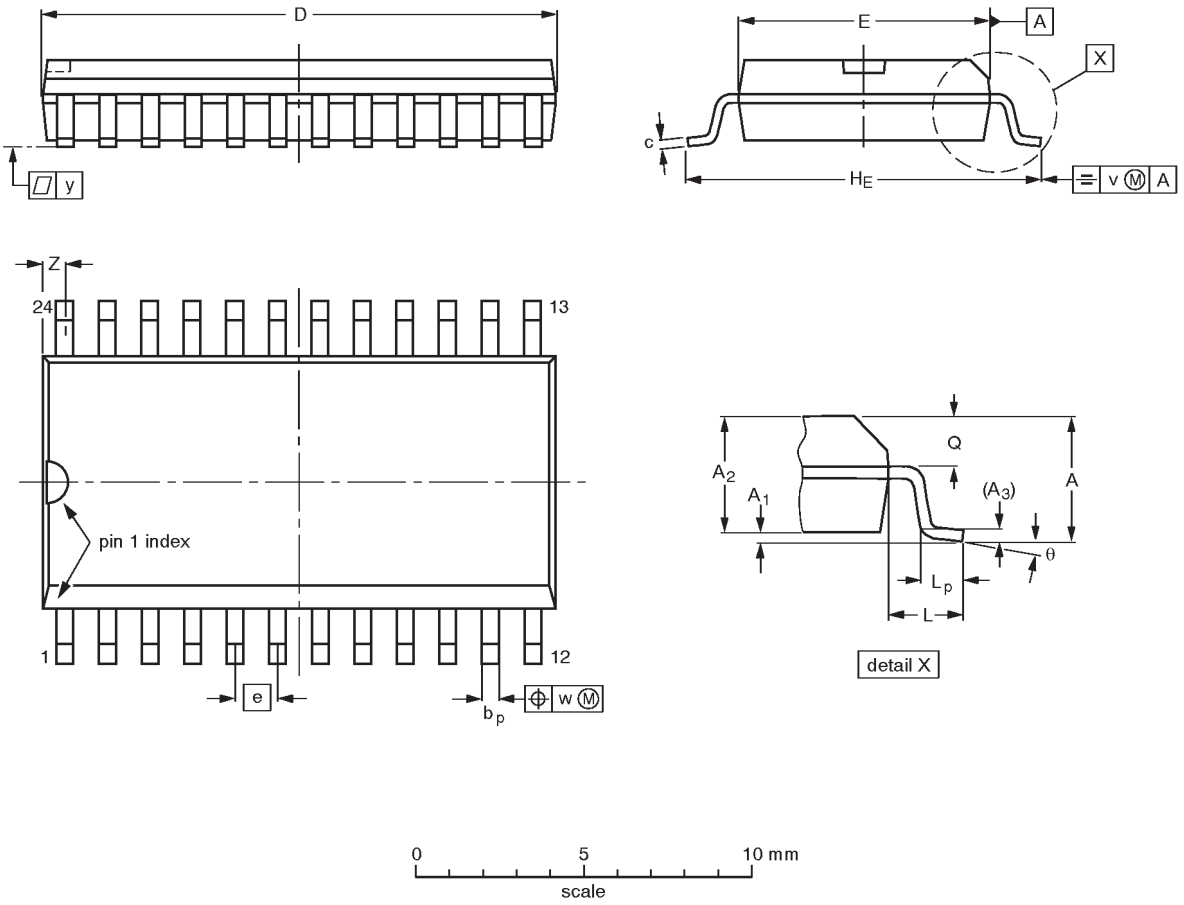
| UNIT | A max. | $A_1$ min. | $A_2$ max. | b | $b_1$ | c | D (1) | E (1) | e | $e_1$ | L | $M_E$ | $M_H$ | w | Z (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.70 | 0.38 | 3.94 | 1.63<br>1.14 | 0.56<br>0.43 | 0.36<br>0.25 | 31.9<br>31.5 | 6.73<br>6.48 | 2.54 | 7.62 | 3.51<br>3.05 | 8.13<br>7.62 | 10.03<br>7.62 | 0.25 | 2.05 |
| inches | 0.185 | 0.015 | 0.155 | 0.064<br>0.045 | 0.022<br>0.017 | 0.014<br>0.010 | 1.256<br>1.240 | 0.265<br>0.255 | 0.100 | 0.300 | 0.138<br>0.120 | 0.32<br>0.30 | 0.395<br>0.300 | 0.01 | 0.081 |

**Note**

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT222-1 | | MS-001AF | | | | 95-03-11 |

**SO24: plastic small outline package; 24 leads; body width 7.5 mm** **SOT137-1**







**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.65 | 0.30<br>0.10 | 2.45<br>2.25 | 0.25 | 0.49<br>0.36 | 0.32<br>0.23 | 15.6<br>15.2 | 7.6<br>7.4 | 1.27 | 10.65<br>10.00 | 1.4 | 1.1<br>0.4 | 1.1<br>1.0 | 0.25 | 0.25 | 0.1 | 0.9<br>0.4 | 8°<br>0° |
| inches | 0.10 | 0.012<br>0.004 | 0.096<br>0.089 | 0.01 | 0.019<br>0.014 | 0.013<br>0.009 | 0.61<br>0.60 | 0.30<br>0.29 | 0.050 | 0.42<br>0.39 | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT137-1 | 075E05 | MS-013AD | | | | ~~92-11-17~~<br>95-01-24 |

## DEFINITIONS

| Data Sheet Identification | Product Status | Definition |
|---|---|---|
| *Objective Specification* | Formative or in Design | This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice. |
| *Preliminary Specification* | Preproduction Product | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
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