Ordering number : EN*4030A

CMOS LSI

LC~~89080~~, 89080Q

Video Signal 3-Channel 8-Bit D/A Converter

Preliminary

DISCONTINUED PRODUCT

Overview

The LC89080 and LC89080Q are high-speed current-output D/A converters. They feature 8-bit resolution, provide 3 channels on a single chip, and can be used in demodulators for high-speed signals such as video signals.

Features

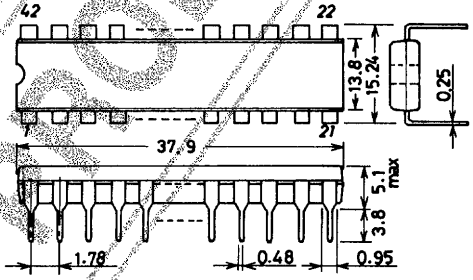
- Resolution: 8 bits
- D/A converters: Three current-output D/A converter channels on a single chip
- Maximum conversion speed: 30 MSPS
- Error: ±1.0 LSB (maximum)
- Power supply: +5 V single-voltage power supply
- Power dissipation: 330 mW
- Inputs: TTL compatible

Package Dimensions

unit: mm

3025B-DIP42S

[LC89080]

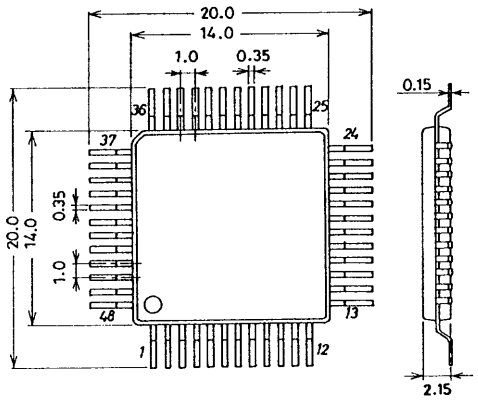


SANYO: DIP42S

unit: mm

3052A-QFP48A

[LC89080Q]



SANYO: QFP48A

SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +7.0	V
Input voltage	V_{IN}		–0.3 to V_{DD} + 0.3	V
Operating temperature	Topr		–30 to +75	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Reference voltage input	V_{REF}IN			1.0	2.0	V
Output resistance	R_O			75		Ω
Input high-level voltage	V_{IH}		2.2		V_{DD} + 0.3	V
Input low-level voltage	V_{IL}		–0.3		+0.8	V
Phase compensation capacitance	Ccomp		1			µF

Electrical Characteristics at Ta = 25°C, V_{DD} = 5.0 V, V_{REF}IN = 1.0 V, R_{REF} = 300 Ω, R_O = 75 Ω

Parameter	Symbol	Conditions	min	typ	max	Unit
Resolution	RES				8	Bits
Maximum conversion speed	Fs max		30			MSPS
Power dissipation	Pd	Fs = 30 MSPS		330	400	mW
Zero-scale output voltage	Vzero	For each channel	–15	0	+15	mV
Full-scale output voltage	Vfull	For each channel	0.92	1.00	1.08	V
Full-scale voltage ratio	FSR		0	4	8	%
Linearity error	I.L.	DC precision			±1.0	LSB
Differential linearity error	D.L.	DC precision			±0.5	LSB
Reference voltage output	V_{REF}OUT		0.99	1.00	1.01	V

DISCONTINUED PRODUCT

Pin Assignment LC89080 (DIP42S)

Pin No.	Symbol	Description
1	DV_{DD}	Digital system power supply (+5 V)
2	DA1	Channel A digital input (MSB)
3 to 8	DA2 to DA7	Channel A digital input
9	DA8	Channel A digital input (LSB)
10	DB1	Channel B digital input (MSB)
11 to 16	DB2 to DB7	Channel B digital input
17	DB8	Channel B digital input (LSB)
18	DC1	Channel C digital input (MSB)
19 to 24	DC2 to DC7	Channel C digital input
25	DC8	Channel C digital input (LSB)
26	CLK	Clock input
27	DV_{DD}	Digital system power supply (+5 V)
28	DGND	Digital system ground (0 V)
29	ICOB	Channel C negative output. Connect to A.GND through an output resistor R_O (usually 75 Ω).
30	ICO	Channel C positive output. Connect to A.GND through an output resistor R_O (usually 75 Ω).
31	AV_{DD}	Analog system power supply (+5 V)
32	IBOB	Channel B negative output. Connect to A.GND through an output resistor R_O (usually 75 Ω).
33	IBO	Channel B positive output. Connect to A.GND through an output resistor R_O (usually 75 Ω).
34	AGND	Analog system ground (0 V)
35	IAOB	Channel A negative output. Connect to A.GND through an output resistor R_O (usually 75 Ω).
36	IAO	Channel A positive output. Connect to A.GND through an output resistor R_O (usually 75 Ω).
37	AV_{DD}	Analog system power supply (+5 V)
38	COMP	Phase compensation capacitor. Connect a 1 µF capacitor between this pin and ground.
39	I_{REF}	Reference current output. Connect a resistor that is 4 times the output resistance R_O to this pin.
40	V_{REF}IN	Reference voltage input. This input pin sets the analog output dynamic range.
41	V_{REF}OUT	Reference voltage output. The output voltage is set to 0.2 times V_{DD} by a resistor divider. When V_{DD} is 5.0 V, a 1.0 V reference voltage can be acquired from pin 40.
42	DGND	Digital system ground (0 V)

DISCONTINUED PRODUCT

Pin Assignment LC89080Q (QFP48A)

Pin No.	Symbol	Description
1 to 3	DA5 to 7	Channel A digital input
4	DA8	Channel A digital input (LSB)
5	DB1	Channel B digital input (MSB)
6	NC	Unused (no connection)
7 to 12	DB2 to DB7	Channel B digital input
13	DB8	Channel B digital input (LSB)
14	DC1	Channel C digital input (MSB)
15 to 18	DC2 to DC5	Channel C digital input
19	DV_{DD}	Digital system power supply (+5 V)
20	DC6	Channel C digital input
21	DC7	Channel C digital input
22	DC8	Channel C digital input (LSB)
23	CLK	Clock input
24	NC	Unused (no connection)
25	DV_{DD}	Digital system power supply (+5 V)
26	DGND	Digital system ground (0 V)
27	ICOB	Channel C negative output. Connect to A.GND through an output resistor R_O (usually 75 Ω).
28	ICO	Channel C positive output. Connect to A.GND through an output resistor R_O (usually 75 Ω).
29	AV_{DD}	Analog system power supply (+5 V)
30	AV_{DD}	Analog system power supply (+5 V)
31	IBOB	Channel B negative output. Connect to A.GND through an output resistor R_O (usually 75 Ω).
32	IBO	Channel B positive output. Connect to A.GND through an output resistor R_O (usually 75 Ω).
33	AGND	Analog system ground (0 V)
34	IAOB	Channel A negative output. Connect to A.GND through an output resistor R_O (usually 75 Ω).
35	IAO	Channel A positive output. Connect to A.GND through an output resistor R_O (usually 75 Ω).
36	AV_{DD}	Analog system power supply (+5 V)
37	COMP	Phase compensation capacitor. Connect a 1 µF capacitor between this pin and ground.
38	NC	Unused (no connection)
39	I_{REF}	Reference current output. Connect a resistor that is 4 times the output resistance R_O to this pin.
40	$V_{REF}IN$	Reference voltage input. This input pin sets the analog output dynamic range.
41	$V_{REF}OUT$	Reference voltage output. The output voltage is set to 0.2 times V_{DD} by a resistor divider. When V_{DD} is 5.0 V, a 1.0 V reference voltage can be acquired from pin 40.
42	DGND	Digital system ground (0 V)
43	DV_{DD}	Digital system power supply (+5 V)
44	DV_{DD}	Digital system power supply (+5 V)
45	DA1	Channel A digital input (MSB)
46 to 48	DA2 to DA4	Channel A digital input

DISCONTINUED PRODUCT

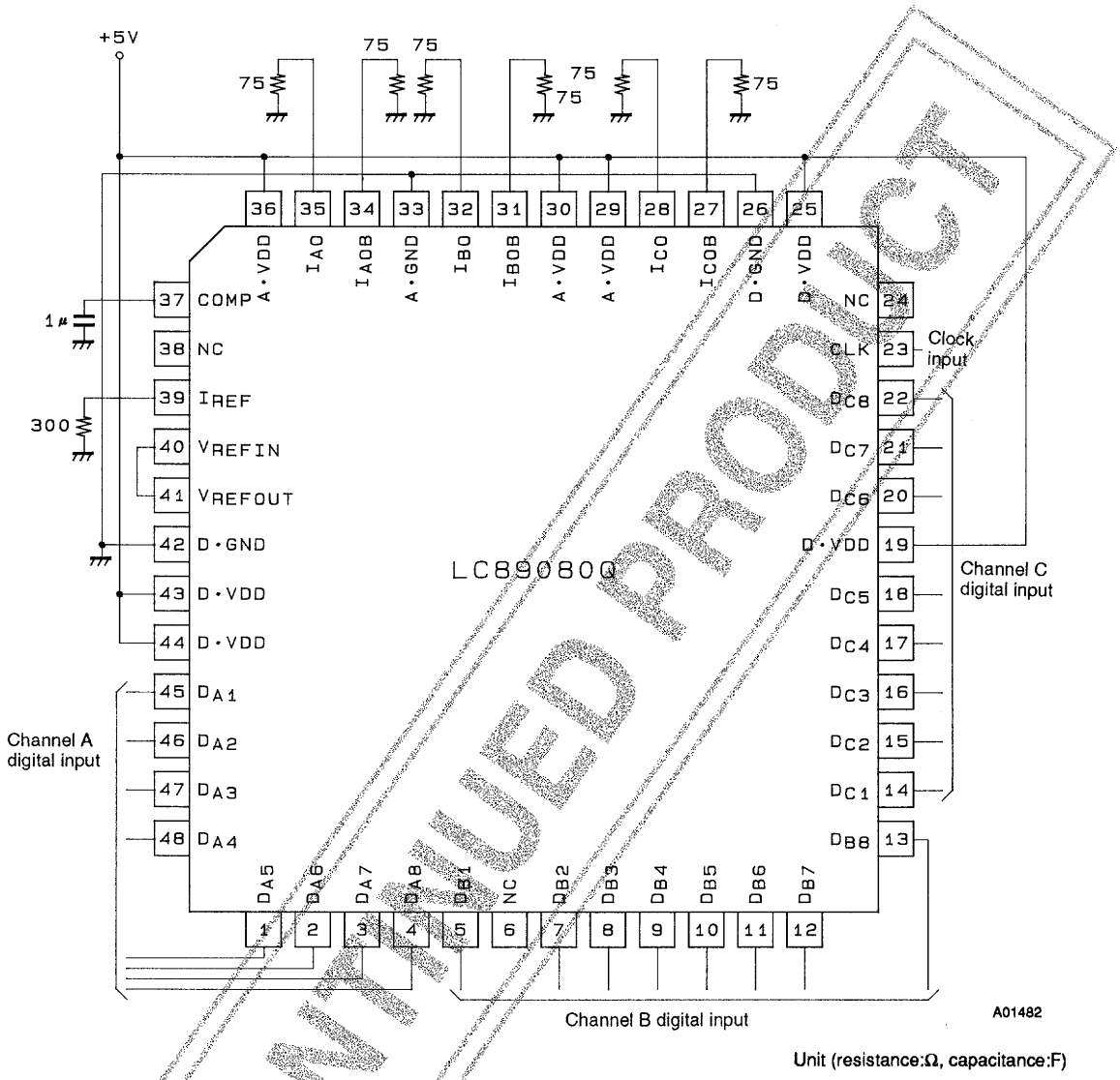
Pin Assignment LC89080Q (QFP48A)

Pin No.	Symbol	Description
1 to 3	DA5 to 7	Channel A digital input
4	DA8	Channel A digital input (LSB)
5	DB1	Channel B digital input (MSB)
6	NC	Unused (no connection)
7 to 12	DB2 to DB7	Channel B digital input
13	DB8	Channel B digital input (LSB)
14	DC1	Channel C digital input (MSB)
15 to 18	DC2 to DC5	Channel C digital input
19	DV_{DD}	Digital system power supply (+5 V)
20	DC6	Channel C digital input
21	DC7	Channel C digital input
22	DC8	Channel C digital input (LSB)
23	CLK	Clock input
24	NC	Unused (no connection)
25	DV_{DD}	Digital system power supply (+5 V)
26	DGND	Digital system ground (0 V)
27	ICOB	Channel C negative output. Connect to A.GND through an output resistor R_O (usually 75 Ω).
28	ICO	Channel C positive output. Connect to A.GND through an output resistor R_O (usually 75 Ω).
29	AV_{DD}	Analog system power supply (+5 V)
30	AV_{DD}	Analog system power supply (+5 V)
31	IBOB	Channel B negative output. Connect to A.GND through an output resistor R_O (usually 75 Ω).
32	IBO	Channel B positive output. Connect to A.GND through an output resistor R_O (usually 75 Ω).
33	AGND	Analog system ground (0 V)
34	IAOB	Channel A negative output. Connect to A.GND through an output resistor R_O (usually 75 Ω).
35	IAO	Channel A positive output. Connect to A.GND through an output resistor R_O (usually 75 Ω).
36	AV_{DD}	Analog system power supply (+5 V)
37	COMP	Phase compensation capacitor. Connect a 1 µF capacitor between this pin and ground.
38	NC	Unused (no connection)
39	I_{REF}	Reference current output. Connect a resistor that is 4 times the output resistance R_O to this pin.
40	V_{REF}IN	Reference voltage input. This input pin sets the analog output dynamic range.
41	V_{REF}OUT	Reference voltage output. The output voltage is set to 0.2 times V_{DD} by a resistor divider. When V_{DD} is 5.0 V, a 1.0 V reference voltage can be acquired from pin 40.
42	DGND	Digital system ground (0 V)
43	DV_{DD}	Digital system power supply (+5 V)
44	DV_{DD}	Digital system power supply (+5 V)
45	DA1	Channel A digital input (MSB)
46 to 48	DA2 to DA4	Channel A digital input

DISCONTINUED PRODUCT

Sample Application Circuit: LC89080Q

Application circuit in which the output resistance is 75 Ω and the internally generated 1-V reference voltage is used.



Unit (resistance:Ω, capacitance:F)

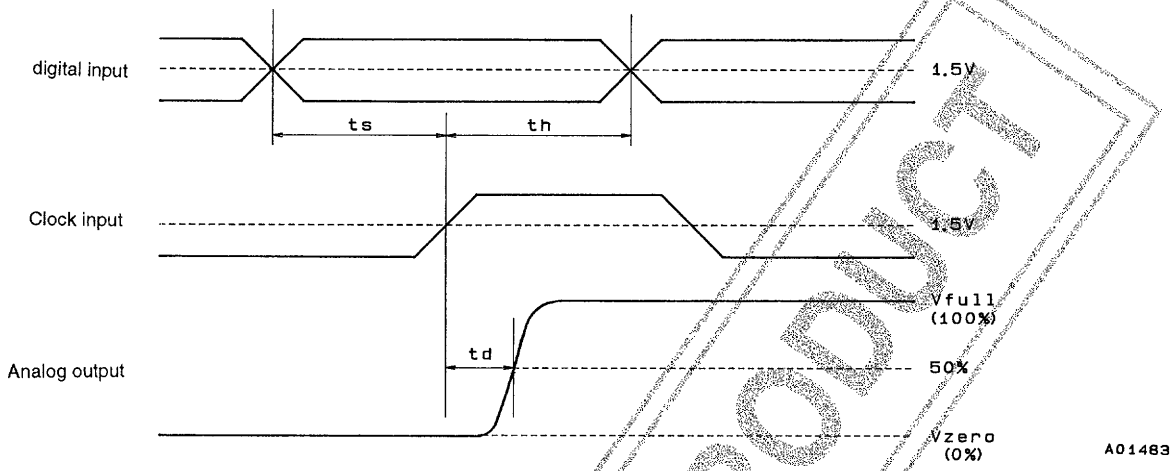
AC Characteristics at Ta = –30 to 70°C, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Data setup time	ts		15			ns
Data hold time	th		15			ns
Output delay time	td			10		ns

DISCONTINUED PRODUCT

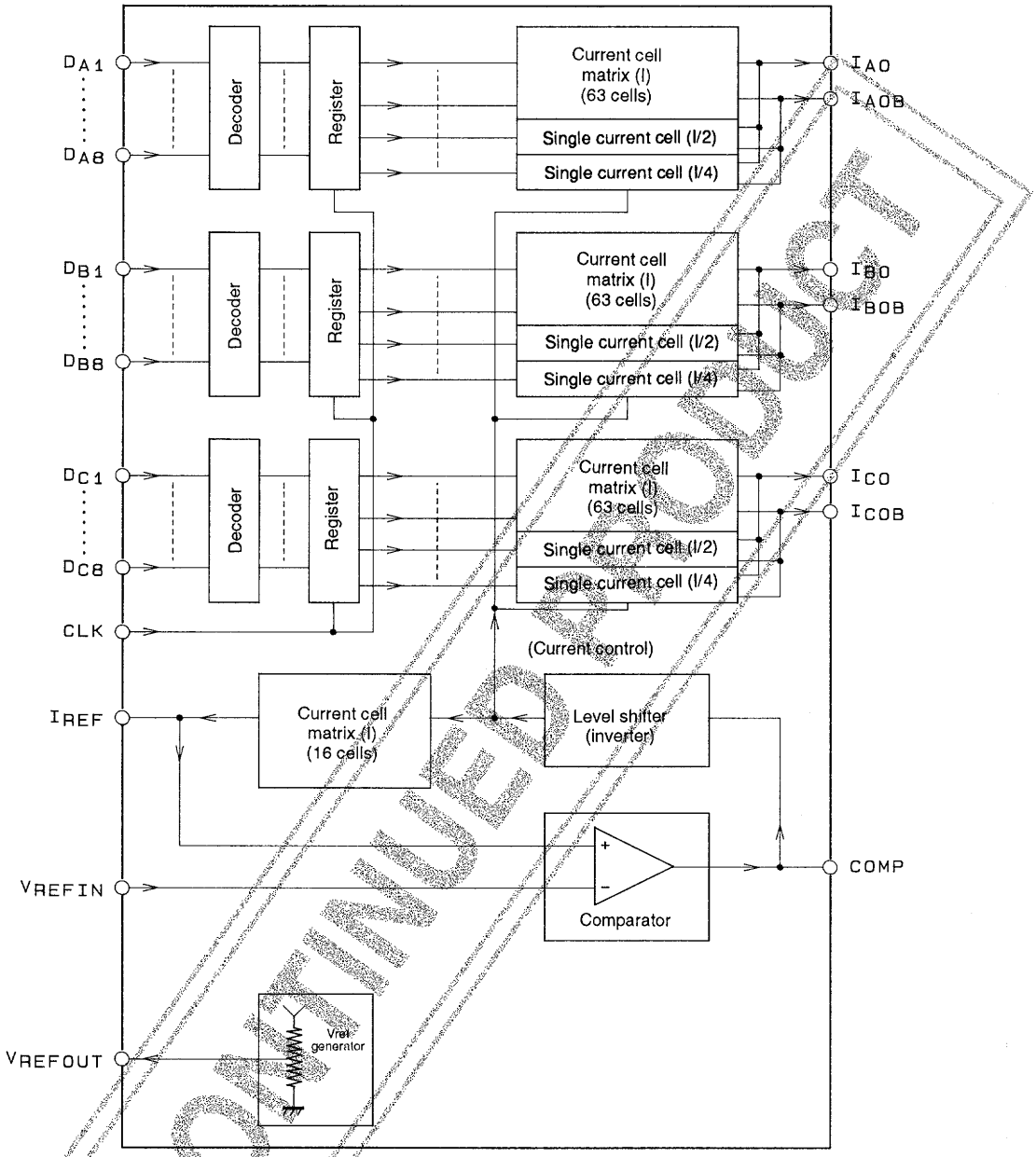
Timing Chart

The digital inputs for all 3 channels are acquired on the rising edge of the clock input, after which the corresponding analog voltages are output.



DISCONTINUED PRODUCT

Block Diagram



DISCONTINUED PRODUCT

■ No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.

■ Anyone purchasing any products described or contained herein for an above-mentioned use shall:
① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use:
② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.

■ Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of February, 1997. Specifications and information herein are subject to change without notice.