

SANYO

No.3085A

LC89060,89060M

6-Bit Video D/A Converters

Overview

The LC89060 and LC89060M are high-speed digital-to-analog converters suitable for use in video equipment and high-speed decoders. They operate from a single 5V supply, and feature a 30 Mega-samples per second conversion rate and low power dissipation.

The LC89060 is available in 16-pin DIPs, and the LC89060M in 20-pin flatpacks.

Features

- 30 MSPS conversion rate
- Low 80mW (typ) power dissipation
- Linearity error within ± 0.5 LSB (max)
- TTL-compatible inputs
- High-speed CMOS process

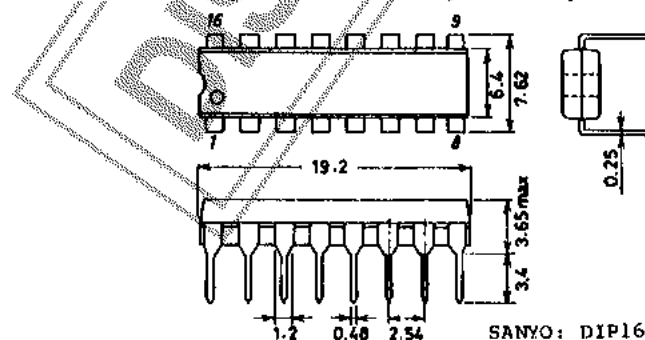
Absolute Maximum Ratings at $T_a = 25^\circ\text{C}, V_{SS} = 0\text{V}$

Parameter	Symbol	Value	unit
Maximum Supply Voltage	V_{DD} max	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.3 to $V_{DD} + 0.3$	V
Operating Temperature	T_{opr}	-30 to +75	$^\circ\text{C}$
Storage Temperature	T_{stg}	-40 to +125	$^\circ\text{C}$

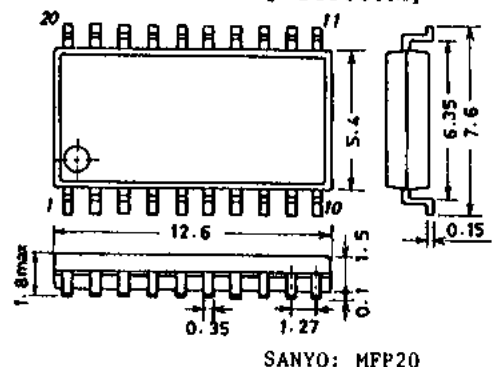
Recommended Operating Conditions

Parameter	Symbol	min	typ	max	unit
Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Reference Voltage (H)	V_{RH}			V_{DD}	V
Reference Voltage (L)	V_{RL}	0			V
Input 'H'-Level Voltage	V_{IH}	2.2	$V_{DD} + 0.3$		V
Input 'L'-Level Voltage	V_{IL}	-0.3		0.8	V
Data Setup Time	t_s		5		ns
Data Hold Time	t_h		20		ns
Operating Temperature	T_a	-30		75	$^\circ\text{C}$

Package Dimensions 3006B
(unit: mm) [LC89060]



Package Dimensions 3036B
(unit: mm) [LC89060M]



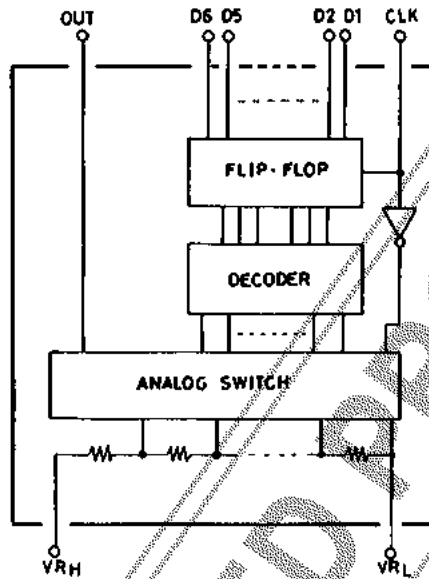
SANYO Electric Co., Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

LC89060, 89060M

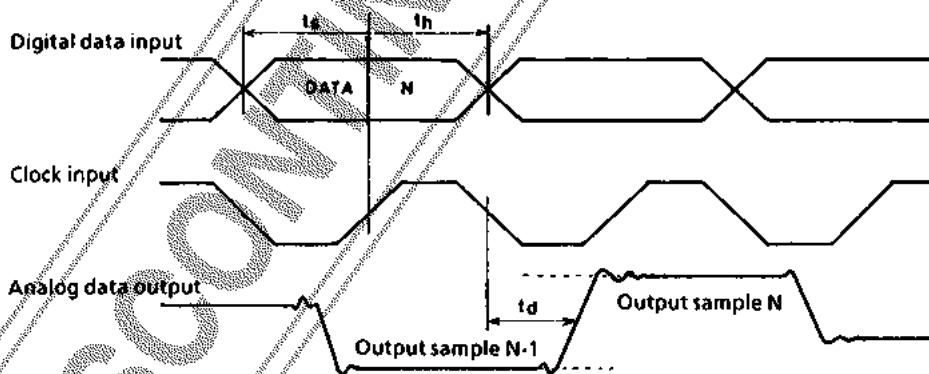
Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{DD} = 5.0\text{V}$, $V_{RH} - V_{RL} = 1.0\text{V}$

		min	typ	max	unit
Resolution	RES			6	bit
Maximum Sampling Frequency	F_s max	30			MSPS
Power Dissipation	P_d		$F_s = 30\text{MHz}$	80	120 mW
Linearity Error	I.L.		DC accuracy	± 0.5	LSB
Differential Linearity Error	D.L.		DC accuracy	± 0.5	LSB

Equivalent Circuit Block Diagram



Timing Chart



Pin Functions

● LC89060

Number	Name	Function
1	V _{DD}	Positive supply
2	N.C.	No connection
3	V _{RL}	Low reference voltage input
4	N.C.	No connection
5	OUT	Analog voltage output
6	V _{RH}	High reference voltage input
7	V _{DD}	Positive supply
8	GND	Supply ground
9	CLK	Clock input
10	D1	Digital input data, most significant bit
11	D2	Digital input data
12	D3	Digital input data
13	D4	Digital input data
14	D5	Digital input data
15	D6	Digital input data, least significant bit
16	GND	Supply ground

● LC89060M

Number	Name	Function
1	V _{DD}	Positive supply
2	N.C.	No connection
3	N.C.	No connection
4	V _{RL}	Low reference voltage input
5	N.C.	No connection
6	OUT	Analog voltage output
7	N.C.	No connection
8	V _{RH}	High reference voltage input
9	V _{DD}	Positive supply
10	GND	Supply ground
11	CLK	Clock input
12	D1	Digital input data, most significant bit
13	N.C.	No connection
14	D2	Digital input data
15	D3	Digital input data
16	D4	Digital input data
17	D5	Digital input data
18	N.C.	No connection
19	D6	Digital input data, least significant bit
20	GND	Supply ground

Functional Description

Data on the input pins D1 to D6 is latched into the input flip-flops on the rising edge of the CLK input signal. This data is processed by the decoder while CLK is HIGH, and output on the falling edge of CLK. CLK should be held LOW if no data is being input to the converter.

V_{RH} and V_{RL} are the converter high and low reference voltages. The output voltage is linearly related to the input data, V_{RH} and V_{RL} , as shown in the table below.

	Input data	Output voltage
0	000000	V_{RL}
1	000001	$V_{RL} + \frac{1}{64} (V_{RH} - V_{RL})$
2	000010	$V_{RL} + \frac{2}{64} (V_{RH} - V_{RL})$
⋮	⋮	⋮
62	111110	$V_{RL} + \frac{62}{64} (V_{RH} - V_{RL})$
63	111111	$V_{RL} + \frac{63}{64} (V_{RH} - V_{RL})$

Application Circuits

The following diagrams show typical application circuits for the LC89060 and LC89060M. The high reference voltage is connected to the positive supply line, and the low reference voltage generated by a voltage divider and emitter follower. The analog output voltage is buffered by a high-speed op-amp or emitter-follower circuit, and low-pass filtered to remove unwanted frequency components.

