



LC868900/10/50/60

Column Driver IC for Dot Matrix Graphic LCD

Preliminary

Overview

The LC868900 is a column (segment) driver with the display RAM for the liquid crystal dot matrix-graphic display. It stores display data sent from the 8-bit microcontroller in the internal display RAM and generates dot matrix LCD signals.

The LC868900 can control the graphic mode, in which each bit of data from the internal RAM either lights or does not light a dot in the LCD.

As the LC868900 is fabricated using CMOS process technology, combining it with a CMOS microcontroller produces an LCD devices of low power demand.

Feature

(1) Classification

- Interfacing allowed with 80-family

LC868900	640×8-bit RAM
LC868910	1280×8-bit RAM
- Interfacing allowed with motorola-family

LC868950	640×8-bit RAM
LC868960	1280×8-bit RAM

(2) Segment outputs

- 80 segment outputs
- Segment display direction programmable

(3) Automatic LCD display controller

- Display duty : 1 / 1 - 1 / 65 duty
- Instruction functions
 - ON / OFF of display
 - Control of the horizontal display bits : (6 - 8 bits)×(horizontal display bytes)
 - Vertical display scroll function : Set of start address register
 - Selectable display data output : 'Logical-OR output' or 'Exclusive-OR output'
 - Read / Write display data
 - Read of busy flag

■ Any and all SANYO products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO representative nearest you before using any SANYO products described or contained herein in such applications.

■ SANYO assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO products described or contained herein.

SANYO Electric Co.,Ltd. Semiconductor Company

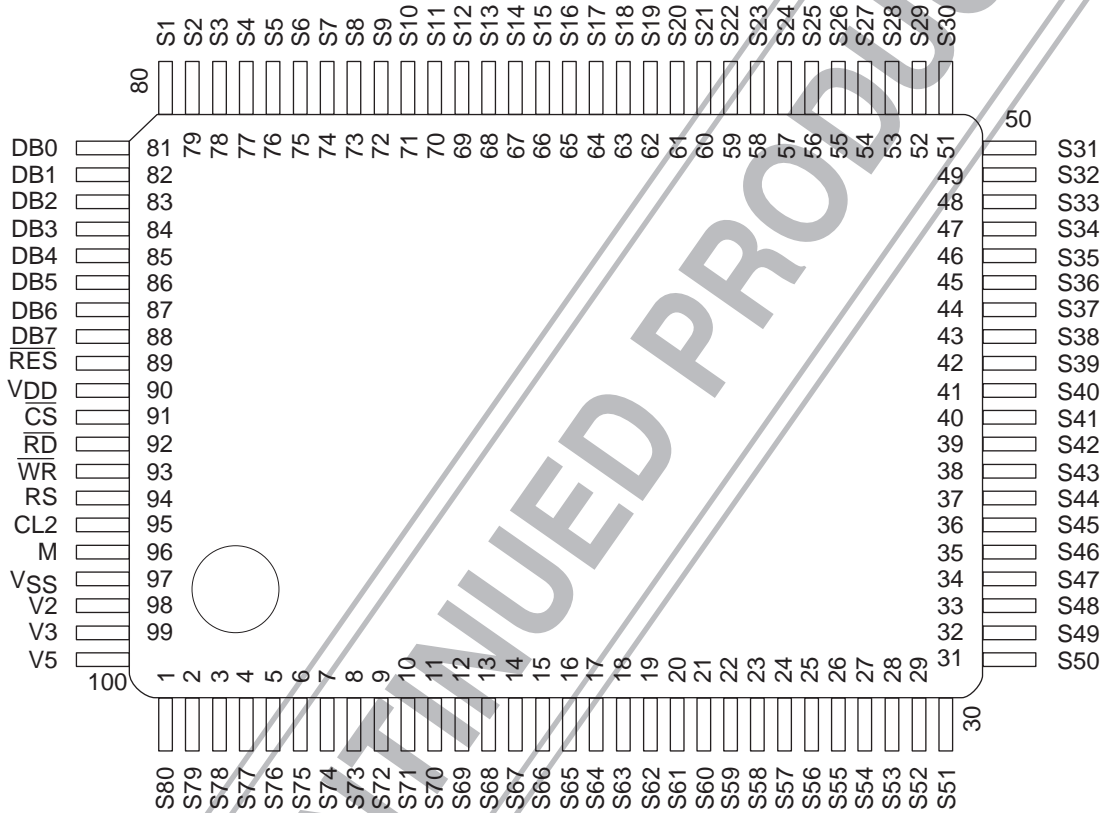
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

- (4) Power supply
 - Logic circuit 3 to 5V (VDD)
 - LCD drive circuit VDD to VDD-15V

(5) CMOS process

- (6) Factory shipment
 - Chip delivery form
 - QFP100

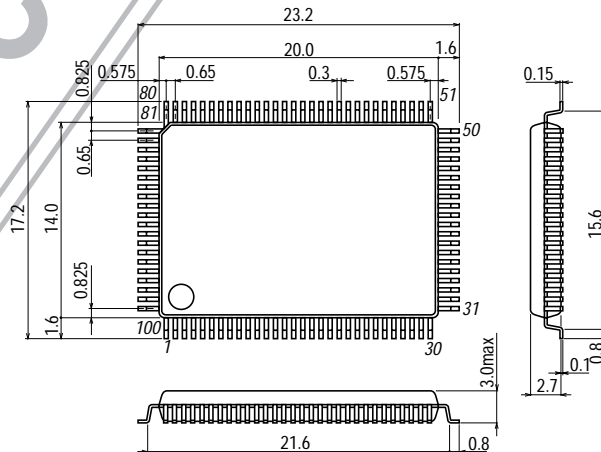
Pin Assignment



ILC00170

Package Dimensions

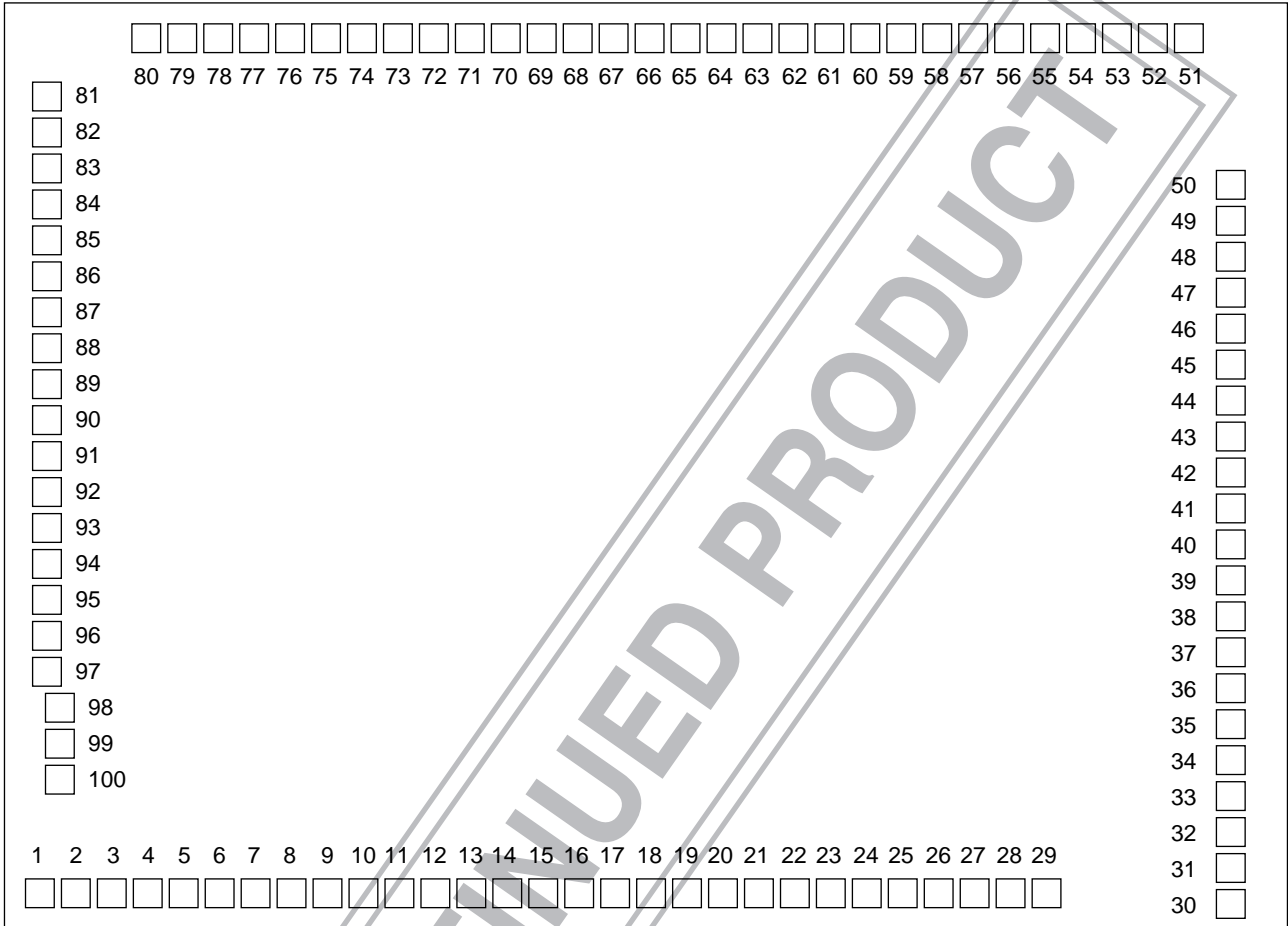
unit : mm
3151



SANYO : QIP-100E

Pad Layout

Chip size (X×Y) : 5.71mm×4.43mm
 Thickness of chip : 480μs
 Pad size : 120μm×120μm



ILC00171

Pad Name and coordinates table

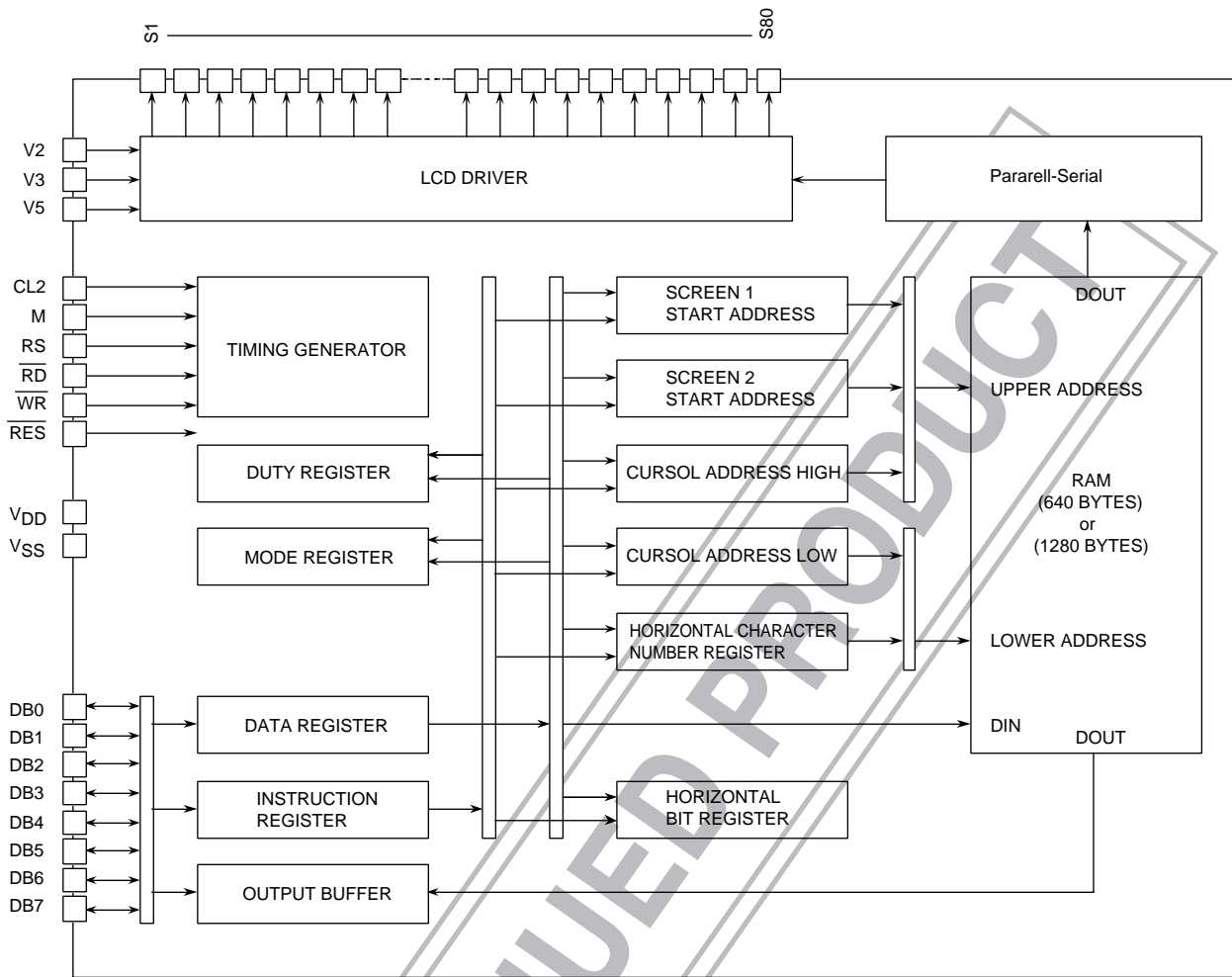
Pin No.	Pad No.	Name	Coordinates	
			X μ m	Y μ m
1	1	S80	-2645	-1974
2	2	S79	-2483	-1974
3	3	S78	-2320	-1974
4	4	S77	-2158	-1974
5	5	S76	-1995	-1974
6	6	S75	-1833	-1974
7	7	S74	-1670	-1974
8	8	S73	-1508	-1974
9	9	S72	-1345	-1974
10	10	S71	-1183	-1974
11	11	S70	-1020	-1974
12	12	S69	-858	-1974
13	13	S68	-695	-1974
14	14	S67	-533	-1974
15	15	S66	-370	-1974
16	16	S65	-208	-1974
17	17	S64	-45	-1974
18	18	S63	117	-1974
19	19	S62	280	-1974
20	20	S61	442	-1974
21	21	S60	605	-1974
22	22	S59	767	-1974
23	23	S58	930	-1974
24	24	S57	1092	-1974
25	25	S56	1255	-1974
26	26	S55	1417	-1974
27	27	S54	1580	-1974
28	28	S53	1742	-1974
29	29	S52	1905	-1974
30	30	S51	2658	-1985
31	31	S50	2658	-1823
32	32	S49	2658	-1660
33	33	S48	2658	-1498
34	34	S47	2658	-1335
35	35	S46	2658	-1173
36	36	S45	2658	-1010
37	37	S44	2658	-848
38	38	S43	2658	-685
39	39	S42	2658	-523
40	40	S41	2658	-360
41	41	S40	2658	-198
42	42	S39	2658	-35
43	43	S38	2658	127
44	44	S37	2658	290
45	45	S36	2658	452
46	46	S35	2658	615
47	47	S34	2658	777
48	48	S33	2658	940
49	49	S32	2658	1102
50	50	S31	2658	1265

Pin No.	Pad No.	Name	Coordinates	
			X μ m	Y μ m
51	51	S30	2572	2019
52	52	S29	2409	2019
53	53	S28	2247	2019
54	54	S27	2084	2019
55	55	S26	1922	2019
56	56	S25	1759	2019
57	57	S24	1597	2019
58	58	S23	1434	2019
59	59	S22	1272	2019
60	60	S21	1109	2019
61	61	S20	947	2019
62	62	S19	784	2019
63	63	S18	622	2019
64	64	S17	459	2019
65	65	S16	297	2019
66	66	S15	134	2019
67	67	S14	-28	2019
68	68	S13	-191	2019
69	69	S12	-353	2019
70	70	S11	-516	2019
71	71	S10	-678	2019
72	72	S9	-841	2019
73	73	S8	-1003	2019
74	74	S7	-1166	2019
75	75	S6	-1328	2019
76	76	S5	-1491	2019
77	77	S4	-1653	2019
78	78	S3	-1816	2019
79	79	S2	-1978	2019
80	80	S1	-2141	2019
81	81	DB0	-2540	1905
82	82	DB1	-2540	1734
83	83	DB2	-2540	1563
84	84	DB3	-2540	1392
85	85	DB4	-2540	1221
86	86	DB5	-2540	1051
87	87	DB6	-2540	880
88	88	DB7	-2540	709
89	89	RES	-2540	538
90	90	VDD	-2540	375
91	91	CS	-2540	213
92	92	RD	-2540	50
93	93	WR	-2540	-112
94	94	RS	-2540	-275
95	95	CL2	-2540	437
96	96	M	2540	-600
97	97	VSS	-2540	-762
98	98	V2	-2517	-943
99	99	V3	-2517	-1106
100	100	V5	-2571	-1268

Notes ;

- When the chip is used, connect the substrate of chip to VDD (or open).
- If the package immerse in the solder tank when mounting the QFP on the substrate, inquire of our company about the conditions of it.

Block Diagram



ILC00172

Pin Description

Pin	Pin No.	Input / Output	Function Description
VSS	97	-	Should be connected with the negative supply voltage pin.
VDD	90	-	Should be connected with the positive supply voltage pin.
DB0 to DB7	81 to 88	Input / Output	Built-in Data bus and pull-up resistor terminal for transmitting / receiving data to / from the MPU
RES	89	Input	Reset, built-in pull-up resistor
CS	91	Input	Chip select : Selection allowed when CS=0, built-in pull-up resistor
RD	92	Input	Read signal : MPU ← LC868900 series, built-in pull-up resistor
WR	93	Input	Write signal : MPU → LC868900 series, built-in pull-up resistor
RS	94	Input	Register select : RS=1 ; instruction register, RS=0 ; data register Built-in Pull-up resistor
CL2	95	Input	Signal for LCD display (clock signal), built-in pull-down resistor
M	96	Input	Signal for LCD display (synchronization), built-in pull-up resistor
V2 V3 V5	98 99 100	-	Voltage supply pins to LCD drivers
S1 to S80	80 to 1	Output	Segment driver pins for LCD display

LC868900/10/50/60

1. Absolute Maximum Ratings at $V_{SS}=0V$ and $T_a=25^{\circ}C$

Parameter	Symbol	Pins	Conditions	Ratings			unit	
				VDD[V]	min.	typ.		max.
Supply voltage	VDD MAX	VDD			-0.3		+7.0	V
Input voltage for LCD	VNMAX	V2, V3, V5			VDD-12		VDD+0.3	
Input voltage	VI(1)	CS, RD, WR, RS CL2, M, RES			-0.3		VDD+0.3	
	VI(2)	DB0 to DB7 (Input mode)			-0.3		VDD+0.3	
Output voltage	VO(1)	S1 to S80			VDD-12		VDD+0.3	
	VO(2)	DB0 to DB7 (Output mode)			-0.3		VDD+0.3	
Power dissipation (max.)	Pdmax	QFP100E	$T_a = -30$ to $+70^{\circ}C$				200	mW
Operating temperature range	Topg				-30		70	$^{\circ}C$
Storage temperature range	Tstg				-55		150	

*Satisfy the next condition : $V_{DD} \geq V_2 \geq V_3 \geq V_5$

DISCONTINUED PRODUCT

LC868900/10/50/60

2. Recommended Operating Range at Ta= -30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	Ratings			unit		
				VDD [V]	min.	typ.		max.	
Operating supply voltage range	VDD	VDD	FCL2 ≤ 500kHz		2.5		6.0	V	
HOLD voltage	VHD	VDD	RAMs and Registers hold voltage at standby mode.		2.0		6.0		
Input high voltage	VIH(1)	DB0 to DB7	Input mode	4.5 to 6.0	2.2		VDD		
				2.5 to 4.5	0.75VDD		VDD		
	VIH(2)	CS, RD, WR, RS		4.5 to 6.0	2.2		VDD		
				2.5 to 4.5	0.75VDD		VDD		
VIH(3)	CL2, M, RES			4.5 to 6.0	0.75VDD		VDD		
				2.5 to 4.5	0.75VDD		VDD		
Input low voltage	VIL(1)	DB0 to DB7	Input mode	4.5 to 6.0	0		0.8		
				2.5 to 4.5	0		0.25VDD		
	VIL(2)	CS, RD, WR, RS			4.5 to 6.0	0		0.8	
					2.5 to 4.5	0		0.25VDD	
VIL(3)	CL2, M, RES			4.5 to 6.0	0		0.25VDD		
				2.5 to 4.5	0		0.25VDD		
Input clock frequency	FCL2	CL2		2.5 to 6.0	0		500	kHz	

[Notes]

The specifications above are for a die mounted in a QFP100E type package.

However, we ship this product as a die only, not a package chip.

Therefore, the operational characteristics may vary depending on the user's packaging techniques.

LC868900/10/50/60

3. Electrical Characteristics at Ta= -30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	Ratings			unit	
				VDD [V]	min.	typ.		max.
Output high voltage	IOH(1)	DB80 to DB7	•Output mode •IOH= -0.6mA	4.5 to 6.0	2.4		VDD	V
			•Output mode •IOH= -0.1mA	2.5 to 6.0	VDD -0.5		VDD	
Output low voltage	VOL(1)	DB0 to DB7	•Output mode •IOH=+0.6mA	4.5 to 6.0	0		0.4	
			•Output mode •IOH=+0.1mA	2.5 to 6.0	0		0.4	
VDD-Si drop voltage (i:1 to 80)	VD(1)	S1 to S80	•Si terminal for -90μA •VDD -V5=11V	4.5 to 6.0				mV
			•Si terminal for -15μA •VDD -V5=11V	2.5 to 6.0			120	
VX-Si drop voltage (X:2, 3) (i:1 to 80)	VD(2)	S1 to S80	•Si terminal for -90μA •VDD -V5=11V	4.5 to 6.0				mV
			•Si terminal for -15μA •VDD -V5=11V	2.5 to 6.0			120	
Pull-up resistor	Rpu(1)	DB0 to DB7	•Input mode •VIN=0V	4.5 to 6.0	150	500	900	kΩ
			•Input mode •VIN=0V	2.5 to 4.5	300	750	1500	
	Rpu(2)	CS, RD, WR, RS, RES	VIN=0V	4.5 to 6.0	150	500	900	
			VIN=0V	2.5 to 4.5	300	750	1500	
Pull-down resistor	RPD(1)	CL2	VIN=0V	4.5 to 6.0	150	500	900	kΩ
			VIN=0V	2.5 to 4.5	300	750	1500	
Hysteresis voltage	VHIS	RES		2.5 to 6.0		0.1VDD		V
Current dissipation at operation	IDD(1)		•FCL2=500kHz •Figure 1	4.5 to 6.0				mA
			•FCL2=500kHz •Figure 1	2.5 to 4.5				
Current dissipation at stand-by mode	IDD(2)		•FCL2=0Hz •V2=V3=V5=VDD •Figure 2	4.5 to 6.0		0.05	30	μA
			•FCL2=0Hz •V2=V3=V5=VDD •Figure 2	2.5 to 4.5		0.02	20	

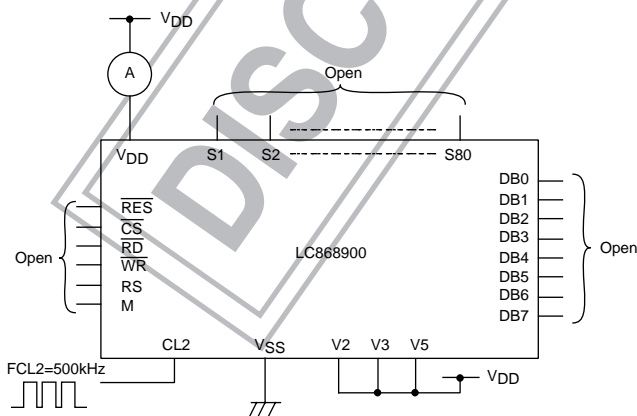


Figure1. Current dissipation measuring circuit at operation

ILC00173

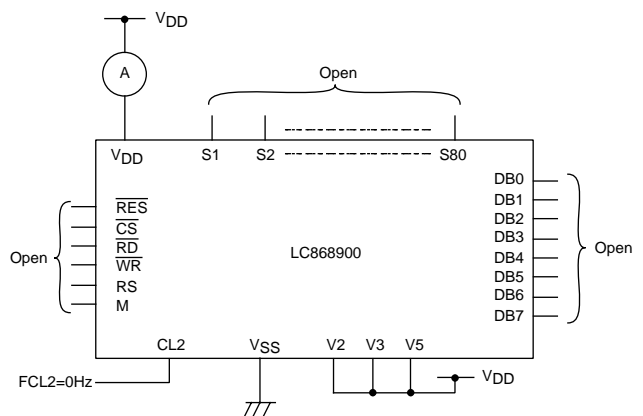
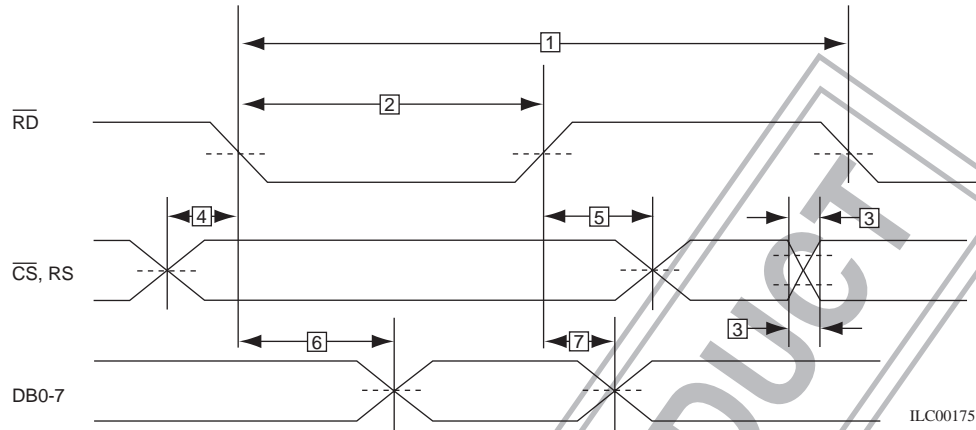


Figure2. Current dissipation measuring circuit at stand-by mode

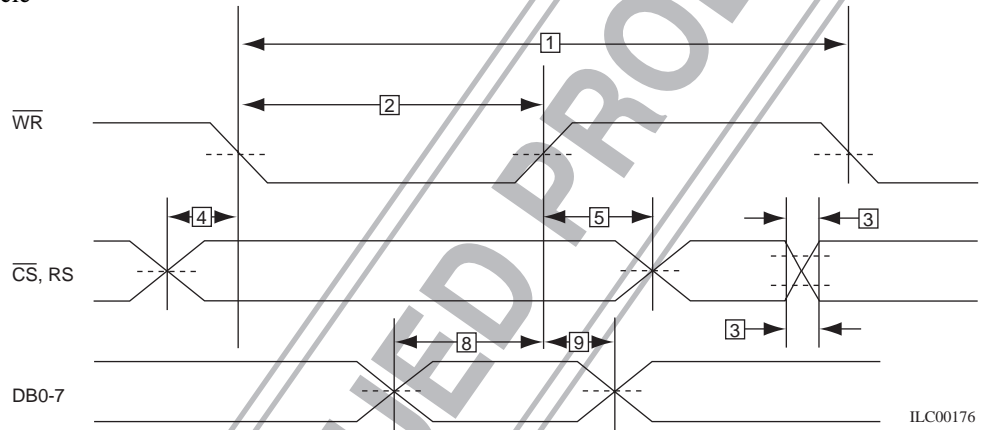
ILC00174

4. AC Characteristics at Ta= -30°C to +70°C, VSS=0V

(1) MPU Interface
1. Reading cycle



2. Writing cycle

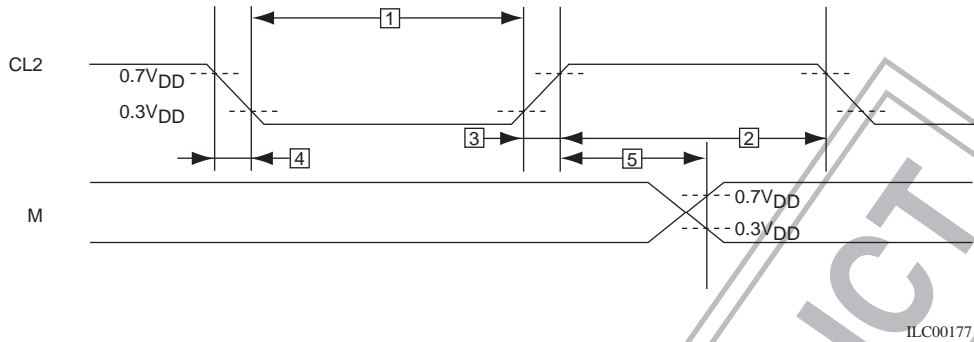


No.	Item	Symbol	Conditions	Value		unit
				VDD [V]	min. max.	
1	RD, WR cycle time	tcyc1	RD	4.5 to 6.0	(500)	ns
			2.5 to 4.5			
		tcyc2	WR	4.5 to 6.0	(500)	ns
			2.5 to 4.5			
2	RD pulse width WR pulse width	tpw1	RD	4.5 to 6.0	(220)	ns
			WR	2.5 to 4.5		
3	Rise / fall time	tr1, tf1	RD	4.5 to 6.0	(20)	ns
			2.5 to 4.5			
4	Address set-up time	tAS1	CS, RS, RD	4.5 to 6.0	(40)	ns
			2.5 to 4.5			
		tAS2	CS, RS, WR	4.5 to 6.0	(40)	ns
			2.5 to 4.5			
5	Address hold time	tAH1	CS, RS, RD	4.5 to 6.0	(10)	ns
			2.5 to 4.5			
		tAH2	CS, RS, WR	4.5 to 6.0	(10)	ns
			2.5 to 4.5			
6	Data delay time	tDDR1	RD, DB0 to DB7, CL=50pF	4.5 to 6.0	(120)	ns
			2.5 to 4.5			
7	Data hold time	tDHR1	RD, DB0 to DB7, CL=50pF	4.5 to 6.0	(20)	ns
			2.5 to 4.5			
8	Data set-up time	tDSW1	WR, DB0 to DB7, CL=50pF	4.5 to 6.0	(60)	ns
			2.5 to 4.5			
9	Data hold time	tDHW1	WR, DB0 to DB7, CL=50pF	4.5 to 6.0	(10)	ns
			2.5 to 4.5			

CL=Load capacitance

LC868900/10/50/60

(2) Display Control Timing / Ta= -30°C to +70°C, VSS=0V



No.	Item	Symbol	Conditions	Value		unit
				VDD [V]		
1	Low level pulse width	tWLCL2	LC2	4.5 to 6.0	(800)	ns
				2.5 to 4.5		
2	High level pulse width	tWLCL2	LC2	4.5 to 6.0	(800)	ns
				2.5 to 4.5		
3	Rise time	tr	CL2	4.5 to 6.0	(20)	ns
				2.5 to 4.5		
4	Fall time	tf	CL2	4.5 to 6.0	(20)	ns
				2.5 to 4.5		
5	M delay time	tDM	M	4.5 to 6.0	(60)	ns
				2.5 to 4.5		

DISCONTINUED PRODUCT

Functions

1. Display Control instructions

- Display is controlled by writing data into the instruction register and 10 data registers.
- The instruction register and the data register are distinguished by the RS signal.
- First, write 4-bit data into the instruction register when RS=1, then specify the code of the data register. Next, with RS=0, write 8-bit data in the data register, which executes the specified instruction.
- A new instruction cannot be accepted while an old instruction is being executed. As the BUSY flag is set under this condition, write an instruction only after reading the BUSY flag and making sure that it is '0'.
- The BUSY flag does not change when data is written into the instruction register (RS=1). The flag is set when the data is written into the data register at RS=0. Therefore, the BUSY flag need not be checked immediately after writing data into the instruction register.

<< **Instruction register and 10 data registers** >>

1. Set display mode

Write code '00H' (in hexadecimal notation) into the instruction register and specify the mode control register.

REGISTER	R / W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction	0	1	0	0	0	0	0	0	0	0
MODE	0	0	0	0	0	-	Mode data (MODE)			

- **MODE0** bit0 of MODE
MODE0=1 : Screen1 display ON
MODE0=0 : Screen1 display OFF
- **MODE1** bit1 of MODE
MODE1=1 : Screen2 display ON
MODE1=0 : Screen2 display OFF
- **MODE2** bit2 of MODE
MODE2=1 : Exclusive-OR display between Screen1 and Screen2
MODE2=0 : OR display between Screen1 and Screen2
- **MODE3** bit3 of MODE
MODE3=1 : Output data right-shift (S1 to S80)
MODE3=0 : Output data left-shift (S80 to S1)

[Note]

- MODE7 to MODE5 must take '0'. A malfunction occurs when one of these bits takes '1'.

2. Set display pitch

Write code '01H' (in hexadecimal notation) into the instruction register and specify the Display Pitch register.

REGISTER	R / W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction	0	1	0	0	0	0	0	0	0	1
PITCH	0	0	-	-	-	-	-	Dp-1		

- Dp indicates how many bits (or dots) from RAM appear in a 1-byte display.
- Dp must take one of the following three value.

Dp	DB2	DB1	DB0	Display pitch
6	1	0	1	6
7	1	1	0	7
8	1	1	1	8

3. Set display number

Write code '02H' (in hexadecimal notation) into the instruction register and specify the Display Number register.

REGISTER	R / W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction	0	1	0	0	0	0	0	0	1	0
NUMBER	0	0	-	-	-	-	Dn-1			

- Dn indicates the number of bytes in the horizontal direction.
- The total number of dots positioned horizontally on the screen, N is given by the following formula.

$$N = Dp * Dn \quad (N \leq 80)$$

- Numbers in the range 2 to 10 (in decimal) can be set as Dn.

4. Set number of time division

Write code '03H' (in hexadecimal notation) into the instruction register and specify the Time Division register.

REGISTER	R / W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction	0	1	0	0	0	0	0	0	1	1
Division	0	0	0	Nx-1						

- Nx represents the number of time divisions.
- Consequently, 1 / Nx is the display duty.
- Numbers in the range 2 to 65 (in decimal) can be set as Nx.

5. Set screen1 display start address

Write code '08H' (in hexadecimal notation) into the instruction register and specify the Screen1 Start Address register.

REGISTER	R / W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction	0	1	0	0	0	0	1	0	0	0
Screen1	0	0	0	Screen1 Start Address						

- This instruction writes the display-start upper address value in the Screen1 Start Address register.
- The display start address is the RAM address at which data to be displayed at the leftmost position (MODE3=0) or the rightmost position (MODE3=1) of the top line of the screen is stored.

MODE3=1 : Start the rightmost position
 MODE3=0 : Start the leftmost position

- The start upper address counter is a 7-bit down-counter with preset function. The start upper address is decremented by one when a start lower address has an underflow. When the start upper address is decremented during 0 state, it is set the start address value automatically.

Internal RAM=1280 bytes : Start upper address counter=7FH
 Internal RAM= 640 bytes : Start upper address counter=3FH

6. Set screen2 display start address

Write code '09H' (in hexadecimal notation) into the instruction register and specify the Screen2 Start Address register.

REGISTER	R / W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction	0	1	0	0	0	0	1	0	0	1
Screen2	0	0	0	Screen2 Start Address						

- This instruction writes the display-start upper address value in the Screen2 Start Address register.
- The display start address is the RAM address at which data to be displayed at the leftmost position (MODE3=0) or the rightmost position (MODE3=1) of the top line of the screen is stored.

MODE3=1 : Start the rightmost position
 MODE3=0 : Start the leftmost position

- The start upper address counter is a 7-bit down-counter with preset function. The start upper address is decremented by one when a start lower address has an underflow. When the start upper address is decremented during 0 state, it is set the start address value automatically.

Internal RAM=1280 bytes : Start upper address counter=7FH
 Internal RAM= 640 bytes : Start upper address counter=3FH

7. Set cursor (lower) address (RAM read/write lower address)

Write code '0AH' (in hexadecimal notation) into the instruction register and the lower cursor address register.

REGISTER	R / W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction	0	1	0	0	0	0	1	0	1	0
Lower	0	0	0	0	0	0	Lower cursor address			

- This instruction writes the cursor address value in the cursor address counter. The cursor address indicates the address for exchanging display data with display RAM. In other words, data at the address specified by the cursor address is read from or written into display RAM. The cursor address is divided into a lower address (4 bits).

The cursor lower address counter is a 4-bit down-counter with preset function. The cursor lower address is decreased by one every RAM read/write timing. When the cursor lower address is decreased during 0 state, it is set Dn-1 automatically.

8. Set cursor (upper) address (RAM read / write upper address)

Write code '0BH' (in hexadecimal notation) into the instruction register and the upper cursor address register.

REGISTER	R / W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction	0	1	0	0	0	0	1	0	1	1
Upper	0	0	0	Upper cursor address						

- This instruction writes the cursor address value in the cursor address counter. The cursor address indicates the address for exchanging display data with display RAM. In other words, data at the address specified by the cursor address is read from or written into display RAM. The cursor address is divided into an upper address (7 bits).

The cursor upper address counter is a 7-bit down-counter with preset function. The cursor upper address is decreased by one when cursor lower address has an underflow. When the cursor upper address is decreased during 0 state, it is set cursor upper address number automatically.

9. Writing display data

Write code '0EH' (in hexadecimal notation) into the instruction register.

REGISTER	R / W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Instruction	0	1	0	0	0	0	1	1	1	0	
RAM	0	0	MSB							LSB	

- After writing code '0EH', write 8-bit data with RS=0, and the data is written into RAM as display data at the address specified by the cursor address counter. After writing, the count of the cursor address counter decrements by one.

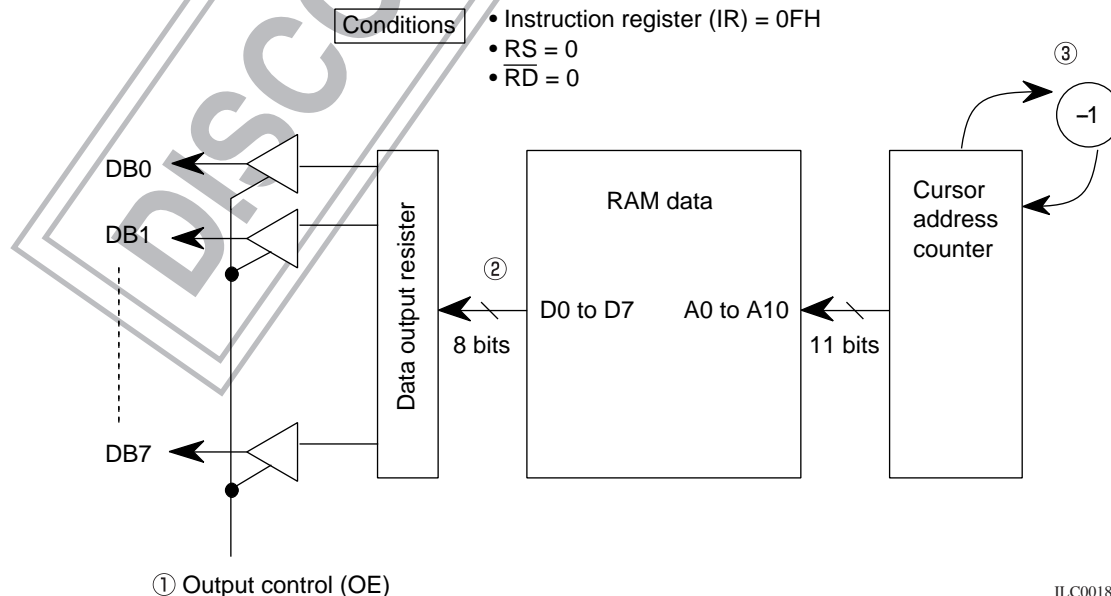
10. Reading display data

Write code '0FH' (in hexadecimal notation) into the instruction register.

REGISTER	R / W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Instruction	0	1	0	0	0	0	1	1	1	1	
RAM	1	0	MSB							LSB	

The read status is established with RS=0, and data in RAM can be read. The procedure for reading data is as follows:

1. The instruction outputs the contents of the data output register to DB0 to DB7.
2. Transfer the RAM data indicated by the cursor address to the data output register.
3. It then decrements the cursor address by one. Refer to next figure.



- The correct data cannot be read in the first read operation. The specified value is output in the second read operation. Accordingly, a dummy read operation must be performed once when reading data after setting the cursor address.

11. Read Busy flag

REGISTER	R / W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction	0	1	0	0	0	0	1	1	1	1
Busy	1	1	1 / 0	no meaning						

- The Busy flag is output to DB7 when read mode is established with RS=1. The Busy flag is set to 1 while any of the instructions (1) through (10) is being executed. It is set to 0 at the completion of the execution, allowing the next instruction to be accepted. No other instruction can be accepted when the Busy flag is 1. Accordingly, before writing an instruction and data, it is necessary to ensure that the Busy flag is 0. However, the next instruction can be executed without checking the Busy flag when the maximum read cycle time or the write cycle time has been exceeded after execution of the previous data read instruction or the data write instruction.

The Busy flag does not change when data is written into the instruction register (RS=1).

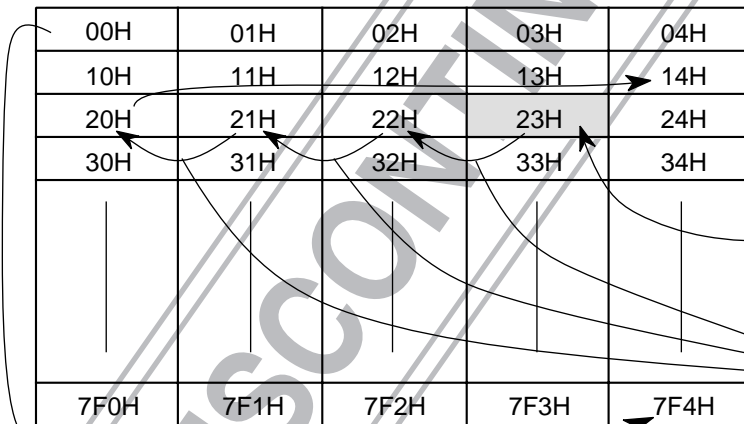
This flag is set when data is written into the data register (RS=0). Therefore, the Busy flag need not be checked immediately after writing data into the instruction register. Specification of the instruction register is unnecessary to read the Busy flag.

ex.) Writing (reading) data to display RAM

- Lower cursor address (CAL) = 03H
- Upper cursor address (CAH) = 02H
- Display number (Dn) = 05H
- Internal RAM size = 1280 bytes

• If writing operation is executed when the CAL counter is '0', the CAH counter is decremented by 1 after writing operation. The CAL counter is set to (Dp -1).

RAM Address



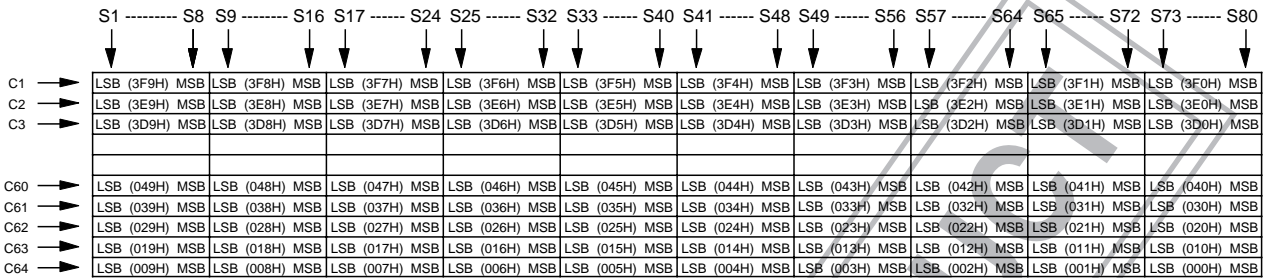
• Specification by the cursor address
First of all, data is written this RAM address.

• Decrement by 1 after writing operation.

• If writing operation is executed when the cursor address is '00H', the address specified by the internal RAM size is set to the CAH counter after writing operation.
Internal RAM size 1280 bytes --> 7FH
Internal RAM size 640 bytes --> 3FH
The CAL counter is set to (Dp -1).

Display examples

1. Mode control register=01H (screen1 : ON, screen2 : OFF, S80 → S1)
 Dp=8, Dn=10, Nx=64, Screen1 start address register=3FH



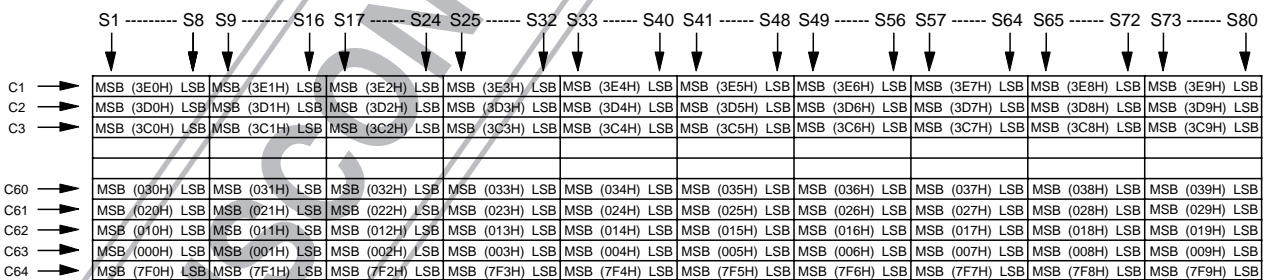
ILC00182

2. Mode control register=09H (screen1 : ON, screen2 : OFF, S1 → S80)
 Dp=8, Dn=10, Nx=64, Screen1 start address register=3FH



ILC00183

3. Mode control register=09H (screen1 : ON, screen2 : OFF, S1 → S80)
 Dp=8, Dn=10, Nx=64, Screen1 start address register=3EH
 Internal display RAM : 1280 bytes



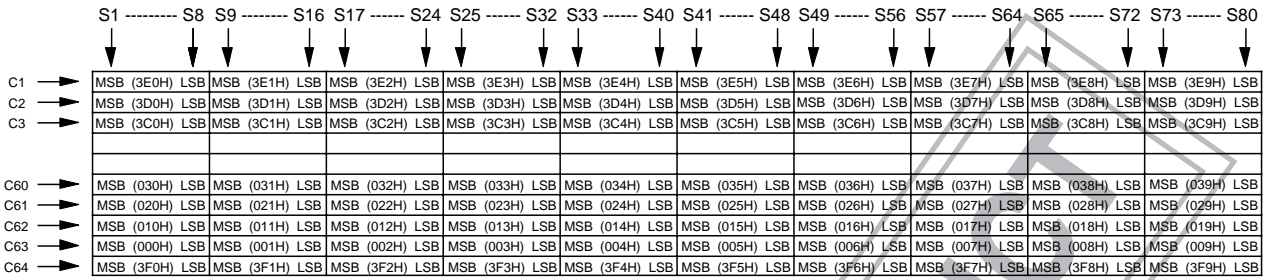
ILC00184

LC868900/10/50/60

4. Mode control register=09H (screen1 : ON, screen2 : OFF, S1 → S80)

Dp=8, Dn=10, Nx=64, Screen1 start address register=3EH

Internal display RAM : 640 bytes

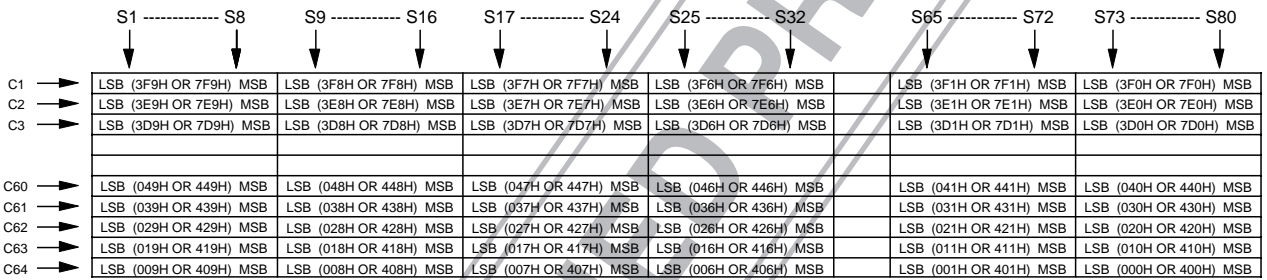


ILC00185

5. Mode control register=03H (screen1 : ON, screen2 : ON, logical or output of screen1 and screen2, S80 → S1)

Dp=8, Dn=10, Nx=64, Screen1 start address register=3FH

Screen2 start address register=7FH, Internal display RAM : 1280 bytes

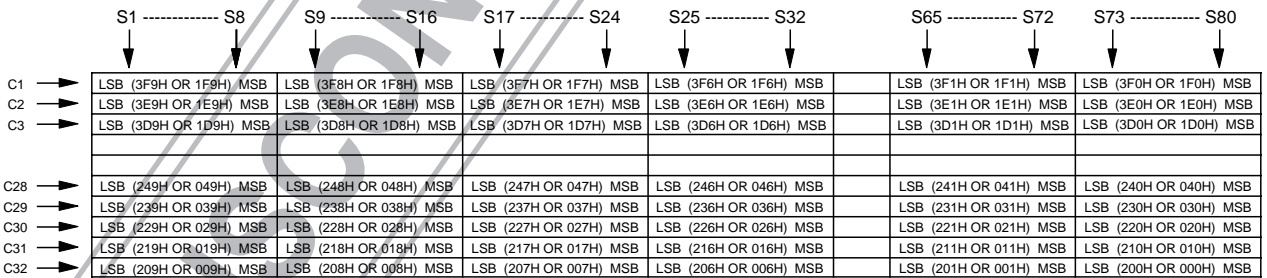


ILC00186

6. Mode control register=03H (screen1 : ON, screen2 : ON, logical or output of screen1 and screen2, S80 → S1)

Dp=8, Dn=10, Nx=32, Screen1 start address register=3FH

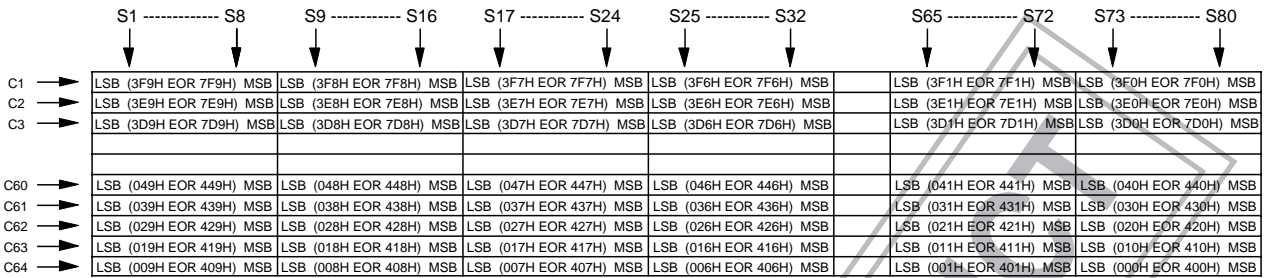
Screen2 start address register=1FH, Internal display RAM : 640 bytes



ILC00187

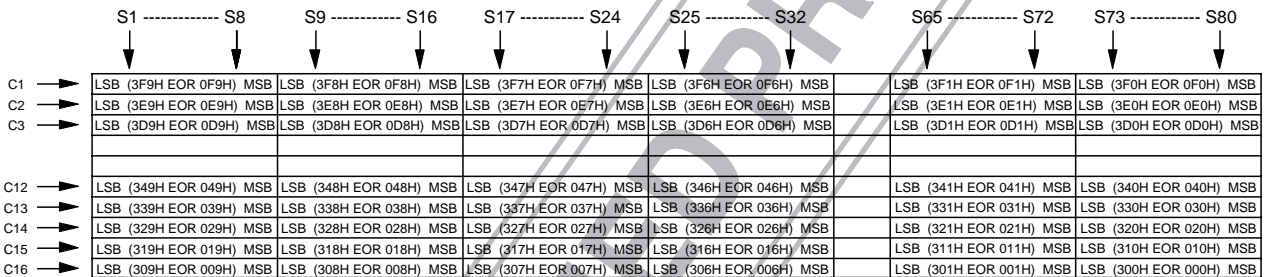
LC868900/10/50/60

7. Mode control register=07H (screen1 : ON, screen2 : ON, exclusive-OR output of screen1 and screen2, S80 → S1)
 Dp=8, Dn=10, Nx=64, Screen1 start address register=3FH
 Screen2 start address register=7FH, Internal display RAM : 1280 bytes



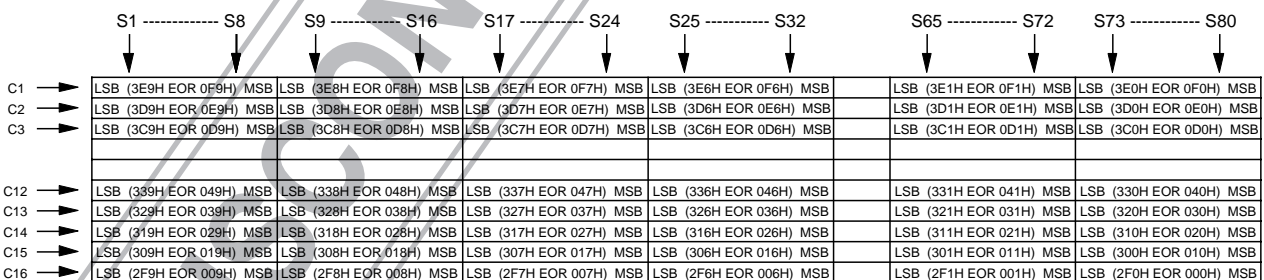
ILC00188

8. Mode control register=07H (screen1 : ON, screen2 : ON, exclusive-OR output of screen1 and screen2, S80 → S1)
 Dp=8, Dn=10, Nx=16, Screen1 start address register=3FH
 Screen2 start address register=0FH



ILC00189

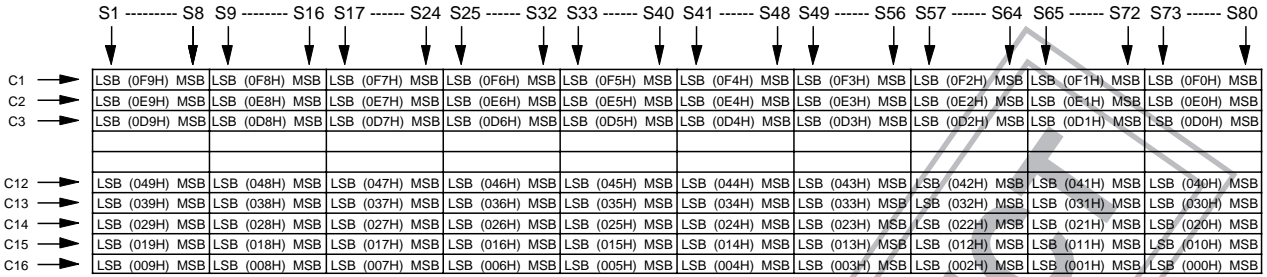
9. Mode control register=07H (screen1 : ON, screen2 : ON, OR output of screen1 and screen2, S80 → S1)
 Dp=8, Dn=10, Nx=16, Screen1 start address register=3EH
 Screen2 start address register=0FH



ILC00190

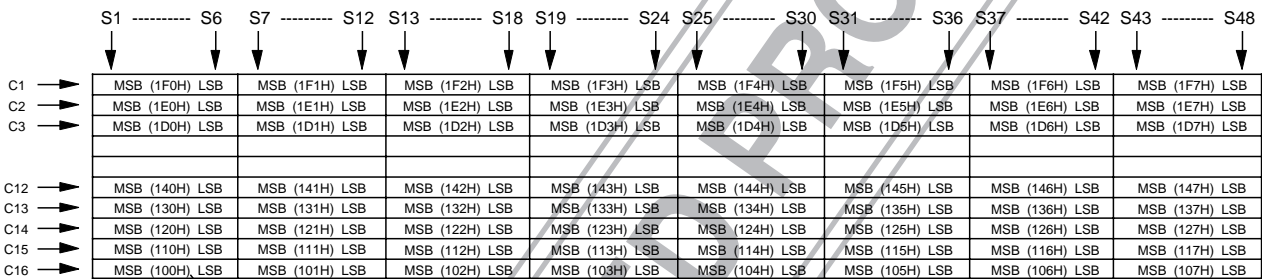
LC868900/10/50/60

10. Mode control register=02H (screen1 : OFF, screen2 : ON, S80 → S1)
 Dp=8, Dn=10, Nx=16, Screen2 start address register=0FH

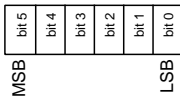


ILC00200

11. Mode control register=09H (screen1 : ON, screen2 : OFF, S1 → S80)
 Dp=6, Dn=8, Nx=16, Screen1 start address register=1FH



In this example, all RAM is constructed like the following.



ILC00201

- Specifications of any and all SANYO products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.
- SANYO Electric Co., Ltd. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO products(including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of SANYO Electric Co., Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only ; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of December, 2000. Specifications and information herein are subject to change without notice.