Ordering number: EN4013A

CMOS LSI

SANYO No. 4013A

LC83015E

Digital Signal Processor for Audio Applications

OVERVIEW

The LC83015E is a digital signal processor IC designed for medium- and high-class home audio systems, such as AV amplifiers, mini, super-mini and car audio component systems.

The LC83015E is part of the LC83010N/NE family. It features an internal ROM, with a large standard program library, an internal RAM for user programs and a wide variety of interface capabilities. The standard program library includes sound-field simulation, theater surround and karaoke programs.

The LC83015E operates from a 5 V supply and is available in 80-pin QFPs.

FEATURES

- 80 ns cycle time at fs = 48 kHz (256 cycles/fs)
- Dual-Harvard architecture allows single-cycle stereo signal integration and playback, with two of each of the following.
  - 24 × 16-bit fixed decimal point multiplier
  - 32-bit arithmetic operation and 24-bit arithmetic logic operation ALU/shifter
  - 32-bit accumulator
  - 8 × 32-bit temporary storage registers
  - 64 × 24-bit internal data RAM
  - 128 × 16-bit internal coefficient RAM
  - 304 × 16-bit internal coefficient ROM
- Large program memory
  - 1024 × 32-bit standard program ROM
  - 256 × 32-bit user program RAM
- Standard program ROM
  - Sound-field simulation library
    - Auditorium simulation
    - Stereo, 3-band graphic equalizer
    - 12-band spectrum analyzer
  - Karaoke function library
    - Pitch shift (realized in program RAM)
    - Vocal mute
    - Microphone echo
- Coefficient ROM
  - Logarithmic conversion coefficients
- Audio interface
  - 2 input channels compatible with a variety of formats
  - 3 output channels compatible with a variety of 32/64fs formats
- External memory interface
  - DRAM interface
    - 120 ns (maximum) RAS access time
    - 1 Mbyte (256 Kbyte × 4) or 256 Kbyte (64 Kbyte × 4)
    - 1 or 2 units

SANYO Electric Co.,Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

- SRAM/ROM interface
  - 100 ns (maximum) address access time
  - 1 Mbyte (128 Kbyte × 8) or 256 Kbyte (32 Kbyte × 8)
  - 1 unit
- Pseudo-SRAM interface
  - 70 ns (maximum) CE access time
  - 1 Mbyte (128 Kbyte × 8) or 256 Kbyte (32 Kbyte × 8)
  - 1 unit
- Maximum external memory access per sampling period
  - 42/32 access for 16- /24-bit, with 2 DRAMs
  - 51/36 access for 16- /24-bit, with 2 SRAM
  - 64/42 access for 16- /24-bit, with 1 pseudo-SRAM

■ Serial microprocessor interface
- 8-bit
- Input and output synchronization control
- 8 × 16-bit LIFO register

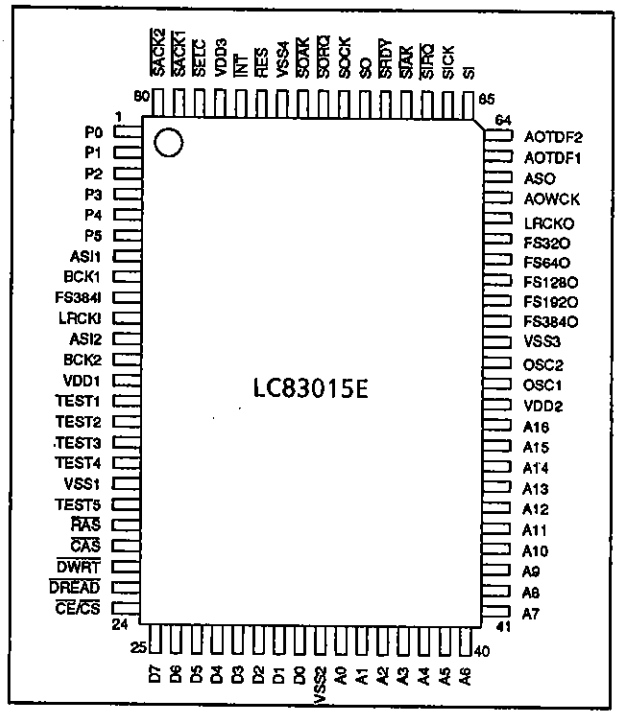
■ Other functions
- Interrupt input
- 4-level stack nesting
- 12-bit interval timer

■ Compatible with LC83EV015 (PGA120) evaluation IC

■ 5 V supply voltage

■ 80-pin QFP

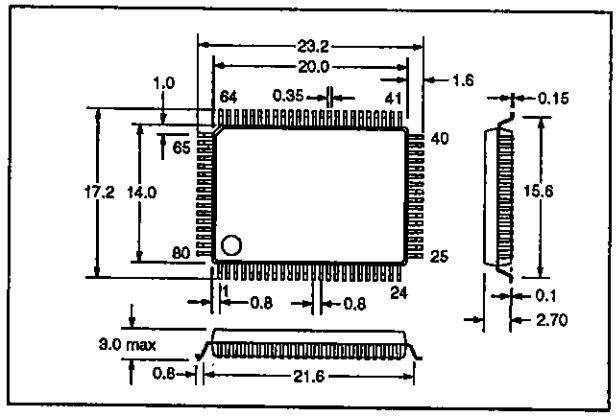
PIN ASSIGNMENT



PACKAGE DIMENSIONS

Unit: mm

3174-QIP80E



PIN DESCRIPTION

Number	Name	Description
1 to 6	P0 to P5	General-purpose input/output port. Internal pull-up resistor
7	ASI1	Audio data serial input 1
8	BCK1	64fs or 32fs bit clock input for ASI1
9	FS384I	384fs or 512fs input
10	LRCKI	Left-/right-channel clock input
11	ASI2	Audio data serial input 2
12	BCK2	64fs or 32fs bit clock input for ASI2
13, 51, 77	VDD1 to VDD3	Supply voltage connections
14 to 17	TEST1 to TEST4	Test inputs. Connect to ground for normal operation.
18, 33, 54, 74	VSS1 to VSS4	Ground connections
19	TEST5	Test output. Leave open for normal operation.
20	$\overline{RAS}$	DRAM interface $\overline{RAS}$ output
21	$\overline{CAS}$	DRAM interface $\overline{CAS}$ output
22	$\overline{DWRT}$	Data write output
23	$\overline{DREAD}$	Data read output
24	$\overline{CE/CS}$	External SRAM or pseudo-SRAM chip enable output
25 to 32	D7 to D0	External memory data bus
34 to 50	A0 to A16	External memory address bus
52	OSC1	Crystal oscillator input. Connect to V_{DD} or V_{SS} when not used.
53	OSC2	Crystal oscillator output. Leave open when not used.
55	FS384O	384fs or 512fs output (Same as FS384I or OSC1/OSC2 clock)
56	FS192O	192fs or 256fs output (1/2 of FS384O)
57	FS128O	128fs output (1/3 or 1/4 of FS384O)
58	FS64O	64fs or 32fs output (BCK1 of 1/2 of FS128O)
59	FS32O	32fs or 16fs output (1/2 of FS64O)
60	LRCKO	1fs output (LRCKI or 1/64 of FS64O)
61	AOWCK	2fs or 1fs output (1/32 of FS64O)
62	ASO	Audio data serial output 1
63	AOTDF1	Audio data serial output 2
64	AOTDF2	Audio data serial output 3
65	SI	8-bit serial data input
66	SICK	SI clock input
67	$\overline{SIRQ}$	Serial data input request input
68	$\overline{SIAK}$	Serial data input acknowledge output

Number	Name	Description
69	$\overline{\text{SRDY}}$	Serial data input ready input
70	SO	8-bit serial data output
71	SOCK	SO clock input
72	$\overline{\text{SORQ}}$	Serial data output request input
73	$\overline{\text{SOAK}}$	Serial data output acknowledge output
75	$\overline{\text{RES}}$	Reset input. Internal pull-up resistor
76	$\overline{\text{INT}}$	Interrupt request input. Internal pull-up resistor
78	$\overline{\text{SELC}}$	Instruction clock source selection input. Internal pull-down resistor
79	$\overline{\text{SACK1}}$	FS384O selection terminal. Internal pull-down resistor
80	$\overline{\text{SACK2}}$	Fs output clock source selection input. Internal pull-down resistor

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD1}, V_{DD2}, V_{DD3}	−0.3 to 7.0	V
Input voltage range	V_I	−0.3 to V_{DD} + 0.3	V
Output voltage range	V_{O1}	−0.3 to V_{DD} + 0.3	V
OSC2 output voltage	V_{O2}	Up to approved oscillator voltage	V
Audio data and external memory interface output current range. See note 1.	I_{O1}	−2 to 4	mA
SO, $\overline{SOAK}$ and $\overline{SIAK}$ output current range	I_{O2}	−2 to 10	mA
P0 to P5 output current range	I_{O3}	−1 to 10	mA
Power dissipation	P_D	700	mW
Operating temperature range	Topr	−30 to 70	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Note

1. Pins ASO, AOTDF1, AOTDF2, FS384O, FS192O, FS128O, FS64O, FS32O, AOWCK, LRCKO, D0 to D7, A0 to A16, $\overline{RAS}$, $\overline{CAS}$, $\overline{DREAD}$, $\overline{DWRT}$ and $\overline{CE/CS}$

Recommended Operating Conditions

V_{SS1} to V_{SS4} = 0 V, T_a = −30 to 70 °C

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD1}, V_{DD2}, V_{DD3}	4.75 to 5.25	V

Electrical Characteristics

V_{DD1} to V_{DD3} = 4.75 to 5.25 V, V_{SS1} to V_{SS4} = 0 V, T_a = −30 to 70 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Current consumption	I_{DD}	25 MHz external clock. See note 8.	–	50	105	mA
Audio data and external memory interface LOW-level input voltage. See note 1.	V_{IL1}		–	–	0.8	V
Audio data and external memory interface HIGH-level input voltage. See note 1.	V_{IH1}		2.4	–	–	V
LOW-level input voltage. See note 2.	V_{IL2}		–	–	$0.3V_{DD}$	V
HIGH-level input voltage. See note 2.	V_{IH2}		$0.7V_{DD}$	–	–	V
Serial interface LOW-level input voltage. See note 3.	V_{IL3}		–	–	$0.25V_{DD}$	V
Serial interface HIGH-level input voltage. See note 3.	V_{IH3}		$0.75V_{DD}$	–	–	V
LOW-level output voltage	V_{OL}	I_{OL} = 2 mA	–	–	0.4	V
		I_{OL} = 10 mA	–	–	1.5	

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
HIGH-level output voltage	V_{OH}	I_{OH} = –0.4 mA	4.0	–	–	V
		I_{OH} = –50 µA	V_{DD} – 1.2	–	–	
$\overline{RES}$ and $\overline{INT}$ LOW-level input current	I_{IL1}	$V_I = V_{SS}$	–250	–	–	µA
P0 to P5 LOW-level input current	I_{IL2}	$V_I = V_{SS}$	–1000	–	–	µA
Other LOW-level input current	I_{IL3}	$V_I = V_{SS}$	–10	–	–	µA
$\overline{SELC}$, $\overline{SACK1}$ and $\overline{SACK2}$ HIGH-level input current	I_{IH1}	$V_I = V_{DD}$	–	–	250	µA
HIGH-level input current	I_{IH2}	$V_I = V_{DD}$	–	–	10	µA
$\overline{RAS}$, $\overline{CAS}$, $\overline{DWRT}$, $\overline{DREAD}$ and $\overline{CE/CS}$ total output current	ΣI_{OA1}		–10	–	10	mA
D0 to D7 and A0 to A16 total output current	ΣI_{OA2}		–20	–	20	mA
Total output current. See note 6.	ΣI_{OA3}		–15	–	15	mA
Total output current. See note 7.	ΣI_{OA4}		–10	–	10	mA
Output leakage current	I_{OFF}		–40	–	40	µA
Input capacitance	C_I		–	–	10	pF

Notes

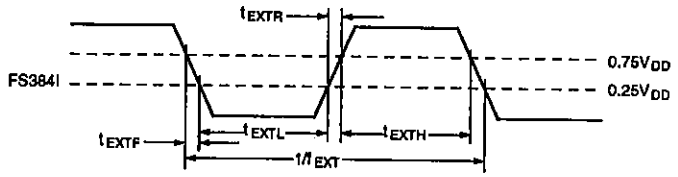
1. Pins BCK1, BCK2, ASI1, ASI2, LRCKI and D0 to D7. Schmitt trigger inputs
2. Pins P0 to P5, TEST1 to TEST4, $\overline{SELC}$, $\overline{SACK1}$ and $\overline{SACK2}$
3. Pins $\overline{RES}$, $\overline{INT}$, SI, SICK, $\overline{SIRQ}$, $\overline{SRDY}$, SOCK, $\overline{SORQ}$, FS384I and OSC1. Schmitt trigger inputs
4. Pins ASO, AOTDF1, AOTDF2, FS384O, FS192O, FS128O, FS64O, FS32O, AOWCK, LRCKO, D0 to D7, A0 to A16, $\overline{RAS}$, $\overline{CAS}$, $\overline{DREAD}$, $\overline{DWRT}$ and $\overline{CE/CS}$. TTL-level outputs
5. Pins $\overline{RAS}$ $\overline{CAS}$, $\overline{DWRT}$, $\overline{DREAD}$ and $\overline{CE/CS}$
6. Pins FS384O, FS192O, FS128O, FS64O, FS32O, LRCKO, AOWCK, ASO and AOTDF1/2
7. Pins $\overline{SIAK}$, $\overline{SRDY}$, SO, $\overline{SOAK}$ and P0 to P5
8. See section DESIGN NOTES for measurement conditions.

System clock

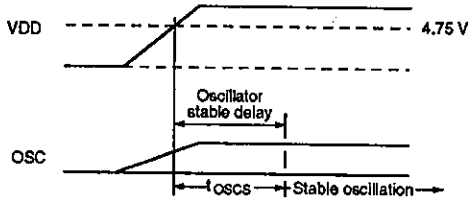
V_{DD1} to V_{DD3} = 4.75 to 5.25 V, V_{SS1} to V_{SS4} = 0 V, T_a = –30 to 70 °C

Parameter	Symbol	Rating			Unit
		min	typ	max	
FS384I external clock frequency	f_{EXT}	12.16	–	24.83	MHz
FS384I external clock LOW- and HIGH-level pulsewidth	t_{EXTL}, t_{EXTH}	16	–	–	ns
FS384I external clock rise and fall time	t_{EXTR}, t_{EXTF}	–	–	9	ns
OSC1/OSC2 crystal oscillator frequency	f_{OSC}	–	–	24.83	MHz
OSC1/OSC2 crystal oscillator stable delay	t_{OSCS}	–	–	100	ms
Operating period	T_{CYC}	79	–	169	ns

External clock timing



Oscillator stable delay time



Audio data interface

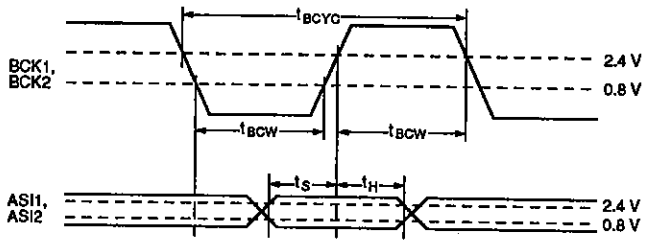
V_{DD1} to V_{DD3} = 4.75 to 5.25 V, V_{SS1} to V_{SS4} = 0 V, T_a = –30 to 70 °C

Parameter	Symbol	Rating			Unit
		min	typ	max	
Input bit clock period	t_{BCYC}	325	–	–	ns
Input bit clock pulsewidth	t_{BCW}	100	–	–	ns
Data setup time	t_S	70	–	–	ns
Data hold time	t_H	70	–	–	ns
Output data propagation delay	t_{OD}	–	–	50	ns
Output data hold time	t_{OH}	0	–	–	ns

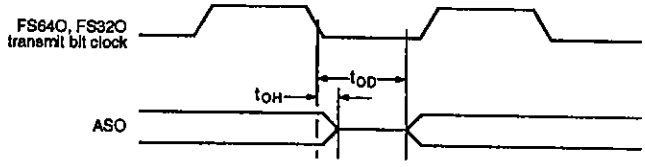
Note

Output timing values are measured with a load capacitance of 50 pF.

Audio data input timing



Audio data output timing



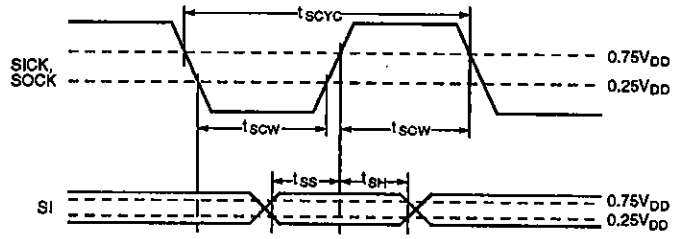
Serial data interface

V_{DD1} to V_{DD3} = 4.75 to 5.25 V, V_{SS1} to V_{SS4} = 0 V, T_a = –30 to 70 °C

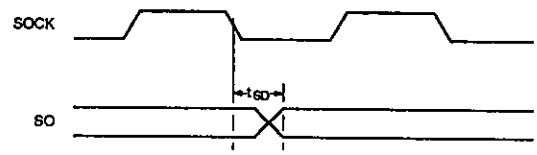
Parameter	Symbol	Rating			Unit
		min	typ	max	
Serial clock period	t_{SCYC}	480	–	–	ns
Serial clock pulsewidth	t_{SCW}	200	–	–	ns
Input data setup time	t_{SS}	70	–	–	ns
Input data hold time	t_{SH}	70	–	–	ns
Output data propagation delay	t_{SD}	–	–	100	ns

Note
Output timing values are measured with a load capacitance of 50 pF.

Serial data input timing



Serial data output timing



External DRAM interface

V_{DD1} to V_{DD3} = 4.75 to 5.25 V, V_{SS1} to V_{SS4} = 0 V, T_a = –30 to 70 °C

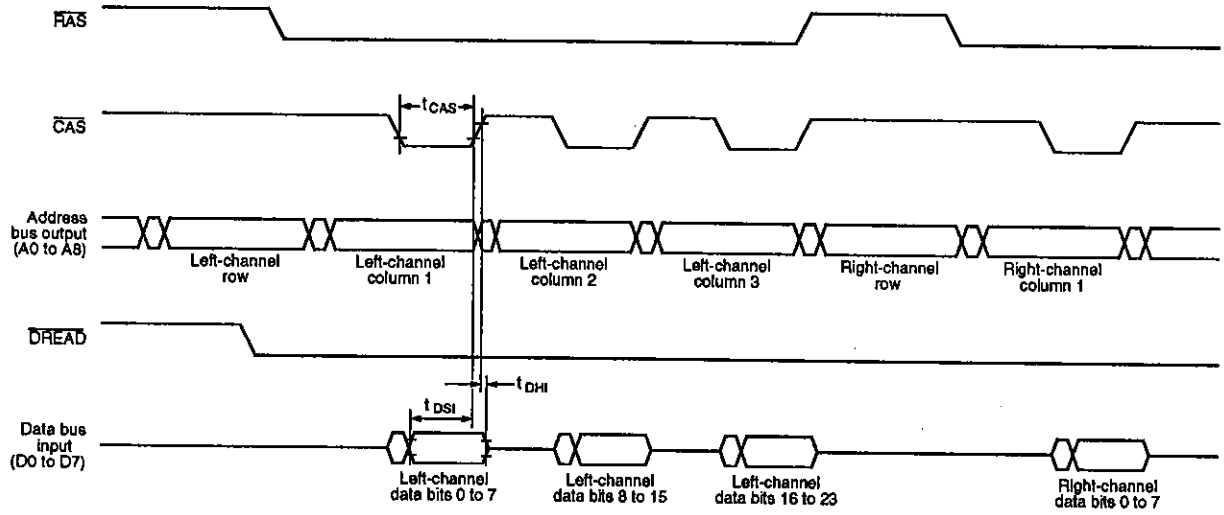
Parameter	Symbol	Rating			Unit
		min	typ	max	
Input data setup time	t_{DSI1}	15	–	–	ns
Input data hold time	t_{DHI1}	0	–	–	ns
$\overline{CAS}$ LOW-level pulsewidth	t_{CAS}	75	–	–	ns
$\overline{CAS}$ HIGH-level pulsewidth	t_{CP}	75	–	–	ns
$\overline{RAS}$ LOW-level pulsewidth	t_{RAS}	350	–	–	ns
$\overline{RAS}$ HIGH-level pulsewidth	t_{RP}	110	–	–	ns
$\overline{CAS}$ period	t_{PC}	160	–	–	ns
$\overline{RAS}$ to $\overline{CAS}$ propagation delay	t_{RCD}	110	–	–	ns
$\overline{CAS}$ hold time	t_{CSH}	190	–	–	ns
$\overline{RAS}$ hold time	t_{RSH}	70	–	–	ns
$\overline{RAS}$ address setup time	t_{ASR}	140	–	–	ns

Parameter	Symbol	Rating			Unit
		min	typ	max	
$\overline{RAS}$ address hold time	t_{RAH}	30	–	–	ns
$\overline{CAS}$ address setup time	t_{ASC}	70	–	–	ns
$\overline{CAS}$ address hold time	t_{CAH}	70	–	–	ns
$\overline{DWRT}$ pulsewidth	t_{WP}	75	–	–	ns
Write command setup time	t_{WCS}	30	–	–	ns
Write command hold time	t_{WCH}	30	–	–	ns
Output data setup time	t_{DSO1}	50	–	–	ns
Outut data hold time	t_{DHO1}	50	–	–	ns

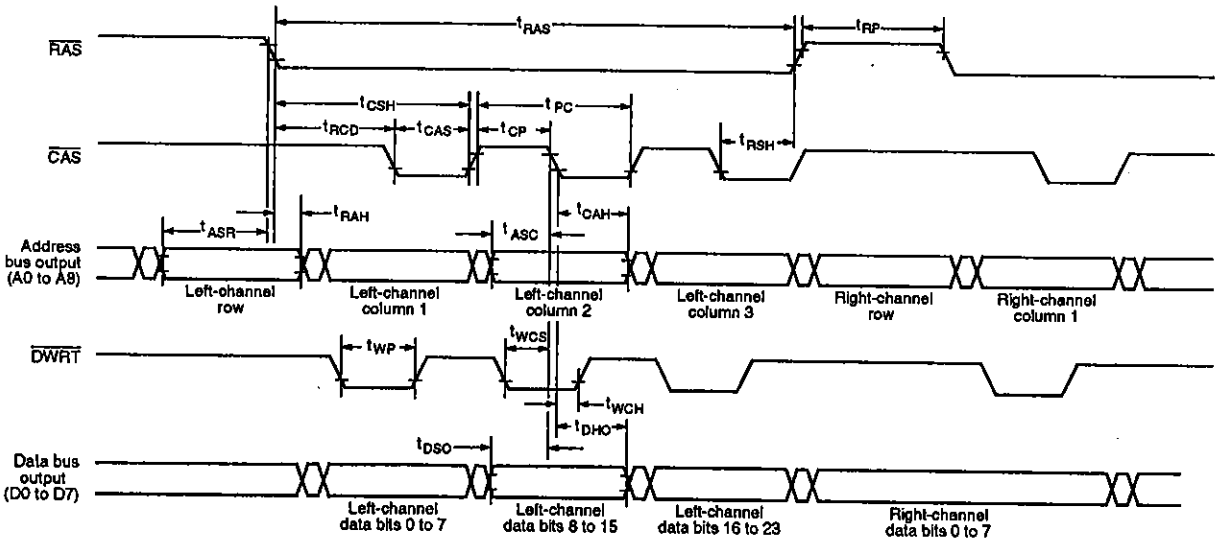
Note

Output timing values are measured with a load capacitance of 50 pF.

External DRAM input timing



External DRAM output timing



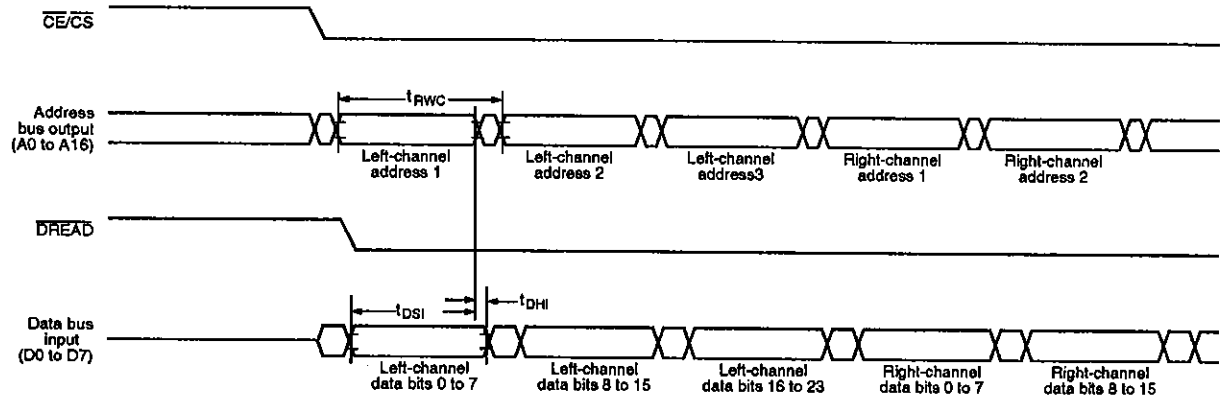
External SRAM interface

V_{DD1} to V_{DD3} = 4.75 to 5.25 V, V_{SS1} to V_{SS4} = 0 V, T_a = −30 to 70 °C

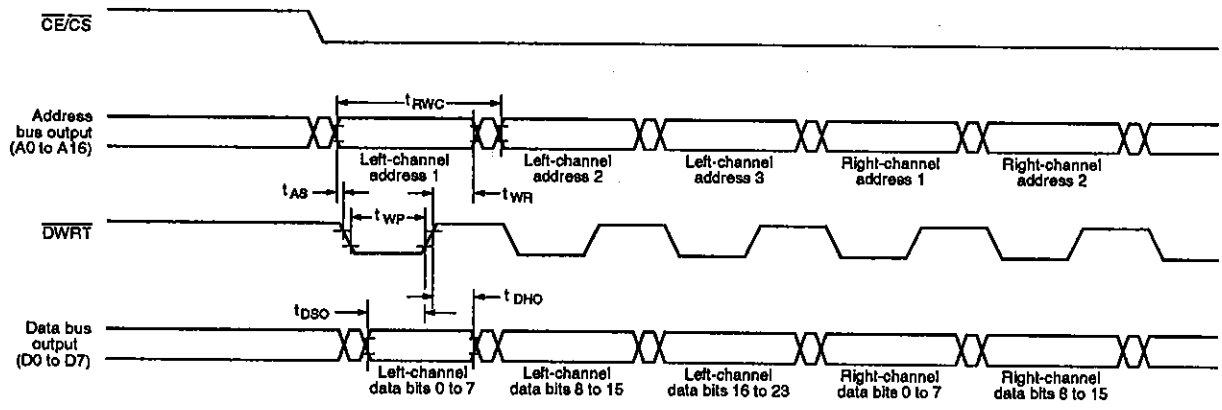
Parameter	Symbol	Rating			Unit
		min	typ	max	
Input data setup time	t_{DSI2}	60	–	–	ns
Input data hold time	t_{DHI2}	0	–	–	ns
Read/write cycle time	t_{RWC}	160	–	–	ns
Address setup time	t_{AS}	10	–	–	ns
Write recovery time	t_{WR}	30	–	–	ns
$\overline{DWRT}$ pulsewidth	t_{WP}	75	–	–	ns
Output data setup time	t_{DSO2}	50	–	–	ns
Outut data hold time	t_{DHO2}	30	–	–	ns

Note
Output timing values are measured with a load capacitance of 50 pF.

External SRAM input timing



External SRAM output timing



External pseudo-SRAM interface

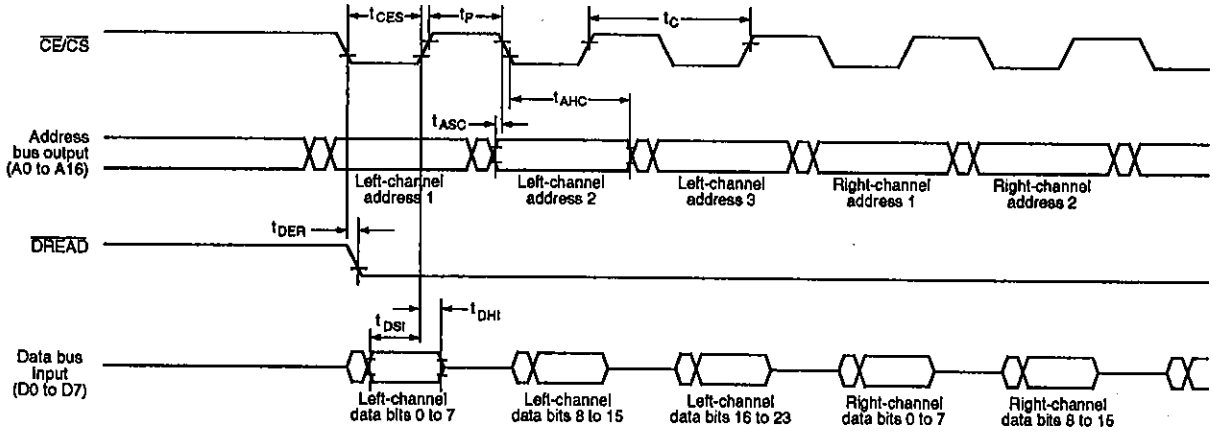
V_{DD1} to V_{DD3} = 4.75 to 5.25 V, V_{SS1} to V_{SS4} = 0 V, T_a = –30 to 70 °C

Parameter	Symbol	Rating			Unit
		min	typ	max	
Input data setup time	t_{DSI3}	10	–	–	ns
Input data hold time	t_{DHI3}	0	–	–	ns
$\overline{CE/CS}$ period	t_C	160	–	–	ns
$\overline{CE/CS}$ pulsewidth	t_{CES}	75	–	–	ns
$\overline{CE/CS}$ pre-charge time	t_P	75	–	–	ns
$\overline{CE/CS}$ address setup time	t_{ASC}	15	–	–	ns
$\overline{CE/CS}$ address hold time	t_{AHC}	100	–	–	ns
Write command hold time	t_{WCH}	70	–	–	ns
Write command read time	t_{CWL}	70	–	–	ns
$\overline{DWRT}$ pulsewidth	t_{WP}	75	–	–	ns
$\overline{DWRT}$ output data setup time	t_{DSW}	50	–	–	ns
$\overline{DWRT}$ output data hold time	t_{DHW}	30	–	–	ns
$\overline{CE/CS}$ output data setup time	t_{DSC}	50	–	–	ns
$\overline{CE/CS}$ output data hold time	t_{DHC}	30	–	–	ns
$\overline{CE/CS}$ to $\overline{DREAD}$ propagation delay	t_{DER}	0	–	30	ns

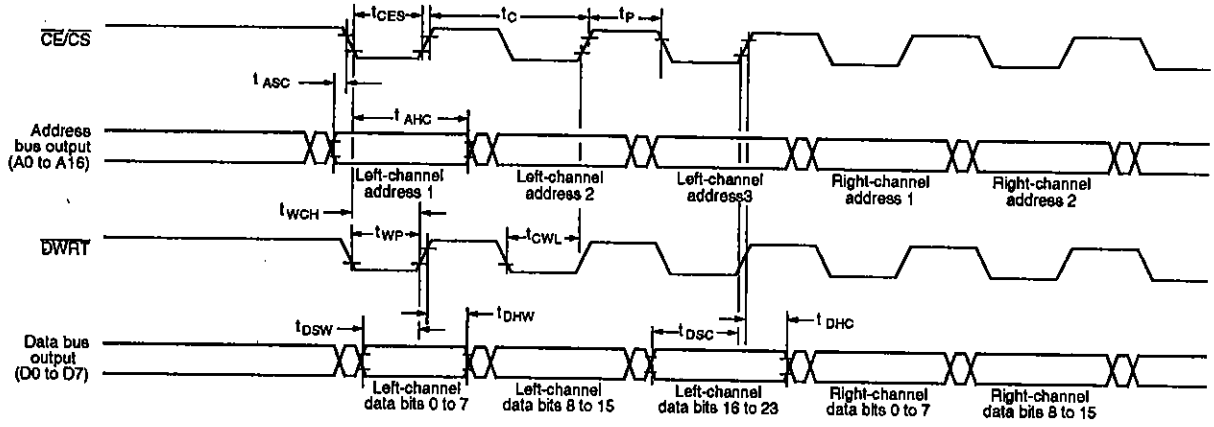
Note

Output timing values are measured with a load capacitance of 50 pF.

External pseudo-SRAM input timing



External pseudo-SRAM output timing



DESIGN NOTES

When $\overline{\text{SELC}}$ is LOW, the LC83015E system clock is generated from FS384I. When $\overline{\text{SELC}}$ is HIGH, it is generated from the free-running oscillator, OSC1. When $\overline{\text{SACK1}}$ is LOW, FS384O output is 1/3 of FS128O output. When $\overline{\text{SACK1}}$ is HIGH, it is 1/4 of FS128O output. When $\overline{\text{SACK2}}$ is LOW, the output clock is generated from FS384I, LRCKI and BCK1. When $\overline{\text{SACK2}}$ is HIGH, it is generated from the free-running oscillator, OSC1.

When the LC83015E is used with one DRAM unit, only D0 to D3 of the data bus are used. When the LC83015E is used with two DRAM units, SRAM or pseudo-SRAM, D0 to D7 are used.

The typical supply current, I_{DD}, is measured with Sanyo Standard Theatre Mode in operation under the input/output conditions shown in figure 1.

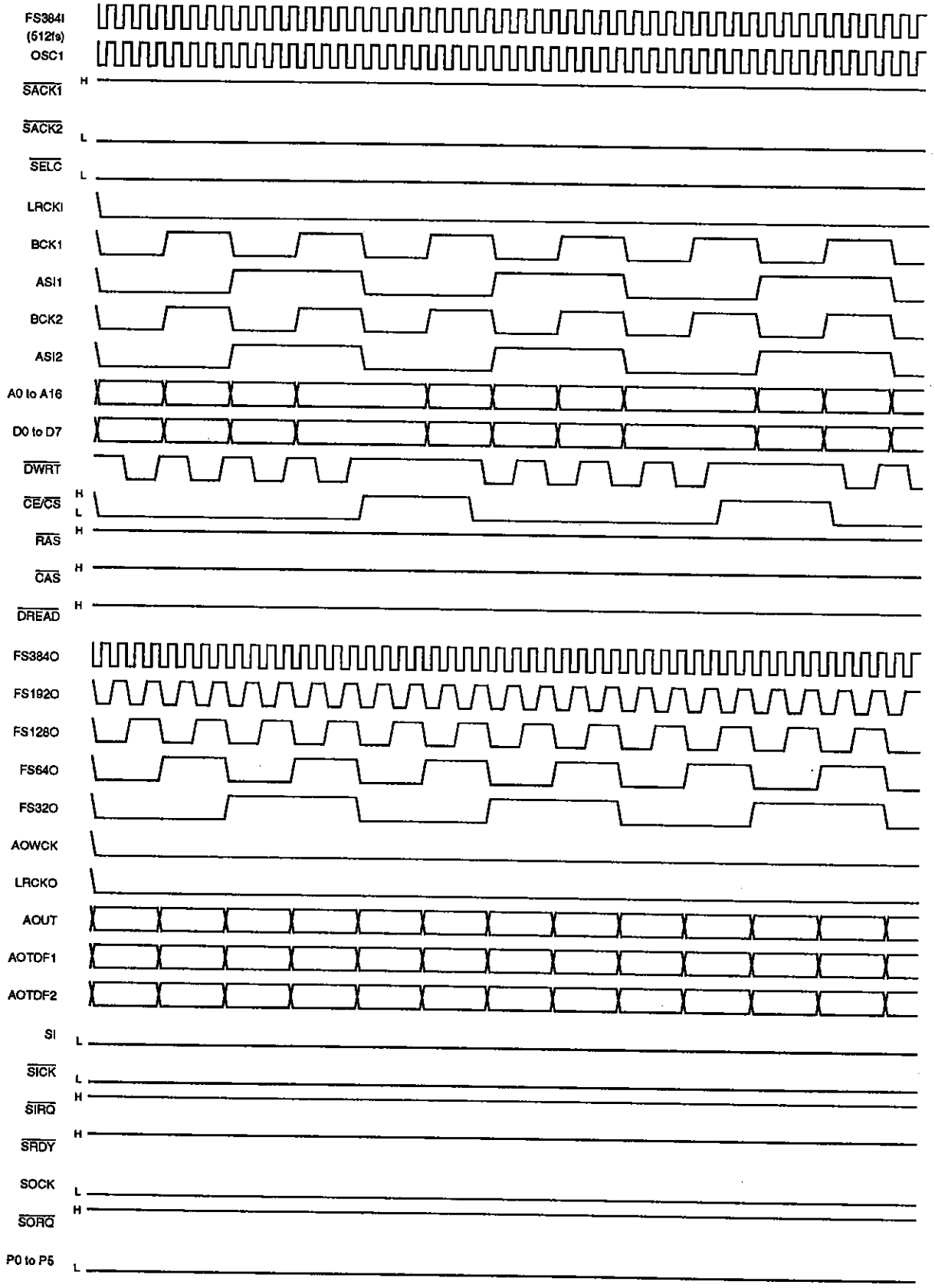


Figure 1. Measurement conditions for I_{DD}

The LC83015E has three voltage supply pins (VDD1 to VDD3) and four ground pins (VSS1 to VSS4). The connections between these pins must conduct sufficiently to ensure that there are no voltage differences between each of the voltage supply pins and each of the ground pins when the device is powered-up. Connections similar to those shown in figure 2 should be used.

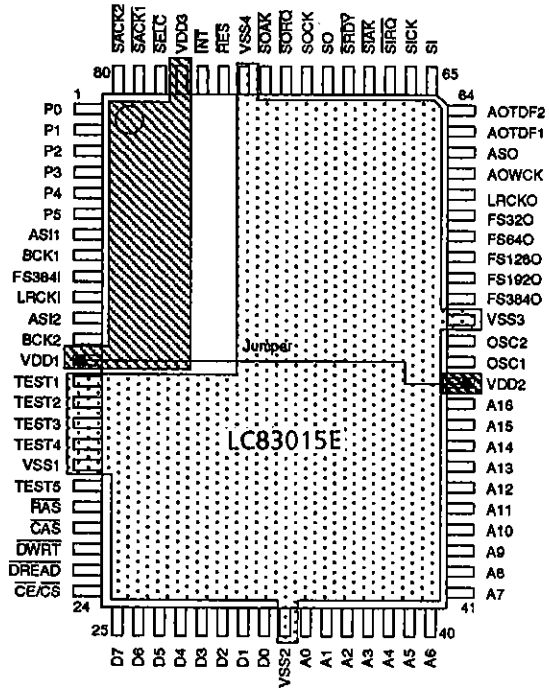


Figure 2. Voltage supply and ground connection template

Figure 3 shows the connection of a crystal oscillator to the LC83015E Table 1 shows oscillator frequencies and capacitances for a Nippon Denpa Kogyo NR-18 crystal oscillator.

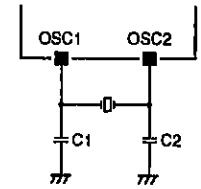


Figure 3. Crystal oscillator connection

Table 1. Oscillator frequency selection

C1, C2 (pF)	Oscillator frequency (MHz)
18	12.288
12	16.9344
10	18.432
12	16.834
8	22.5792
6	24.576

LC83015E Development Environment

The following software tools are available.

- LC83015.EXE assembler
- S83015.EXE debugger and simulator
- STI.EXE ROM sorting software for microprocessor
- STO.EXE ROM sorting software for external ROM

The following hardware tools are intended for use with the LC83015E.

- IBM PC/AT or AX personal computer
- In-Circuit Emulator (ICE) comprising
  - ICE83015
  - POD83
  - IC149-080-021-S5
  - E83015.EXE software
- Simple model evaluation board comprising
  - PRBD15
  - D2SP.EXE software

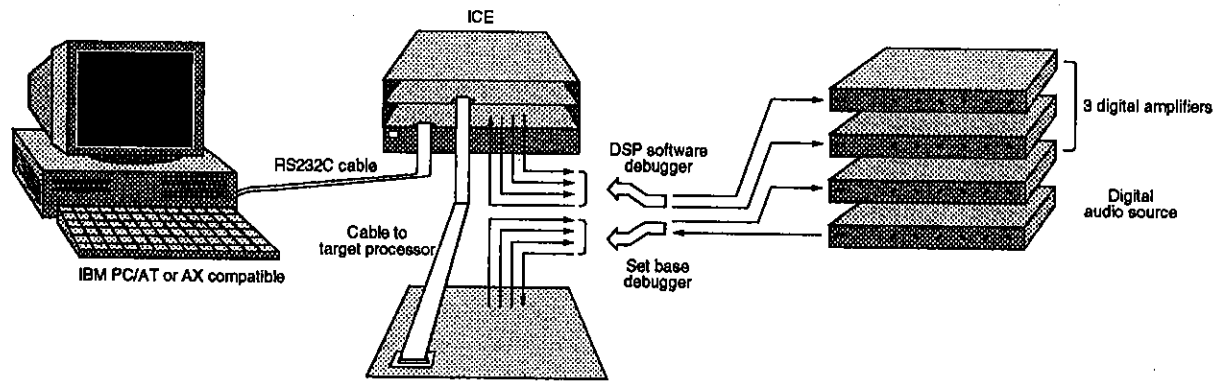


Figure 4. ICE configuration

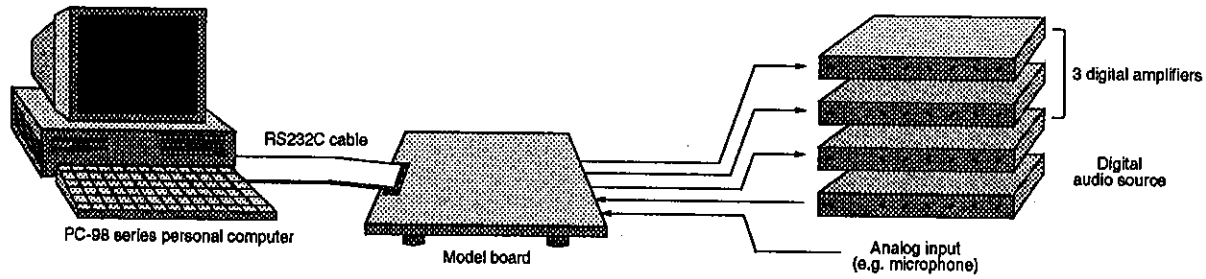
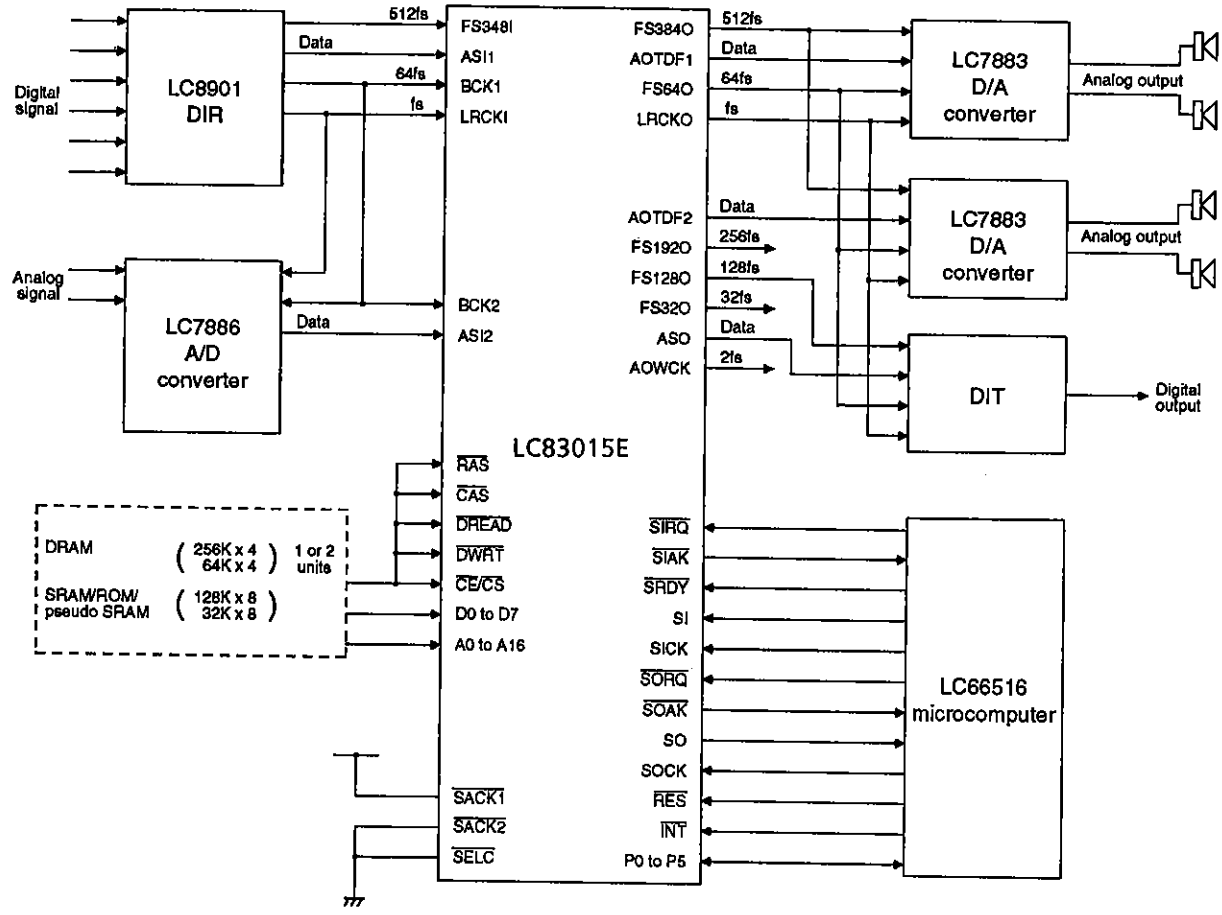


Figure 5. Model board configuration

APPLICATION EXAMPLE



Note

The LC83015E is in external synchronization mode in this application.