Ordering number : EN 2330D

SANYO No.2330D

LC7942A

CMOS LSI

Dot Matrix LCD Drivers

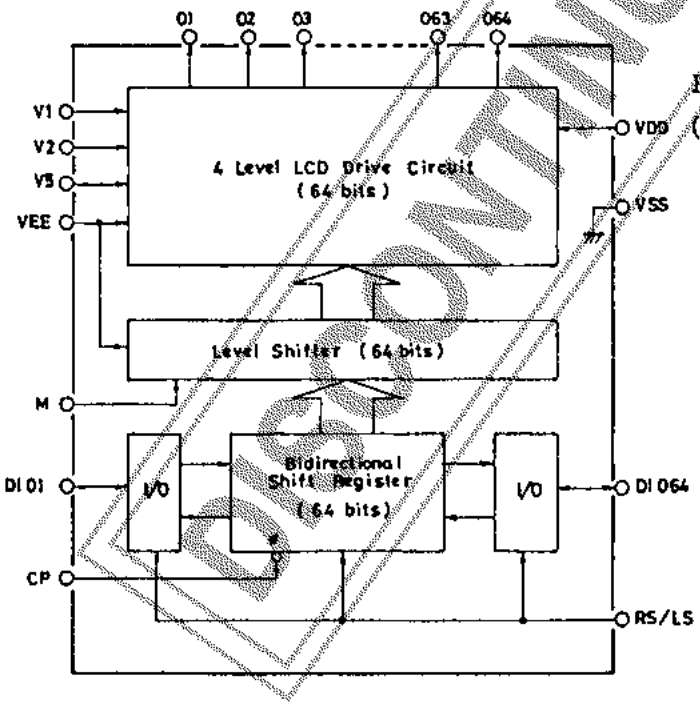
Overview

The LC7942A is a large-scale dot matrix LCD segment driver LSI. The LC7942A contains a 64-bit bidirectional shift register and a 4-level LCD driver. The input/output pins for cascade connection can be used to further increase the number of bits. The LC7942A can be used in conjunction with segment driver LC7940A or LC7941A (QIP100) to drive a wide-screen LCD panel and provide high-density packaging.

Features

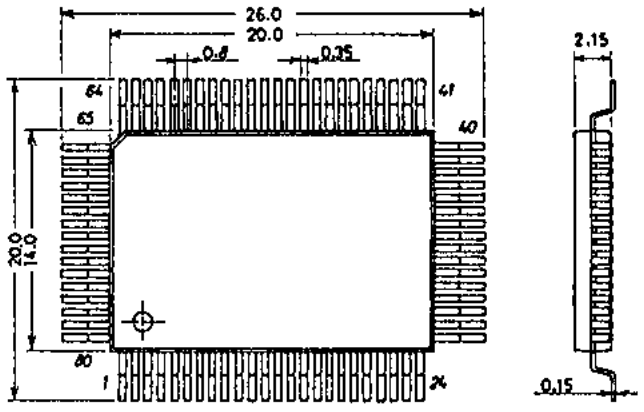
- On-chip LCD drive circuit (64 bits)
- Display duty : 1/64 to 1/128
- On-chip input/output pins used to further increase the number of bits
- Possible to apply the bias voltage externally
- Operating voltage/operating temperature
  V_{DD} (logic section) : 5V ± 10%/ – 20 to + 85°C
  $V_{DD} - V_{EE}$ (LCD section) : V_{DD} to 20V/ – 20 to + 85°C
- CMOS process
- 80-pin flat plastic package

Equivalent Circuit Block Diagram



Package Dimensions 3044B

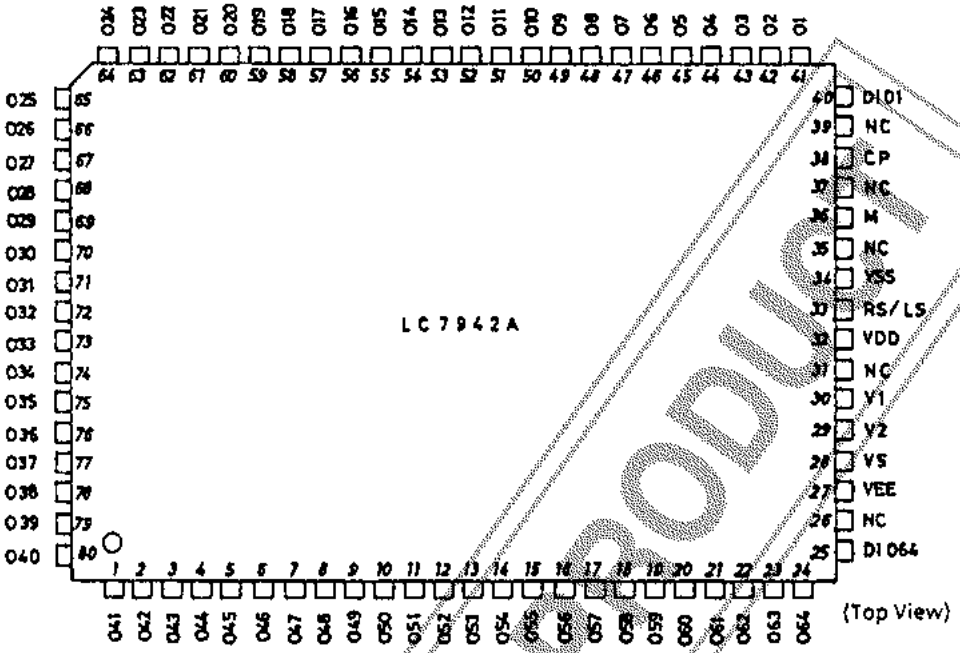
(unit : mm)



SANYO: QIP80A

SANYO Electric Co.,Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10,1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

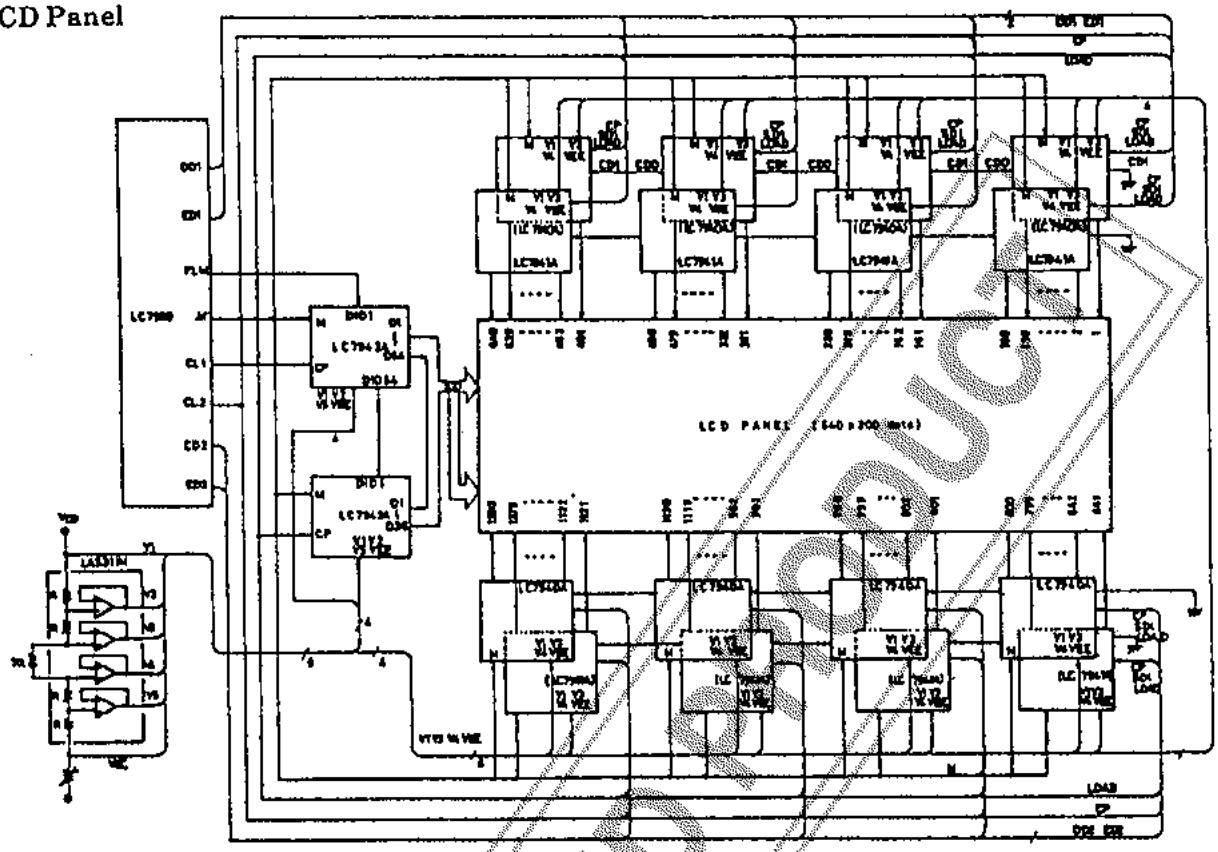
Pin Assignment



Pin Description

Pin Number	Pin Name	Input/ Output	Function
32 34 27	V_{DD} V_{SS} V_{EE}	Power supply	V_{DD} to V_{SS} Power supply for logic section V_{DD} to V_{EE} Power supply for LCD section
30 29 28	V1 V2 V5	Power supply	Power supply for LCD drive level V1, V_{EE} : Select level V2, V5 : Nonselect level
38	CP	Input	Bidirectional shift register shift clock (triggering on the trailing edge)
40 25 33	D_{IL1} D_{IO64} RS/LS	Input/ output Input	RS/LS = L: D_{IO1} Input, D_{IO64} Output, Shift direction O1→O64 RS/LS = H: D_{IO1} Output, D_{IO64} Input, Shift direction O64→O1
36	M	Input	Signal to cause LCD drive ouptut to alternate
41 to 80 1 to 24	O1 to O40 O41 to O64	Output	LCD driver output The combination of scan data and M signal provides the following output levels. Data = "H", M = "H": V1 Data = "H", M = "L": V_{EE} Data = "L", M = "H": V5 Data = "L", M = "L": V2

LCD Panel



Absolute Maximum Ratings at Ta = 25 ± 2°C, V_{SS} = 0V

			unit
Maximum Supply Voltage (LOGIC)	V_{DD} max	−0.3 to +7.0	V
Maximum Supply Voltage (LCD)	$V_{DD} - V_{EE}$ max	0 to 22	V
Maximum Input Voltage	V_I max	−0.3 to V_{DD} + 0.3	V
Operating Temperature	Topg	−20 to +85	°C
Storage Temperature	Tstg	−40 to +125	°C

Note : With $V_{DD} \geq V1 > V2 > V5 > V_{EE}$ held
When mounting the QIP package on the board, do not dip it in solder.

Allowable Operating Conditions at Ta = −20 to +85°C, V_{SS} = 0V

		min	typ	max	unit
Supply Voltage (LOGIC)	V_{DD}	4.5		5.5	V
Supply Voltage (LCD)	$V_{DD} - V_{EE}$	V_{DD}		20	V
Input 'H'-Level Voltage	V_{IH}	0.8V_{DD}			V
Input 'L'-Level Voltage	V_{IL}			0.2V_{DD}	V
CP (Shift Clock)	f_{CP}			1	MHz
CP Pulse Width	t_{WC}	125			ns
Setup Time	t_{SETUP}	100			ns
Hold Time	t_{HOLD}	100			ns
Rise/Fall Time	t_R			50	ns
	t_F			50	ns

Electrical Characteristics at Ta = 25 ± 2°C, V_{SS} = 0V, V_{DD} = 5V ± 0%

			min	typ	max	unit
Input 'H'-Level Current	I_{IH}	$V_{IN} = V_{DD}$ DIO1,DIO64,CP,M,RS/LS			1	μA
Input 'L'-Level Current	I_{IL}	$V_{IN} = V_{SS}$ DIO1,DIO64,CP,M,RS/LS	−1			μA
Output 'H'-Level Voltage	V_{OH}	I_{OH} = −0.4mA, DIO1,DIO64	V_{DD} − 0.4			V
Output 'L'-Level Voltage	V_{OL}	I_{OL} = 0.4mA, DIO1,DIO64			0.4	V

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			min	typ	max	unit
Driver ON-State Resistance	R_{ON}	$V_{DD}-V_{EE}=18V$, $\lvert V_{DE}-V_O\rvert=0.25V$ (Note) (O1 to O64)			1.5	kΩ
Quiescent Current	I_{DD}	$V_{DD}-V_{EE}=18V$, CP=DC			100	μA
Input Capacitance	C_I	f=1MHz		5		pF

(Note) : $V_{DE}=V_{DD}$ to V_{EE}, $V1=V_{DD}$, $V2=10/11\ (V_{DD}-V_{EE})$, $V5=1/11\ (V_{DD}-V_{EE})$

Switching Characteristics

		min	typ	max	unit
Output Delay Time	t_{PLH}			250	ns
	t_{PHL}			250	ns

Switching Characteristic