Ordering number: EN 4104A

CMOS LSI

No. 4104A

LC7931D

80-channel Liquid-crystal Display Driver

OVERVIEW

The LC7931D is an 80-channel liquid-crystal display segment driver that incorporates an 80-bit, bidirectional shift register and an 80-bit latch for serial-to-parallel conversion.

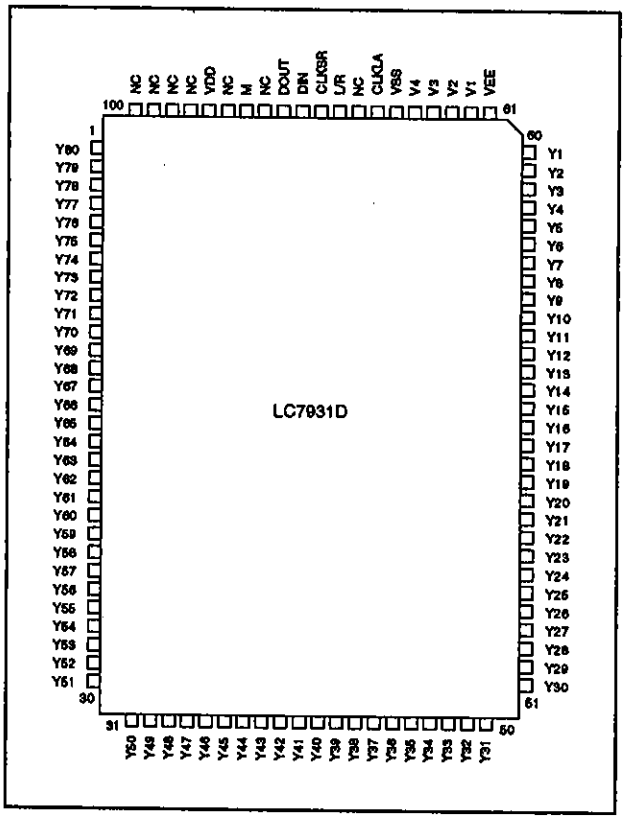
The LC7931D features a maximum drive duty of 1/16. It can interface to a LC7985 LCD controller, a LC86104 4-bit CPU and a LC86108 8-bit CPU.

The LC7931D operates from a 4.5 to 5.5 V supply and is available in 100-pin QIPs.

FEATURES

- 80 liquid-crystal display segment driver outputs
- Bidirectional, 80-bit shift register with single-pin direction control
- 1/16 maximum drive duty
- Compatible with LC7930N interface
- Can interface to LC7985, LC86104 and LC86108.
- 3.0 to 6.0 V driver supply voltage
- 4.5 to 5.5 V logic supply voltage
- 100-pin QIP

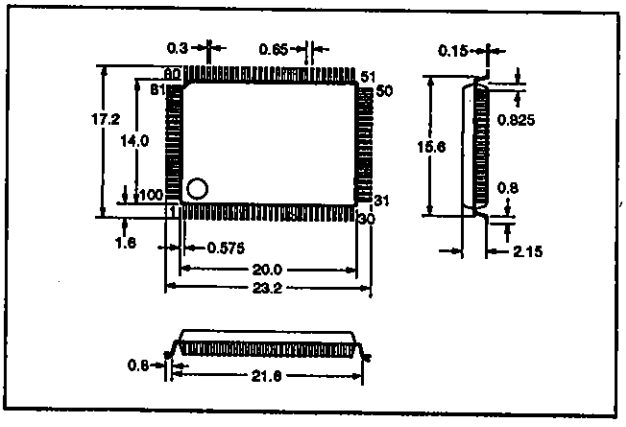
PIN ASSIGNMENT



PACKAGE DIMENSIONS

Unit: mm

3180-QIP100D



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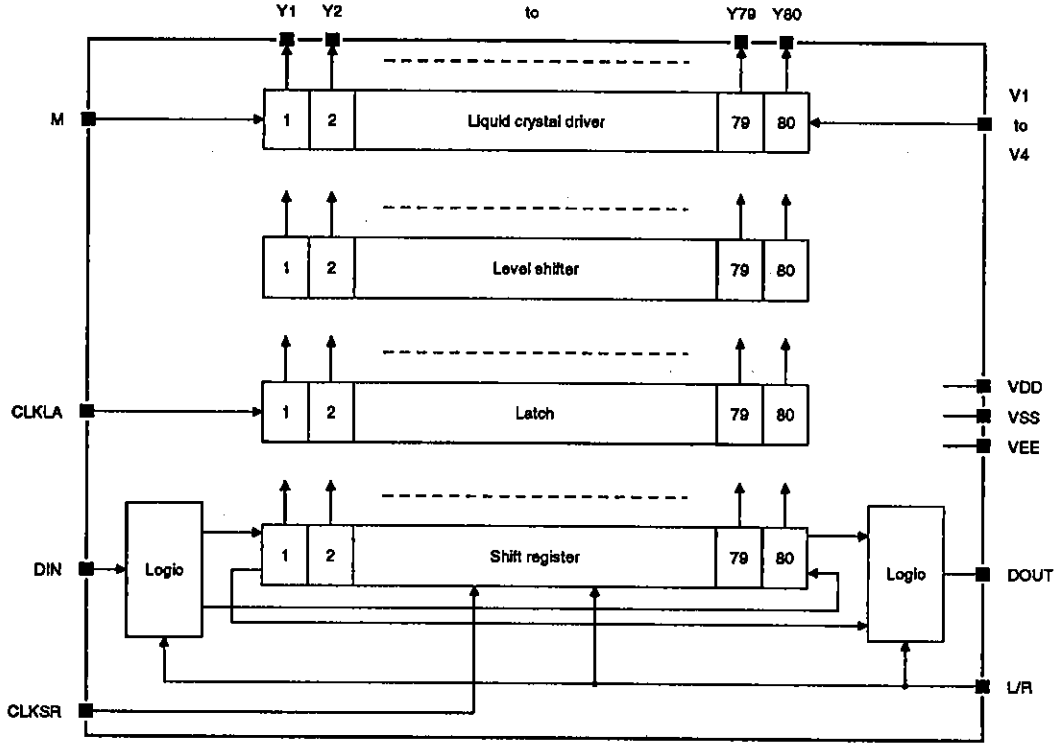
BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	Description
1 to 80	Y80 to Y1	Segment driver outputs
81	VEE	LCD panel ground
82	V1	LCD driver supply voltage 1
83	V2	LCD driver supply voltage 2
84	V3	LCD driver supply voltage 3
85	V4	LCD driver supply voltage 4
86	VSS	Logic circuit ground
87	CLKLA	Latch clock input
88	NC	No connection
89	L/R	Shift register direction control input
90	CLKSR	Shift register clock input
91	DIN	Data input
92	DOUT	Data output
93	NC	No connection
94	M	LCD driver AC control input
95	NC	No connection
96	VDD	Supply voltage
97 to 100	NC	No connection

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Logic supply voltage range	V_{DD}	−0.3 to 7.0	V
LCD driver supply voltage range	$V_{DD} - V_{EE}$	−0.3 to 7.0	V
Input voltage range	V_{I1}	−0.3 to V_{DD} + 0.3	V
V1 to V4 input voltage range	V_{I2}	V_{DD} + 0.3 to V_{EE} − 0.3	V
Power dissipation	P_D	200	mW
Operating temperature range	Topr	−20 to 75	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Recommended Operating Conditions

V_{SS} = 0 V, T_a = 25 °C

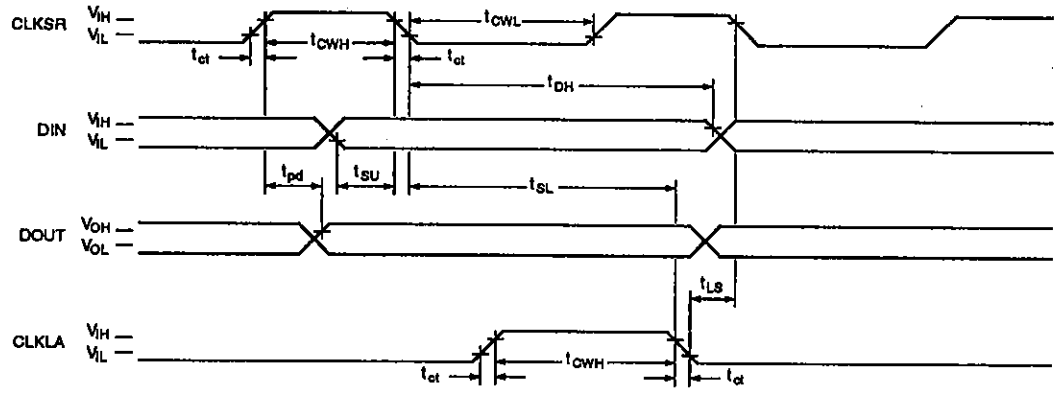
Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{DD}	5	V
Logic supply voltage range	V_{DD}	4.5 to 5.5	V
Driver supply voltage range	$V_{DD} - V_{EE}$	3.0 to 6.0	V

Electrical Characteristics

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, $V_{DD} - V_{EE}$ = 3 to 6 V, T_a = −20 to 75 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply current	I_{DD}	f_{CLKSR} = 1.0 MHz, V_{IL} = V_{SS}, V_{IH} = V_{DD}	–	–	2.0	mA
	I_{EE}	f_{CLKLA} = 2.5 kHz, V_{IL} = V_{SS}, V_{IH} = V_{DD}	–	–	0.1	
CLKLA, CLKSR, M, L/R and DIN LOW-level input voltage	V_{IL}		V_{SS}	–	0.3V_{DD}	V
CLKLA, CLKSR, M, L/R and DIN HIGH-level input voltage	V_{IH}		0.7V_{DD}	–	V_{DD}	V
DOUT LOW-level output voltage	V_{OL}	I_O = 0.4 mA	–	–	0.4	V
DOUT HIGH-level output voltage	V_{OH}	I_O = −0.4 mA	V_{DD} − 0.4	–	–	V
Vi to Yj voltage drop	V_D	i = 1 to 4, j = 1 to 80, one Yj output ON, I_{ON} = 100 µA	–	–	1.1	V
		i = 1 to 4, j = 1 to 80, I_{ON} = 50 µA, all Yj outputs ON	–	–	1.5	
CLKLA, CLKSR, M, DIN and L/R input leakage current	I_{IL}	V_I = V_{SS} to V_{DD}	−5.0	–	5.0	µA
V1 to V4 leakage current	I_V	V_I = V_{EE} to V_{DD}, outputs open	−5.0	–	5.0	µA

Timing Characteristics



$V_{DD} - V_{EE}$ = 3 to 6 V, V_{SS} = 0 V, T_a = −20 to 75 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
CLKSR shift clock frequency	f_{CL}		–	–	1	MHz
CLKSR LOW-level pulsewidth	t_{CWL}		450	–	–	ns
CLKLA and CLKSR HIGH-level pulsewidth	t_{CWH}		450	–	–	ns
DIN data setup time	t_{SU}		100	–	–	ns
CLKSR to CLKLA clock setup time	t_{SL}		200	–	–	ns
CLKLA to CLKSR clock setup time	t_{LS}		200	–	–	ns
DIN data hold time	t_{DH}		100	–	–	ns
CLKLA and CLKSR transition time	t_{ct}		–	–	50	ns
DOUT output propagation delay	t_{pd}	C_L = 30 pF	–	–	250	ns

FUNCTIONAL DESCRIPTION

Shift Register

The input data on DIN is clocked into the shift register and all data in the register is shifted by one bit on the falling edge of the shift register clock, CLKSR. The output bit appears on DOUT on the rising edge of CLKSR. See figure 1.

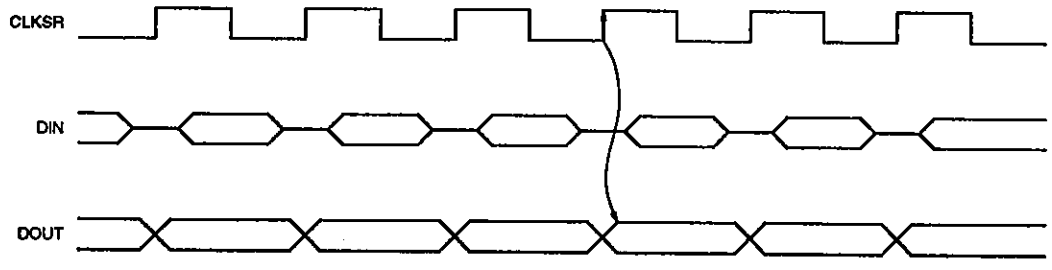


Figure 1. Shift clock timing

Data is shifted to the right (1 to 80) when L/R is LOW, and to the left (80 to 1), when L/R is HIGH, as shown in figures 2 and 3, respectively.

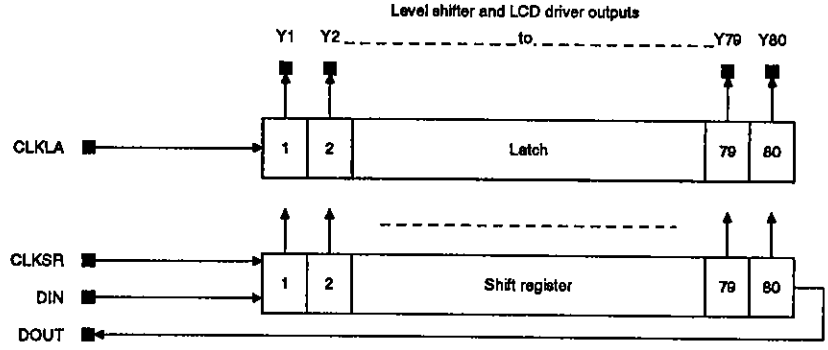


Figure 2. Data shift (L/R = LOW)

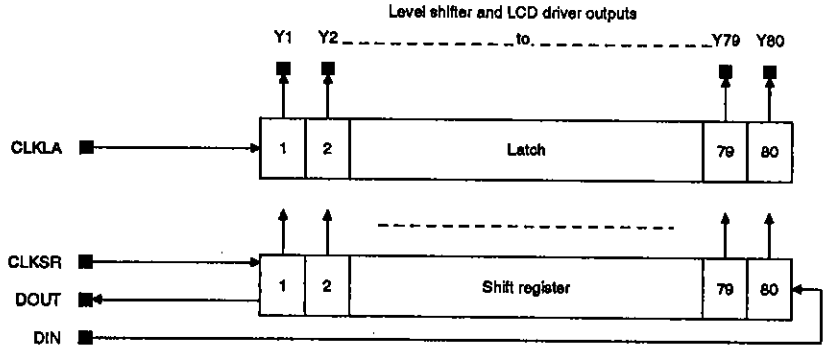


Figure 3. Data shift (L/R = HIGH)

Data is latched and passed to the liquid-crystal display driver level shifter, and the driver outputs change state on the falling edge of the latch clock, CLKLA, as shown in figure 4.

Figure 4. Output driver transition timing

Data is clocked out onto the driver outputs in reverse order (D80 on Y1) when L/R is LOW, and in normal order (D1 on Y1), when L/R is HIGH, as shown in figures 5 and 6, respectively.

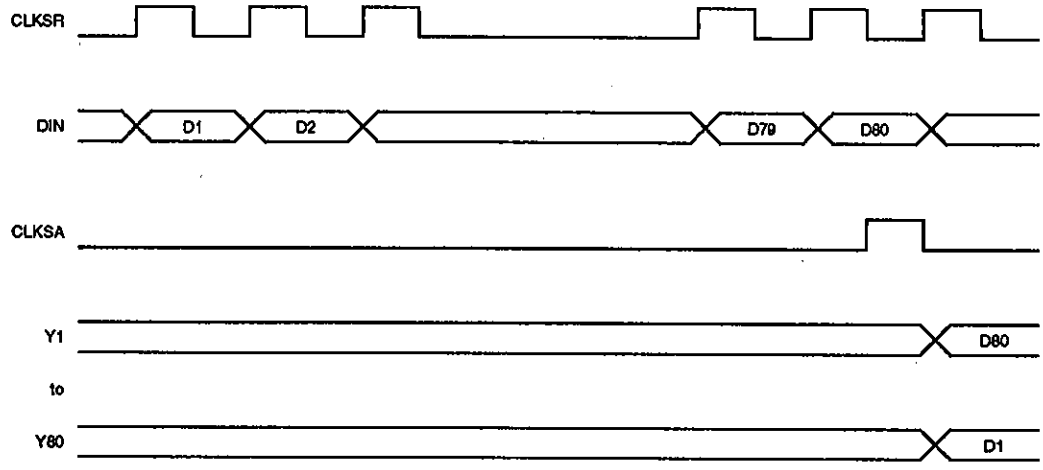


Figure 5. Driver output data (L/R = LOW)

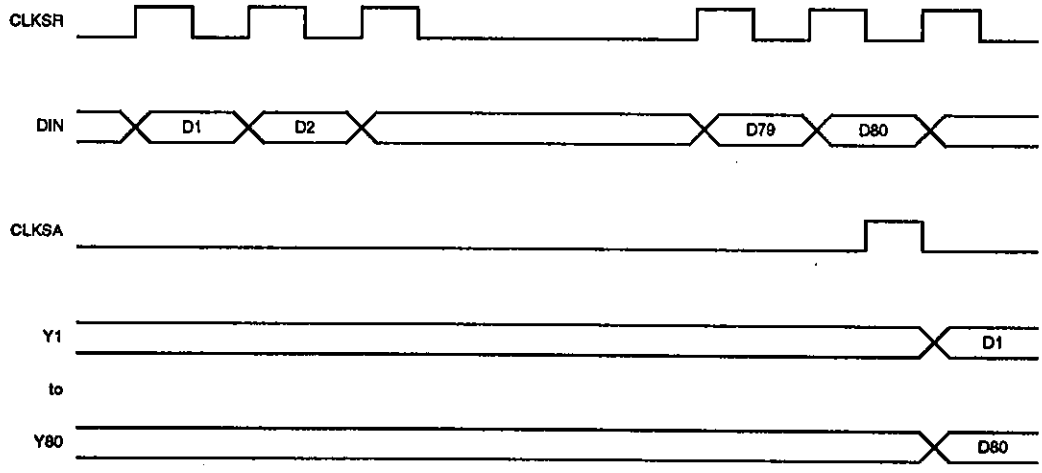


Figure 6. Driver output data (L/R = HIGH)

LCD Driver

The driver outputs one of four voltage levels to drive the LCD panel, determined by the AC control input, M, and the latched data D*i* as shown in table 1.

Table 1. Driver supply voltages

M	D*i*	Voltage
1	1	V1
1	0	V3
0	1	V2
0	0	V4

The voltage levels are used to select and deselect output segments as shown in figure 7.

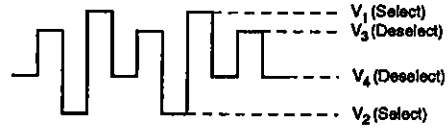
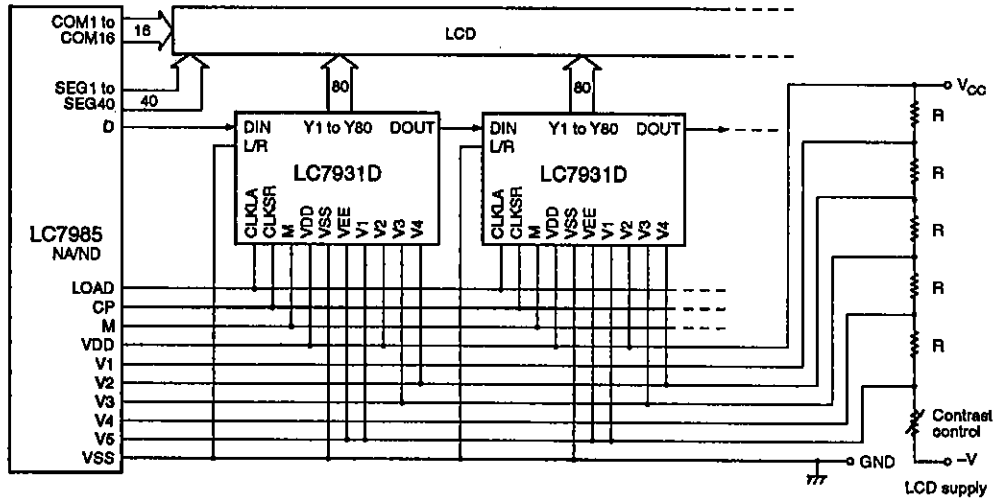


Figure 7. Driver supply voltage levels

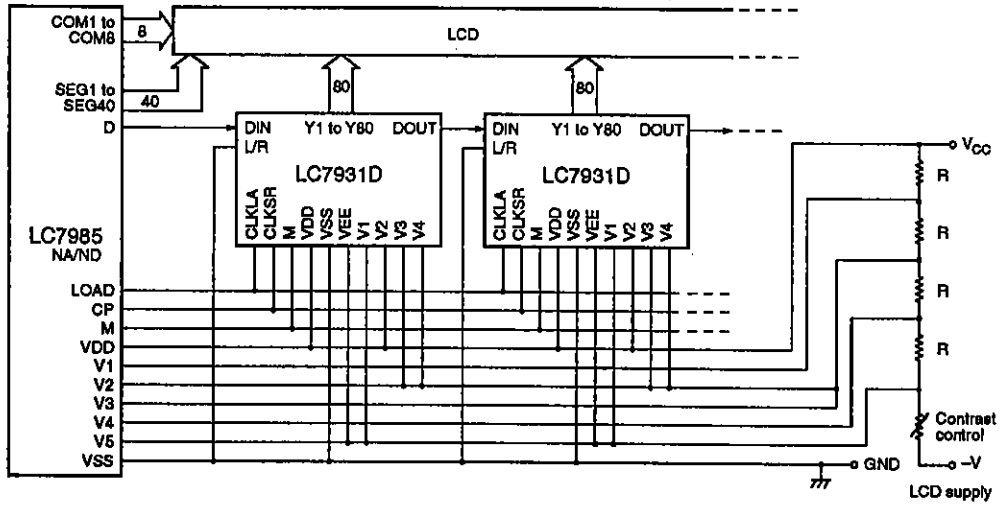
TYPICAL APPLICATIONS

Cascaded LC7931Ds with LC7985NA/ND

1/16 duty and 1/5 bias

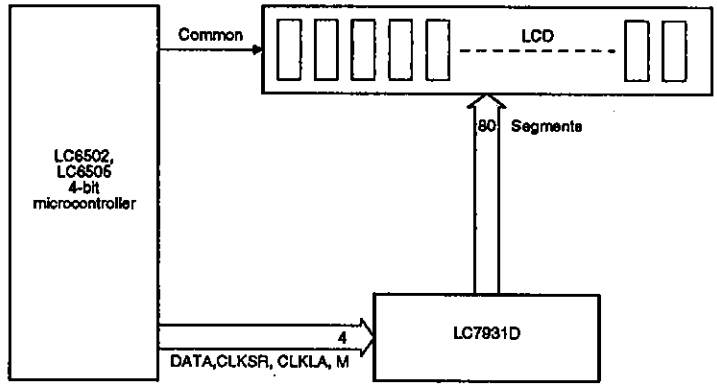


1/8 duty and 1/4 bias



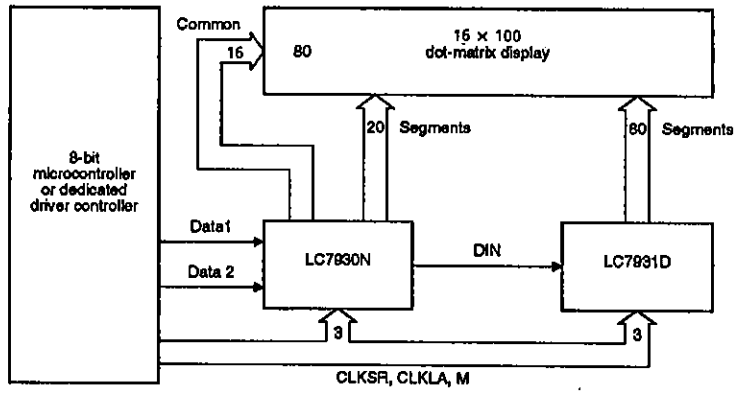
Microcontroller Interfaces

80-segment bar graph display (static)



Note
The LCD driver supply voltage divider circuit is not shown.

16 × 100 - pixel graphics display (1/16 duty and 1/5 bias)



Note
The LCD driver supply voltage divider circuit is not shown.

LC7931D AND LC7930N DEVICE COMPARISON

Parameter	Device	
	LC7931D	LC7930N
Number of driver channels	80	20 × 2
Driver supply voltage range	3 to 6 V	4.5 to 11.0 V
Maximum drive duty	1/16	1/32
Package	100-pin QIP	60-pin QIP
Driver output type	Segment	Segment and common