

**SANYO**

No. ✕4251

**LC78865M**

**16-bit A/D Converter**

Preliminary

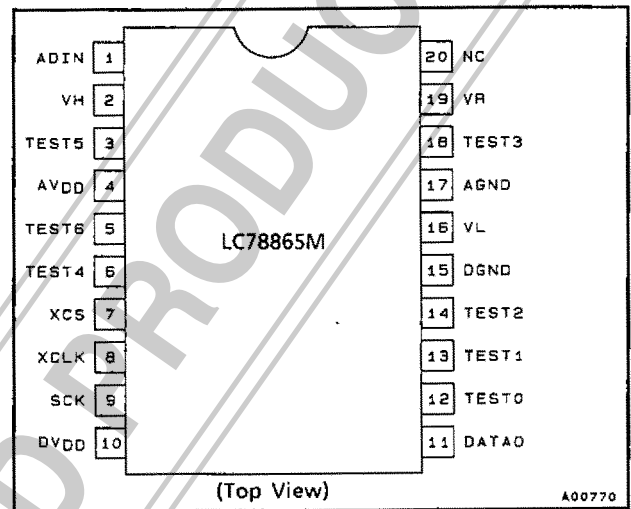
**OVERVIEW**

The LC78865M is a 16-bit single-channel CMOS A/D converter designed for digital audio applications. It uses the charge re-distribution successive approximation conversion technique.

**FEATURES**

- Single-channel 16-bit A/D converter with microcontroller interface
- Uses the charge re-distribution successive approximation conversion technique
- LSB-first, offset-binary output data format
- On-chip sample-and-hold
- Single +5 V supply
- CMOS process

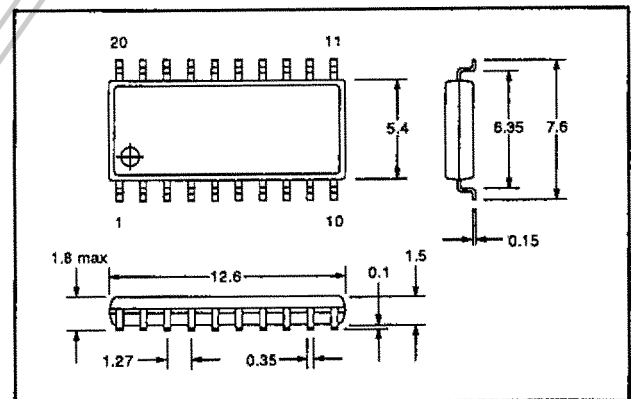
**PIN ASSIGNMENT**



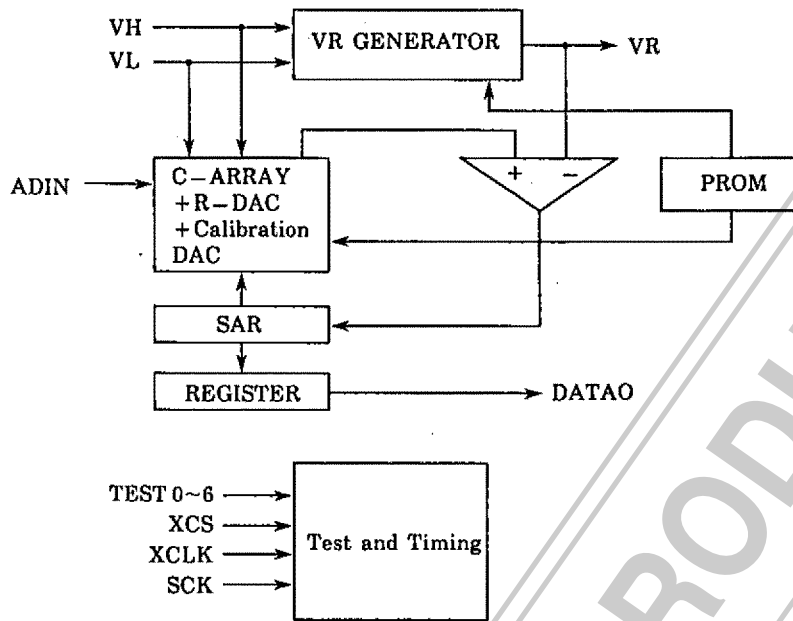
**PACKAGE DIMENSIONS**

Unit: mm

3036B-MFP20



**BLOCK DIAGRAM**



**PIN DESCRIPTION**

Name	Number	Description
1	ADIN	Analog input
2	VH	HIGH-level reference voltage
3	TEST5	Test pin. This pin has internal pull-up. Leave open for normal operation.
4	AVDD	Analog supply voltage
5	TEST6	Test pin. Connect to digital ground for normal operation.
6	TEST4	Test pin. Connect to digital ground for normal operation.
7	XCS	Data control pin. When XCS is LOW, the last-converted data is output on the DATA0 pin. This pin is normally controlled by a microcontroller.
8	XCLK	Data transfer clock input
9	SCK	System clock input
10	DVDD	Digital supply
11	DATA0	Digital output data. This pin is high-impedance when XCS is HIGH.
12	TEST0	Test pin. Connect to digital ground for normal operation.
13	TEST1	Test pin. Connect to digital ground for normal operation.
14	TEST2	Test pin. Connect to digital ground for normal operation.
15	DGND	Digital ground
16	VL	LOW-level reference voltage
17	AGND	Analog ground
18	TEST3	Test pin. Leave open for normal operation.
19	VR	Reference voltage output. The voltage on this pin is equal to $(V_H + V_L)/2$ . Leave it open for normal operation.
20	NC	No connection

**SPECIFICATIONS**

**Absolute Maximum Ratings**

$T_a = 25\text{ }^\circ\text{C}$ ,  $V_{SS} = 0\text{ V}$

Parameter	Symbol	Rating	Unit
Supply voltage	$V_{DD}$	-0.3 to 7.0	V
Input voltage	$V_{IN}$	-0.3 to $V_{DD} + 0.3$	V
Output voltage	$V_{OUT}$	-0.3 to $V_{DD} + 0.3$	V
Operating temperature	$T_{opr}$	-20 to 75	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-40 to 125	$^\circ\text{C}$

**Recommended DC Operating Conditions**

$T_a = 25\text{ }^\circ\text{C}$ ,  $V_{SS} = 0\text{ V}$

Parameter	Symbol	Rating			Unit
		min	typ	max	
Supply voltage	$V_{DD}$	4.5	5.0	5.5	V
HIGH-level reference voltage	$V_H$	3.3	-	$V_{DD}$	V
LOW-level reference voltage	$V_L$	0	-	1.2	V
Analog input voltage	$V_{AIN}$	$V_L$	-	$V_H$	V

**DC Electrical Characteristics**

$T_a = -20\text{ to }75\text{ }^\circ\text{C}$ ,  $V_{DD} = 4.5\text{ to }5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
HIGH-level input voltage	$V_{IH}$	All digital inputs except SCK	2.2	-	-	V
LOW-level input voltage	$V_{IL}$	All digital inputs except SCK	-	-	0.8	V
HIGH-level output voltage	$V_{OH}$	$I_{OH} = -1\text{ }\mu\text{A}$	$V_{DD} - 0.05$	-	-	V
LOW-level output voltage	$V_{OL}$	$I_{OL} = 1\text{ }\mu\text{A}$	-	-	$V_{SS} + 0.05$	V
Clock input pulsewidth	$t_{SCK}$	SCK pin	0.5	-	-	$V_{PP}$

**AC Characteristics**

$T_a = -20\text{ to }75\text{ }^\circ\text{C}$ ,  $V_{DD} = 4.5\text{ to }5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Rating			Unit
			min	typ	max	
XCS setup time	$T_{XCSS}$		1.5	-	-	$\mu\text{s}$
XCS hold time	$T_{XCSh}$		1.5	-	-	$\mu\text{s}$
XCLK cycle time	$T_{XCKC}$		1.0	-	-	$\mu\text{s}$
XCLK pulsewidth	TH		300	-	-	ns
DATA0 delay time	TDL		0	-	150	ns
SCK clock frequency	FSCK		5	14.32	16	MHz

### Analog Characteristics

$T_a = 25\text{ }^\circ\text{C}$ ,  $AV_{DD} = DV_{DD} = 5.0\text{ V}$ ,  $V_H = 5.0\text{ V}$ ,  $V_L = 0\text{ V}$

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
A/D conversion frequency	$f_s$	See note.	17.4	49.7	55.6	kHz
Linearity	LE		-	-	0.025	%
Power consumption	$P_D$		-	70	130	mW

#### Note

One conversion takes 288 SCK cycles. After conversion, the whole output word is loaded into the output register. Thus, while XCS is HIGH, the output register is updated every 288 SCK cycles. When XCS goes LOW, output register update is inhibited and preparation for output takes place.

### Input Impedance

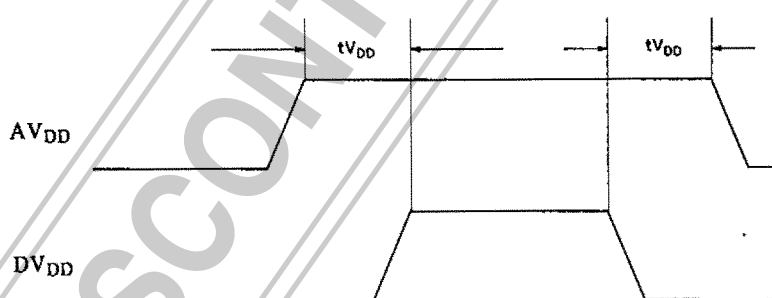
$AV_{DD} = DV_{DD} = 5.0\text{ V}$ ,  $V_H = 5.0\text{ V}$ ,  $V_L = 0\text{ V}$

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Input impedance	ADIN	DC input, Sampling rate = 49.7 kHz	5	-	-	$M\Omega$
		1 kHz AC input, Sampling rate = 49.7 kHz	250	-	-	$k\Omega$

### SUPPLY TIMING

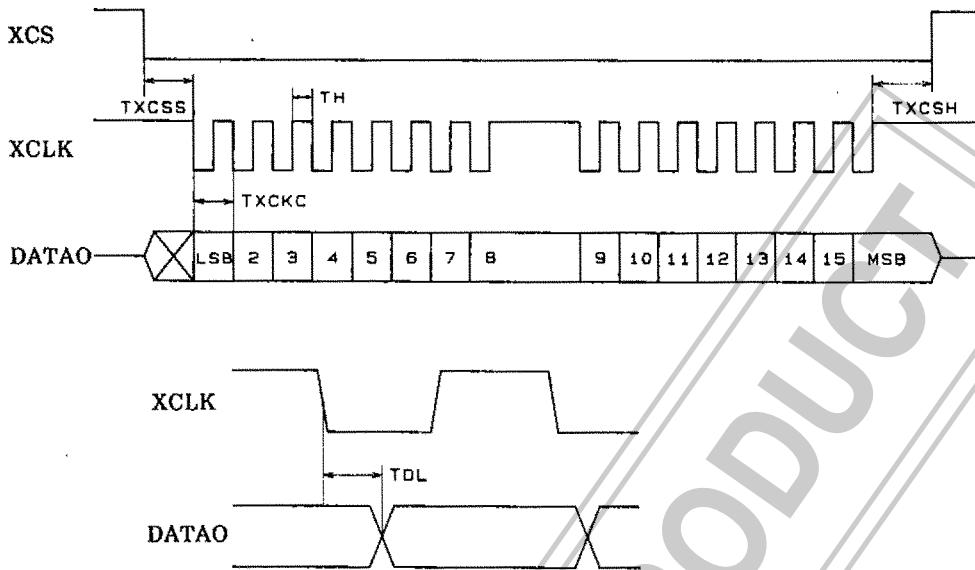
The analog and digital supply lines,  $AV_{DD}$  and  $DV_{DD}$ , are completely independent. The ground lines, AGND and DGND, should be connected together on the circuit board. The two supply lines should power-up and

power-down at exactly the same time. At worst, the digital supply line can come up two or three milliseconds behind the analog line, but never before it. The reverse applies on power-down.



A0076B

**TIMING DIAGRAM**



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**THE CONVERSION TECHNIQUE**

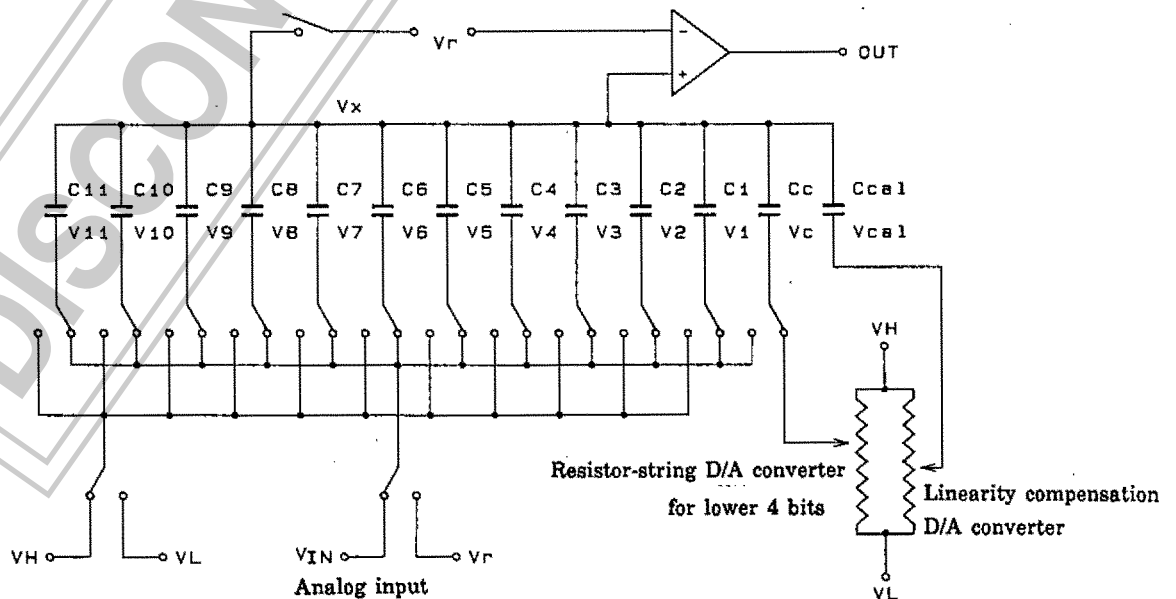
The LC78865M uses the charge re-distribution successive approximation technique. It includes a capacitive charge accumulator for the upper 12 bits, a resistor string DAC for the lower four bits, and a linearity compensation resistor string DAC.

operates from a single supply voltage using a virtual earth voltage,  $V_r$ , halfway between the two reference voltages. The successive approximation comparisons use a signed-magnitude comparison with  $V_r$  as the reference.

The converter works by accumulating a charge proportional to the input voltage in the accumulation capacitors. The voltage produced is compared with the reference voltages. Each bit of the output word is determined sequentially, from most-significant to least-significant. The charge accumulation capacitors also function as a sample-and-hold circuit. The device

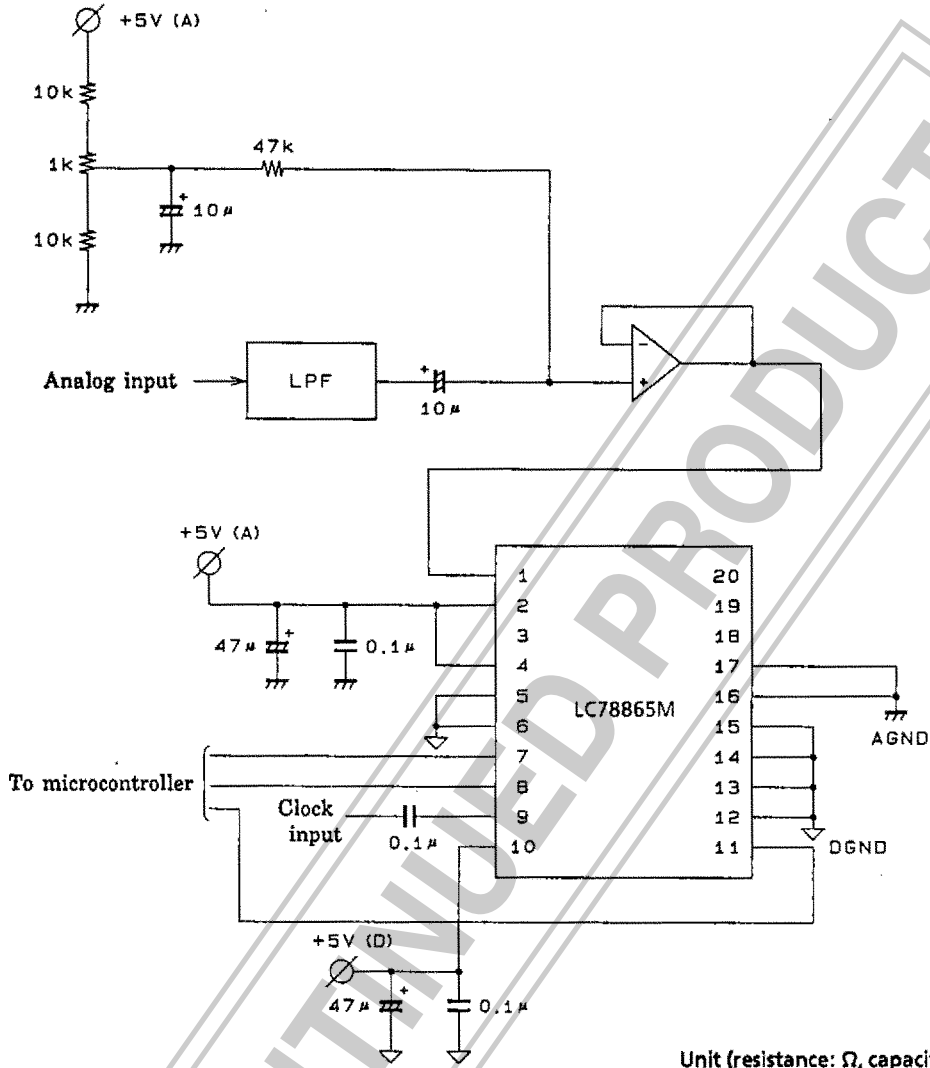
The resolution of the successive approximation technique described above is limited by the accuracy of the internal reference,  $V_r$ , and the accumulation capacitors. Errors caused by these effects are measured at the factory for each device, and the error characteristic stored in internal PROM. The data from the PROM is used to drive the linearity compensation D/A converter.

**Charge Accumulation Successive Approximation Converter**



A00771

## APPLICATION CIRCUIT



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