Ordering number: EN 3744C

CMOS LSI

SANYO No. 3744C

LC78815M

Two-channel, 16-bit D/A Converter for Digital Audio Applications

Overview

The LC78815M is a two-channel, 16-bit D/A converter for digital audio applications. It incorporates two, independent dynamic level-shift converters, each comprising a 512-element resistor string, a 3-bit PWM circuit and a 4-bit level shifter.

The LC78815M reads 2s complement serial input data at a sampling rate of 400kHz. It features 0.09% maximum total harmonic distortion, good channel separation and excellent signal-to-noise ratio. The channel outputs are synchronized.

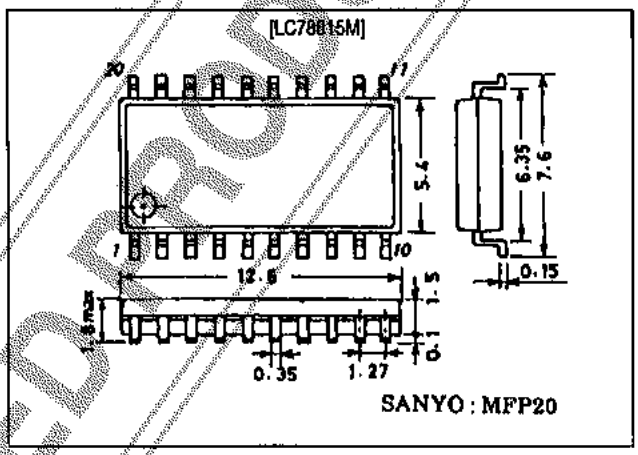
Features

- Two-channel 16-bit D/A conversion
- 2s complement serial input data
- Zero phase difference between left and right channels
- 8-times oversampling at 400kHz
- No external sample-and-hold circuit required
- Low-power silicon-gate CMOS process
- Single 5V supply
- 20-pin MFP

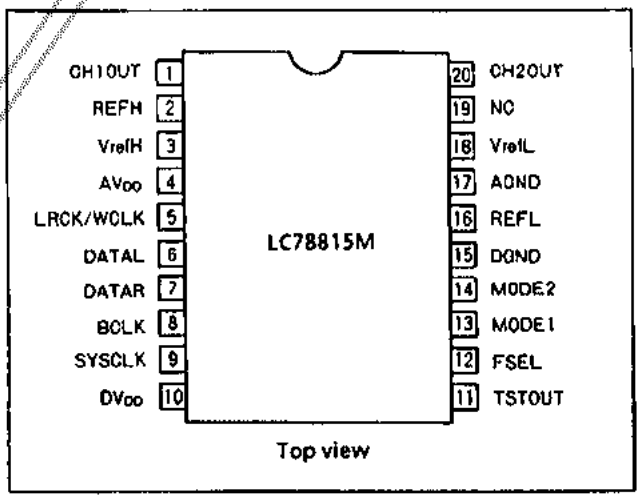
Package Dimensions

unit: mm

3036B-MFP20



Pin Assignment



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Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Ratings	Unit
Supply voltage range	V_{DD} max	−0.3 to +7.0	V
Input voltage range	V_{IN}	−0.3 to V_{DD} + 0.3	V
Output voltage range	V_{OUT}	−0.3 to V_{DD} + 0.3	V
Operating temperature range	Topr	−30 to +75	°C
Storage temperature range	Tstg	−40 to +125	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Ratings			Unit
		min	typ	max	
Supply voltage	V_{DD}	4.5	5.0	5.5	V
High-level reference voltage	VrefH	V_{DD} − 0.5	–	V_{DD}	V
Low-level reference voltage	VrefL	0	–	0.5	V

DC Characteristics at Ta = −30 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
High-level input voltage 1	V_{IH1}	All inputs except SYSCLK	2.2	–	–	V
Low-level input voltage 1	V_{IL1}	All inputs except SYSCLK	–	–	0.8	V
High-level input voltage 2	V_{IH2}	SYSCLK	0.7V_{DD}	–	–	V
Low-level input voltage 2	V_{IL2}	SYSCLK	–	–	0.3V_{DD}	V
Output load resistance	R_L	Between pins 1 and 20	5	–	–	kΩ

AC Characteristics at Ta = −30 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V

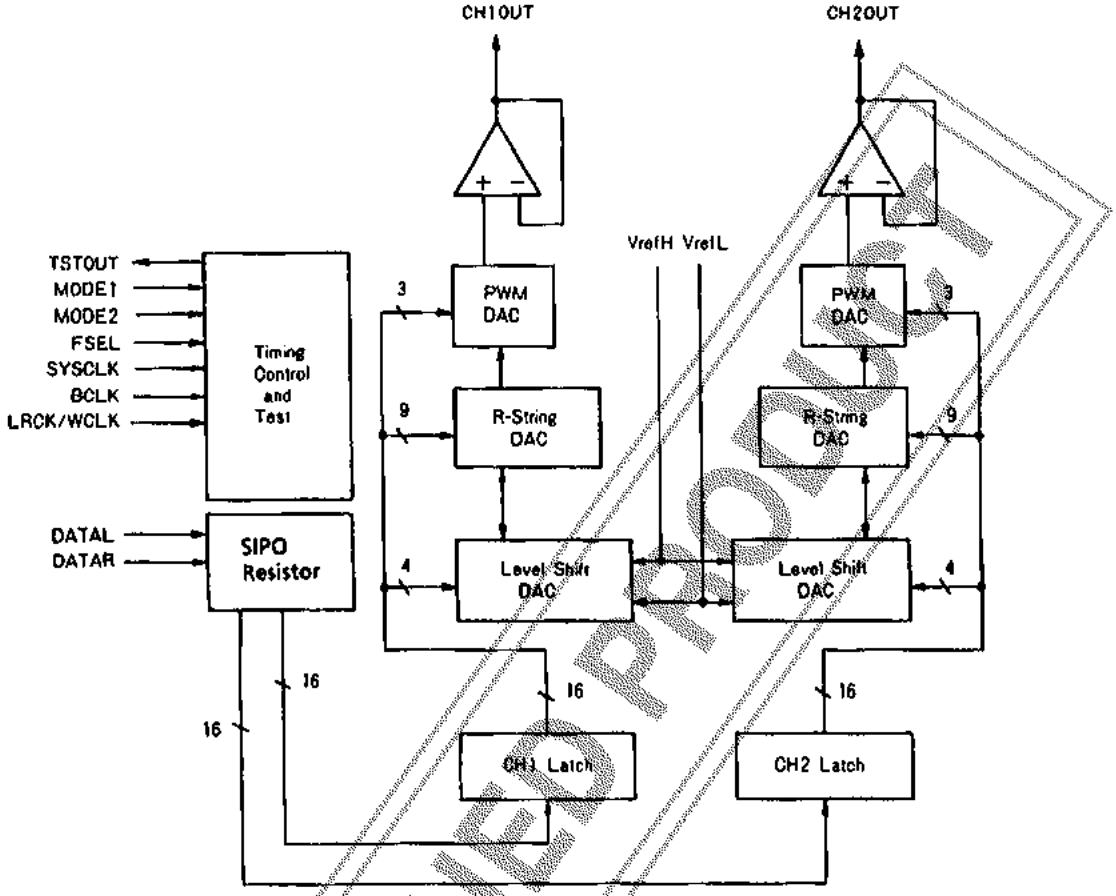
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Clock pulsewidth	t_{CW}	SYSCLK	25	–	–	ns
	t_{BCW}	BCLK	35	–	–	ns
Setup time	t_{DS}	LRCK/WCLK, DATAL, DATAR	20	–	–	ns
Data hold time	t_{DH}		20	–	–	ns

Electrical Characteristics at Ta = 25°C, V_{DD} = 5.0V

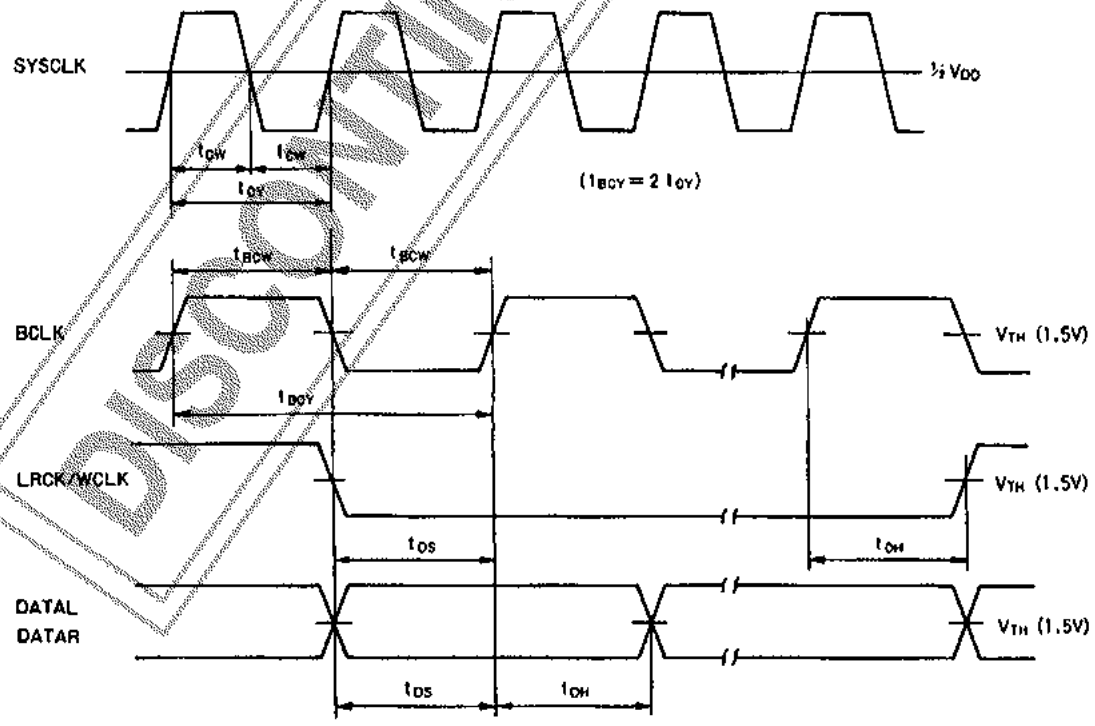
Parameter[1]	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Resolution	RES		–	16	–	bits
Conversion frequency	f_S		–	–	400	kHz
Total harmonic distortion	THD	1kHz, 0dB	–	0.04	0.09	%
Crosstalk	CT	1kHz, 0dB	–	–	−85	dB
Signal-to-noise ratio	S/N	JIS-A	96	–	–	dB
Full-scale output voltage	VFS		–	3.3	–	Vp-p
Power dissipation	Pd		–	35	60	mW

1. f_S = 88.2kHz

Block Diagram



Switching Characteristics



Pin Functions

Number	Name	Functions
1	CH1OUT	Left-channel pulsewidth modulated output
2	REFH	High-level reference voltage input. Normally connected by capacitor to AGND.
3	VrefH	High-level reference voltage input
4	AV_{DD}	5V analog supply
5	LRCK/WCLK	Word latch clock input
6	DATAL	Left-channel serial data input
7	DATAR	Right-channel serial data input
8	BCLK	Serial data bit clock input
9	SYSCLK	System clock input
10	DV_{DD}	5V digital supply
11	TSTOUT	Test mode output. Normally open.
12	FSEL	Digital audio data select input
13	MODE1	Serial input data and timing mode select input 1
14	MODE2	Serial input data and timing mode select input 2
15	DGND	Digital ground
16	REFL	Low-level reference voltage input. Normally connected by capacitor to AGND.
17	AGND	Analog ground
18	VrefL	Low-level reference voltage input
19	NC	No connection
20	CH2OUT	Right-channel pulsewidth modulated output

Functional Description

The LC78815M has two independent channels, each comprising a serial-to-parallel converter, latch, 16-bit level-shift D/A converter and output buffer amplifier. Each 16-bit data word is split into three fields—D0 to D3, D4 to D6, and D7 to D15—and each field is connected to a different section of the D/A converter, as shown in Figure 1.

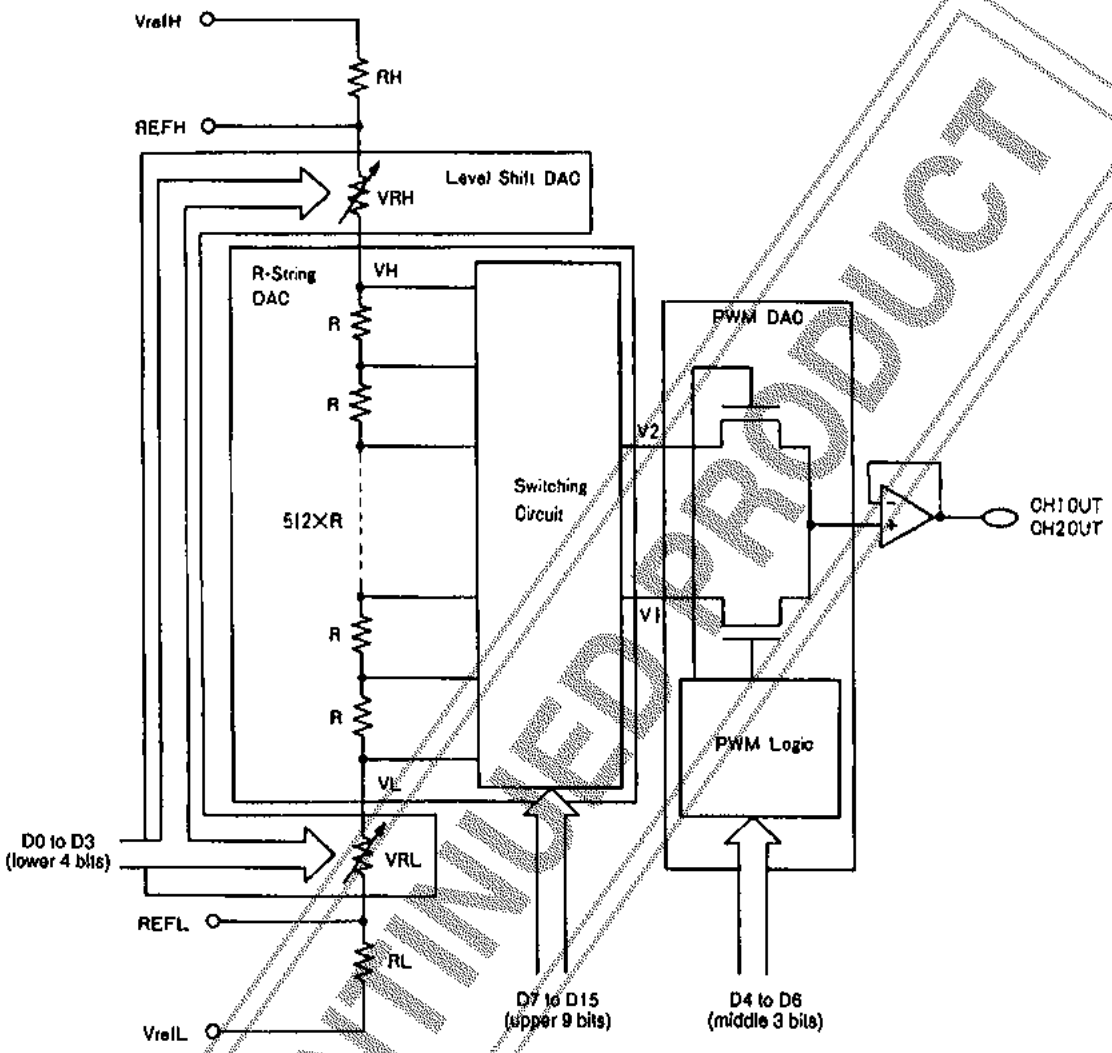


Figure 1. D/A converter

Data Input

Data input is in 2s complement format with the most-significant bit first. Each bit is clocked in on the rising edge of BCLK. When FSEL is LOW, data is clocked serially into DATAL and DATAR, and when HIGH, data is clocked in parallel to DATAL.

The LC78815M supports the data formats shown in Figures 2 to 8. The format shown in Figure 2, for example, is used for the interface to compact disc player digital signal processors such as the LC7860KA and LC7863KA.

Resistor String and Switching Circuit

The resistor-string voltage divider comprises 512 equal-value resistors and is driven by D7 to D15 of the input word. The switching circuit selects a pair of adjacent taps, V1 and V2, from the ladder and connects them to the PWM circuit as shown in Figure 1. The difference between these voltages is $(V_H - V_L)/512$, where V_H and V_L are the HIGH and LOW-level reference voltages, respectively.

PWM Circuit

The PWM circuit modulates the voltage $V_1 - V_2$. The duty cycle is selected by D4 to D6 of the input word. The average output voltage is one of eight equally-spaced voltage levels between V_1 and V_2.

Level Shifter

The level shifter selects one of sixteen equally-spaced voltage levels across the resistor string by changing the resistances VR_L and VR_H. The voltage levels are selected by D0 to D3 of the input word.

VR_L and VR_H are changed in steps of R/128, where R is the resistance of each string resistor. The sum of VR_L and VR_H is constant.

Reference Voltages

The voltages applied to VrefL and VrefH are usually 0V and 5V, respectively. Capacitors of approximately 47μF should be connected between REFL and AGND, and REFH and AGND.

Timing Modes

The LC78815M operates in one of seven timing modes selected by the logic levels applied to MODE1 and MODE2.

Alternate left/right-channel input (FSEL = HIGH)

MODE1 = LOW, MODE2 = LOW

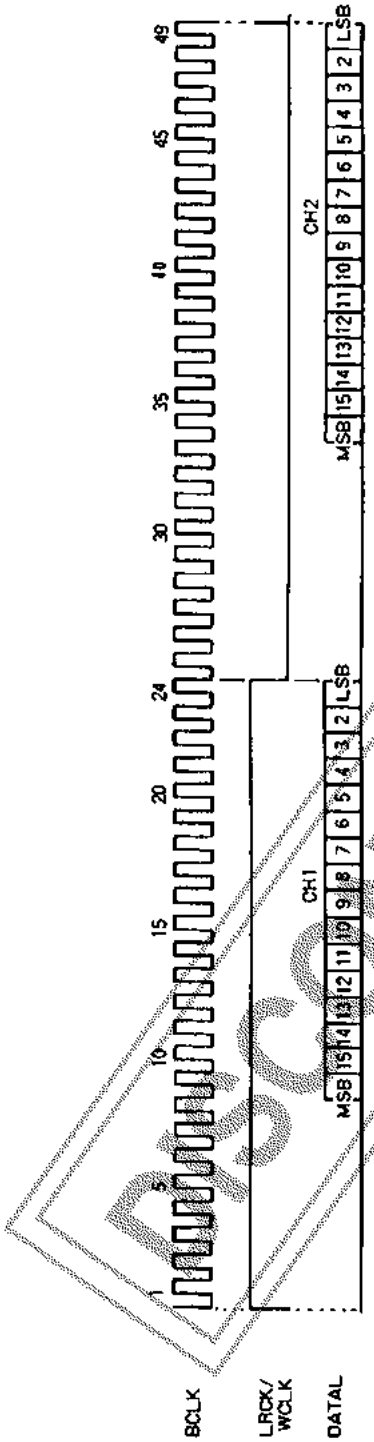


Figure 2. Alternate timing mode 1

MODE1 = LOW, MODE2 = HIGH

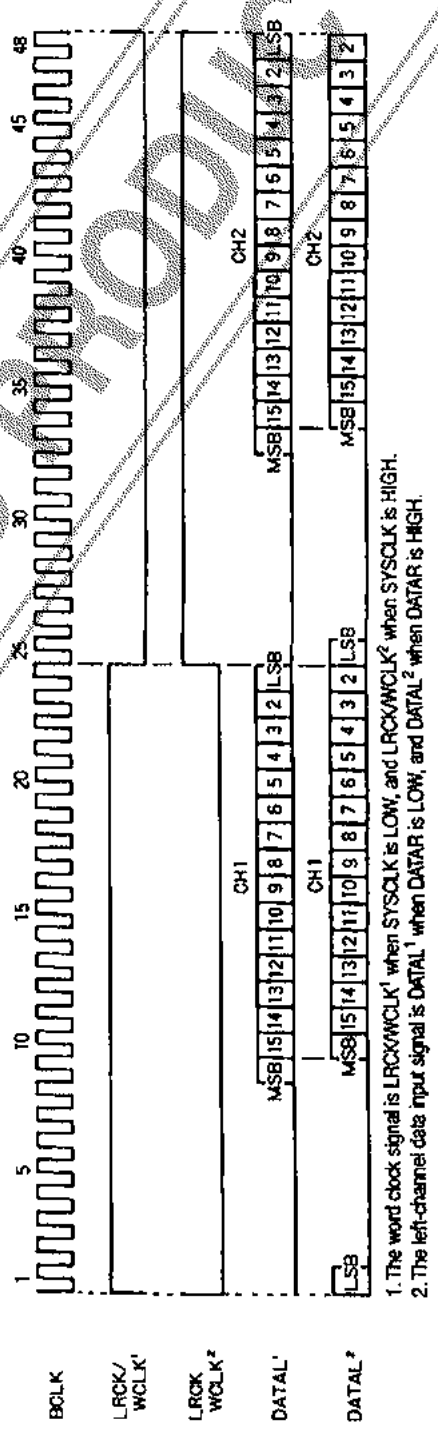


Figure 3. Alternate timing mode 2

MODE1 = HIGH, MODE2 = LOW

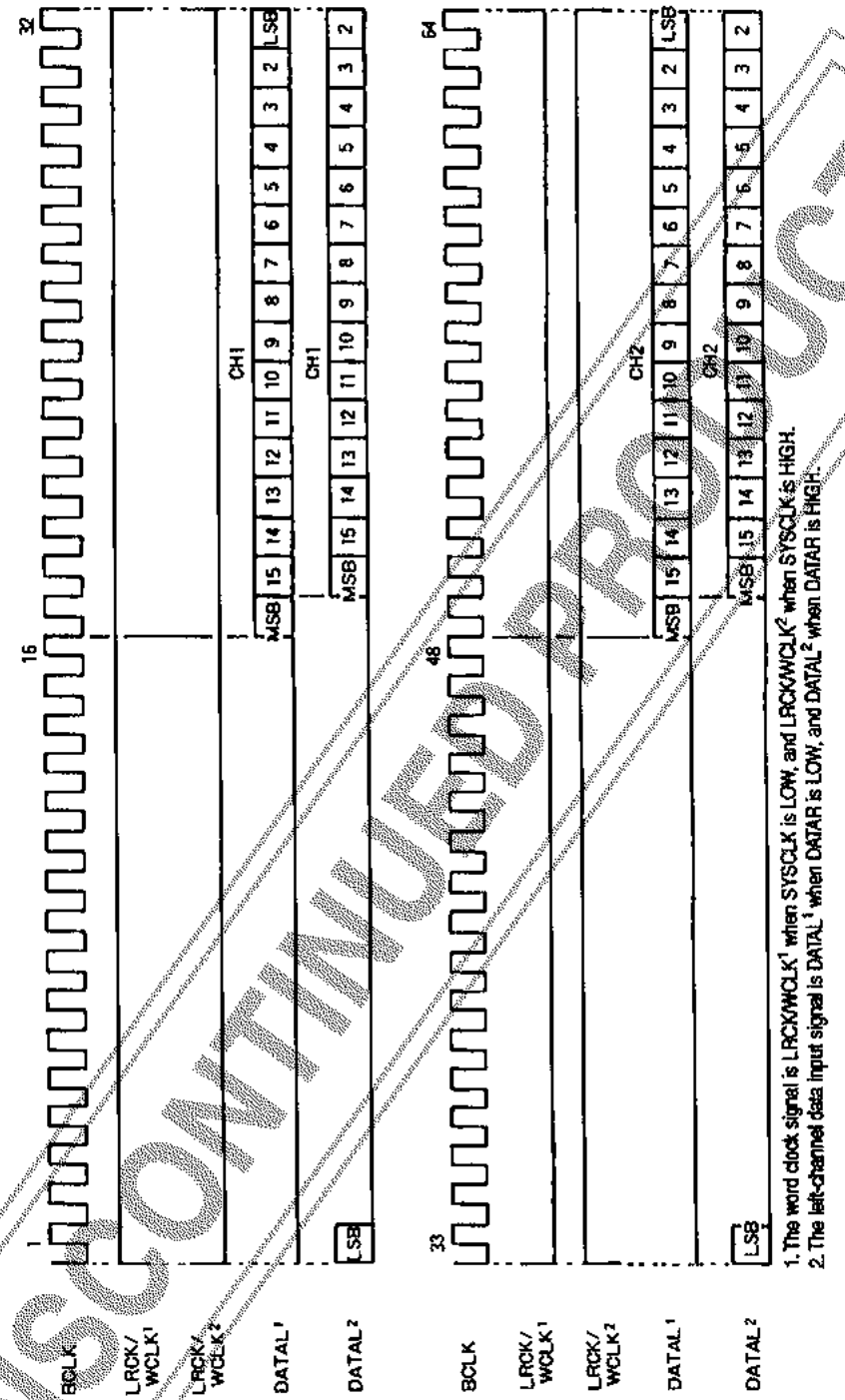


Figure 4. Alternate timing mode 3

MODE1 = HIGH, MODE2 = HIGH

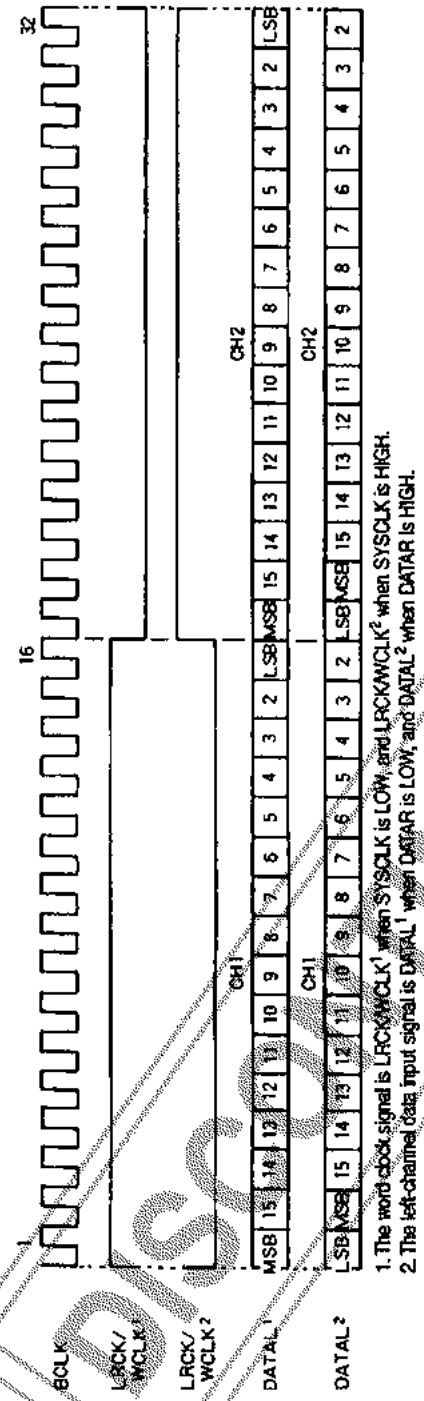


Figure 5. Alternate timing mode 4

Simultaneous left/right-channel input (FSEL = LOW)

MODE1 = LOW, MODE2 = LOW

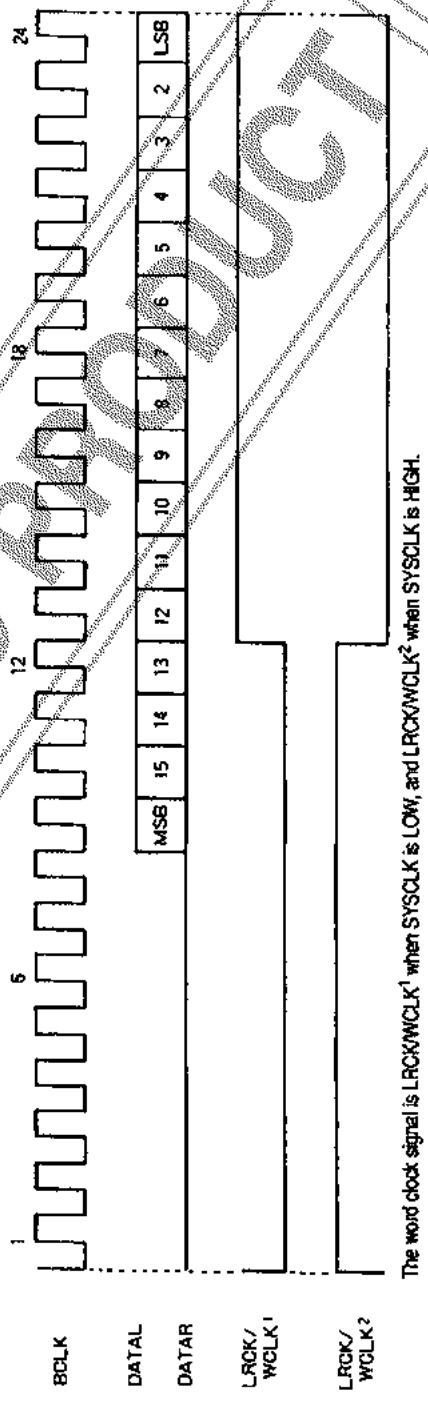


Figure 6. Simultaneous timing mode 1

MODE1 = LOW, MODE2 = HIGH

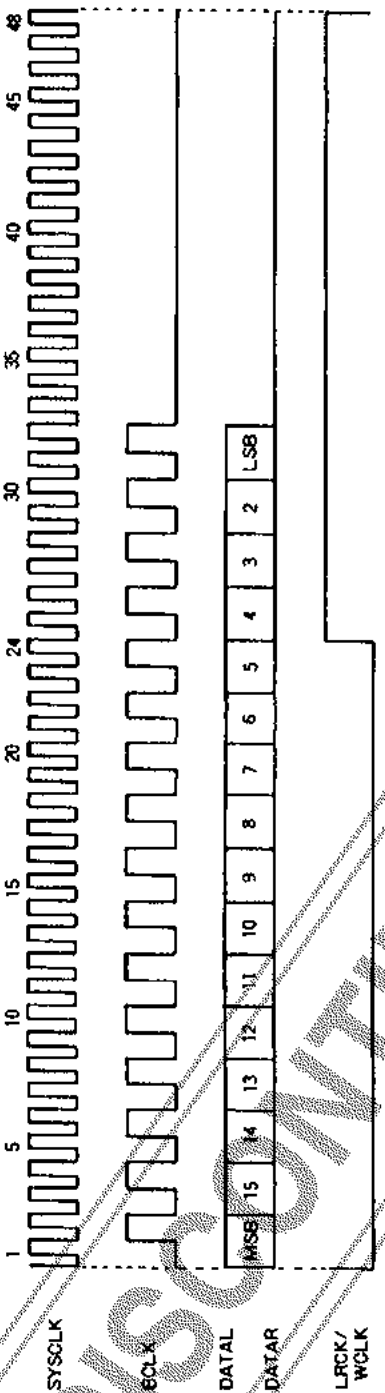


Figure 7. Simultaneous timing mode 2

MODE1 = HIGH, MODE2 = HIGH

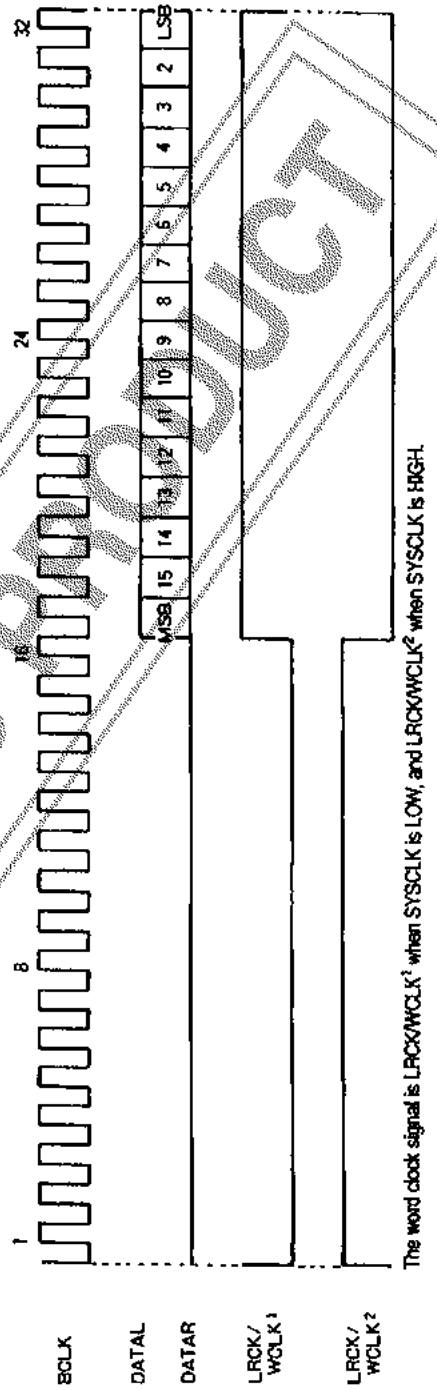


Figure 8. Simultaneous timing mode 4

Design Information

Ground Lines

Ensure that the digital and analog ground lines are separate, and that DGND and AGND are connected correctly.

Supply Voltage

Use a high-stability, low-impedance supply for reference and supply voltages. AVDD and DVDD should be connected to the same supply to prevent possible latch-up.

Sample Application Circuit