Ordering number :EN*5201A

CMOS LSI

LC75391, 75391M

Single-Chip Electronic Volume Control System

CCB

Overview

The LC75391 and LC75391M are single-chip electronic volume and tone control systems that support volume control, tone control, and input and output signal switching functions controlled by serial input data.

Functions

- Input and output signal switching: The four I/O switches can be set to on or off independently.
- Volume control: Independent control of the left and right channels can be used to implement a balance function.
  0 to –20 dB in 2 dB steps, –20 to –32 dB in 3 dB steps, –32 to –53 dB in 4 dB steps, –52 to –70 dB in 4.5 dB steps, and –∞.
- Tone controls: Four frequency characteristic types selectable by setting internal switches.
  Also supports a buffer function that requires no external components.
- Two general-purpose output ports: These ports allow this LSI to control motorized volume controls and general-purpose logic.

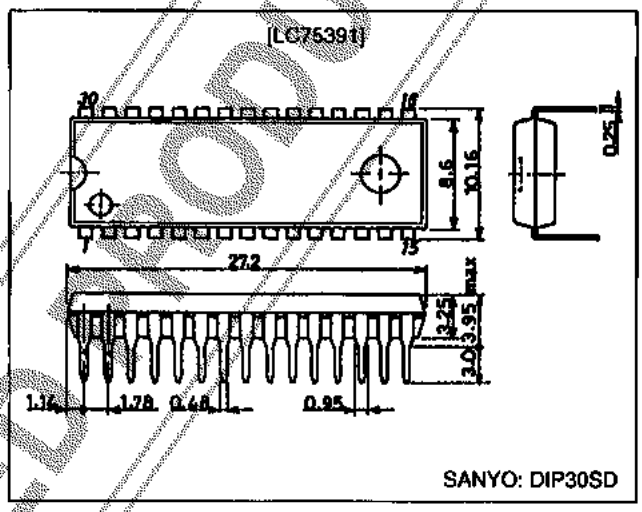
- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

Package Dimensions

unit: mm

3196-DIP30SD

[LC75391]

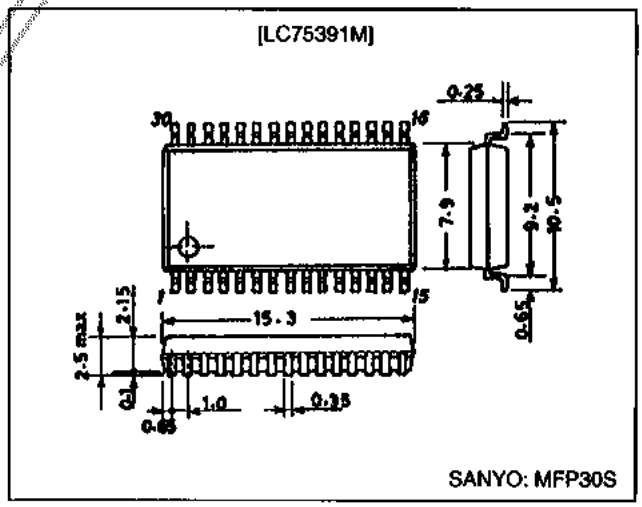


SANYO: DIP30SD

unit: mm

3216-MFP30S

[LC75391M]



SANYO: MFP30S

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	12	V
Maximum input voltage	V_{IN} max	CL, DI, CE, L1 to L4, R1 to R4	V_{SS} – 0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 85°C	160	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–50 to +125	°C

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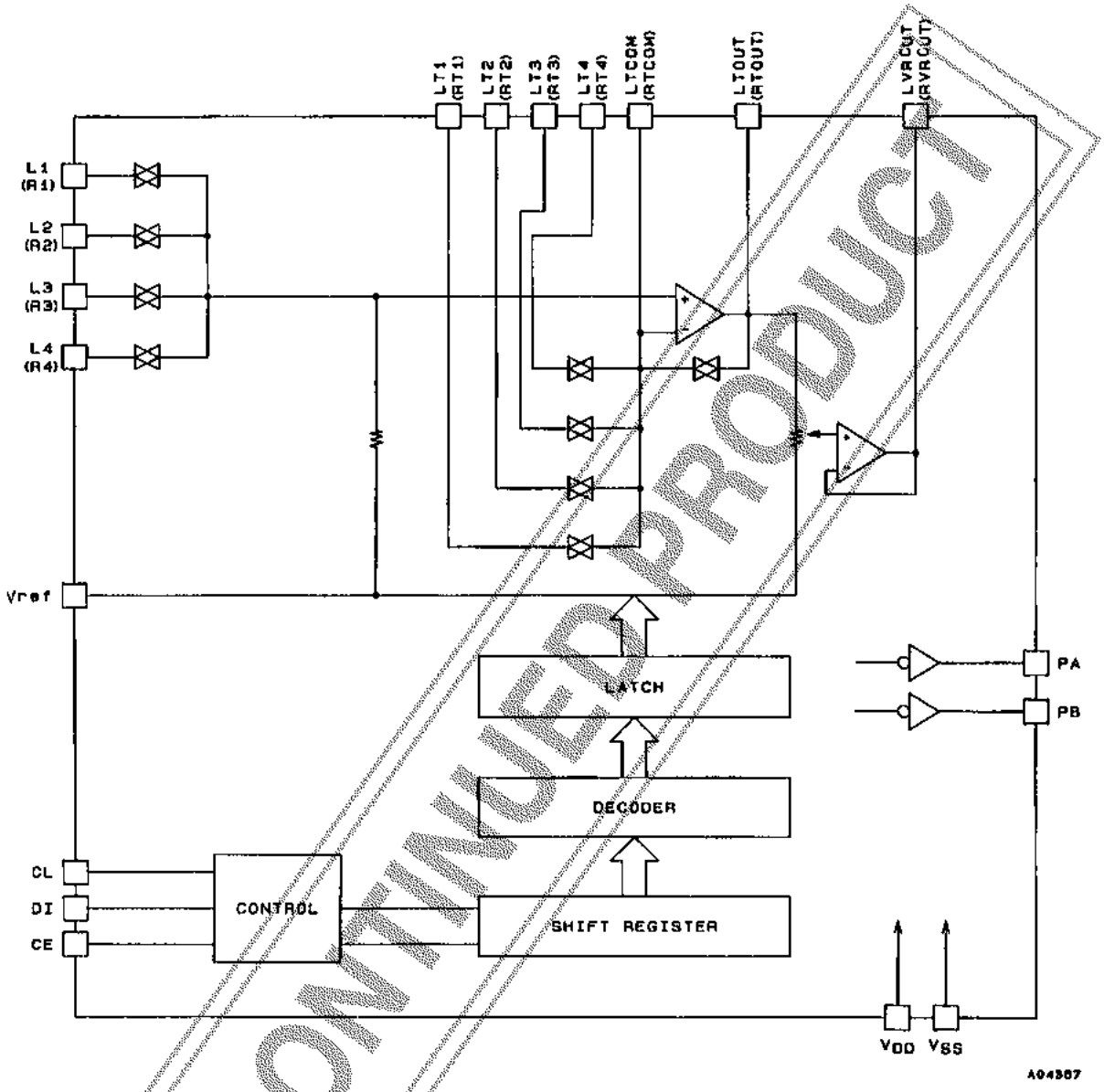
Allowable Operating Ranges at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}	V_{DD}	5.5		11.0	V
Input high-level voltage	V_{IH}	CL, DI, CE	4.0		V_{DD}	V
Input low-level voltage	V_{IL}	CL, DI, CE	V_{SS}		1.0	V
Output high-level voltage	V_{OH}	PA, PB: I_O = 5 mA	V_{DD} – 2		V_{DD}	V
Output low-level voltage	V_{OL}	PA, PB: I_O = 5 mA	V_{SS}		2.0	V
Input voltage amplitude	V_{IN}	L1 to L4, R1 to R4	V_{SS}		V_{DD}	Vp-p
Input pulse width	t_{pW}	CL	1.0			µs
Setup time	$t_{set\ up}$	CL, DI, CE	1.0			µs
Hold time	t_{hold}	CL, DI, CE	1.0			µs
Operating frequency	fopg	CL			500	kHz

Electrical Characteristics at Ta = 25°C, V_{DD} = 10 V, V_{SS} = 0 V

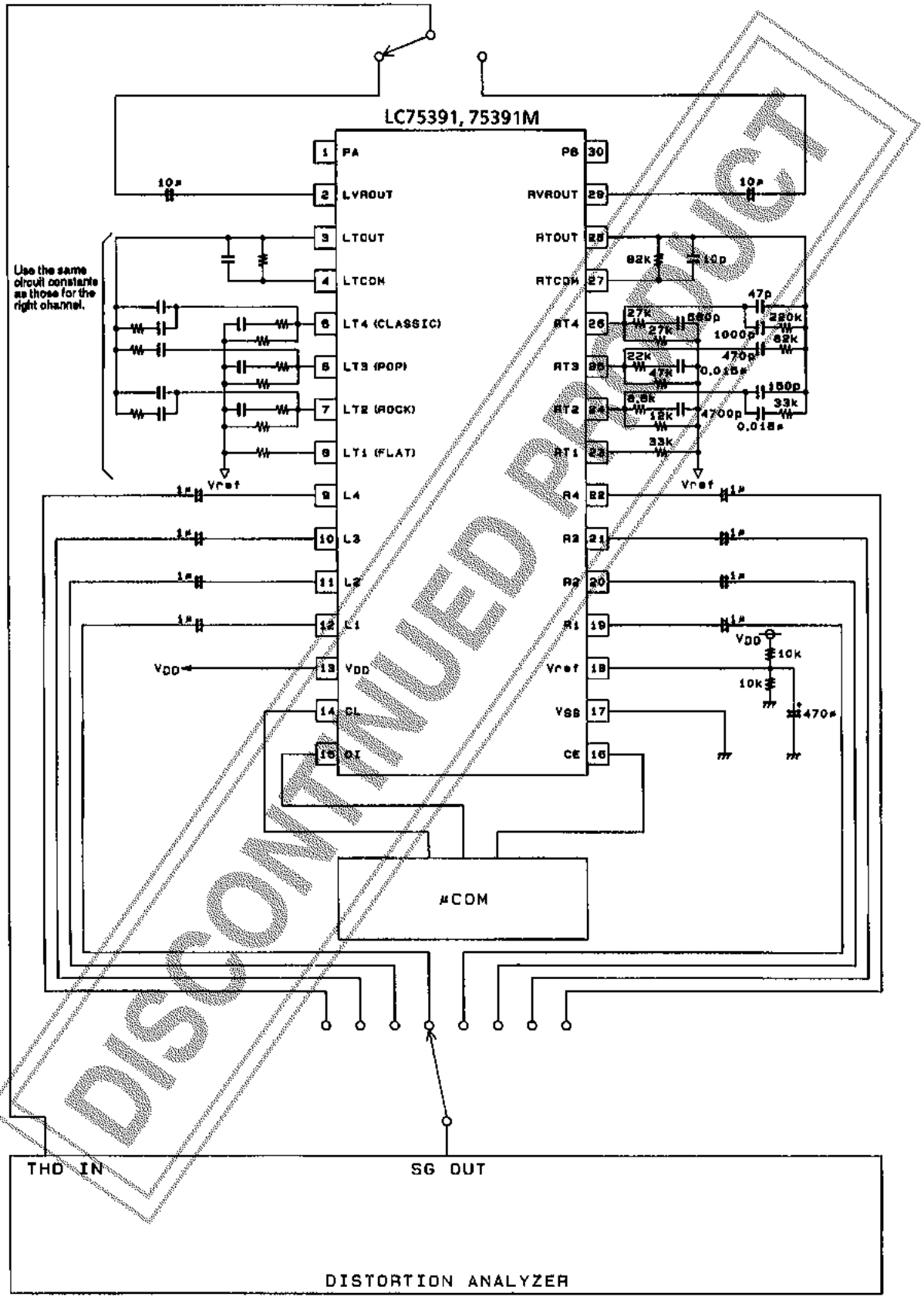
Parameter	Symbol	Conditions	min	typ	max	Unit
[Input Block]						
Input resistance	Rin	L1 to L4, R1 to R4		500		kΩ
[Overall Characteristics]						
Total harmonic distortion	THD (1)	V_{IN} = 100 mVrms, f = 1 kHz, overall, buffer mode off, flat state		0.013		%
	THD (2)	V_{IN} = 100 mVrms, f = 20 kHz, overall, buffer mode off, flat state		0.013		%
Crosstalk	CT	V_{IN} = 1 Vrms, f = 1 kHz, overall, Rg = 1 kΩ, buffer mode off, flat state		81		dB
Maximum attenuation	V_O min	V_{IN} = 1 Vrms, f = 1 kHz, main volume at –∞, buffer mode on		–80		dB
Output noise voltage	V_N (1)	Flat overall (IHF-A), Rg = 1 kΩ, buffer mode off, flat state		15		µV
	V_N (2)	Flat overall (DIN-AUDIO), Rg = 1 kΩ, buffer mode off, flat state		22		µV
Current drain	I_{DD}	V_{DD} – V_{SS} = 11 V		7	10	mA
Input high-level current	I_{IH}	CL, DI, CE, V_{IN} = 10 V			10	µA
Input low-level current	I_{IL}	CL, DI, CE, V_{IN} = 0 V	–10			µA

Equivalent Circuit Block Diagram



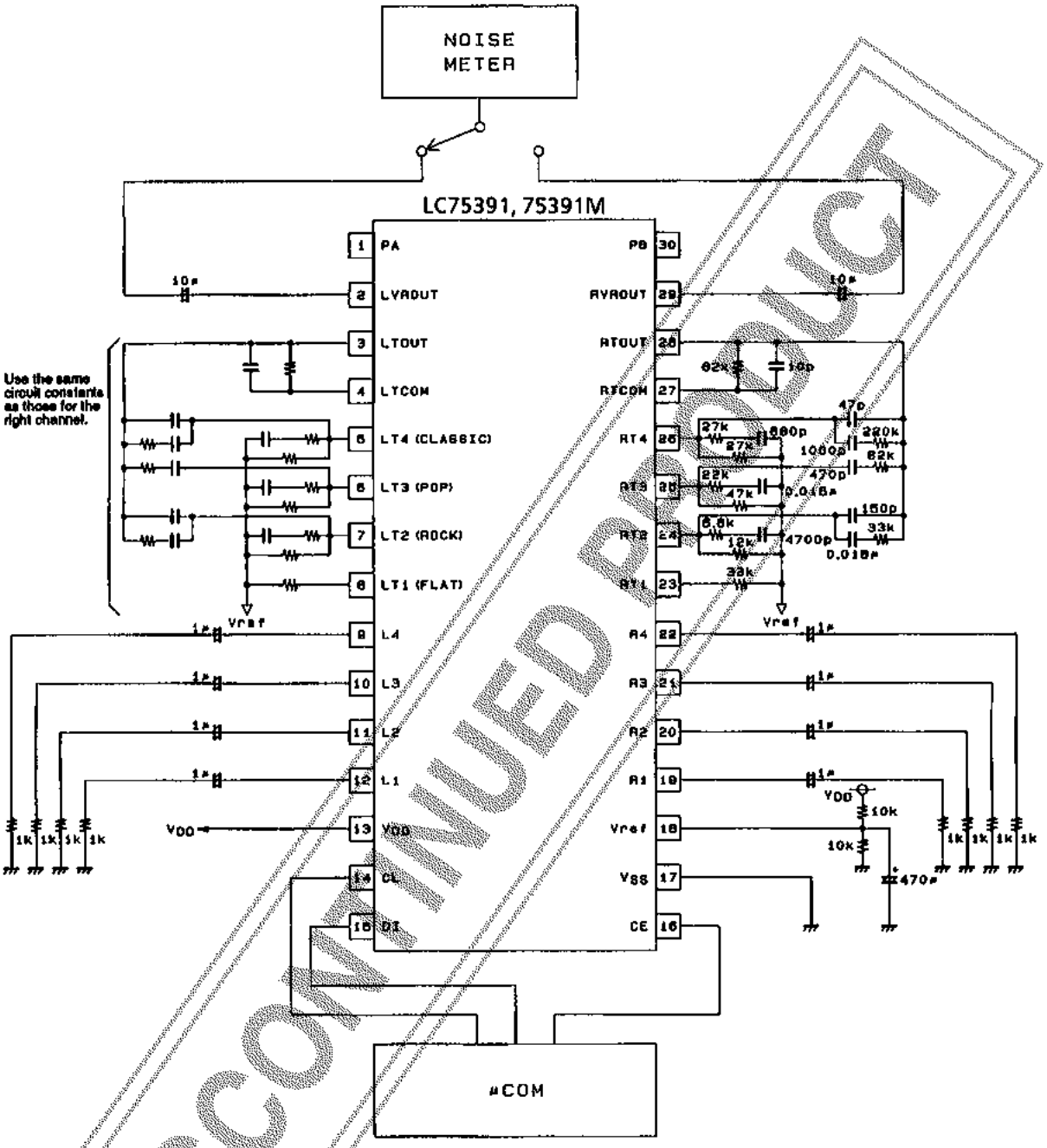
Test Circuits

1. Total harmonic distortion

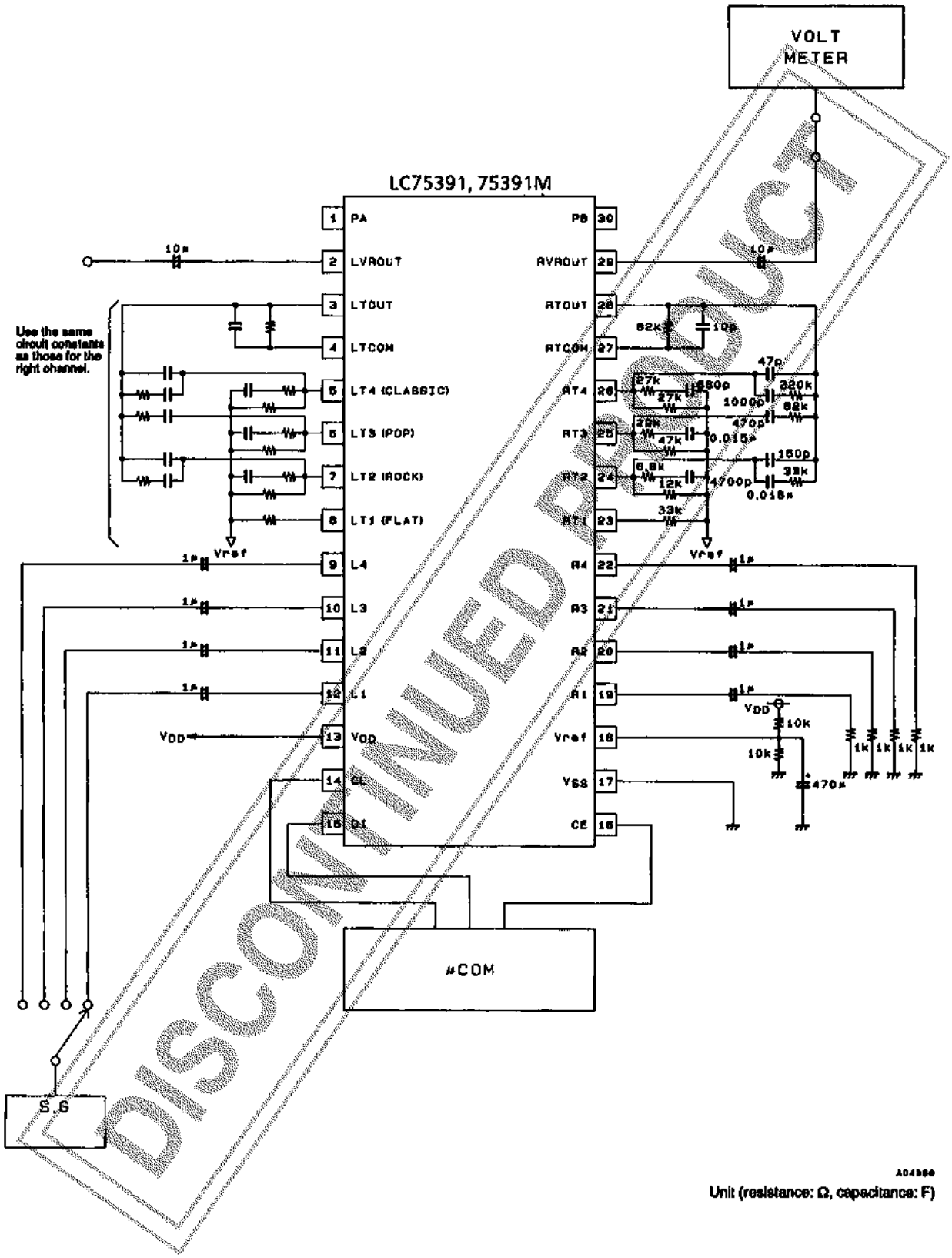


A04958
Unit (resistance: Ω, capacitance: F)

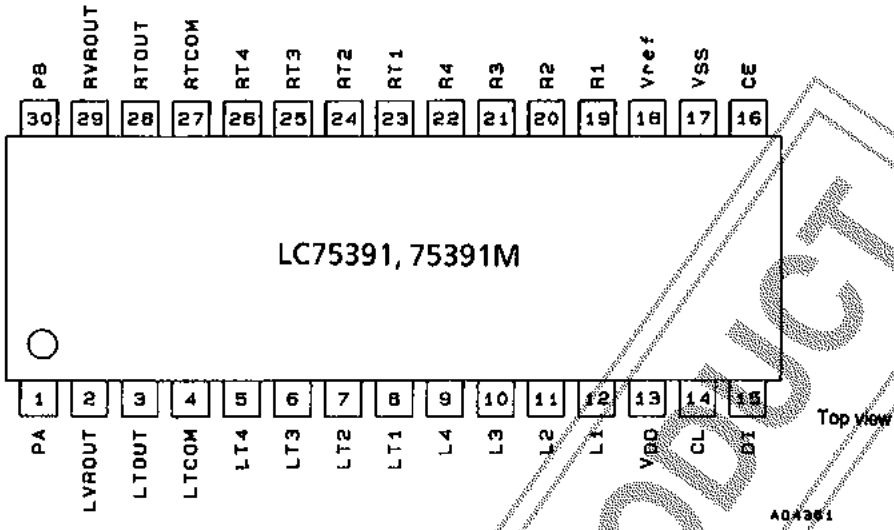
2. Output noise voltage



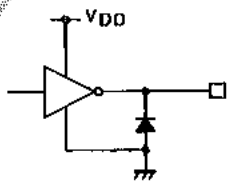
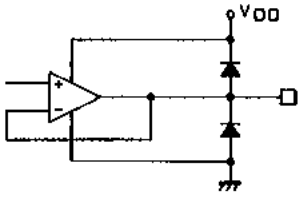
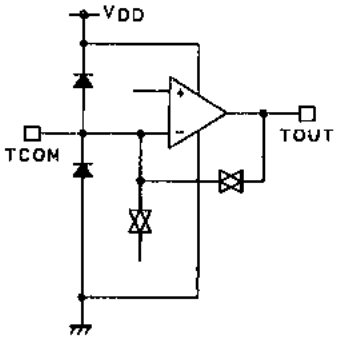
3. Crosstalk



Pin Assignment



Pin Functions

Pin No.	Symbol	Function	Circuit configuration
1 30	PA PB	Digital CMOS output port	 A04362
2 29	LVROUT RVROUT	Volume control circuit outputs	 A04363
3 28	LTOUT RTOUT	Tone control circuit outputs	 A04364
4 27	LTCOM RTCOM	Tone control circuit operational amplifier inverting inputs	

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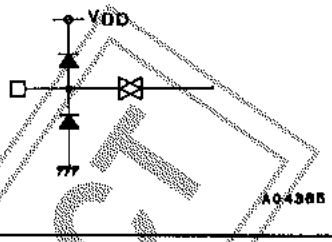
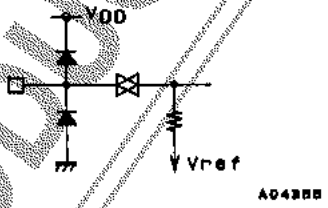
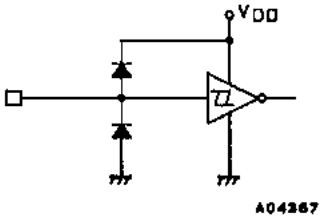
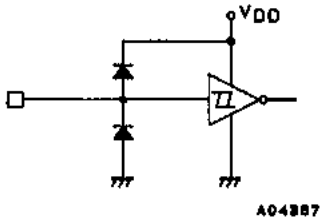
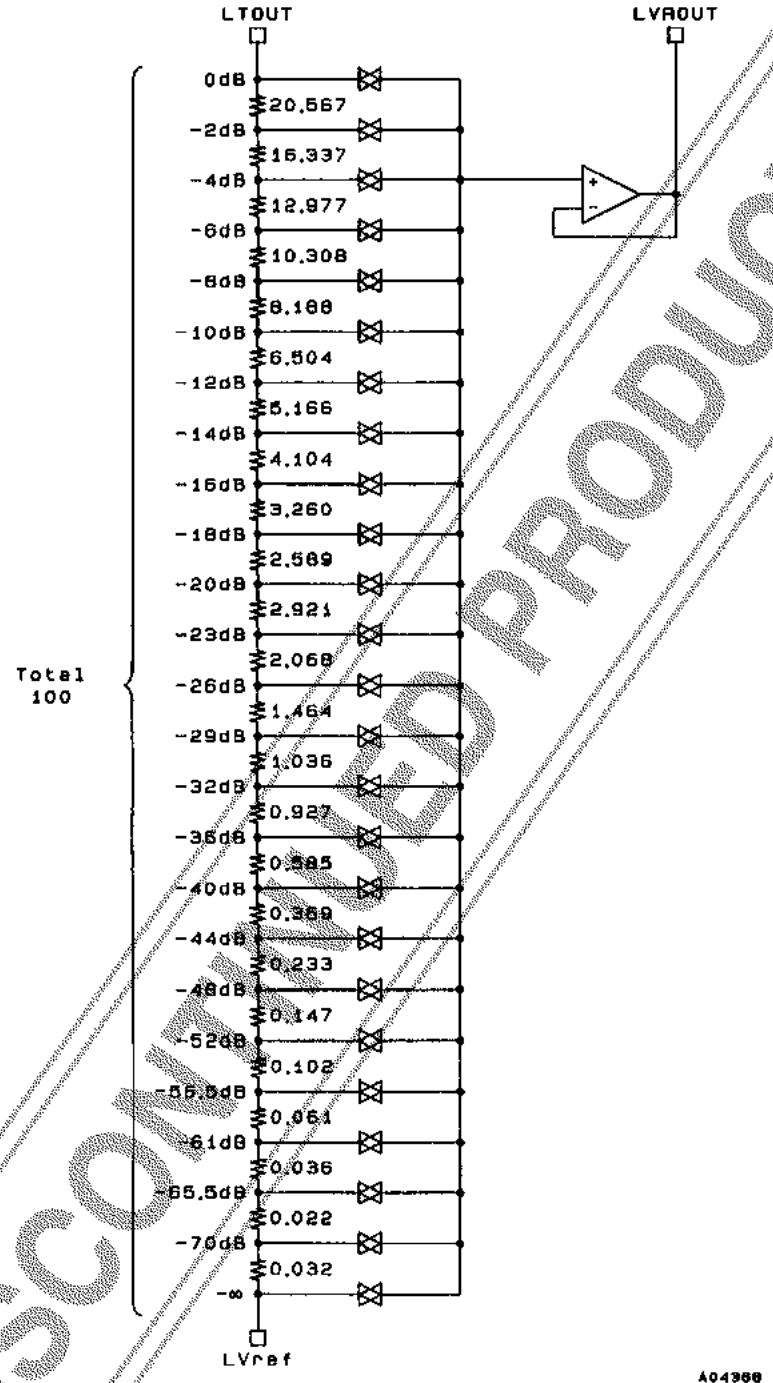
Pin No.	Symbol	Function	Circuit configuration
8 7 6 5 23 24 25 26	LT1 LT2 LT3 LT4 RT1 RT2 RT3 RT4	Connections for the external components that determine the tone control pattern	
12 11 10 9 19 20 21 22	L1 L2 L3 L4 R1 R2 R3 R4	Audio signal inputs and outputs	
13	V_{DD}	Power supply	
18	Vref	Analog system ground	
17	V_{SS}	Ground	
14 15	CL DI	Serial data and clock inputs for device control	
16	CE	Chip enable Data is read into internal latches and all analog switches change state when this input changes from high to low. Data transfer is enabled when this input is high.	

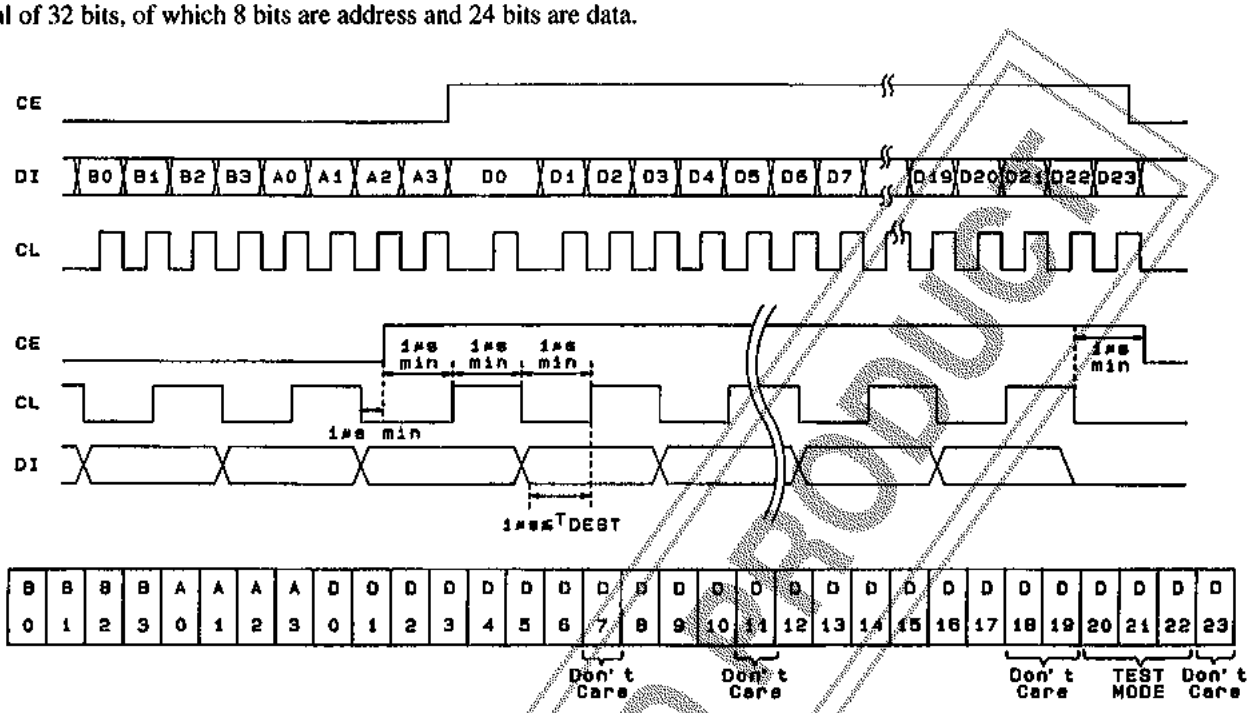
Volume Control Equivalent Circuit



The right channel is identical.
Unit (resistance: kΩ)

Control System Timing and Data Formats

The LC75391 is controlled by applying the stipulated data to the CE, CL, and DI pins. The data structure consists of a total of 32 bits, of which 8 bits are address and 24 bits are data.



B0	B1	B2	B3	A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17	D18	D19	D20	D21	D22	D23
																Don't Care			Don't Care							Don't Care			TEST MODE		Don't Care

Address code

Address code							
B0	B1	B2	B3	A0	A1	A2	A3
0	1	0	0	0	0	0	1

(82HEX)

Volume control data

D2 ~ D6	
00000	−∞
10000	−70dB
01000	−65.5dB
11000	−61dB
00100	−56.5dB
10100	−52dB
01100	−48dB
11100	−44dB
00010	−40dB
10010	−36dB
01010	−32dB
11010	−29dB
00110	−26dB
10110	−23dB
01110	−20dB
11110	−18dB
00001	−16dB
10001	−14dB
01001	−12dB
11001	−10dB
00101	−8dB
10101	−6dB
01101	−4dB
11101	−2dB
00011	0dB

Tone pattern control data

D8	D9	
0	0	T1 ON
1	0	T2 ON
0	1	T3 ON
1	1	T4 ON

Buffer mode

D10	
0	T5 OFF
1	T5 ON

Function switch control data

D12		
0	L1 (R1)	OFF
1	L1 (R1)	ON

D13		
0	L2 (R2)	OFF
1	L2 (R2)	ON

D14		
0	L3 (R3)	OFF
1	L3 (R3)	ON

D15		
0	L4 (R4)	OFF
1	L4 (R4)	ON

General-purpose port (PA) control data

D0	
0	Output low
1	Output high

General-purpose port (PB) control data

D1	
0	Output low
1	Output high

Channel selection

D16	D17	
0	0	
0	1	Lch
1	0	Rch
1	1	Left and right together

Note: The bits D20, D21, and D22 are test mode selection bits. These bits must be set to 0 by user applications.

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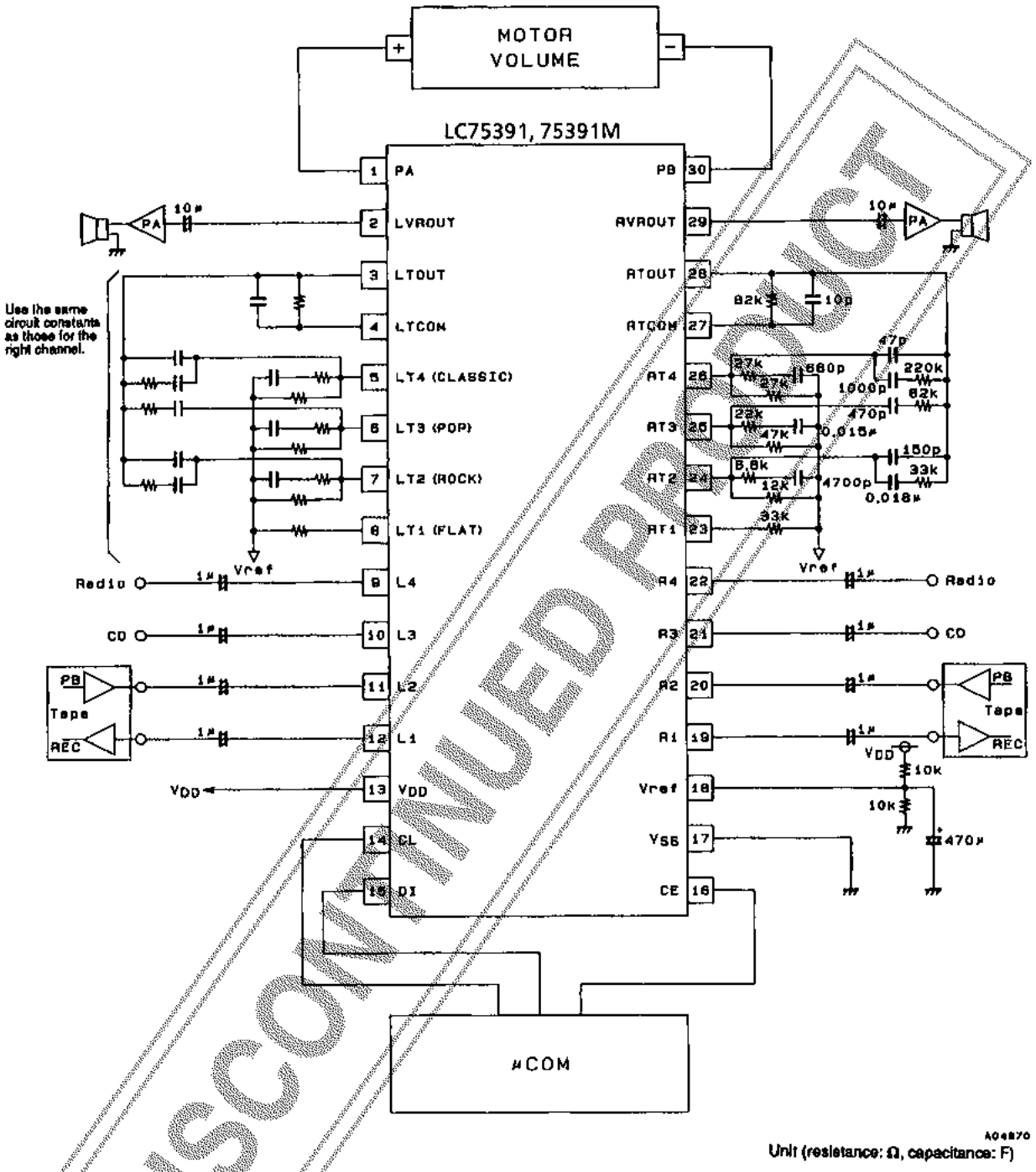
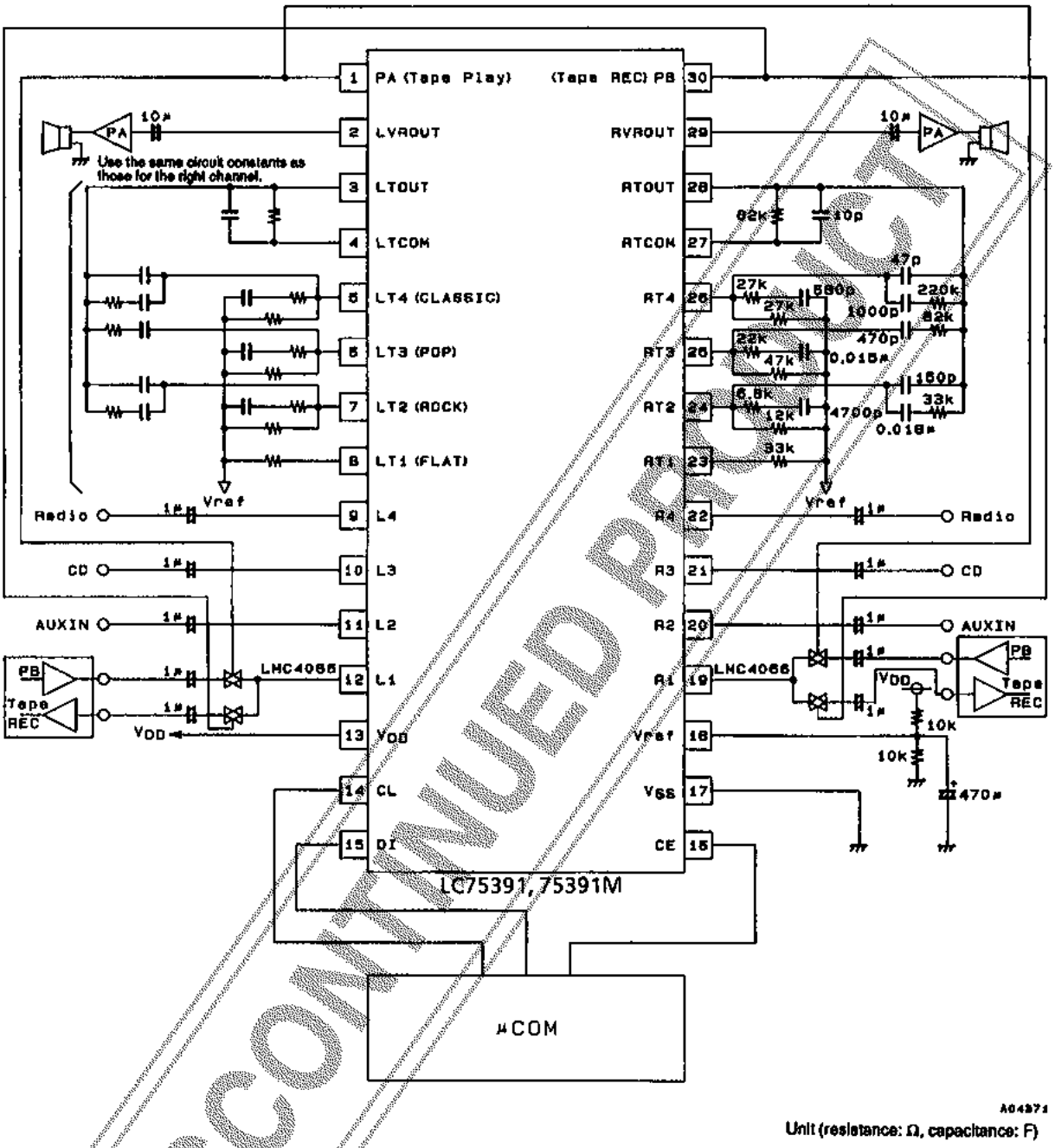
Application Circuit Example 1 (3-input type)



Usage Notes

1. The internal analog switch states are undefined when power is first applied. Signals should be muted externally until the control data has been set up.
2. Cover the CL, DI, and CE pin signal lines with the ground pattern or use shielded cable for those lines to prevent the high-frequency digital signals transmitted to the CL, DI, and CE pins from entering the analog system as noise.
3. Use bipolar capacitors if at all possible for capacitors for which no polarity is indicated.
4. We recommend making large changes in the electronic volume control setting, such as from 0 dB to −∞ dB, by using several intermediate steps as shown in the example below. This can reduce the switching noise associated with large changes.
   Example: 0 dB → −10 dB → −20 dB → −40 dB → −70 dB → −∞

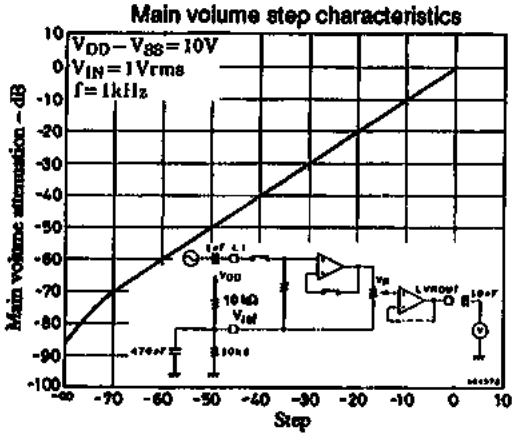
Application Circuit Example 2 (4-input type)



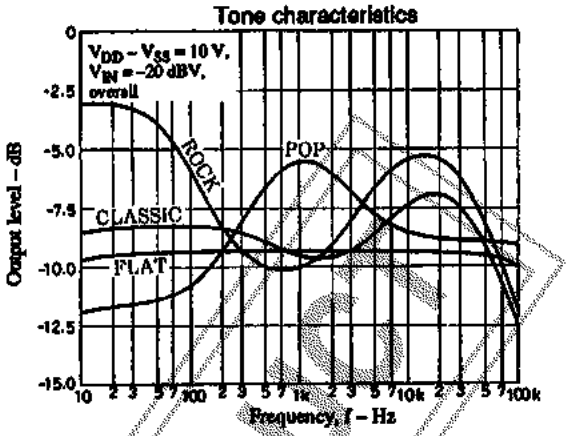
Usage Notes

1. The internal analog switch states are undefined when power is first applied. Signals should be muted externally until the control data has been set up.
2. Cover the CL, DI, and CE pin signal lines with the ground pattern or use shielded cable for those lines to prevent the high-frequency digital signals transmitted to the CL, DI, and CE pins from entering the analog system as noise.
3. If at all possible, use bipolar capacitors for capacitors which have no polarity indicated.
4. We recommend using several intermediate steps as shown in the example below to make large changes in the electronic volume control setting, such as from 0 dB to –∞ dB. This can reduce the switching noise associated with these large changes.
   Example: 0 dB → –10 dB → –20 dB → –40 dB → –70 dB → –∞

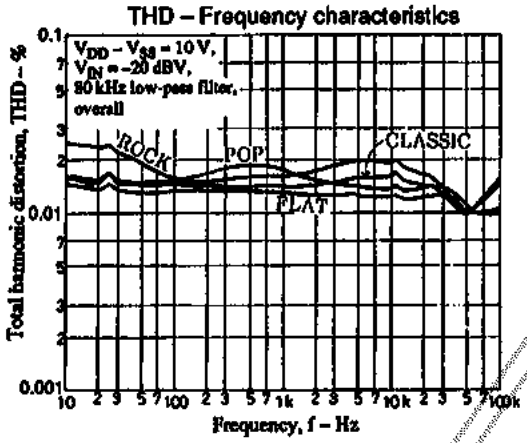
Main volume step characteristics



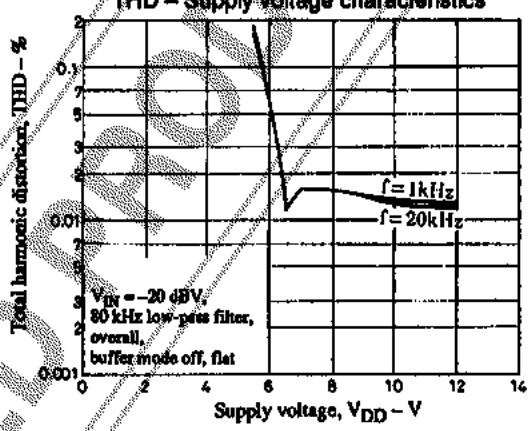
Tone characteristics



THD – Frequency characteristics



THD – Supply voltage characteristics



THD – Input level characteristics