



# LC75383E

## Electronic Volume Control for Car Audio Systems



### Overview

The LC75383E is an electronic volume control that provides volume, balance, fader, bass/treble, input switching and input level controls. The LC75383E supports all these functions while requiring a minimum number of external components.

### Features

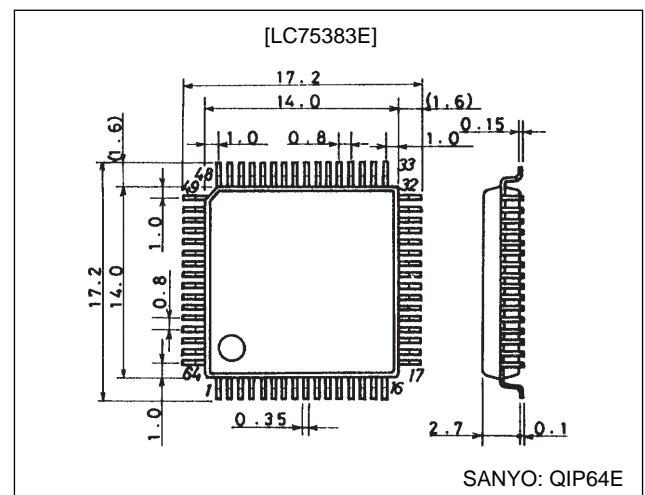
- Volume: 0 dB to -79 dB (in 1 dB steps) and  $-\infty$ ; 81 positions.  
A balance function can be implemented using the LC75383E independent left and right volume control functions.
- Fader: The rear channels or the front channels can be attenuated over 16 positions: from 0 dB to -20 dB in 2 dB steps, from -20 dB to -25 dB in one 5 dB step, from -25 dB to -45 dB in 10 dB steps, -60 dB, and  $-\infty$  for a total of 16 positions.
- Bass/treble: The LC75383E supports 21 position bass and treble controls using external capacitors.
- Input selector: The LC75383E can select one of four L/R inputs. The selected input signal can be amplified from 0 dB to +18 dB in 6 dB steps.
- Built-in operational amplifiers mean that few external components are required.
- Silicon gate process for minimal switching noise.
- All controls can be set from serial input data (CCB).

- CCB is a trademark of SANYO ELECTRIC CO., LTD.
- CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

### Package Dimensions

unit: mm

#### 3159-QFP64E



### Specifications

Absolute Maximum Ratings at  $T_a = 25^\circ\text{C}$ ,  $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\text{ max}}$	$V_{DD}$	12	V
Maximum input voltage	$V_{IN\text{ max}}$	CL, DI, CE, LTIN, RTIN, L10dBIN, R10dBIN, L1dBIN, R1dBIN, LFIN, RFIN, L1 to L4, R1 to R4	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Allowable power dissipation	$P_{d\text{ max}}$	$T_a \leq 85^\circ\text{C}$	310	mW
Operating temperature	$T_{opr}$		-40 to +85	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-50 to +125	$^\circ\text{C}$

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## LC75383E

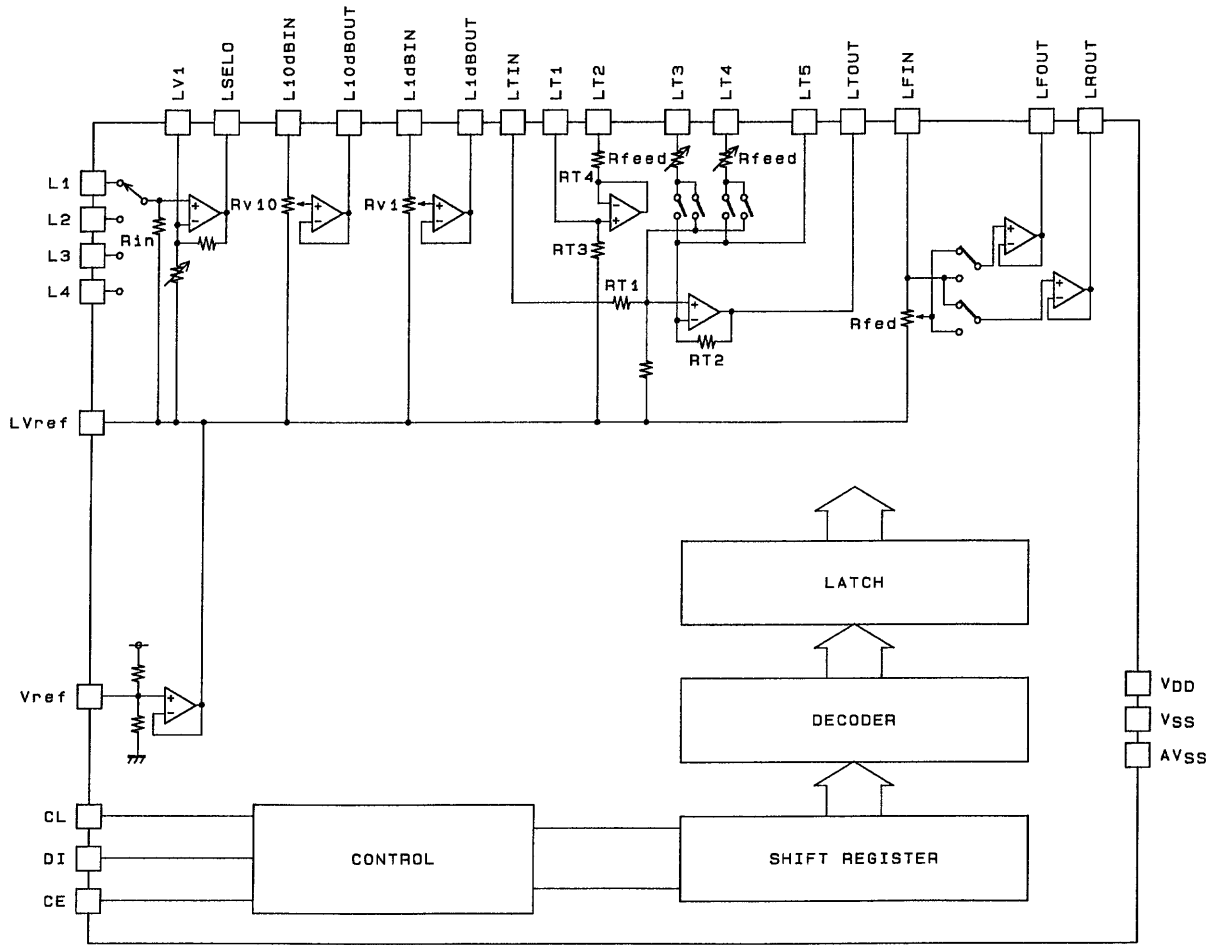
### Allowable Operating Ranges at $T_a = 25^\circ\text{C}$ , $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	$V_{DD}$	$V_{DD}$	6.0		11.0	V
Input high level voltage	$V_{IH}$	CL, DI, CE	4.0		$V_{DD}$	V
Input low level voltage	$V_{IL}$	CL, DI, CE	$V_{SS}$		1.0	V
Input voltage amplitude	$V_{IN}$	LTIN, RTIN, L10dBIN, R10dBIN, L1dBIN, R1dBIN, LFIN, RFIN, L1 to L4, R1 to R4	$V_{SS}$		$V_{DD}$	Vp-p
Input pulse width	$t_{\phi W}$	CL	1			$\mu\text{s}$
Setup time	$t_{SETUP}$	CL, DI, CE	1			$\mu\text{s}$
Hold time	$t_{HOLD}$	CL, DI, CE	1			$\mu\text{s}$
Operating frequency	fopg	CL			500	kHz

### Electrical Characteristics at $T_a = 25^\circ\text{C}$ , $V_{DD} = 9\text{ V}$ , $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	min	typ	max	Unit
[Input Block]						
Input resistance	$R_{in}$	L1, L2, L3, L4, R1, R2, R3, R4		1		M $\Omega$
Clipping level	$V_{cl}$	LSELO, RSELO: THD = 1.0%		2.35		Vrms
Output load resistance	$R_L$	LSELO, RSELO	10			k $\Omega$
Minimum input gain	$G_{in\ min}$		-2	0	+2	dB
Maximum input gain	$G_{in\ max}$		+16.0	+18.0	+20.0	dB
Step resolution	$G_{step}$			+6.0		dB
[Volume Block]						
Input resistance	$R_{v10}$	L10dBIN, R10dBIN: 10 dB steps	21	35	49	k $\Omega$
	$R_{v1}$	L1dBIN, R1dBIN: 1 dB steps	6	10	14	k $\Omega$
Step resolution	$\Delta T_{step}$			1		dB
Step error	$\Delta T_{err}$	Step = 0 to -40 dB, -40 to -60 dB	-1	0	+1	dB
[Fader Volume Block]						
Input resistance	$R_{fed}$	LFIN, RFIN	12	20	28	k $\Omega$
Step resolution	$\Delta T_{step}$	Step = 0 to -20 dB		2		dB
		Step = -20 to -25 dB		5		dB
		Step = -25 to -45 dB		10		dB
Step error	$\Delta T_{err}$	Step = 0 to -40 dB, -40 to -60 dB	-2	0	+2	dB
Output load resistance	$R_L$	LFOUT, LROUT, RFOUT, RROUT	10			k $\Omega$
[Bass/Treble Control Block]						
Control range	$G_{bass}$ $G_{tre}$	Max. boost/cut	$\pm 15$	$\pm 17$	$\pm 19$	dB
Step resolution	$B_{step}$		0.7	1.7	2.7	dB
Internal feedback resistance	$R_{feed}$		46	76	107	k $\Omega$
[Overall]						
Total harmonic distortion	THD (1)	$V_{IN} = 300\text{ mVrms}$ , $f = 1\text{ kHz}$ , all controls flat overall		0.005	0.01	%
	THD (2)	$V_{IN} = 300\text{ mVrms}$ , $f = 20\text{ kHz}$ , all controls flat overall		0.008	0.02	%
Crosstalk	CT	$V_{IN} = 1\text{ Vrms}$ , $f = 1\text{ kHz}$ , all controls flat overall, $R_g = 1\text{ k}\Omega$	60	84.5		dB
Maximum attenuation	$V_o\ min$	$V_{IN} = 1\text{ Vrms}$ , $f = 1\text{ kHz}$ , main volume at $-\infty$	-65	-80		dB
Output noise voltage	$V_N$ (1)	All controls flat overall (IHF-A), $R_g = 1\text{ k}\Omega$		5.2	12	$\mu\text{V}$
	$V_N$ (2)	All controls flat overall (DIN-AUDIO), $R_g = 1\text{ k}\Omega$		7.2	16	$\mu\text{V}$
	$V_N$ (3)	All controls flat overall (NO-FILTER), $R_g = 1\text{ k}\Omega$		9.2	20	$\mu\text{V}$
	$V_N$ (4)	$G_v = +18\text{ dB}$ (IHF-A), $R_g = 1\text{ k}\Omega$		23	50	$\mu\text{V}$
	$V_N$ (5)	Bass = max. boost, treble = max. boost (IHF-A), $R_g = 1\text{ k}\Omega$		48	120	$\mu\text{V}$
Current drain	$I_{DD}$	$V_{DD} - V_{SS} = 11\text{ V}$		28	33	mA
Input high level current	$I_{IH}$	CL, DI, CE, $V_{IN} = 9\text{ V}$			10	$\mu\text{A}$
Input low level current	$I_{IL}$	CL, DI, CE, $V_{IN} = 0\text{ V}$	-10			$\mu\text{A}$

Equivalent Circuit Block Diagram



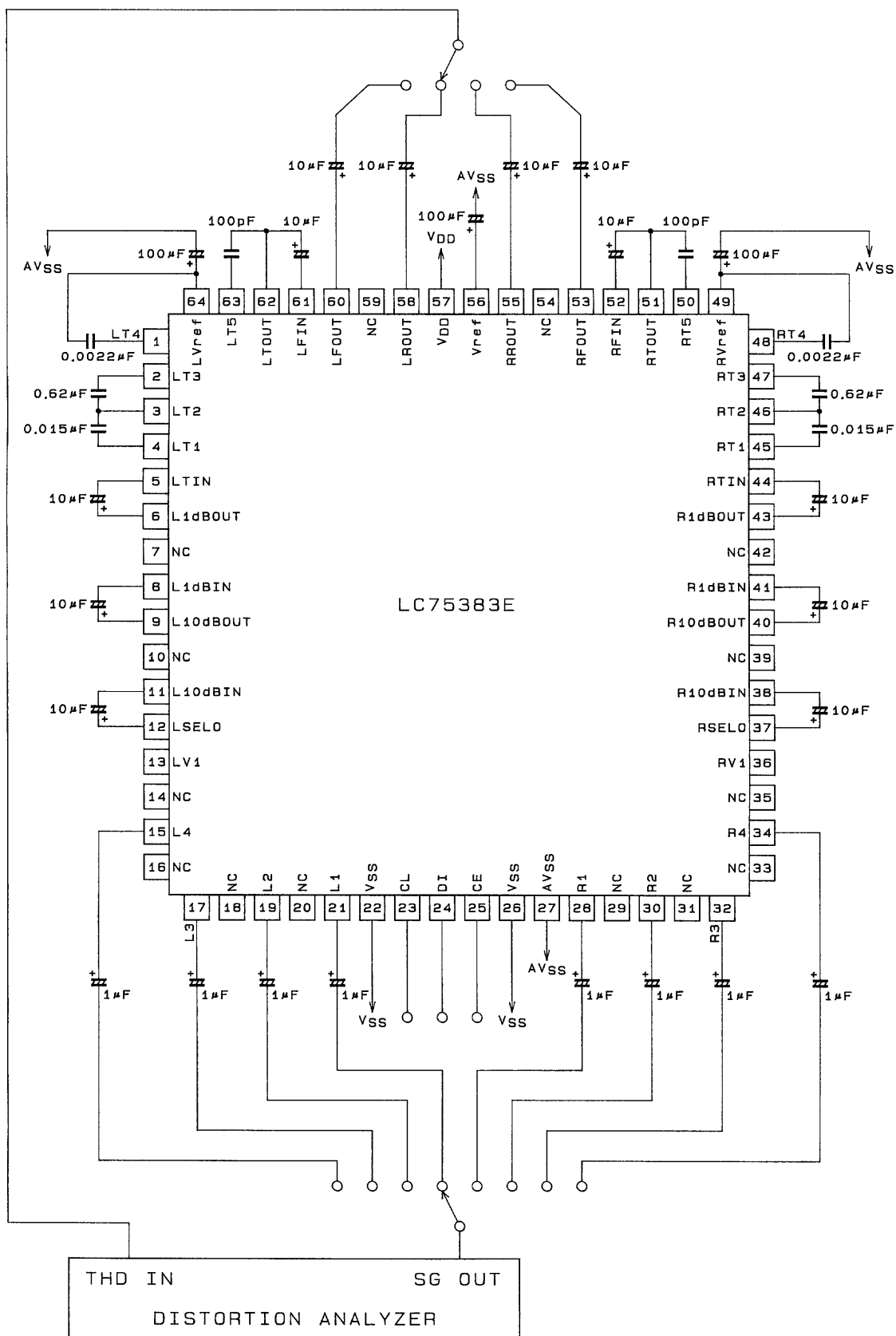
The right channel is identical.

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# LC75383E

## Electrical Characteristics Test Circuits

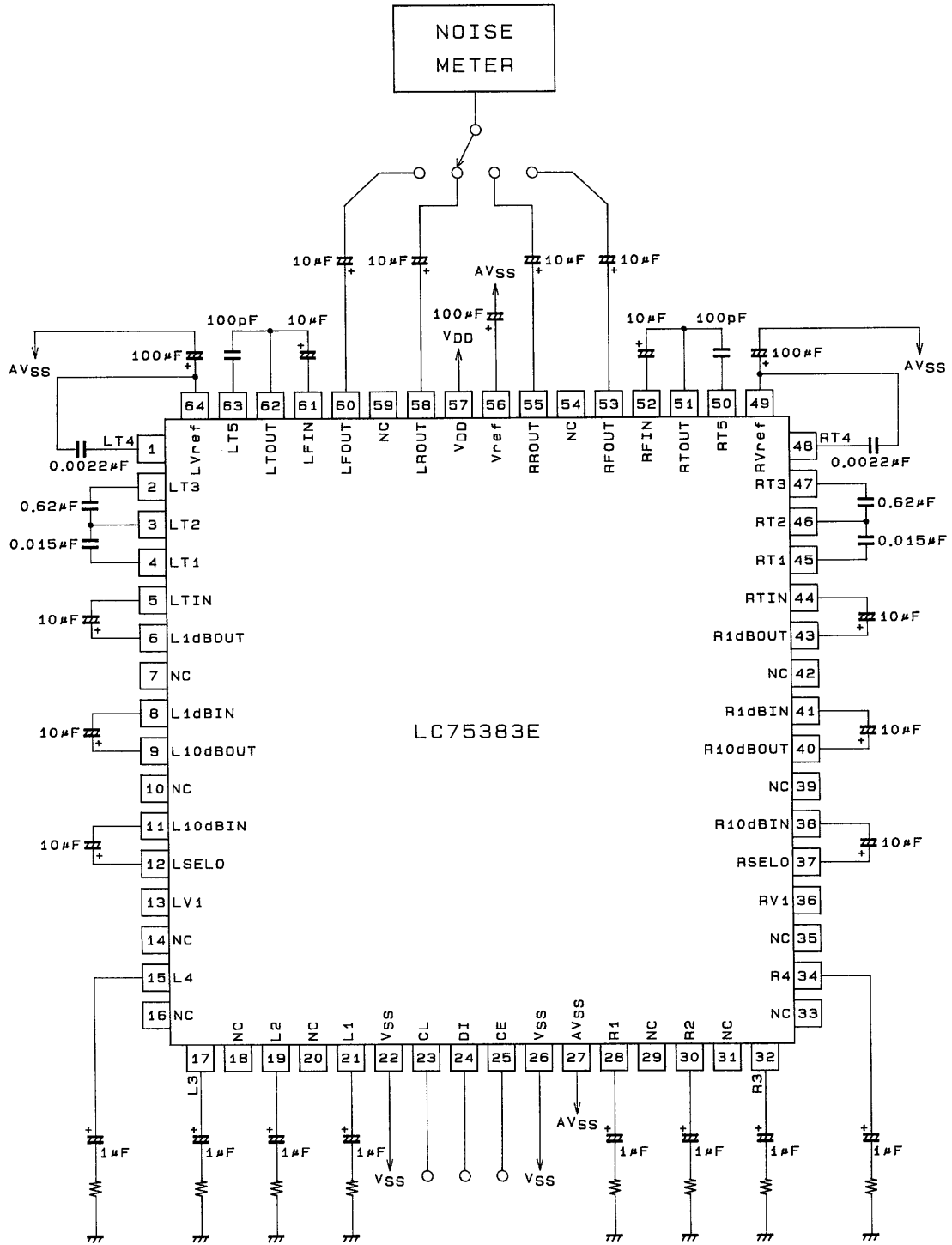
### 1. Total Harmonic Distortion



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# LC75383E

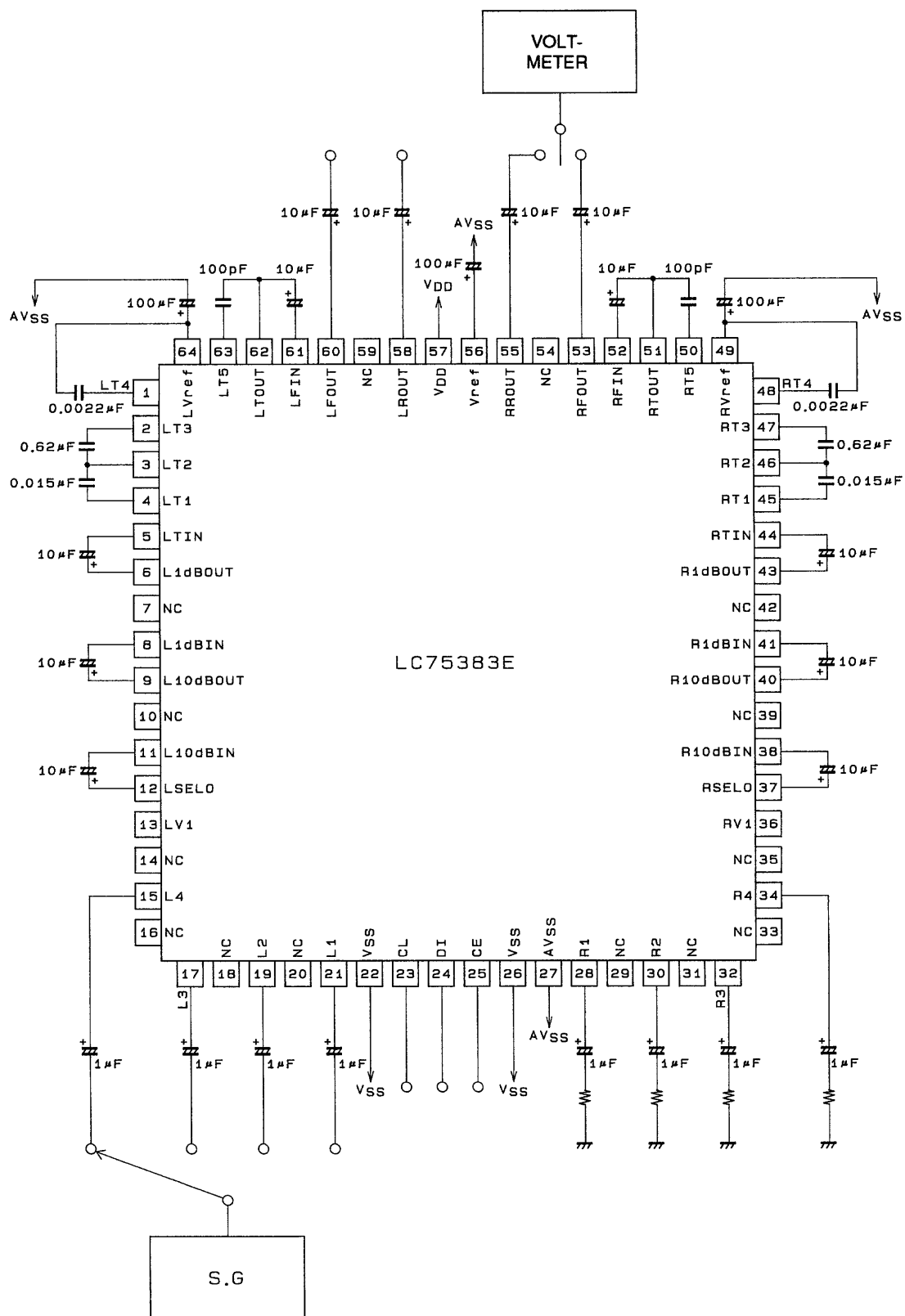
## 2. Output Noise Voltage



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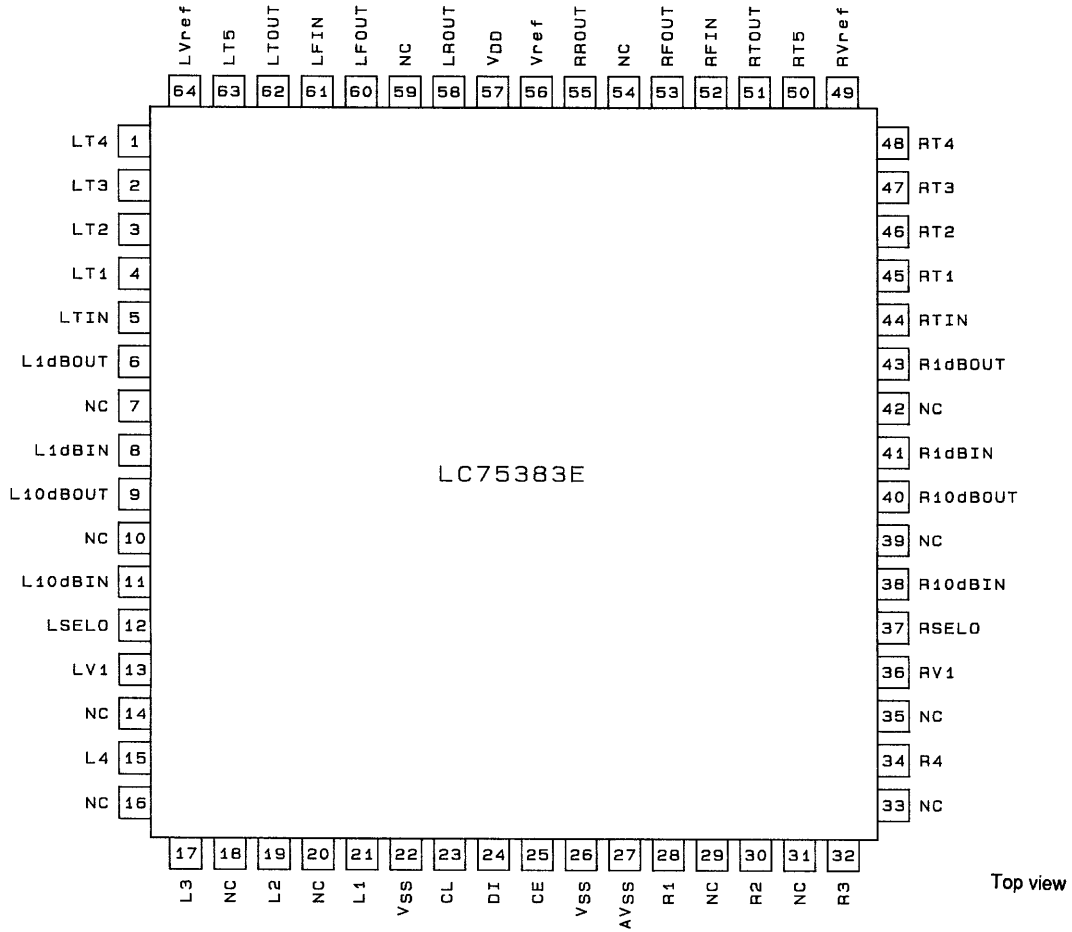
## 3. Crosstalk



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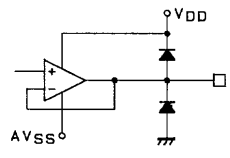
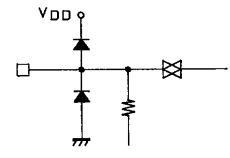
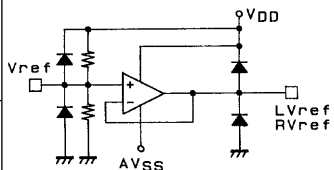
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## Pin Assignment



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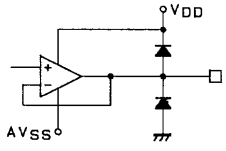
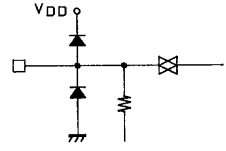
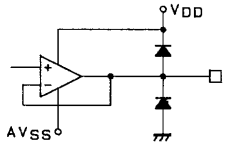
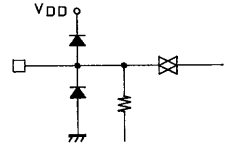
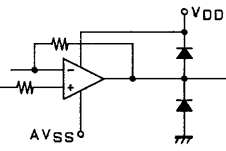
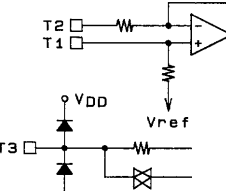
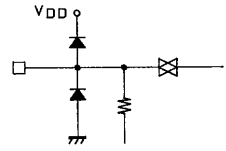
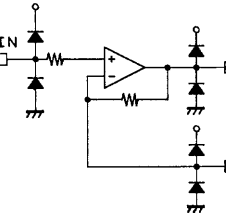
## Pin Functions

Pin No.	Symbol	Function	Note
58 60 55 53	LROUT LFOUT RROUT RFOUT	Fader block outputs. Only the front or rear channels are attenuated. The left and right attenuations are identical. Since these are operational amplifier outputs, the output is low impedance.	 A03374
61 52	LFIN RFIN	Fader block inputs. Must be driven by low impedance circuits.	 A03375
64 49	LVref RVref	Common connections for the main volume, fader block, tone block and gain control block.	 A03376
56	Vref	Capacitors of about 100 μF must be inserted between Vref and AVSS (VSS) to reduce power supply ripple in the V <sub>DD</sub> /2 voltage generation block.	

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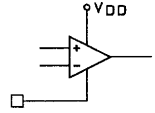
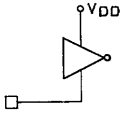
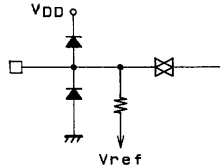
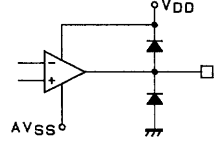
Pin No.	Symbol	Function	Note
6 43	L1dBOUT R1dBOUT	Main volume 1 dB step attenuator outputs	 <p style="text-align: right;">A03374</p>
8 41	L1dBIN R1dBIN	Main volume 1 dB step attenuator inputs Must be driven by low impedance circuits.	 <p style="text-align: right;">A03375</p>
9 40	L10dBOUT R10dBOUT	Main volume 10 dB step attenuator outputs	 <p style="text-align: right;">A03374</p>
11 38	L10dBIN R10dBIN	Main volume 10 dB step attenuator inputs Must be driven by low impedance circuits.	 <p style="text-align: right;">A03375</p>
62 51	LTOUT RTOUT	Tone control outputs	 <p style="text-align: right;">A03377</p>
4 3 2 45 46 47	LT1 LT2 LT3 RT1 RT2 RT3	Connections for the capacitors that form the low frequency (bass) tone control filters Low frequency compensation capacitors must be connected between T1 and T2 and between T2 and T3.	 <p style="text-align: right;">A03378</p>
1 48	LT4 RT4	Connections for the capacitors that form the high frequency (treble) tone control filters High frequency compensation capacitors must be connected between the T4 pins and Vref.	 <p style="text-align: right;">A03375</p>
63 50	LT5 RT5	Inverting inputs for the operational amplifiers that form the tone control circuit filters Unnecessary frequencies can be excluded by inserting capacitors of desired values between the T5 and TOUT pin pairs.	 <p style="text-align: right;">A03379</p>
5 44	LTIN RTIN	Tone control circuit inputs Must be driven by low impedance circuits.	

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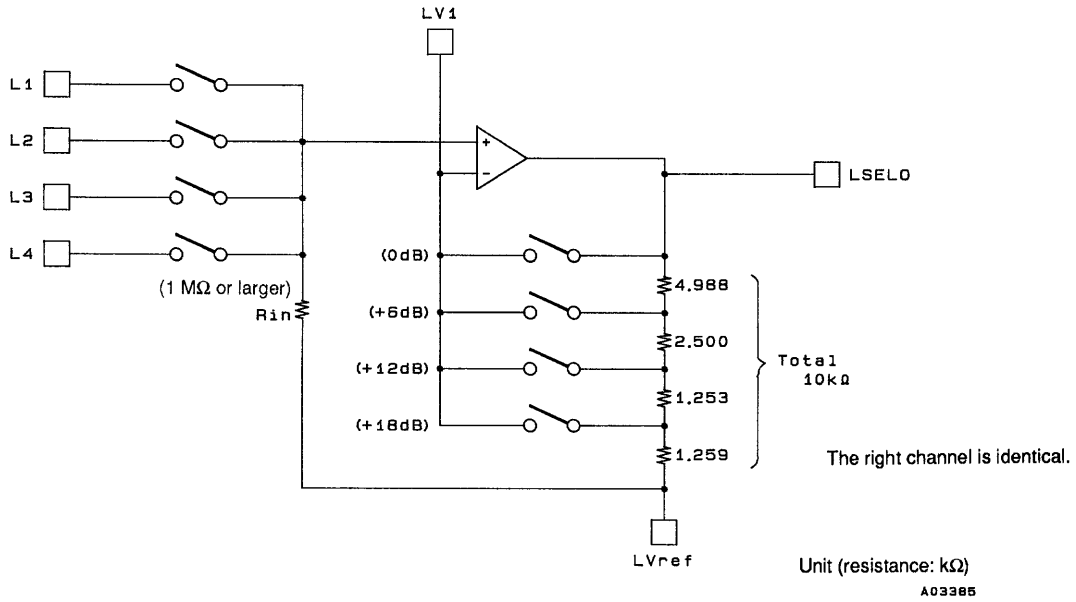
## LC75383E

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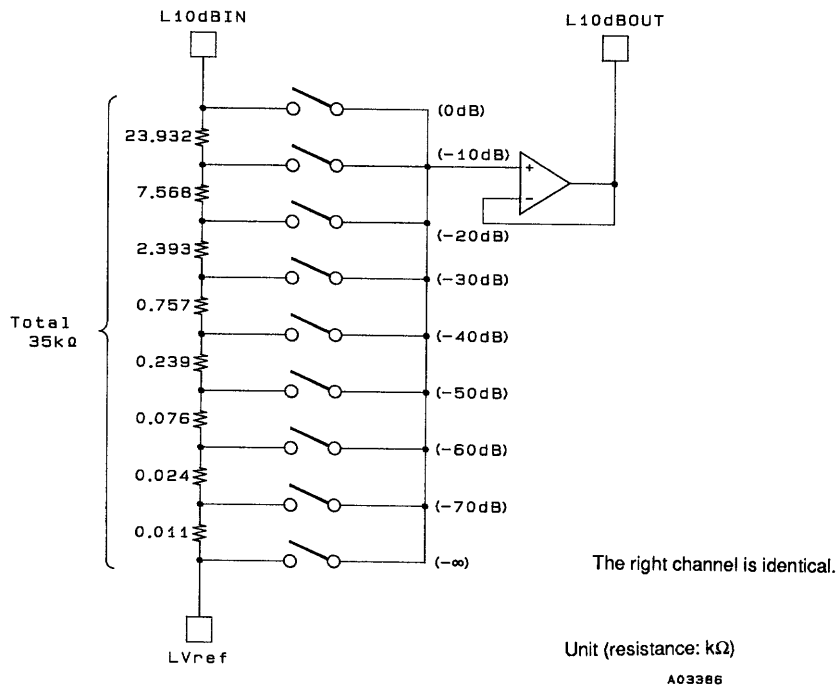
Pin No.	Symbol	Function	Note
57	V <sub>DD</sub>	Power supply	
27	A. V <sub>SS</sub>	Ground for internal operational amplifiers	 A03380
22, 26	V <sub>SS</sub>	Ground for the internal logic system	 A03381
21 19 17 15 28 30 32 34	L1 L2 L3 L4 R1 R2 R3 R4	Audio signal inputs	 A03382
12 37	LSELO RSELO	Input selector outputs	 A03383
25	CE	Chip enable. Data is written to the internal latch when this pin goes from high to low. The analog switches operate at that point also. Data transfer is enabled when this pin is high.	
24 23	DI CL	Serial data and clock pins for IC control	
13 36	LV1 RV1	Test pins. These pins must be left open.	
7, 10, 14, 16, 18, 20, 29, 31, 33, 35, 39, 42, 54, 59	NC	No connection pins. These pins must be left open or tied to V <sub>SS</sub> .	

Equivalent Circuit Details

Input Block Equivalent Circuit

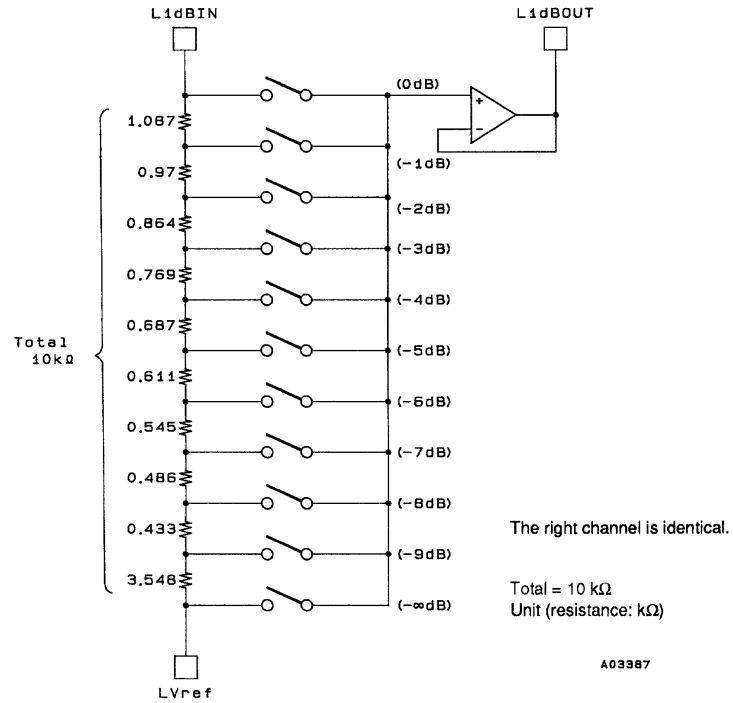


10 dB Step Volume Control Equivalent Circuit

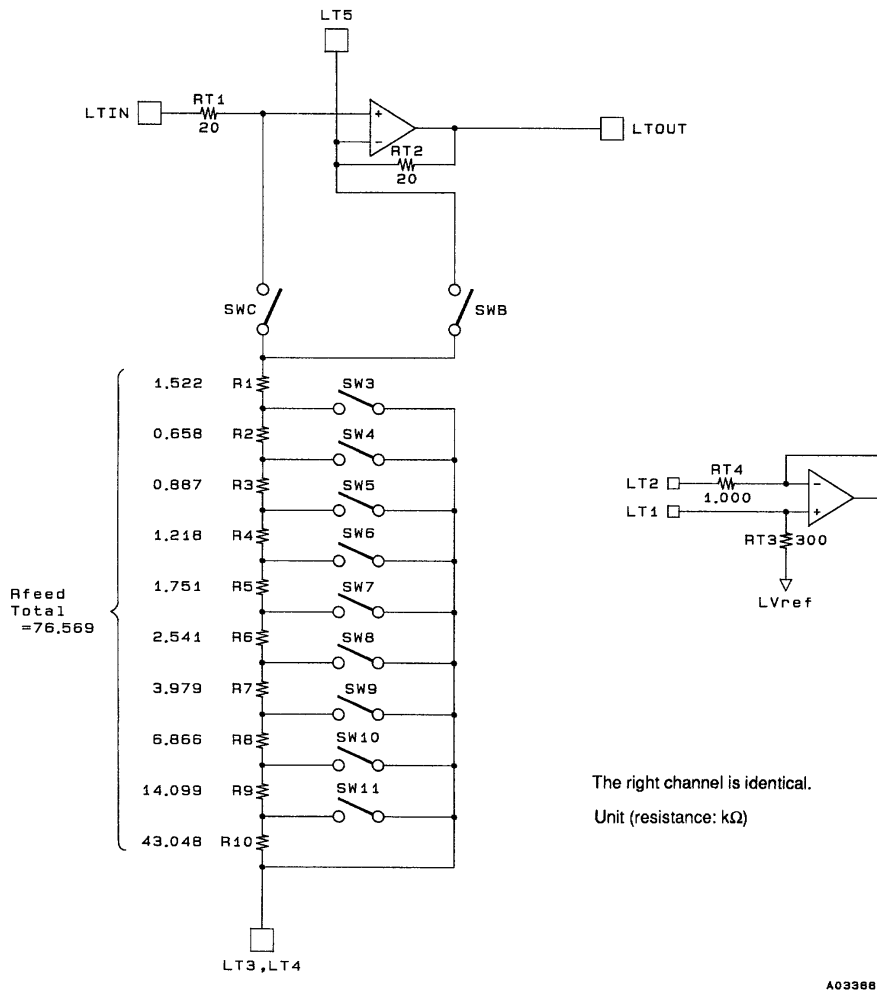


# LC75383E

## 1 dB Step Volume Control Equivalent Circuit



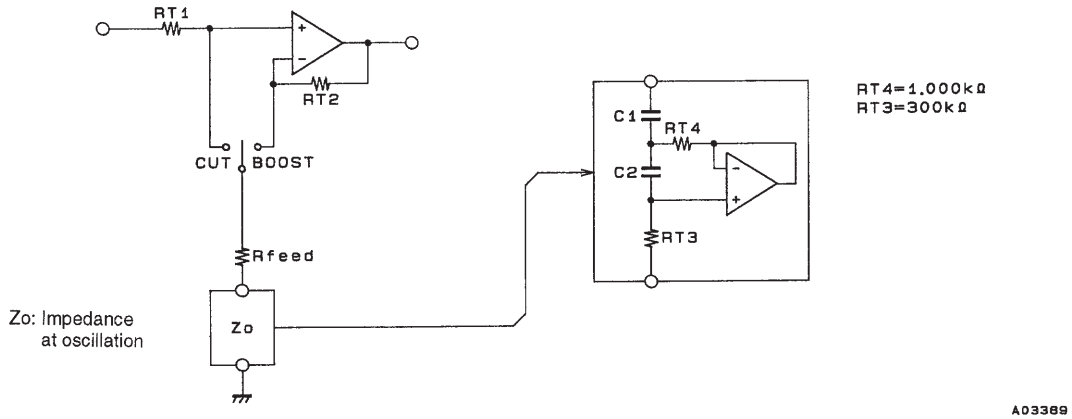
## Tone Block Equivalent Circuit



**Sample Calculation for the Tone Block External Capacitors**

The external capacitors used with the LC75383E are the structural components in semiconductor inductors, i.e., simulated inductors. Here we present the equivalent circuit and the formulas required to acquire the desired center frequency.

1. Semiconductor inductor equivalent circuit



2. Sample calculation

Specifications: 1) Center frequency:  $F_o = 100 \text{ Hz}$

2) Q at maximum boost:  $Q_{\text{max}} = 1.05$

- Derive the sharpness,  $Q_o$ , of the semiconductor inductor itself

$$Q_o = \frac{(RT4 + Rfeed)}{RT4} \times Q_{\text{max}} \approx 2.6481$$

- Calculate C1

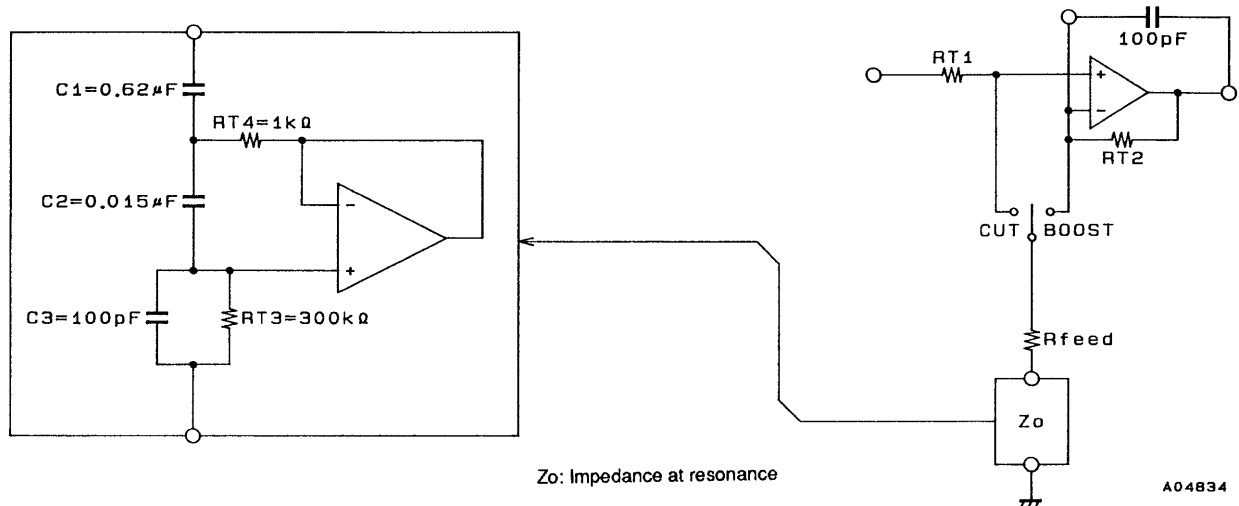
$$C1 = 1/2\pi F_o RT4 Q_o \approx 0.60 \text{ } (\mu\text{F})$$

- Calculate C2

$$C2 = Q_o / 2\pi F_o RT3 \approx 0.014 \text{ } (\mu\text{F})$$

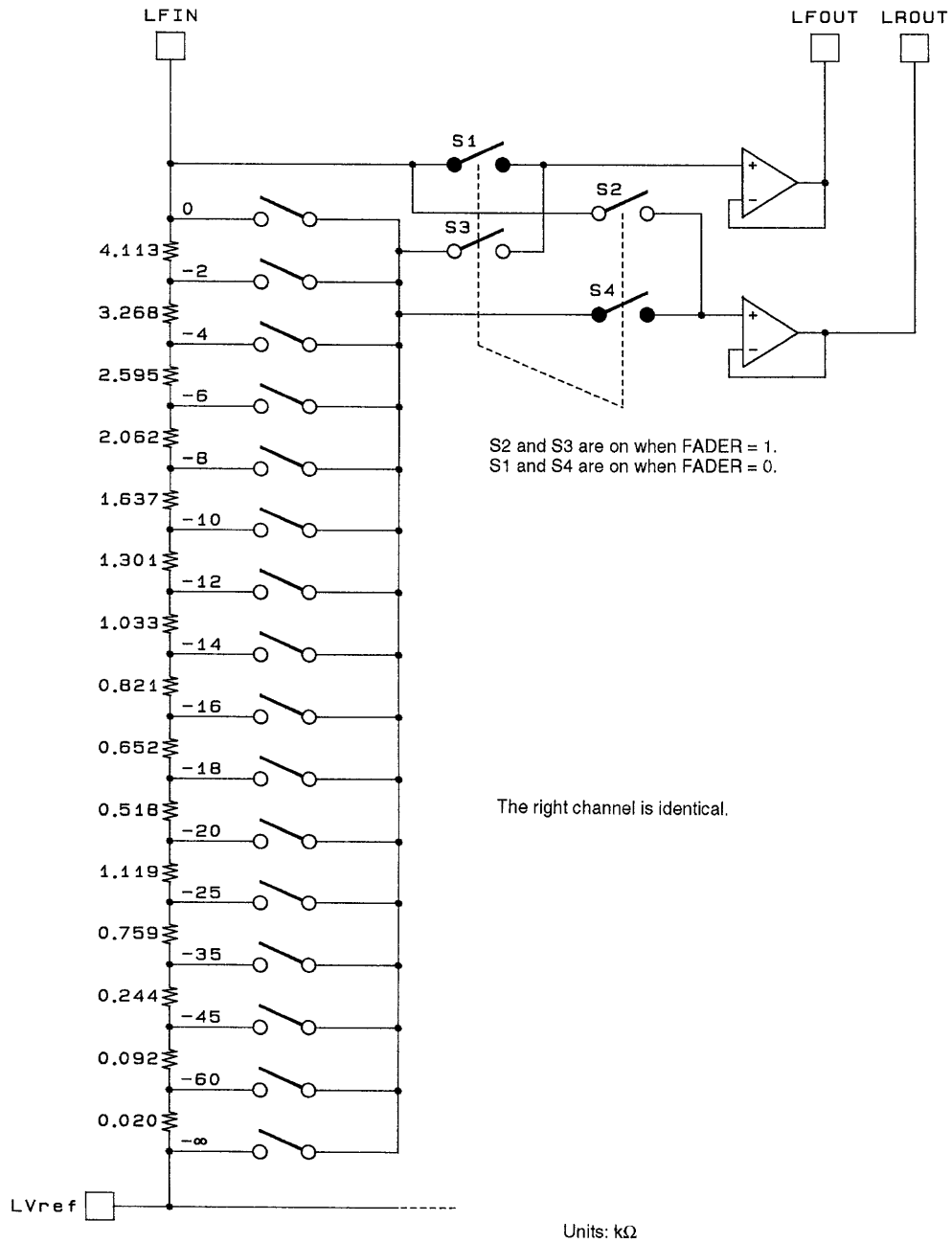
Note: See the tone block equivalent circuit for the internal resistance.

**Technique for Reducing Noise in the Tone Circuit Output**



The output noise can be improved by about 6 dB by providing an external impedance at resonance of  $Z_o$  and adding the capacitor C3 with a value of about 100 pF. An even larger noise reduction effect can be acquired by using a low noise operational amplifier in the external circuit.

Fader Volume Control Equivalent Circuit



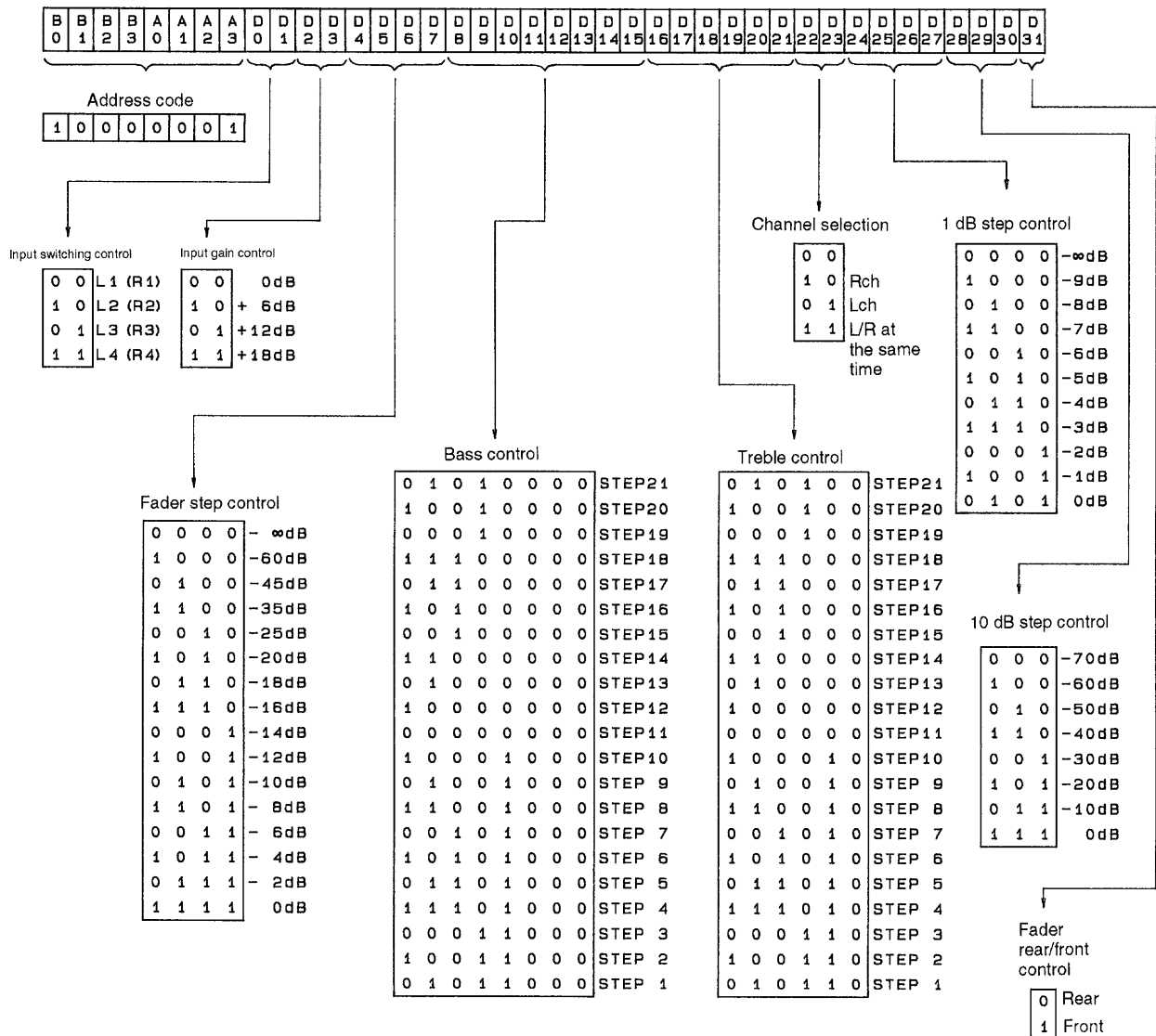
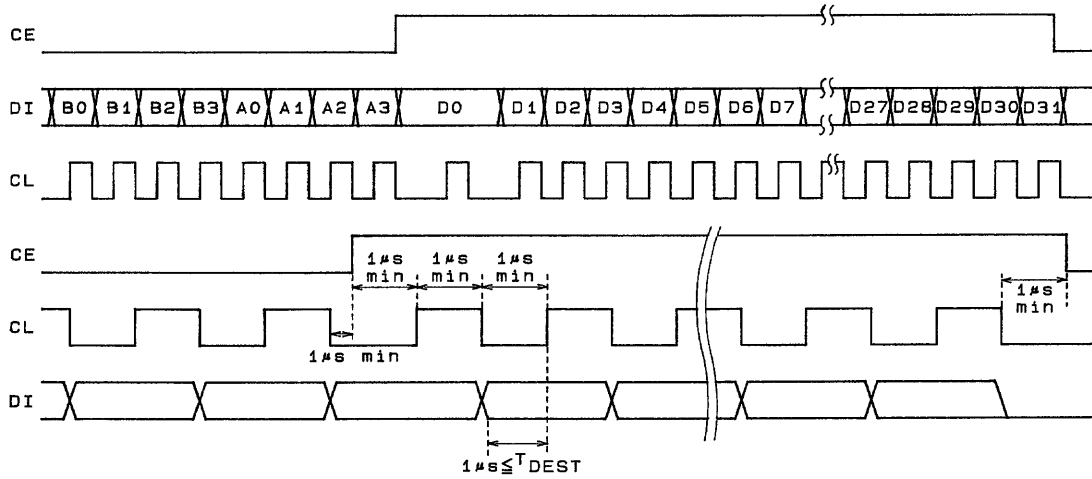
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When the main volume 1dBSTEP setting is set to the data value for  $-\infty$ , S1 and S2 will be open and at the same time S3 and S4 will be on.

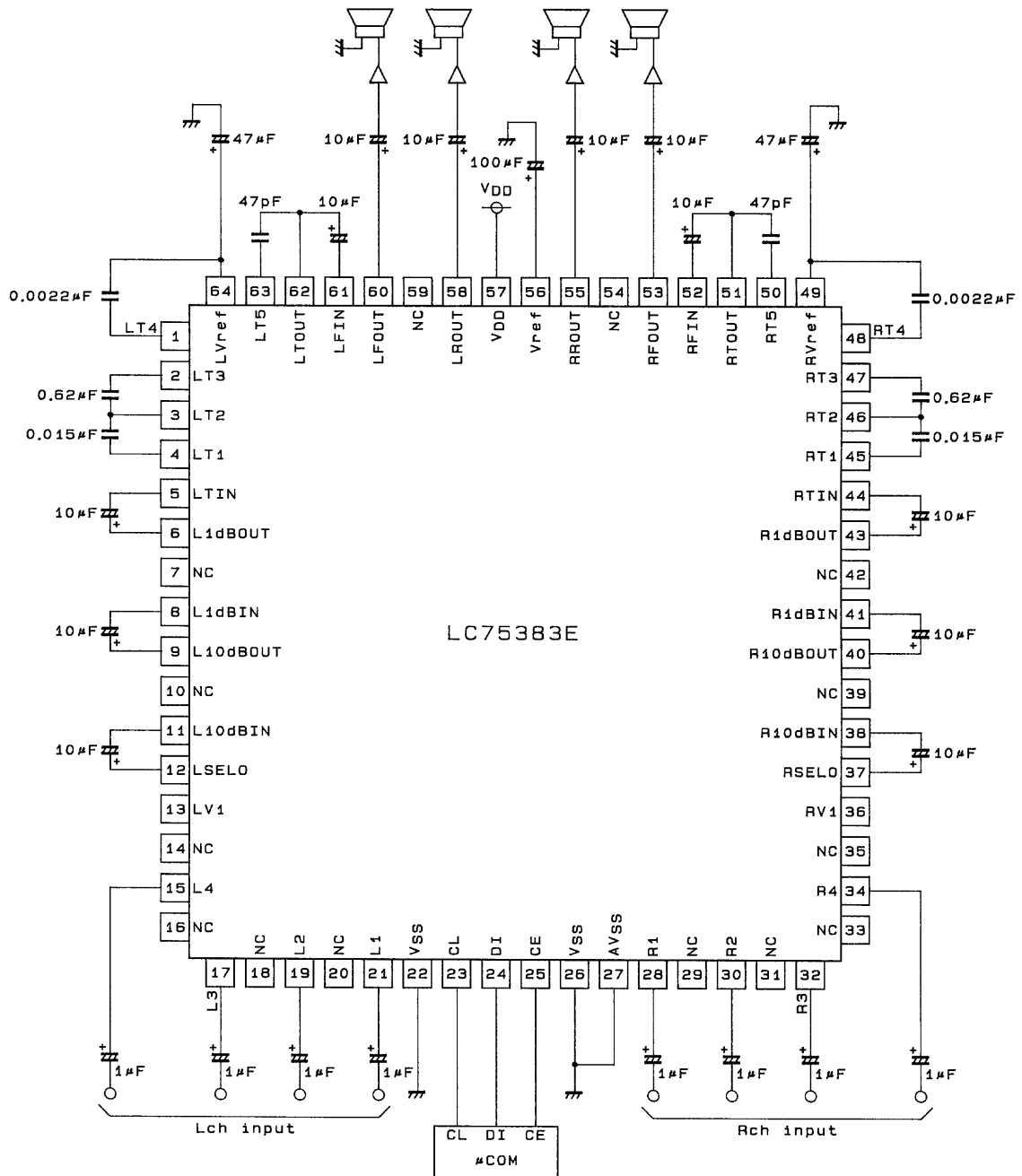
# LC75383E

## Control System Timing and Data Format

The LC75383E is controlled by inputting the stipulated serial data to the CE, CL and DI pins. The data structure consists of a total of 40 bits, of which 8 bits are address and 32 bits are setting data.



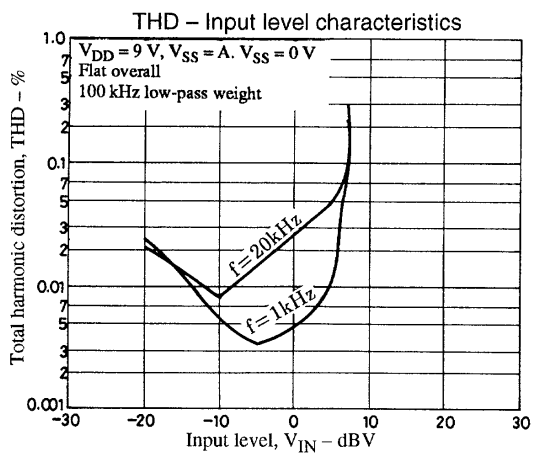
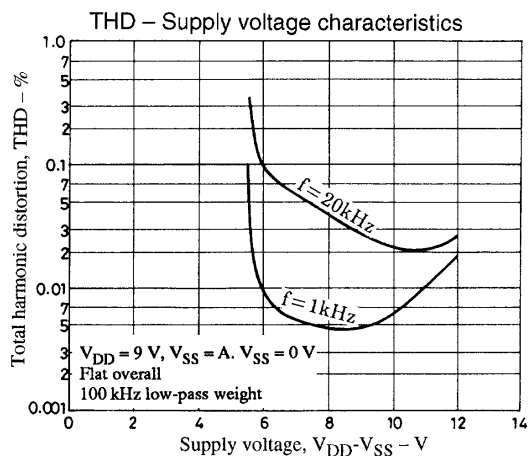
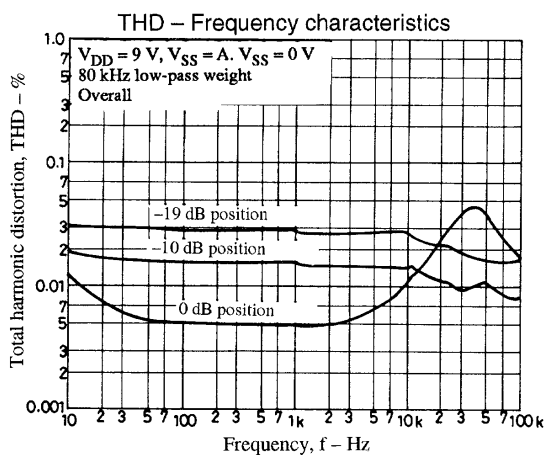
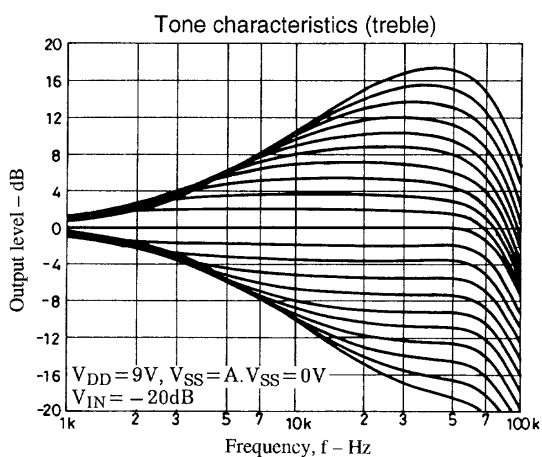
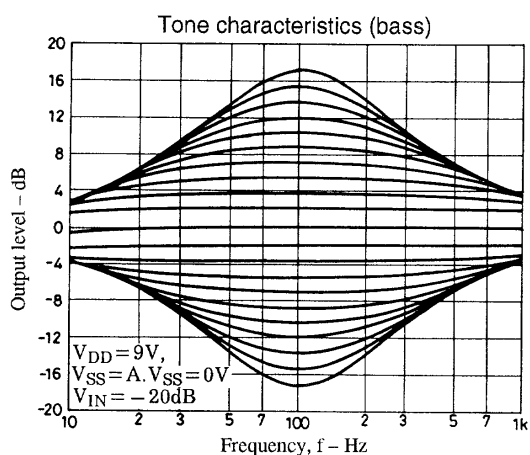
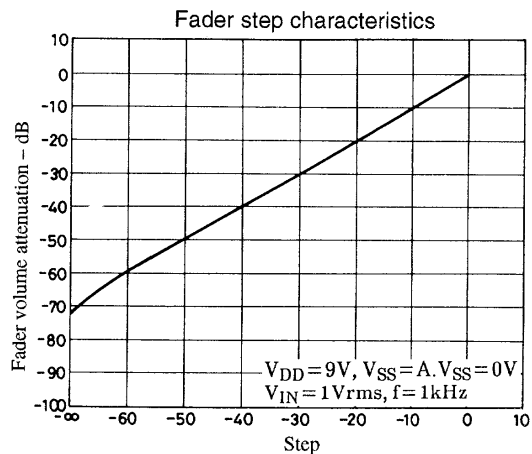
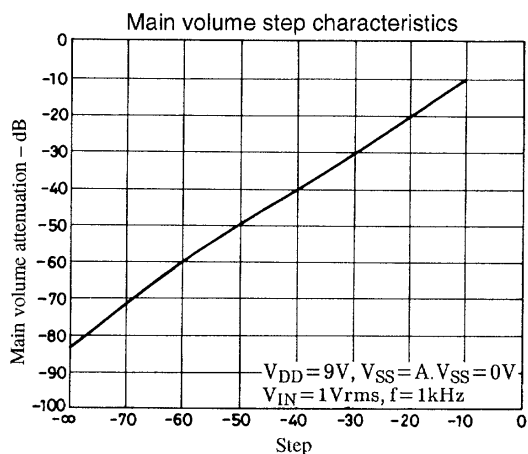
Sample Application Circuit



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Usage Notes

1. The states of the internal analog switches are undefined when power is first applied. Muting should be applied externally until control data has been transferred and stored.
2. The signal lines for the CL, DI and CE pins should either be covered by the pattern ground or be formed from shielded cable to prevent the high-frequency digital signals transmitted over these lines from entering the analog system.





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