



LC75371M

Car Stereo Electronic Tone and Volume Control



Overview

The LC75371M is an electronic tone/volume control LSI that can implement, with minimal external components, volume, balance, fader, bass and treble, loudness, input switching, and input level controls.

Functions

- Volume control: From 0 to -79 dB in 1-dB steps plus $-\infty$ for a total of 81 settings. Since the left and right levels can be set independently, this function can also be used to implement a balance function.
- Fader: Attenuates either the rear or front channels to one of 16 levels. (Provides 16 settings, namely, from 0 to -20 dB in 2-dB steps, from -20 to -25 dB in one 5-dB step, from -25 to -45 dB in 10-dB steps, -60 dB, and $-\infty$.)
- Bass and treble controls: Forms an NF-type tone control circuit (LUX type) using external capacitors. Provides 15 settings each for the bass and treble controls.
- Loudness control: A loudness function can be implemented by attaching external RC circuits at the taps provided from the volume control resistor ladder starting at the -20-dB position.
- The input signal can be selected from one of three inputs for each of the left and right channels. The input signal can be amplified by between 0 and +18 dB in 6-dB steps.
- Serial data input: Supports CCB* format communication with the system controller.

Features

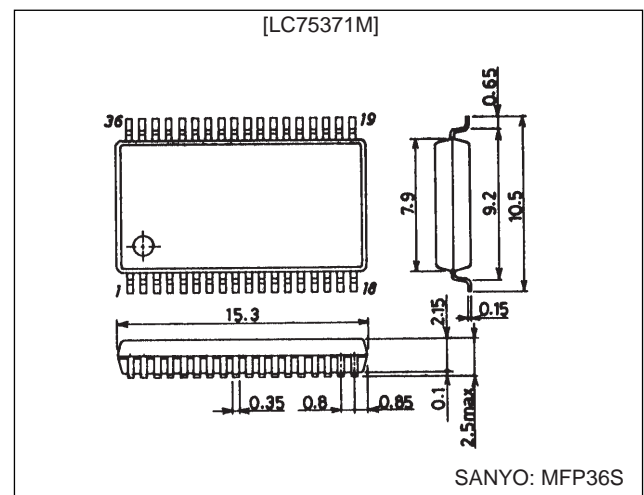
- Built-in buffer amplifiers allow applications to be implemented with few external components.
- A $V_{DD}/2$ reference voltage generation circuit is provided on chip.

- CCB is a trademark of SANYO ELECTRIC CO., LTD.
- CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

Package Dimensions

unit: mm

3204-MFP36S



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Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\text{ max}}$	V_{DD}	12	V
Maximum input voltage	$V_{IN\text{ max}}$	CL, DI, CE, LIN, RIN, LFIN, RFIN, L1 to L3, R1 to R3	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Allowable power dissipation	$Pd\text{ max}$	$T_a \leq 85^\circ\text{C}$	230	mW
Operating temperature	T_{opr}		-40 to +85	$^\circ\text{C}$
Storage temperature	T_{stg}		-50 to +125	$^\circ\text{C}$

Allowable Operating Ranges at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}	V_{DD}	6.0		11.0	V
Input high-level voltage	V_{IH}	CL, DI, CE	4.0		V_{DD}	V
Input low-level voltage	V_{IL}	CL, DI, CE	V_{SS}		1.0	V
Input voltage amplitude	V_{IN}	CL, DI, CE, LIN, RIN, LFIN, RFIN, L1 to L3, R1 to R3	V_{SS}		V_{DD}	Vp-p
Input pulse width	t_{pW}	CL	1			μs
Setup time	t_{setup}	CL, DI, CE	1			μs
Hold time	t_{hold}	CL, DI, CE	1			μs
Operating frequency	f_{opg}	CL			500	kHz

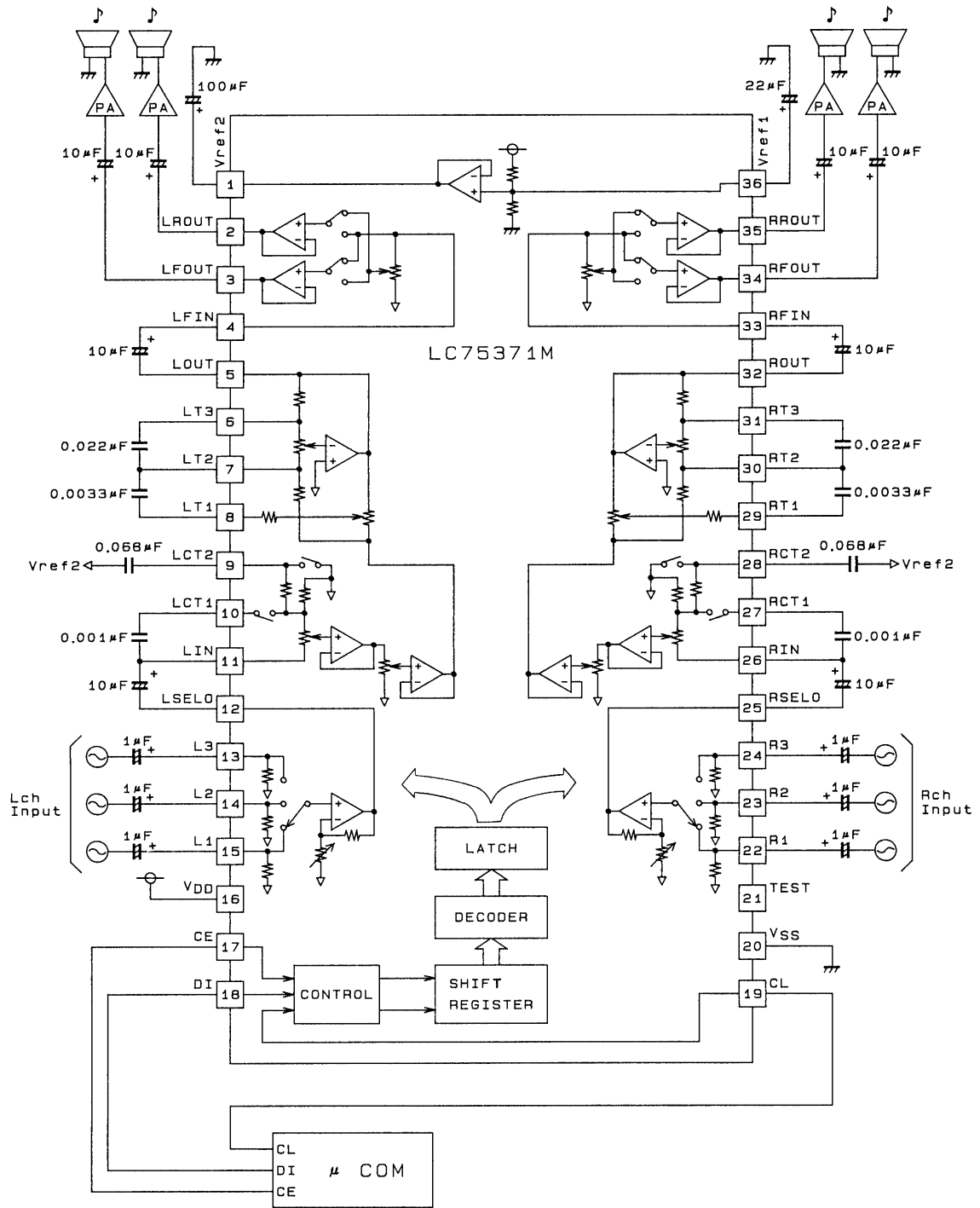
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Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{DD} = 9\text{ V}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	min	typ	max	Unit
[Input Block]						
Input resistance	R _{in}	L1 to L3, R1 to R3	30	50	70	k Ω
Minimum input gain	G _{in min}		-2	0	+2	dB
Maximum input gain	G _{in max}		+16.0	+18.0	+20.0	dB
Step resolution	G _{step}			+6.0		dB
[Volume Control Block]						
Input resistance	R _{v10}	LIN, RIN: 10-dB steps, loudness off	30	50	70	k Ω
	R _{v1}	1-dB steps	6	10	14	k Ω
Step resolution	A _T step			1		dB
Step error	A _T err	step = 0 to -20 dB	-1	0	+1	dB
		step = -20 to -50 dB	-3	0	+3	dB
[Fader Block]						
Input resistance	R _{fed}	LFIN, RFIN	12	20	28	k Ω
Step resolution	A _T step	step = 0 to -20 dB		2		dB
		step = -20 to -25 dB		5		dB
		step = -25 to -45 dB		10		dB
Step error	A _T err	step = 0 to -45 dB	-2	0	+2	dB
		step = -45 dB	-3	0	+3	dB
Output load resistance	R _L	LFOUT, LROUT, RFOUT, RROUT	20			k Ω
[Bass and Treble Control Block]						
Bass control range	G _{bass}	Max. boost/cut	± 9	± 10.5	± 12	dB
Treble control range	G _{tre}	Max. boost/cut	± 8	± 10.5	± 13	dB
[Overall Characteristics]						
Total harmonic distortion	THD1	V _{IN} = 1 V _{rms} , f = 1 kHz, all settings flat overall		0.045		%
	THD2	V _{IN} = 1 V _{rms} , f = 20 kHz, all settings flat overall		0.045		%
Crosstalk	CT	V _{IN} = 1 V _{rms} , f = 1 kHz, all settings flat overall, R _g = 1 k Ω		70		dB
Output at maximum attenuation	V _{O min}	V _{IN} = 1 V _{rms} , f = 1 kHz, main volume control at $-\infty$		-76		dB
		V _{IN} = 1 V _{rms} , f = 1 kHz, main volume control at $-\infty$, INMUTE		-80		dB
Output noise voltage	V _{N1}	All settings flat overall (IHF-A), R _g = 1 k Ω		12	30	μV
	V _{N2}	All settings flat overall (DIN-AUDIO), R _g = 1 k Ω		16	40	μV
Current drain	I _{DD}	V _{DD} - V _{SS} = 11 V		19	22.8	mA
Input high-level current	I _{IH}	CL, DI, CE: V _{IN} = 9 V			10	μA
Input low-level current	I _{IL}	CL, DI, CE: V _{IN} = 0 V	-10			μA
Maximum input level	V _{CL}	THD = 1%, R _L = 20 k Ω , all tsettings flat overall, test point = fader output.		2		V _{rms}

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Equivalent Circuit Block Diagram and Sample Application Circuit

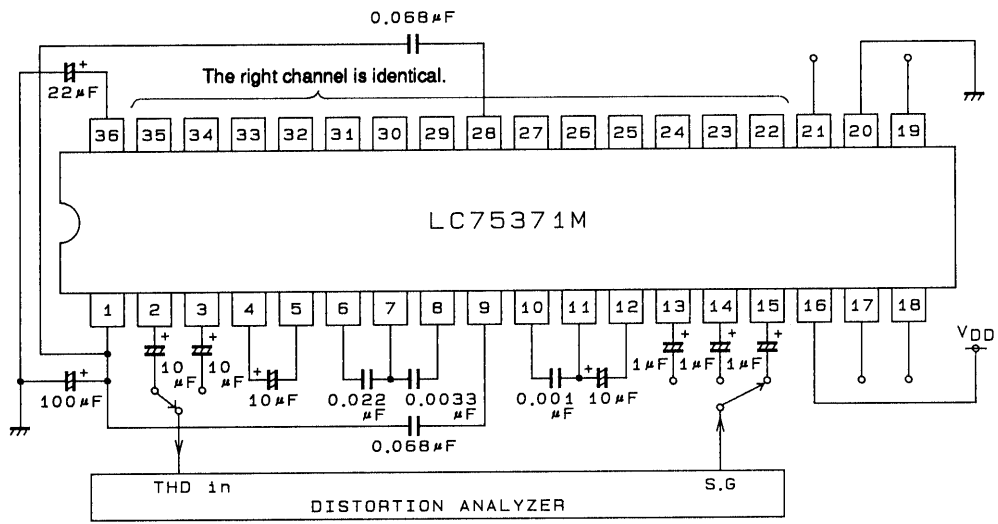


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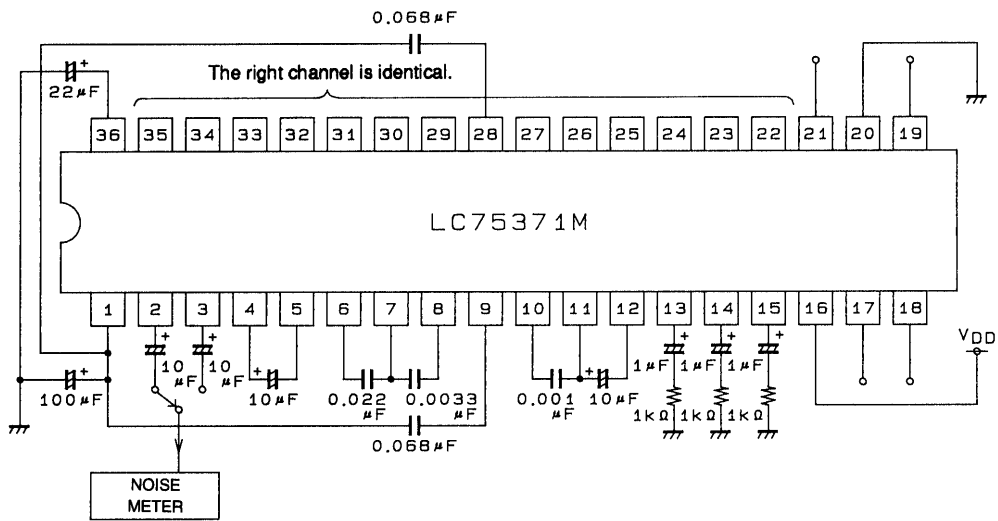
Test Circuits

1. Total harmonic distortion



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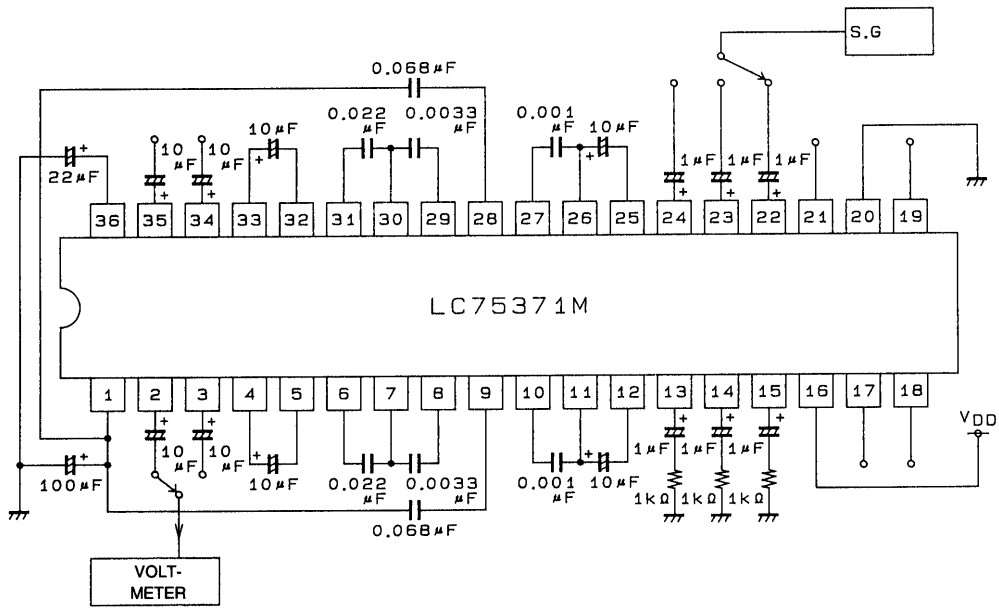
2. Output noise voltage



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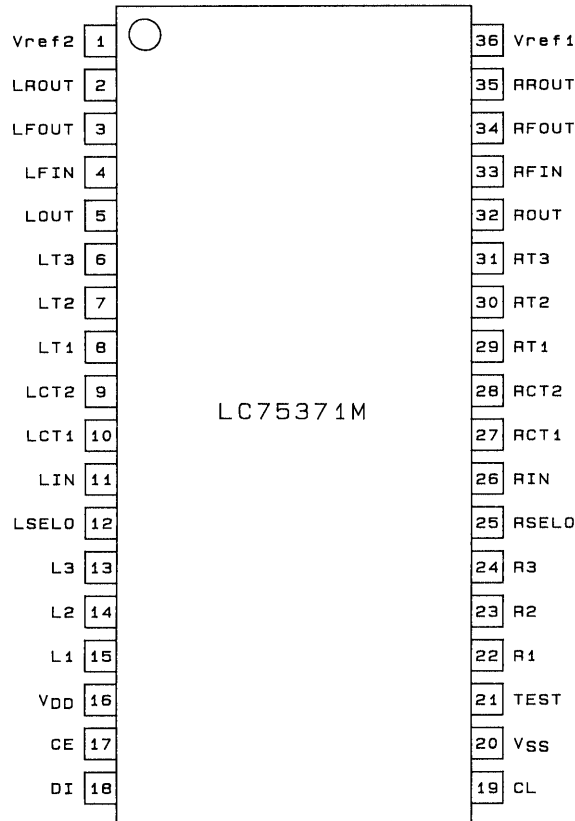
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3. Crosstalk



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Pin Assignment



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Top view

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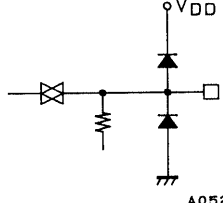
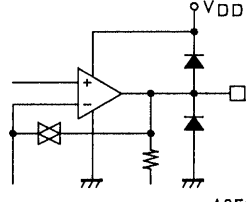
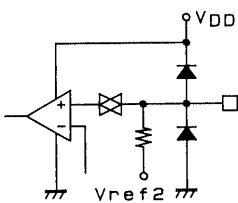
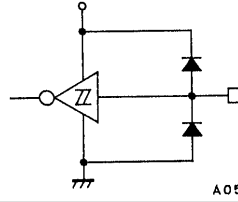
Pin Functions

Pin No.	Symbol	Function	Notes
1	Vref2	<ul style="list-style-type: none"> Common pin for the main volume control block, fader block, tone control block, gain control block, and input switching block. Since the capacitor connected between Vref2 and V_{SS} becomes the residual resistance when the volume control is set to maximum attenuation, the value of this capacitor must be selected carefully. The voltage applied to this pin must never exceed V_{DD}. 	<p style="text-align: right;">A05229</p>
36	Vref1	$V_{DD}/2$ voltage generation block. A capacitor must be connected between Vref1 and V_{SS} to suppress power supply ripple.	<p style="text-align: right;">A05230</p>
2 3 35 34	LROUT LFOUT RROUT RFOUT	<ul style="list-style-type: none"> Fader outputs. The front and rear can be attenuated independently. The left and right attenuation levels are identical. These are low-impedance outputs, since they have built-in operational amplifiers. 	<p style="text-align: right;">A05231</p>
4 33	LFIN RFIN	<ul style="list-style-type: none"> Fader inputs These inputs must be driven by low-impedance outputs. 	<p style="text-align: right;">A05232</p>
5 32	LOUT ROUT	Tone control outputs	<p style="text-align: right;">A05233</p>
8 7 6 29 30 31	LT1 LT2 LT3 RT1 RT2 RT3	Connections for the bass and treble supplementary capacitors for the tone control circuit Connect high-frequency compensation capacitors between the T1/T2 pairs. Connect low-frequency compensation capacitors between the T2/T3 pairs.	<p style="text-align: right;">A05234</p>
10 9 27 28	LCT1 LCT2 RCT1 RCT2	Loudness circuit connections. Connect high-frequency compensation capacitors between the LCT1/RCT1 and LIN/RIN pins, and connect low-frequency compensation capacitors between LCT2/RCT2 and Vref2.	

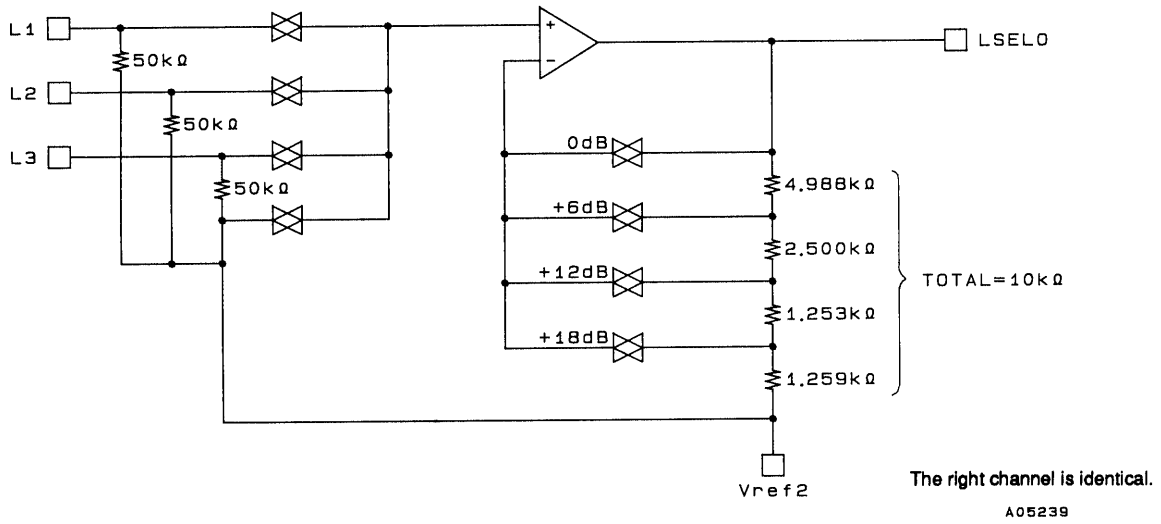
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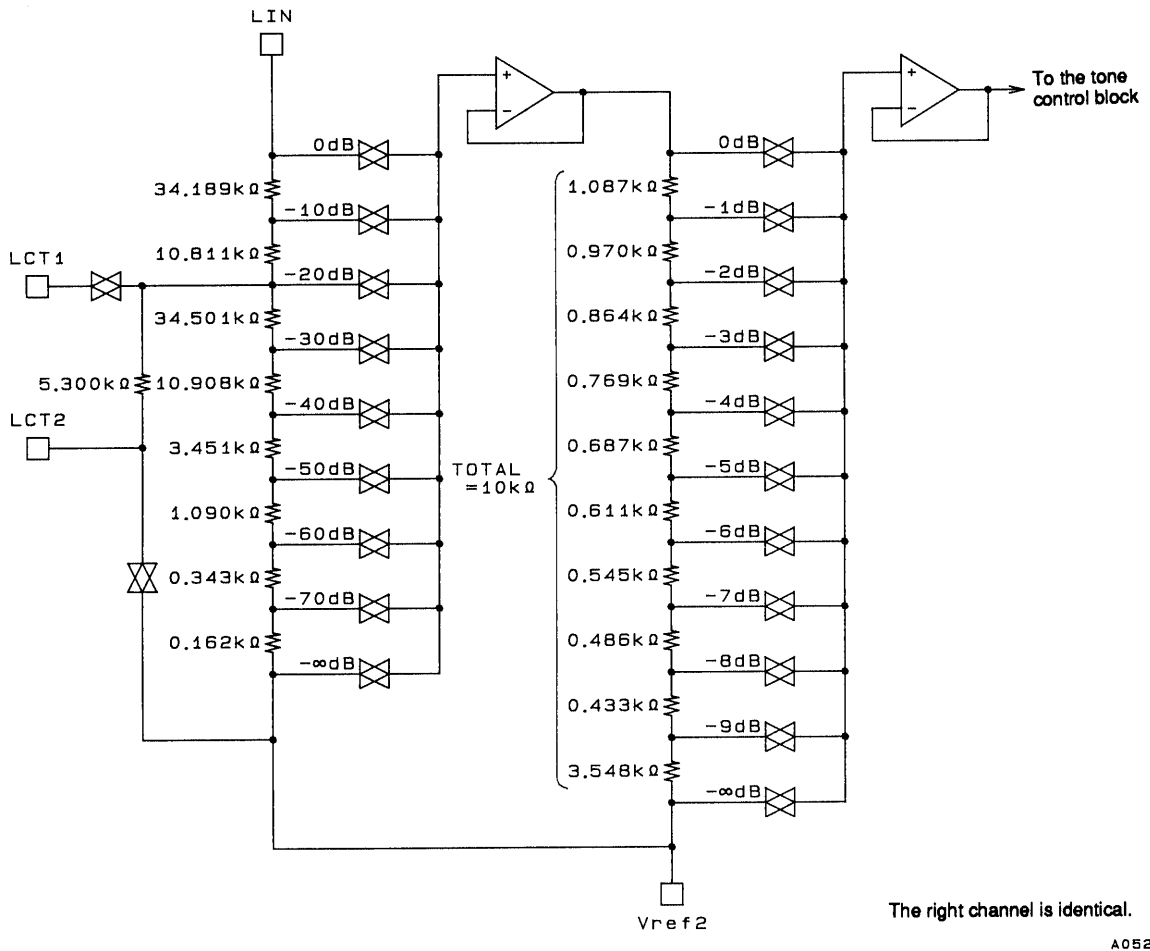
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Pin No.	Symbol	Function	Notes
11 26	LIN RIN	<ul style="list-style-type: none"> • Main volume control inputs • These inputs must be driven by low-impedance outputs. 	 <p style="text-align: right;">A05235</p>
12 25	LSELO RSELO	Input selector outputs	 <p style="text-align: right;">A05236</p>
15 14 13 22 23 24	L1 L2 L3 R1 R2 R3	Signal inputs	 <p style="text-align: right;">A05237</p>
16	V _{DD}	Power supply	
20	V _{SS}	Ground	
17	CE	Chip enable. Data is loaded into the internal latch when this pin goes from high to low, and all analog switches operate at that time. Data transfers are enabled when this pin is high.	 <p style="text-align: right;">A05238</p>
18 19	DI CL	Serial data and clock inputs for LSI control.	
21	TEST	Test pin. This pin must be left open.	

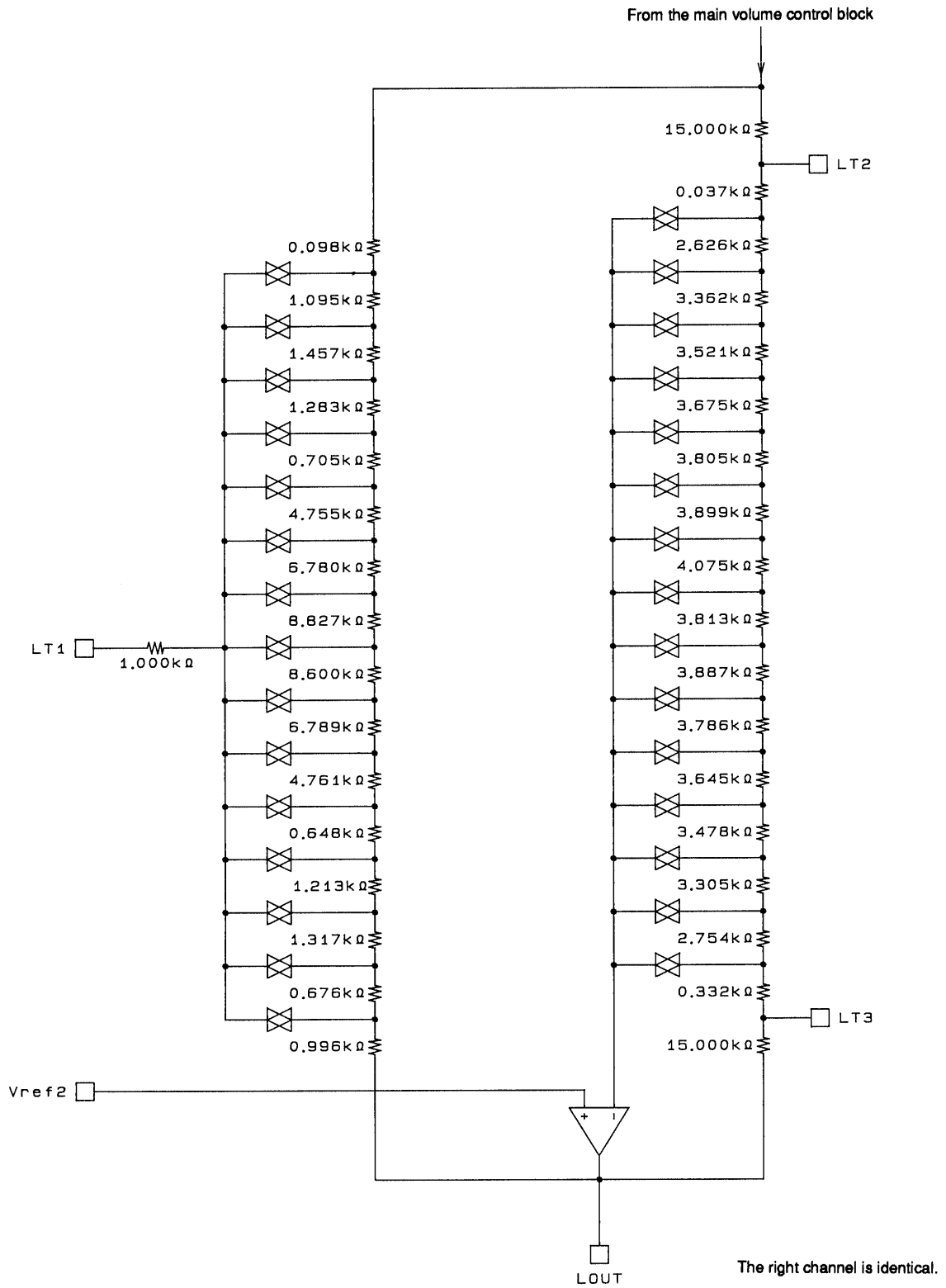
Input Block Equivalent Circuit Diagram



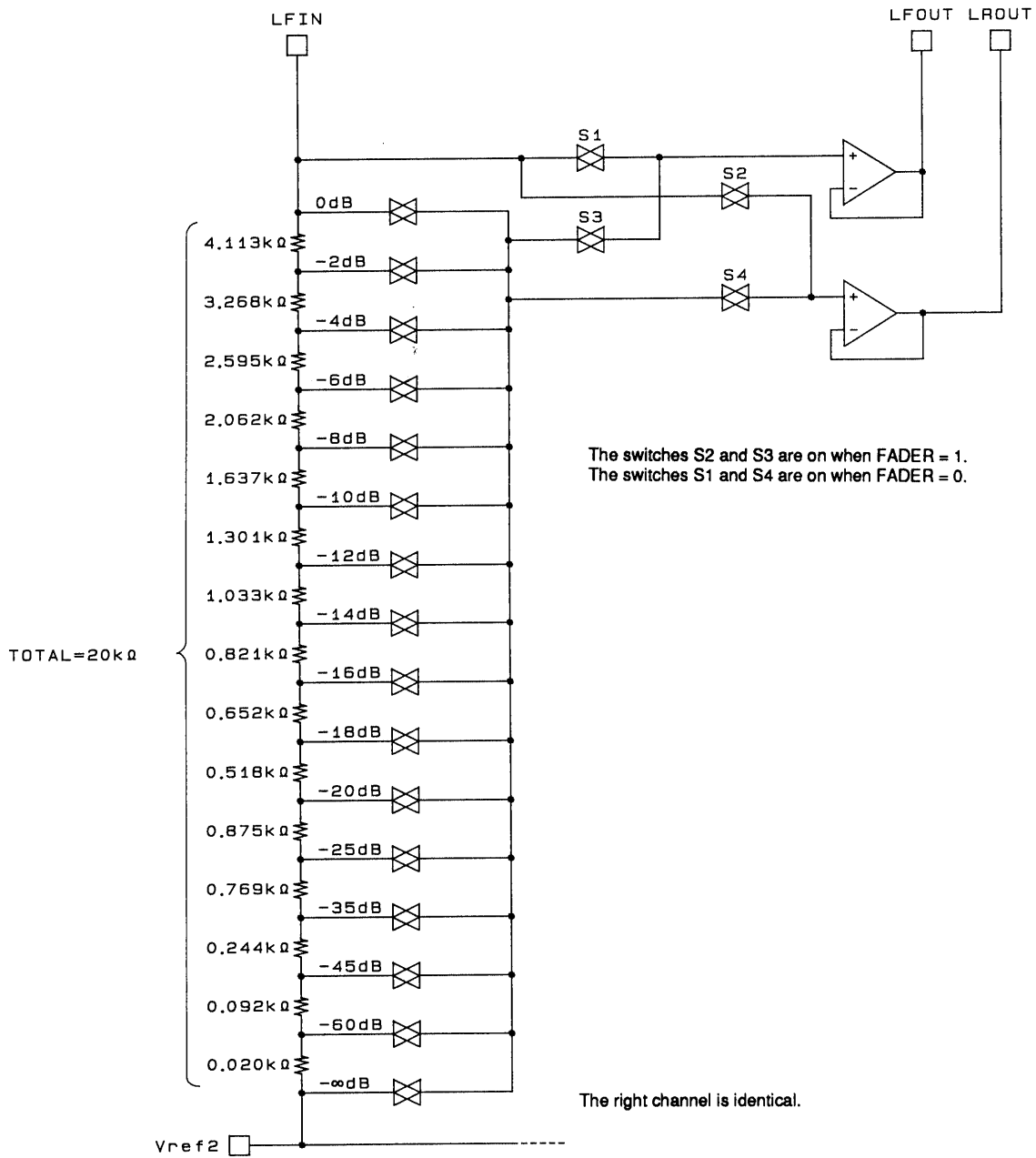
Main Volume Control Block Equivalent Circuit Diagram



Tone Control Block Equivalent Circuit Diagram



Fader Block Equivalent Circuit Diagram



If data setting the main volume control 1-dB step to $-\infty$ is sent to the LSI, the S1 and S2 switches will be opened and the S3 and S4 switches will be turned on (closed).

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Sample Calculation of the Loudness Circuit External Constants

First, see the LC75371M 10-dB step internal equivalent circuit shown on page 9. Figure 1 below shows a version of that circuit to which the loudness circuit external components have been added, and which has been simplified for this calculation. The sample calculation below uses this circuit diagram to acquire a 5-dB boost at $f = 100$ Hz.

($f = 100$ Hz, 5-dB boost)

Assuming that the resistors and capacitors in Figure 1 have the following values:

$$R1 = R2 = 50 \text{ k}\Omega$$

$$R3 = 5 \text{ k}\Omega$$

$$\text{And } C1 = Z1 \text{ and } C2 = Z2.$$

Then:

$$V_{OUT} = \frac{\frac{R2 (R3 + Z2)}{R2 + R3 + Z2}}{\frac{R1 \cdot Z1}{R1 + Z1} + \frac{R2 (R3 + Z2)}{R2 + R3 + Z2}} = -20 \text{ dB}$$

(at = 1 kHz)

$$V_{OUT} = \frac{\frac{R2 (R3 + 10 \cdot Z2)}{R2 + R3 + 10 \cdot Z2}}{\frac{R1 \cdot 10 \cdot Z1}{R1 + 10 \cdot Z1} + \frac{R2 (R3 + 10 \cdot Z2)}{R2 + R3 + 10 \cdot Z2}} = -15 \text{ dB}$$

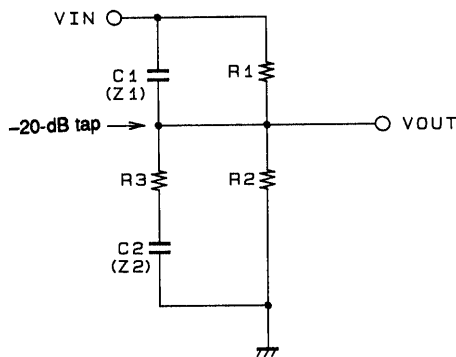
(at = 100 Hz)

From the above equations we find:

$$Z1 = 891.5 \text{ k}\Omega \text{ and } Z2 = 880 \Omega.$$

Therefore, the specifications will be met if capacitors that have these impedances at $f = 1$ kHz are connected externally.

The result is that $C1 = 178.5 \text{ pF}$ and $C2 = 0.18 \mu\text{F}$.



R1, R2, R3: LC75371M internal resistances
 C1: External high-band compensation capacitor
 C2: External low-band compensation capacitor

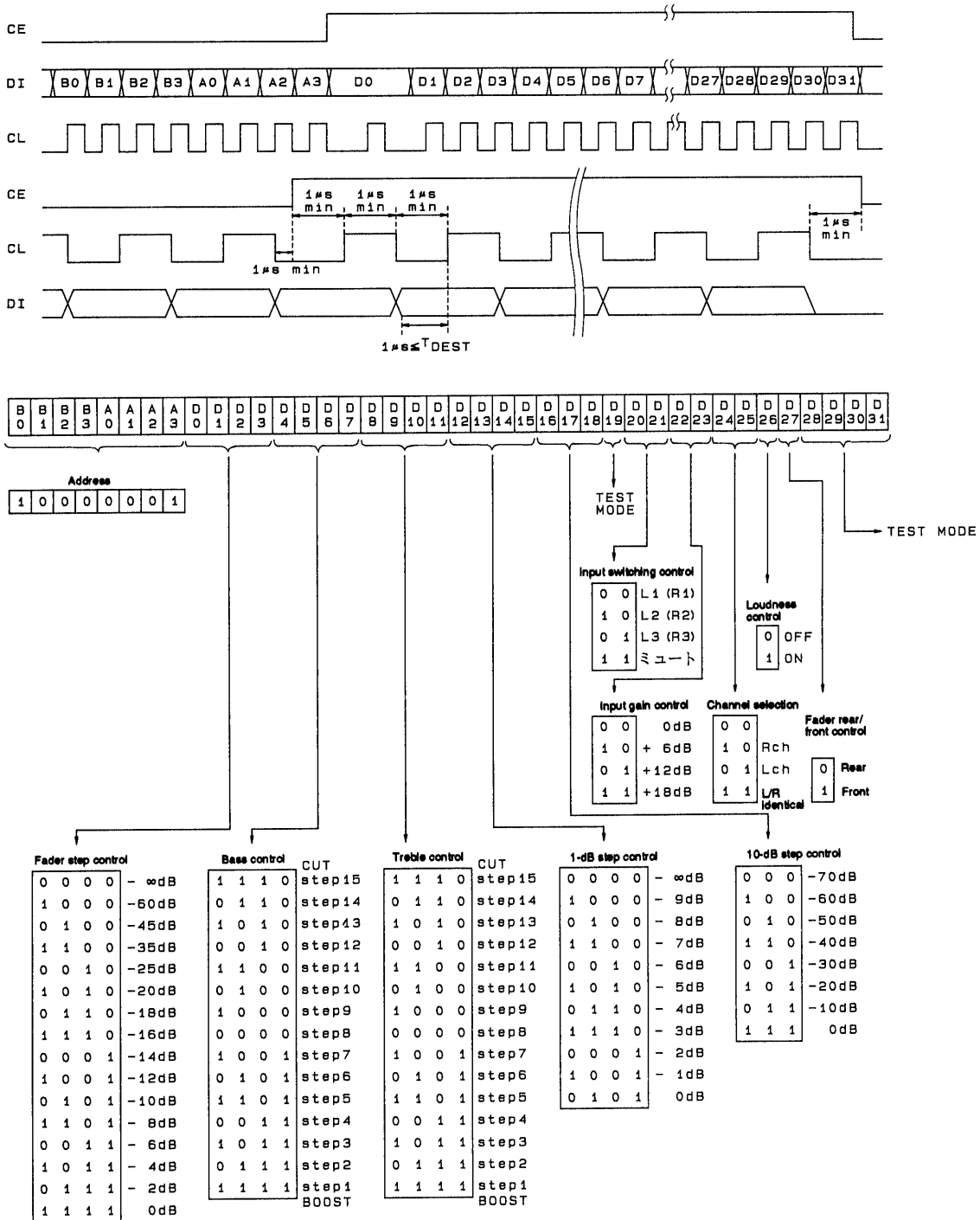
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Figure 1

LC75371M

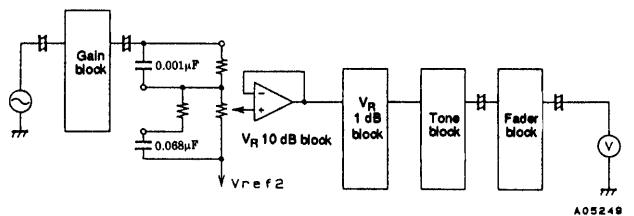
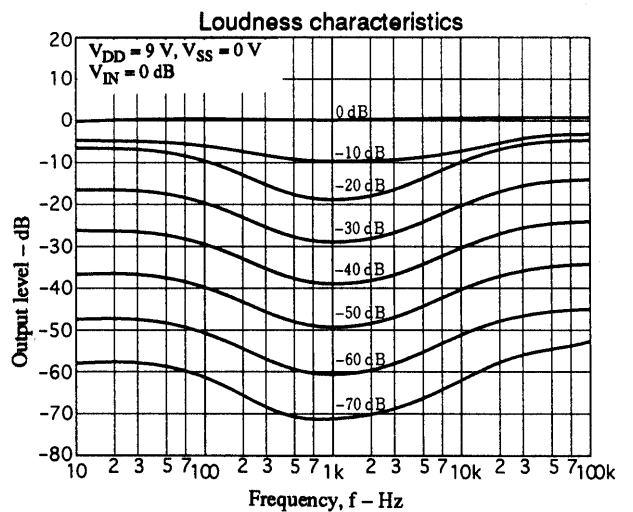
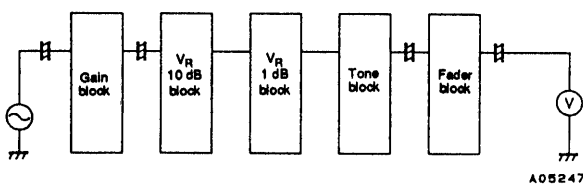
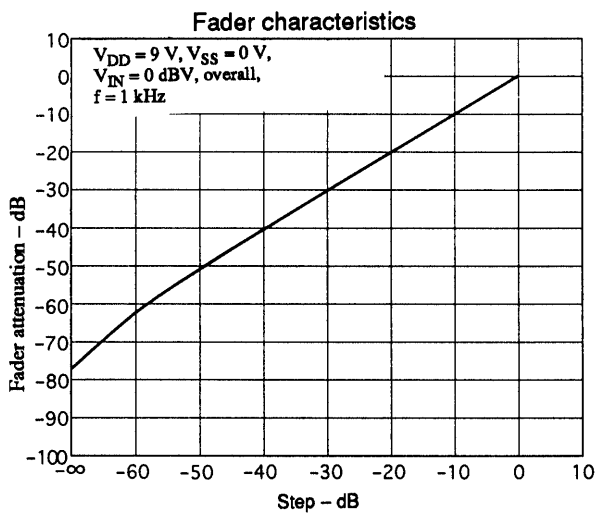
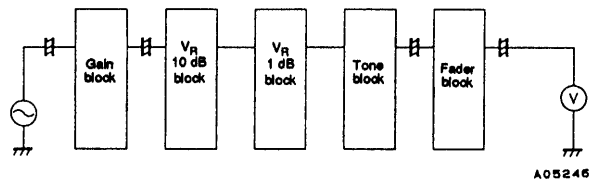
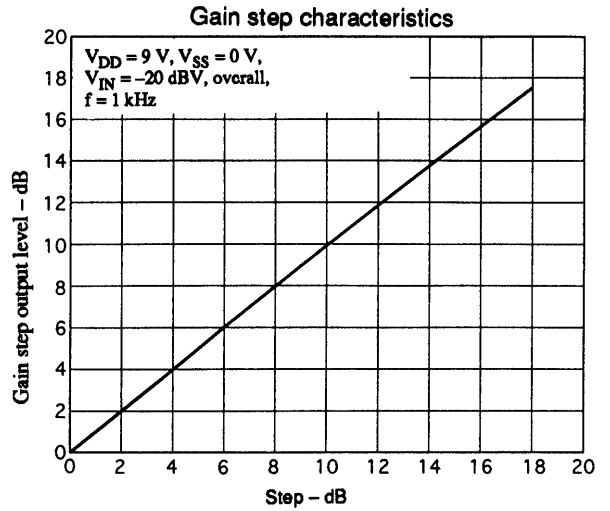
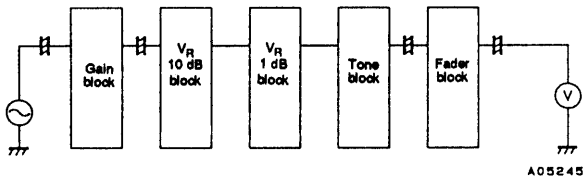
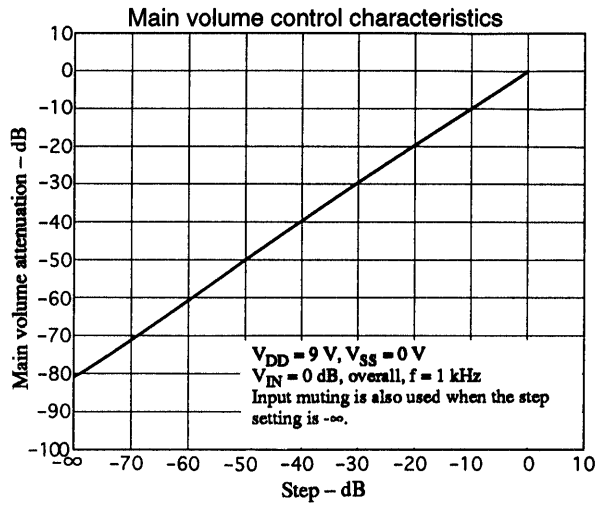
Control System Timing and Data Format

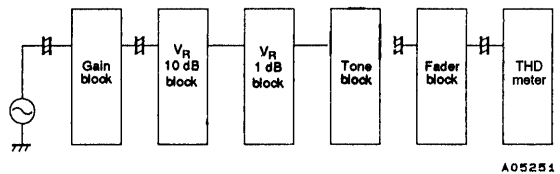
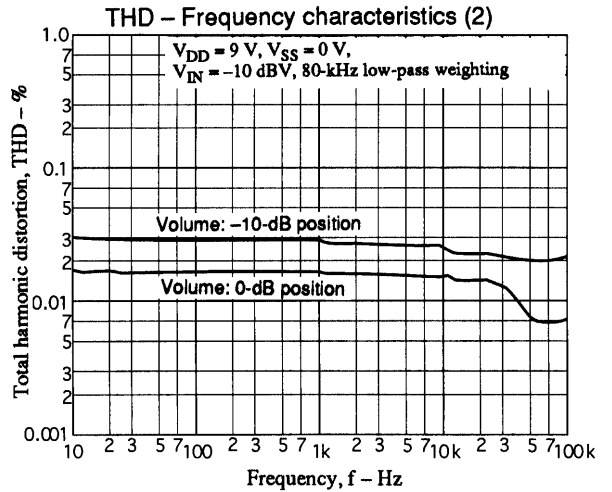
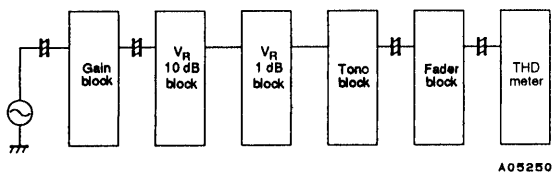
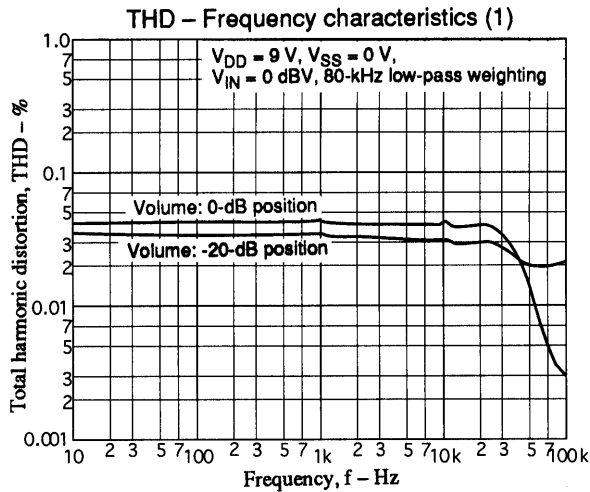
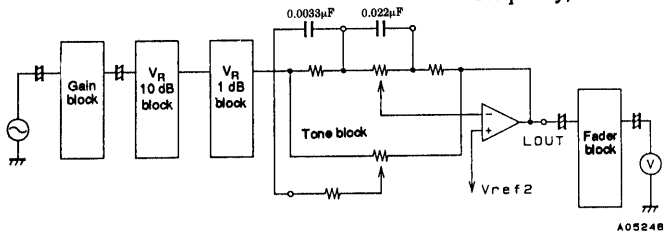
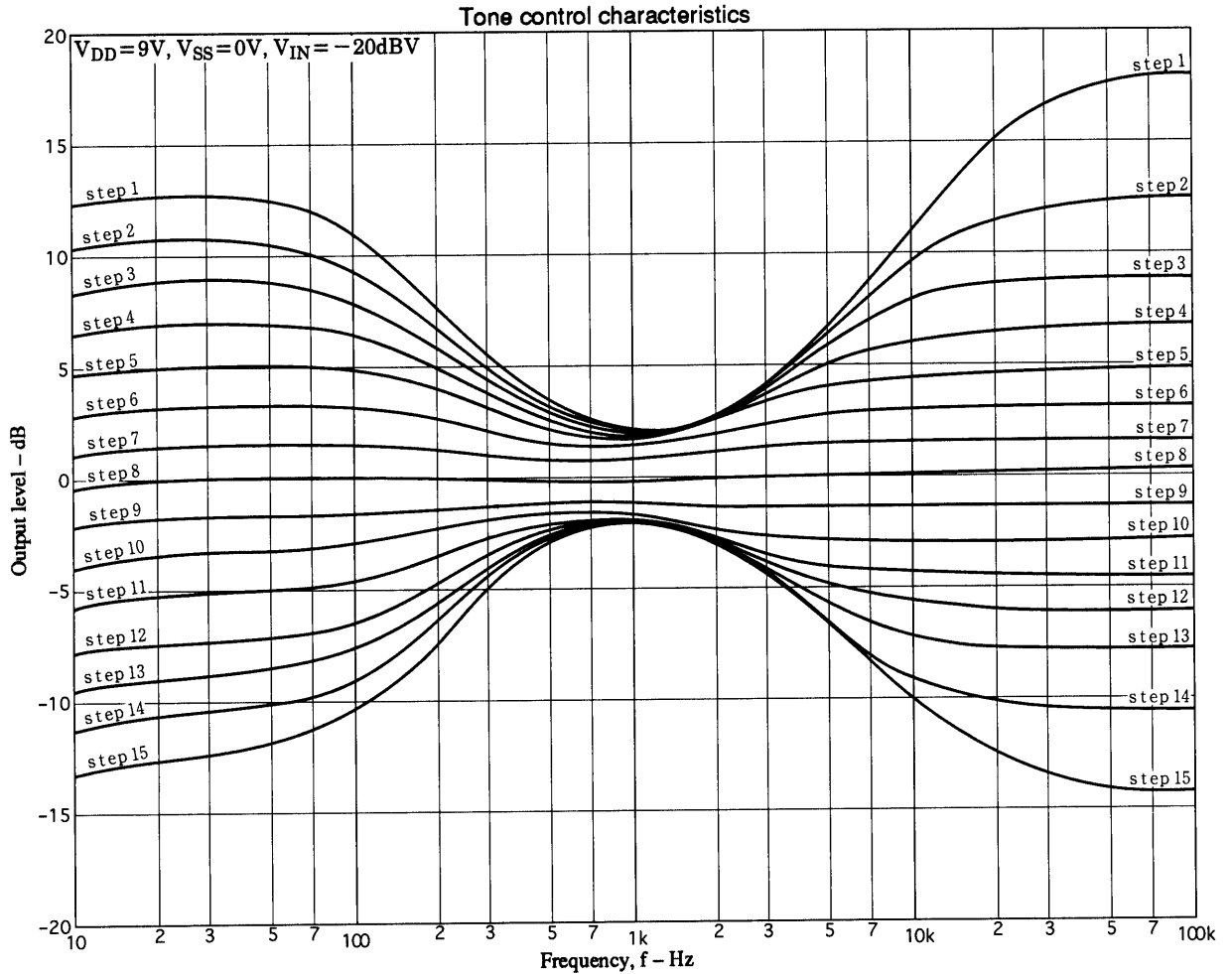
The LC75371M is controlled by applying data in the stipulated format to the CE, CL, and DI pins. The data consists of 40 bits, of which 8 bits are the chip address and 32 bits are the data.

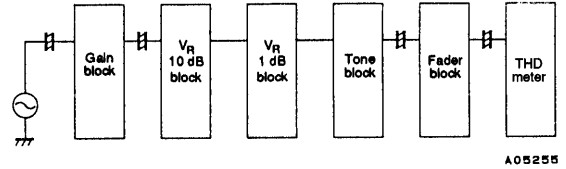
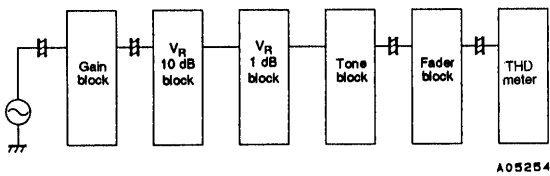
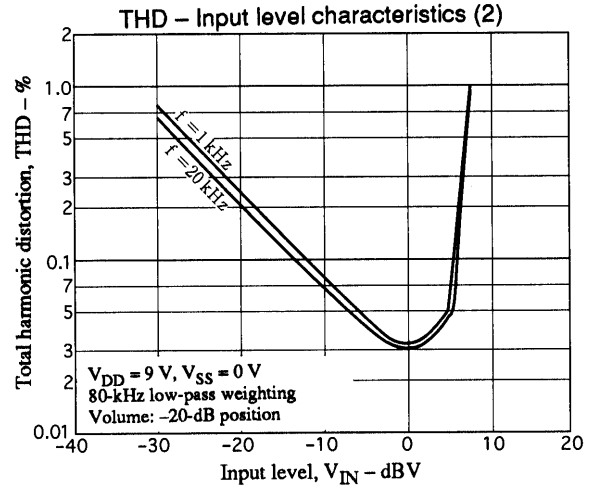
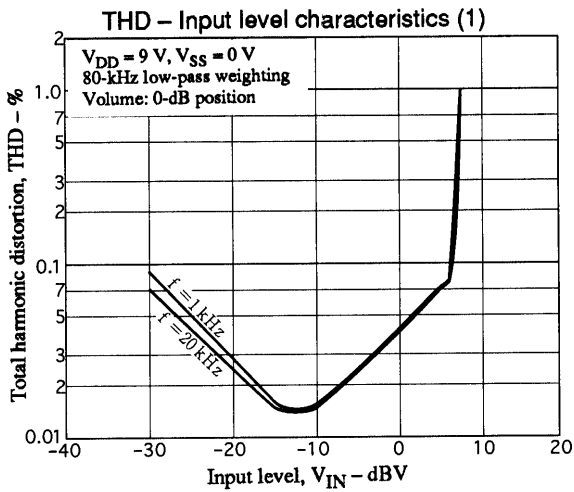
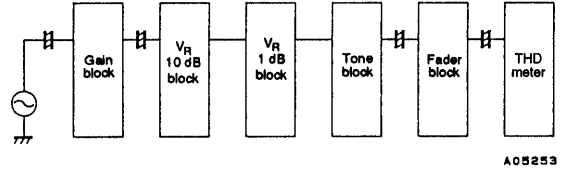
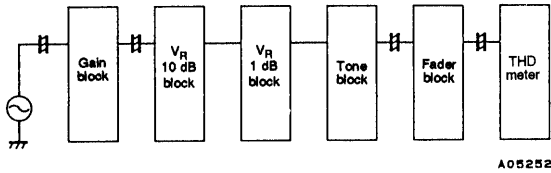
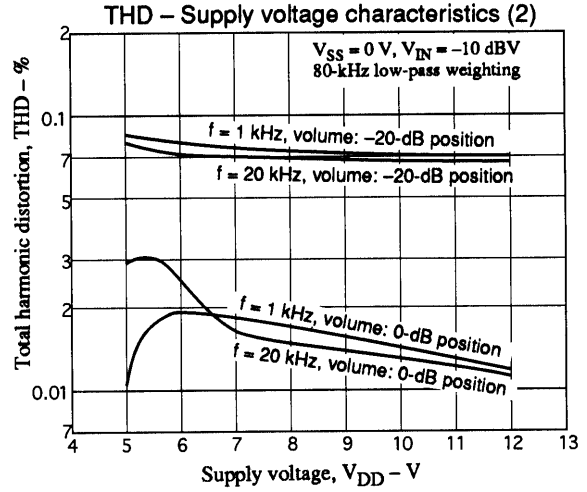
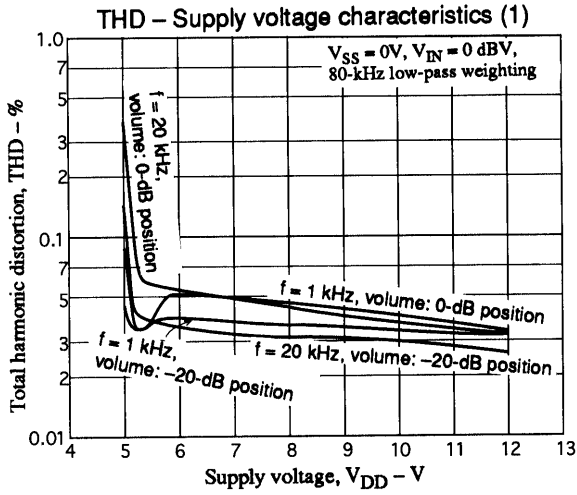


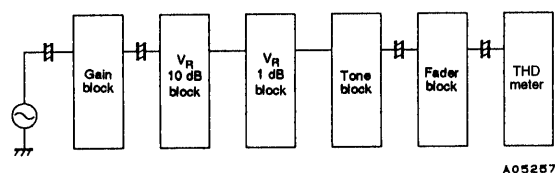
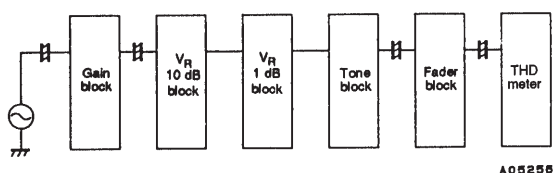
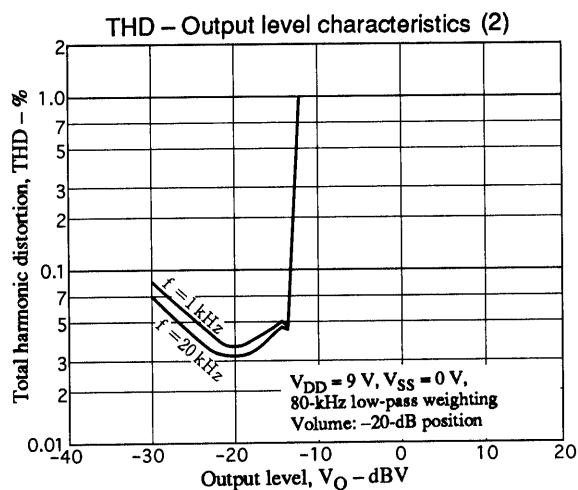
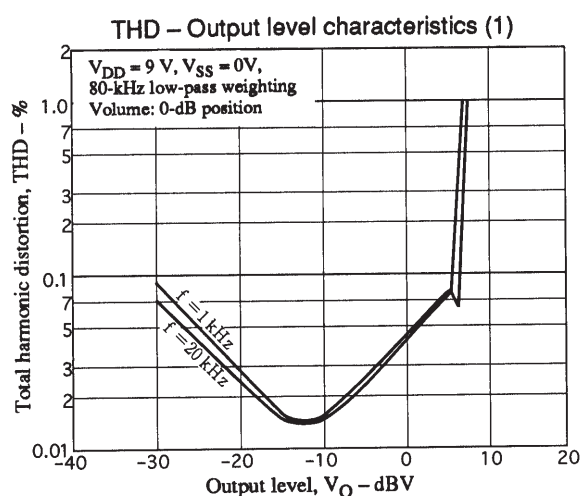
Note: The bits D19 and D28 to D31 are LSI test bits, and must be set to 0.

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Usage Notes

1. The states of the internal analog switches are undefined when power is first applied. Use an external muting circuit or other technique to mute the outputs until correct control data has been set up in the LC75371M.
2. Either cover the lines connected to the CL, DI, and CE pins with the ground pattern or use shielded cable for those lines to prevent the high-frequency digital signals on those lines from entering the analog system.
3. Muting by input switching must be used in conjunction with the volume control setting when the maximum volume control attenuation (the VOL = $-\infty$ position) is used.
4. Since there is significant sample-to-sample variation in the magnitude of the main volume switching noise, request a switching noise verification sample to verify the maximum switching noise.

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