Ordering number : EN5520A

CMOS LSI

LC74785, LC74785M

On-Screen Display Controller LSI

Overview

The LC74785 and LC74785M are on-chip EDS CMOS LSIs for on-screen display, a function that displays characters and patterns on a TV screen under microprocessor control. These LSIs support 12 × 18 dot characters and can display 12 lines by 24 characters of text.

Features

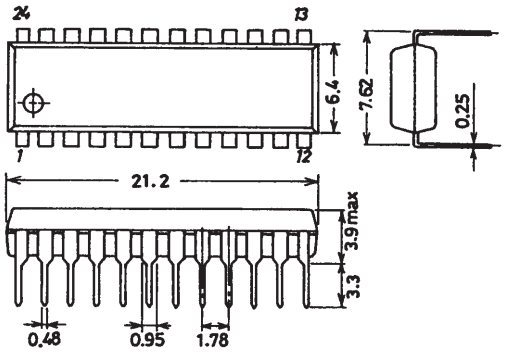
- Display format: 24 characters by 12 rows (Up to 288 characters)
- Character format: 12 (horizontal) × 18 (vertical) dots
- Character sizes: Three sizes each in the horizontal and vertical directions
- Characters in font: 128
- Initial display positions: 64 horizontal positions and 64 vertical positions
- Blinking: Specifiable in character units
- Blinking types: Two periods supported: About 1.0 second and about 0.5 second
- Blanking: Over the whole font (12 × 18 dots)
- Background color
  - — Background coloring: 8 colors (internal synchronization mode): 4fsc
  - — Background coloring: 6 colors (internal synchronization mode): 2fsc
- Line background color
  - — Can be set for 3 lines
  - — Line background coloring: 8 colors (internal synchronization mode): 4fsc
  - — Line background coloring: 6 colors (internal synchronization mode): 2fsc
- External control input: 8-bit serial input format
- On-chip sync separator circuit
- EDS support
- Video output
  - — NTSC-format composite output
- Package
  24-pin plastic DIP (300 mil)
  24-pin plastic SOP (375 mil)

Package Dimensions

unit: mm

3067-DIP24S

[LC74785]

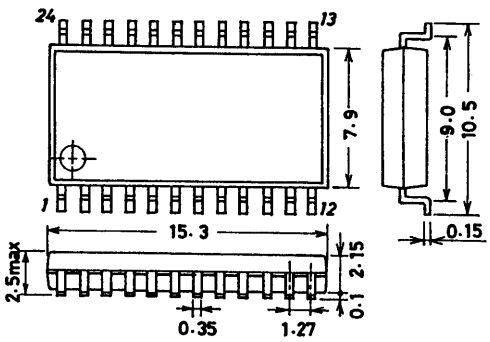


SANYO: DIP24S

unit: mm

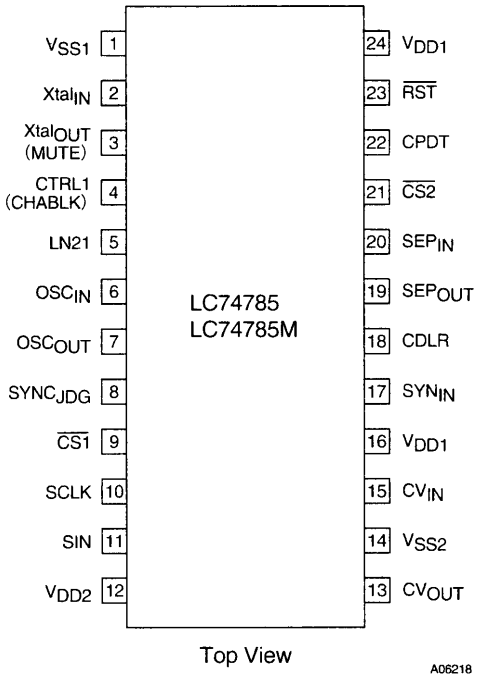
3045B-MFP24

[LC74785M]



SANYO: MFP24

Pin Assignment



Pin Functions

Pin No.	Pin	Function	Notes
1	$V_{SS}1$	Ground	Ground connection (digital system ground)
2	Xtal $_{IN}$	Crystal oscillator (MUTE input)	These pins are used either to connect the crystal and capacitor used to form an external crystal oscillator used to generate the internal synchronizing signals, or to input an external clock signal (2fsc or 4fsc). As a mask option, the Xtalout pin can be set to function as the MUTE input pin. When this pin is set low, the video output is held at the pedestal level. (A pull-up resistor is built in and the input has hysteresis characteristics.)
3	Xtal $_{OUT}$ (MUTE)		
4	CTRL1 (CHABLK)	Crystal oscillator input switching (CHABLK output)	Switches the mode between external clock input and crystal oscillator operation. A low level selects crystal oscillator operation and a high level selects external clock input. As a mask option, the CTRL1 input pin can be set to function as the CHABLK (character border) output. This is a 3-value output.
5	LN21	Data output	Line 21H pulse output (Even fields when MOD1 is low, both fields when MOD1 is high)
6	OSC $_{IN}$	LC oscillator	Connections for the coil and capacitor that form the character output dot clock generation oscillator.
7	OSC $_{OUT}$		
8	SYNC $_{JDG}$	External synchronizing signal judgment output	Outputs the state of the external synchronizing signal presence/absence judgment. Outputs a high level when synchronizing signals are present. Outputs a field discrimination pulse (O/E pulse) when SEL2 is high.(HLFTON: Valid when 0) HLFTON: A signal in the range specified by LNA*, LNB*, and LNC* is output when HLFTON is high.) Outputs the dot clock (LC oscillator) when $\overline{CS1}$ is high and $\overline{RST}$ is low. (This signal is not output on command resets.) Outputs the crystal oscillator clock when $\overline{CS1}$ is low and $\overline{RST}$ is low. (This signal is not output on command resets.)
9	$\overline{CS1}$	Enable input	Enable input pin for the OSD serial data input function. Serial data input is enabled when this pin is low. A pull-up resistor is built in. (The input has hysteresis characteristics.)
10	SCLK	Clock input	Input for the serial data input clock. A pull-up resistor is built in. (The input has hysteresis characteristics.)
11	SIN	Data input	Serial data input. A pull-up resistor is built in. (The input has hysteresis characteristics.)
12	$V_{DD}2$	Power supply	Composite video signal level adjustment power supply (analog system power supply)
13	CV_{OUT}	Video signal output	Composite video signal output
14	$V_{SS}2$	Ground	Ground connection (analog system ground)

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Pin No.	Pin	Function	Notes
15	CV_{IN}	Video signal input	Composite video signal input
16	$V_{DD}1$	Power supply	Power supply (+5 V: digital system power supply)
17	SYN_{IN}	Sync separator circuit input	Video signal input for the built-in sync separator circuit
18	CDLR	Background color phase adjustment	Background color phase adjustment. Connect to ground through a resistor and a capacitor.
19	SEP_{OUT}	Composite synchronizing signal output	Video signal output for the built-in sync separator circuit. Can be switched to function as an output for signal (high or ST. pulse) due to MOD0 by setting SEL0 high.
20	SEP_{IN}	Vertical synchronizing signal input	Inputs the vertical synchronizing signal created by integrating the SEP_{OUT} pin output signal. An integration circuit must be connected to the SEP_{OUT} pin. This pin must be tied to $V_{DD}1$ if unused. This pin can be switched to function as the frame signal input mode by setting SEL1 high. (This is valid when CTL3 is set to 1.)
21	$\overline{CS2}$	Enable input	EDS data output enable input. EDS data output is enabled when this pin is low. A pull-up resistor is built in. (The input has hysteresis characteristics.)
22	CPDT	Data output	EDS data output (This pin can be either an n-channel open-drain output or a CMOS output.)
23	$\overline{RST}$	Reset input	System reset input A pull-up resistor is built in. (The input has hysteresis characteristics.)
24	$V_{DD}1$	Power supply (+5 V)	Power supply (+5 V: digital system power supply)

Note: Both $V_{DD}1$ pins must be connected to the power supply.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}	$V_{DD}1$ and $V_{DD}2$	V_{SS}–0.3 to V_{SS}+7.0	V
Input voltage	V_{IN}	All input pins	V_{SS}–0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	LN21, CPDT, SEP_{OUT}, and $SYNC_{JDG}$	V_{SS}–0.3 to V_{DD}+0.3	V
Allowable power dissipation	Pd max	Ta = 25°C	350	mW
Operating temperature	Topr		–30 to +70	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges at Ta = –30 to +70°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD}1$	$V_{DD}1$	4.5	5.0	5.5	V
	$V_{DD}2$	$V_{DD}2$	4.5	5.0	$1.27V_{DD}1$	V
Input high-level voltage	$V_{IH}1$	$\overline{RST}$, $\overline{CS1}$, $\overline{CS2}$, SIN, SCLK, SEP_{IN}, and MUTE	$0.8V_{DD}1$		$V_{DD}1 + 0.3$	V
	$V_{IH}2$	CTRL1	$0.7V_{DD}1$		$V_{DD}1 + 0.3$	V
Input low-level voltage	$V_{IL}1$	$\overline{RST}$, $\overline{CS1}$, $\overline{CS2}$, SIN, SCLK, SEP_{IN}, and MUTE	$V_{SS} – 0.3$		$0.2V_{DD}1$	V
	$V_{IL}2$	CTRL1	$V_{SS} – 0.3$		$0.3V_{DD}1$	V
Pull-up resistance	R_{PU}	Applies to pins set for the $\overline{RST}$, $\overline{CS1}$, $\overline{CS2}$, SIN, SCLK, and MUTE pin options.	25	50	90	kΩ
Composite video signal input voltage	$V_{IN}1$	CV_{IN}; $V_{DD}1$ = 5 V		2.0		Vp-p
	$V_{IN}2$	SYN_{IN}; $V_{DD}1$ = 5 V	1.5	2.0	2.5	Vp-p
Input voltage	$V_{IN}3$	$Xtal_{IN}$ (When external clock input is used) f_{in} = 2 fsc or 4 fsc ; $V_{DD}1$ = 5 V	0.10		5.0	Vp-p
Oscillator frequency	$F_{OSC}1$	The $Xtal_{IN}$ and $Xtal_{OUT}$ oscillator pins (2 fsc: NTSC)		7.159		MHz
	$F_{OSC}1$	The $Xtal_{IN}$ and $Xtal_{OUT}$ oscillator pins (4 fsc: NTSC)		14.318		MHz
	$F_{OSC}2$	The OSC_{IN} and OSC_{OUT} oscillator pins (LC oscillator)	5		10	MHz

Note: When the $Xtal_{IN}$ pin is used in clock input mode, extreme care must be taken to prevent noise from entering the input signal.

Electrical Characteristics at Ta = –30 to +70°C, $V_{DD}1$ = 5 V unless otherwise specified.

Parameter	Symbol	Conditions		Ratings min	Ratings typ	Ratings max	Unit
Input off leakage current	$I_{leak}1$	CV_{IN}				1	µA
Output off leakage current	$I_{leak}2$	CV_{OUT}				1	µA
Output high-level voltage	$V_{OH}1$	LN21, $SYNC_{JDG}$, CPDT, and SEP_{OUT}; $V_{DD}1$ = 4.5 V, I_{OH} = –1.0 mA		3.5			V
Output low-level voltage	$V_{OL}1$	LN21, $SYNC_{JDG}$, CPDT, and SEP_{OUT}; $V_{DD}1$ = 4.5 V, I_{OL} = 1.0 mA				1.0	V
Three-value output voltage	V_O	CHABLK; $V_{DD}1$ = 5.0 V	H	3.3		5.0	V
			M	1.8		2.3	V
			L	0		0.8	V
Input current	I_{IH}	$\overline{RST}$, $\overline{CS1}$, $\overline{CS2}$, SIN, SCLK, CTRL1, SEP_{IN}, and MUTE; V_{IN} = $V_{DD}1$				1	µA
	I_{IL}	CTRL1 and OSC_{IN}; V_{IN} = $V_{SS}1$		–1			µA
Operating mode current drain	$I_{DD}1$	$V_{DD}1$; All outputs open, Xtal: 7.159 MHz, LC: 8 MHz				30	mA
	$I_{DD}2$	$V_{DD}2$: $V_{DD}2$ = 5 V				20	mA
SYNC level	V_{SN}	CV_{OUT}; $V_{DD}1$ = 5.0 V, $V_{DD}2$ = 5.0 V	*1	0.70	0.82	0.94	V
			*2	0.89	1.01	1.13	V
			*3	1.18	1.30	1.42	V
Pedestal level	V_{PD}	CV_{OUT}; $V_{DD}1$ = 5.0 V, $V_{DD}2$ = 5.0 V	*1	1.32	1.44	1.56	V
			*2	1.52	1.64	1.76	V
			*3	1.81	1.93	2.05	V
Color burst low level	V_{CBL}	CV_{OUT}; $V_{DD}1$ = 5.0 V, $V_{DD}2$ = 5.0 V	*1	0.98	1.10	1.22	V
			*2	1.17	1.29	1.41	V
			*3	1.46	1.58	1.70	V
Color burst high level	V_{CBH}	CV_{OUT}; $V_{DD}1$ = 5.0 V, $V_{DD}2$ = 5.0 V	*1	1.63	1.75	1.87	V
			*2	1.83	1.95	2.07	V
			*3	2.11	2.23	2.35	V
Background color other than blue low level	$V_{RSL}0$	CV_{OUT}; $V_{DD}1$ = 5.0 V, $V_{DD}2$ = 5.0 V	*1	1.17	1.29	1.41	V
			*2	1.36	1.48	1.60	V
			*3	1.65	1.77	1.89	V
Background color other than blue high level	$V_{RSH}0$	CV_{OUT}; $V_{DD}1$ = 5.0 V, $V_{DD}2$ = 5.0 V	*1	2.33	2.45	2.57	V
			*2	2.52	2.64	2.76	V
			*3	2.81	2.93	3.05	V
Blue background color 1low level	$V_{RSL}1$	CV_{OUT}; $V_{DD}1$ = 5.0 V, $V_{DD}2$ = 5.0 V	*1	1.08	1.20	1.32	V
			*2	1.27	1.39	1.51	V
			*3	1.56	1.68	1.80	V
Blue background color 2 low level	$V_{RSL}2$	CV_{OUT}; $V_{DD}1$ = 5.0 V, $V_{DD}2$ = 5.0 V	*1	1.49	1.61	1.83	V
			*2	1.68	1.80	1.92	V
			*3	1.97	2.09	2.21	V
Blue background color 1, 2 high level	$V_{RSH}1$ $V_{RSH}2$	CV_{OUT}; $V_{DD}1$ = 5.0 V, $V_{DD}2$ = 5.0 V	*1	1.97	2.09	2.21	V
			*2	2.17	2.29	2.41	V
			*3	2.46	2.58	2.70	V
Frame level 0	$V_{BK}0$	CV_{OUT}; $V_{DD}1$ = 5.0 V, $V_{DD}2$ = 5.0 V	*1	1.40	1.52	1.64	V
			*2	1.60	1.72	1.84	V
			*3	1.89	2.01	2.13	V
Frame level 1	$V_{BK}1$	CV_{OUT}; $V_{DD}1$ = 5.0 V, $V_{DD}2$ = 5.0 V	*1	1.97	2.09	2.21	V
			*2	2.17	2.29	2.41	V
			*3	2.46	2.58	2.70	V
Character level	V_{CHA}	CV_{OUT}; $V_{DD}1$ = 5.0 V, $V_{DD}2$ = 5.0 V	*1	2.55	2.67	2.79	V
			*2	2.75	2.87	2.99	V
			*3	3.04	3.16	3.28	V

Note: 1. When the sync level is 0.8 V
2. When the sync level is 1.0 V
3. When the sync level is 1.3 V

Timing Characteristics at Ta = –30 to +70°C, $V_{DD}1$ = 5 ±0.5 V

OSD write (See Figure 1.)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Minimum input pulse width	$t_{W(SCLK)}$	SCLK	200			ns
	$t_{W(CS1)}$	$\overline{CS1}$ (The period when $\overline{CS1}$ is high)	1			µs
Data setup time	$t_{SU(CS1)}$	$\overline{CS1}$	200			ns
	$t_{SU(SIN)}$	SIN	200			ns
Data hold time	$t_{h(CS1)}$	$\overline{CS1}$	2			µs
	$t_{h(SIN)}$	SIN	200			ns
One word write time	t_{word}	The time to write 8 bits of data	4.2			µs
	t_{wt}	The RAM data write time	1			µs

EDS read (For the n-channel open-drain circuit, see Figure 2.)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Minimum input pulse width	t_{CKCY}	SCLK	2			µs
	t_{CKL}	SCLK	1			µs
	t_{CKH}	SCLK	1			µs
Setup time	t_{ICK}	SCLK	10			µs
Output delay time	t_{CKO}	CPDT			0.5	µs

Note: The CMOS output circuit follows the OSD timing.

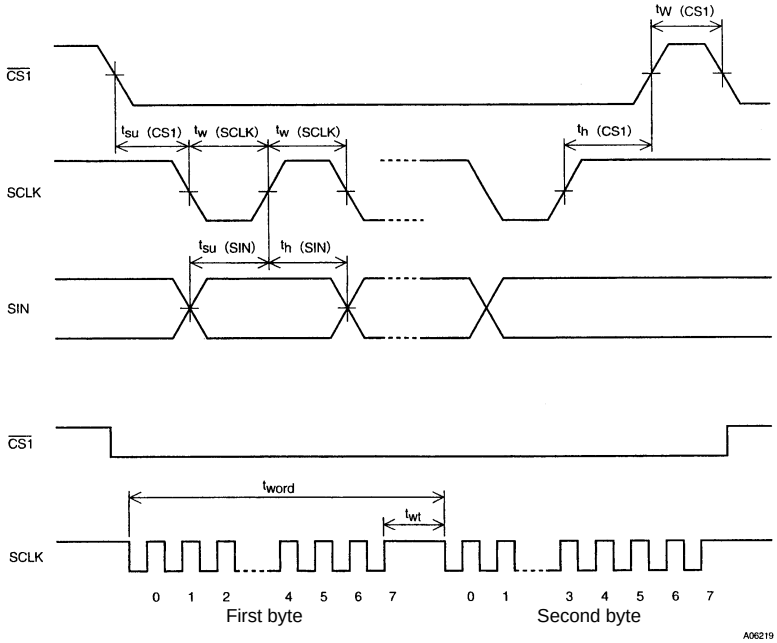
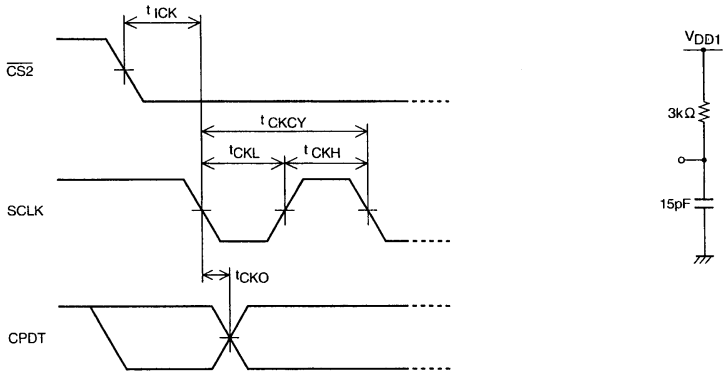
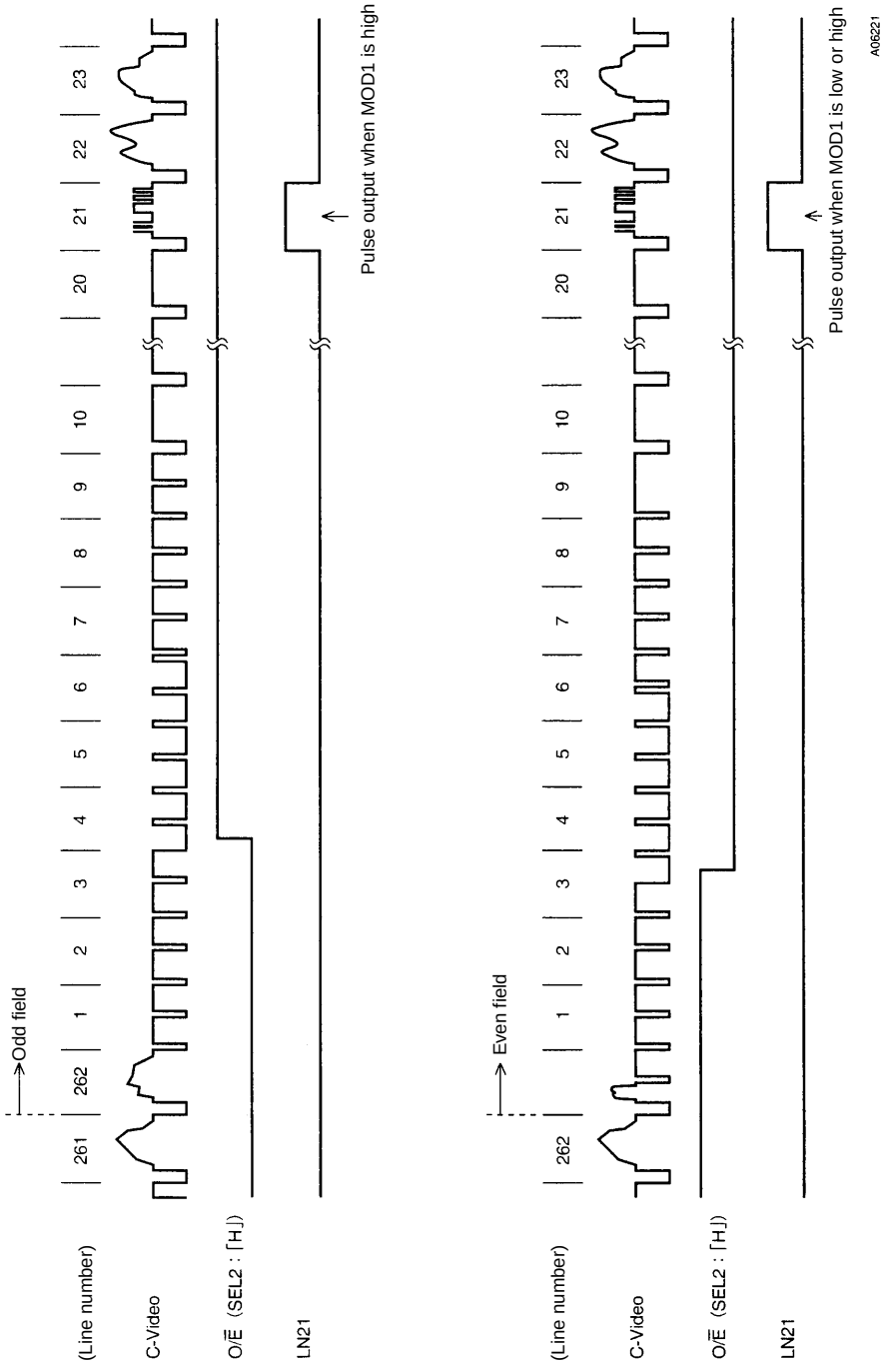


Figure 1 OSD Serial Data Input Timing



Note: CPDT goes to the high-impedance state when $\overline{CS2}$ is high.

Figure 2 EDS Serial Output Test Conditions (For the n-channel open-drain circuit.)



Note: The $\overline{O/E}$ signal is output from the $SYNC_{IDG}$ pin when SEL2 is high.
LN21 is output for even fields when MOD1 is low and for both fields when MOD1 is high.

Figure 3 O/$\overline{E}$ and LN21 Output Timing

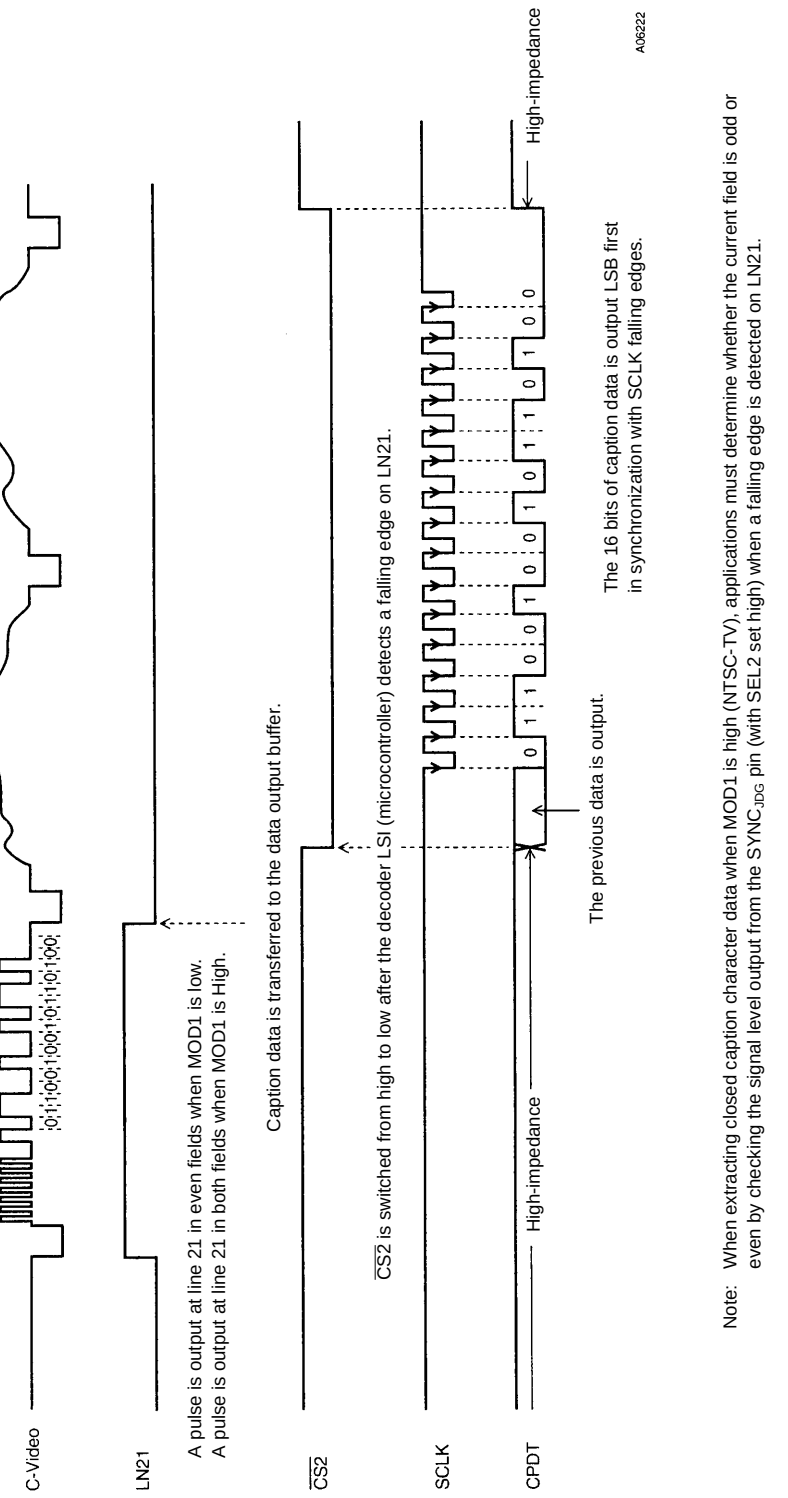


Figure 4 Transferring caption data from the LC74785/M to the decoder LSI (microcontroller): Method 1 (Basic LC74785/M usage)

The timing of the transfer of caption data to the data output buffer is synchronized with the falling edge of the pulse output from LN21. Therefore, the software processing shown below is required if the decoder LSI (microcontroller) does not detect LN21 falling edges.

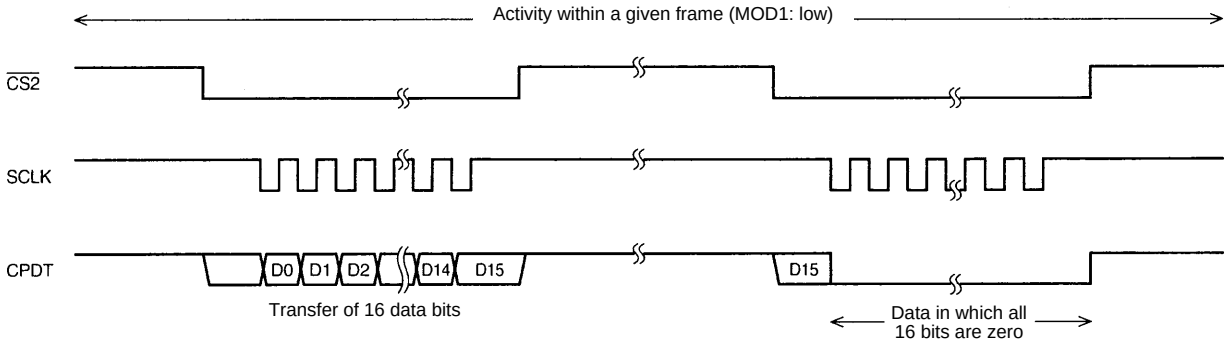


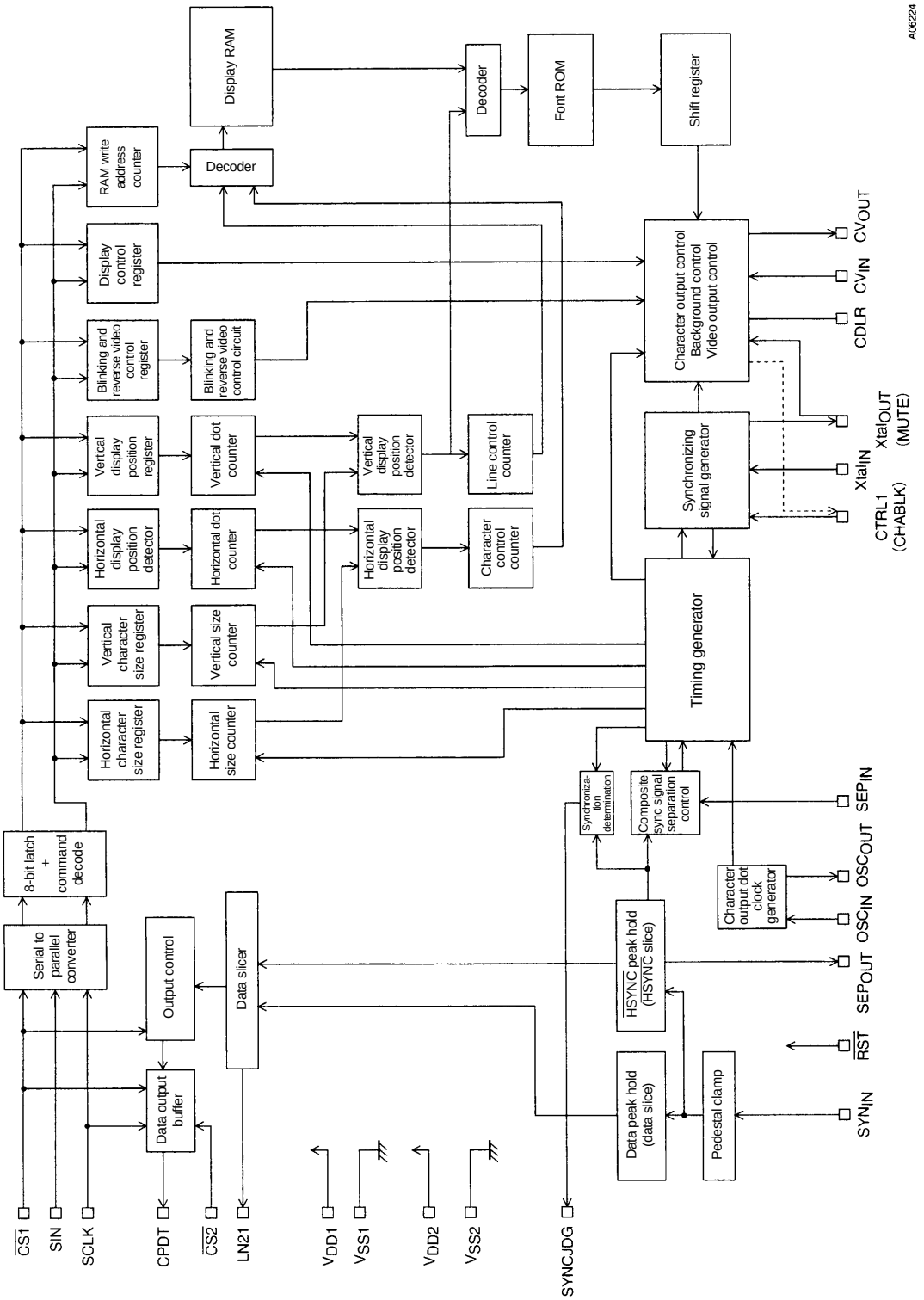
Figure 5 Transferring caption data from the LC74785/M to the decoder LSI (microcontroller): Method 2 (When it is not possible to allocate a port on the decoder LSI (microcontroller) to detect falling edges on LN21.)

Since data is output to the output buffer once (during the even field) when MOD1 is low, the data transfer control operation from the decoder LSI (microcontroller) must be performed at least twice in a single frame (about 32 ms).

If a transfer control operation is performed twice in the same frame, the CPDT output on the second operation will be 16 bits of zero data. This allows the decoder LSI to determine that the data for the next frame has not been transferred yet.

Note: If $\overline{CS2}$ remains low, the hardware will not be able to transfer the data to the output buffer. Therefore, the decoder LSI (microcontroller) must reset $\underline{CS2}$ to high from low after it completes a data transfer control operation.
Transfer method 2 cannot be used if MOD1 is high (NTSC-TV).

System Block Diagram



Display Control Commands

Display control commands have an 8-bit format and are transferred using the serial input function. Commands consist of a command identification code in the first byte and command data in the following bytes. The following commands are supported.

1 COMMAND0: Display memory (VRAM) write address setup command
2 COMMAND1: Display character data write command
3 COMMAND2: Vertical display start position and vertical character size setup command
4 COMMAND3: Horizontal display start position and horizontal character size setup command
5 COMMAND4: Display control setup command
6 COMMAND5: Display control setup command
7 COMMAND6: Synchronizing signal detection setup command
8 COMMAND7: Display control setup command
9 COMMAND8: Display control setup command
10 COMMAND9: Display control setup command
11 COMMAND10: Display control setup command

Display Control Command Table

Command	First byte								Second byte							
	Command identification code				Data				Data							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND0 Write address setup	1	0	0	0	V3	V2	V1	V0	0	0	0	H4	H3	H2	H1	H0
COMMAND1 Character write	1	0	0	1	0	0	0	0	at	c6	c5	c4	c3	c2	c1	c0
COMMAND2 Vertical character size and vertical display start position	1	0	1	0	VS 21	VS 20	VS 11	VS 10	0	FS	VP 5	VP 4	VP 3	VP 2	VP 1	VP 0
COMMAND3 Horizontal character size and horizontal display start position	1	0	1	1	HS 21	HS 20	HS 11	HS 10	0	LC	HP 5	HP 4	HP 3	HP 2	HP 1	HP 0
COMMAND4 Display control	1	1	0	0	TST MOD	RAM ERS	OSC STP	SYS RST	0	BLK 2	BLK 1	BLK 0	BK 1	BK 0	RV	DSP ON
COMMAND5 Display control	1	1	0	1	0	HLF TON	NON	INT	0	0	0	BCL	CB	PH 2	PH 1	PH 0
COMMAND6 Synchronizing signal detection	1	1	1	0	SEL 0	MOD 0	DIS LIN	MUT	0	RN 2	RN 1	RN 0	SN 3	SN 2	SN 1	SN 0
COMMAND7 Display control	1	1	1	1	0	0	SEL 1	CTL 3	0	0	0	VNP SEL	VSP SEL	MSK ERS	MSK SEL	EGL
COMMAND8 Display control	1	1	1	1	0	1	SEL 2	MOD 1	0	LNA 3	LNA 2	LNA 1	LNA 0	LPA 2	LPA 1	LPA 0
COMMAND9 Display control	1	1	1	1	1	0	LNB SEL	MOD 2	0	LNB 3	LNB 2	LNB 1	LNB 0	LPB 2	LPB 1	LPB 0
COMMAND10 Display control	1	1	1	1	1	1	LNC SEL	MOD 3	0	LNC 3	LNC 2	LNC 1	LNC 0	LPC 2	LPC 1	LPC 0

Once written, the command identification code in the first byte is stored until the next first byte is written. However, when the display character data write command (COMMAND1) is written, the LC74785/M locks into the display character data write mode, and another first byte cannot be written.

When the $\overline{CS1}$ pin is set high, the LC74785/M is set to the COMMAND0 (display memory write address setup mode) state.

COMMAND0 (Display memory write address setup command)

First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 0 identification code Sets the display memory write address.	
6	—	0		
5	—	0		
4	—	0		
3	V3	0	Display memory line address (0 to B hexadecimal)	
		1		
2	V2	0		
		1		
1	V1	0		
		1		
0	V0	0		
		1		

Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification code	
6	—	0		
5	—	0		
4	H4	0	Display memory column address (0 to 17 hexadecimal)	
		1		
3	H3	0		
		1		
2	H2	0		
		1		
1	H1	0		
		1		
0	H0	0		
		1		

Note: All registers are set to 0 when the LC74785/M is reset by the $\overline{\text{RST}}$ pin.

COMMAND1 (Display character data write setup command)

First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 1 identification code Sets up display character data write mode.	When this command is input, the LC74785/M locks in the display character data write mode until the $\overline{\text{CS1}}$ pin goes high.
6	—	0		
5	—	0		
4	—	1		
3	—	0		
2	—	0		
1	—	0		
0	—	0		

Second byte

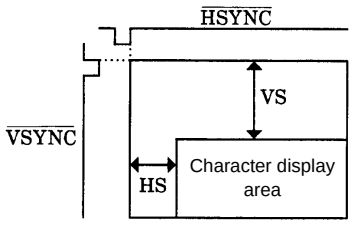
DA 0 to 7	Register	Contents		Notes
		State	Function	
7	at	0	Character attribute off	
		1	Character attribute on	
6	c6	0	Character code (00 to 7F hexadecimal)	
		1		
5	c5	0		
		1		
4	c4	0		
		1		
3	c3	0		
		1		
2	c2	0		
		1		
1	c1	0		
		1		
0	c0	0		
		1		

Note: All registers are set to 0 when the LC74785/M is reset by the $\overline{RST}$ pin.

COMMAND2 Vertical display start position and vertical character size setup command
First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 2 identification code Sets the vertical display start position and the vertical character size	
6	—	0		
5	—	1		
4	—	0		
3	VS21	0	VS21 \ VS20 / 0 / 1 0 / 1H/dot / 2H/dot 1 / 3H/dot / 1H/dot	Second line vertical character size
		1		
2	VS20	0		
		1		
1	VS11	0	VS11 \ VS10 / 0 / 1 0 / 1H/dot / 2H/dot 1 / 3H/dot / 1H/dot	First line vertical character size
		1		
0	VS10	0		
		1		

Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	FS	0	Crystal oscillator frequency: 2fsc	
		1	Crystal oscillator frequency: 4fsc	
5	VP5 (MSB)	0	If VS is the vertical display start position then: $VS = H \times (2 \sum_{n=0}^{5} 2^n VP_n)$ H: the horizontal synchronization pulse period  	The vertical display start position is set by the 6 bits VP0 to VP5. The weight of bit 1 is 2H.
		1		
4	VP4	0		
		1		
3	VP3	0		
		1		
2	VP2	0		
		1		
1	VP1	0		
		1		
0	VP0 (LSB)	0		
		1		

Note: All registers are set to 0 when the LC74785/M is reset by the $\overline{RST}$ pin.

COMMAND3 (Horizontal display start position and horizontal size setup command)

First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 3 identification code Sets the horizontal display start position and the horizontal character size.	
6	—	0		
5	—	1		
4	—	1		
3	HS21	0	HS21 \ HS20 / 0 / 1 0 / 1Tc/dot / 2Tc/dot 1 / 3Tc/dot / 1Tc/dot	Second line horizontal character size
		1		
2	HS20	0		
		1		
1	HS11	0	HS11 \ HS10 / 0 / 1 0 / 1Tc/dot / 2Tc/dot 1 / 3Tc/dot / 1Tc/dot	First line horizontal character size
		1		
0	HS10	0		
		1		

Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	LC	0	Use the LC oscillator for the dot clock	Selects the dot clock used for character display in the horizontal direction.
		1	Use the crystal oscillator for the dot clock	
5	HP5 (MSB)	0	If HS is the horizontal start position then: $HS = Tc \times (2 \sum_{n=0}^{5} 2^n HP_n)$ Tc: Period of the oscillator connected to OSCIN/OSCOUT in operating mode.	The horizontal display start position is set by the 6 bits HP0 to HP5. The weight of bit 1 is 2Tc.
		1		
4	HP4	0		
		1		
3	HP3	0		
		1		
2	HP2	0		
		1		
1	HP1	0		
		1		
0	HP0 (LSB)	0		
		1		

Note: All registers are set to 0 when the LC74785/M is reset by the $\overline{RST}$ pin.

COMMAND4 (Display control setup command)

First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 4 identification code Display control setup	
6	—	1		
5	—	0		
4	—	0		
3	TSTMOD	0	Normal operating mode	This bit must be set to 0.
		1	Test mode	
2	RAMERS	0		Erasing RAM takes about 500 µs. (This operation must be executed in the DSPOFF state.)
		1	Erase display RAM. (Set the RAM data to 7F hexadecimal.)	
1	OSCSTP	0	Do not stop the crystal and LC oscillators.	Valid in external synchronization mode when character display is off.
		1	Stop the crystal and LC oscillators.	
0	SYSRST	0		The registers are reset when the $\overline{CS1}$ pin is low, and the reset state is cleared when $\overline{CS1}$ is set high,
		1	Reset all registers and turn display off.	

Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	BLK2	0	Character display area	Specifies the size for complete fill in
		1	Video display area	
5	BLK1	0	BLK1 \ BLK0: 0 = Blanking off; 1 = Character size; 1 = Border size; 1 = Full character size	Changes the blanking size
		1		
4	BLK0	0		
		1		
3	BK1	0	Blinking period: About 0.5 s	Switches the blinking period
		1	Blinking period: About 1.0 s	
2	BK0	0	Blinking off	Blinking in reverse video mode switches the display between normal character display and reverse video display.
		1	Blinking on	
1	RV	0	Reverse (character reversing) off	
		1	Reverse (character reversing) on	
0	DSPON	0	Character display off	
		1	Character display on	

Note: All registers are set to 0 when the LC74785/M is reset by the $\overline{RST}$ pin.

COMMAND5 (Display control setup command)

First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 5 identification code Display control setup	
6	—	1		
5	—	0		
4	—	1		
3	—	0		
2	HLFTON	0	External synchronizing signal judgment output signal	Switches the $SYNC_{JDG}$ (pin 8) output.
		1	A signal in the range specified by LNA*, LNB*, and LNC* is output.	
1	NON	0	Interlaced	Switches between interlaced and noninterlaced video.
		1	Noninterlaced	
0	INT	0	External synchronization	Switches between external and internal synchronization
		1	Internal synchronization	

Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	—	0		
4	BCL	0	Background coloring on	Only valid in internal synchronization mode.
		1	No background coloring (Only the background level is set)	
3	CB	0	Color burst signal output.	Only valid when BCL is high.
		1	Color burst signal output stopped.	
2	PH2	0		Background color specification
		1		
1	PH1	0		
		1		
0	PH0	0		
		1		

PH2	PH1	PH0	Background color (phase)
0	0	0	Cyan *
0	0	1	Yellow *
0	1	0	Red *
0	1	1	Blue *
1	0	0	Cyan - blue
1	0	1	Green *
1	1	0	Orange
1	1	1	Magenta *

*: When 2 fsc is used.

Note: All registers are set to 0 when the LC74785/M is reset by the $\overline{RST}$ pin.

COMMAND6 (Synchronizing signal detection setup command)

First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 6 identification code Sets up synchronizing signal control.	
6	—	1		
5	—	1		
4	—	0		
3	SEL0	0	Sync separator signal	Switches the SEP_{OUT} (pin 19) output.
		1	Output signal set by MOD0	
2	MOD0	0	High-level output	Only valid when SEL0 is high.
		1	ST pulse signal	
1	DISLIN	0	12 lines	Switches the number of lines displayed.
		1	10 lines	
0	MUT	0	Normal output	CV_{OUT} switching
		1	CV_{IN} is cut and CV_{OUT} is held at the pedestal level.	

Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	RN2	0	RN2 RN1 RN0 Number of times HSYNC detected 0 0 0 0 times 0 0 1 4 times 0 1 0 8 times 1 0 0 16 times	External synchronizing signal detection control Signal absent → signal present transition detection Sets the sampling period in which SYNC can be detected continuously in the horizontal synchronizing signal period (1H).
		1		
5	RN1	0		
		1		
4	RN0	0		
		1		
3	SN3	0	SN3 SN2 SN1 SN0 Number of times HSYNC detected 0 0 0 0 Not detected 0 0 0 1 32 times 0 0 1 0 64 times 0 1 0 0 128 times 1 0 0 0 256 times	External synchronizing signal detection control Signal present → signal absent transition detection Sets the sampling period in which SYNC cannot be detected continuously in the horizontal synchronizing signal period (1H).
		1		
2	SN2	0		
		1		
1	SN1	0		
		1		
0	SN0	0		
		1		

Note: All registers are set to 0 when the LC74785/M is reset by the $\overline{RST}$ pin.

COMMAND7 (Display control setup command)

First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 7 identification code Display control setup	
6	—	1		
5	—	1		
4	—	1		
3	—	0	Extended command 0 identification code	
2	—	0		
1	SEL1	0	Vertical synchronizing signal (external V separation) input	Switches the SEP_{IN} (pin 20) input. Only valid when CTL3 is high.
		1	Frame signal input	
0	CTL3	0	Use internal V separation.	Switches V separation.
		1	Do not use internal V separation.	

Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	—	0		
4	VNPSEL	0	V falling edge detection	Switches the V acquisition polarity in external mode when internal V separation is used.
		1	V rising edge detection	
3	VSPSEL	0	VSEP: about 8.9 µs	Switches the internal V separation period.
		1	VSEP: about 17.8 µs	
2	MSKERS	0	Mask valid	Clears the HSYNC and VSYNK masks.
		1	Mask invalid	
1	MSKSEL	0	3H	Switches the VSYNC mask.
		1	20H	
0	EGL	0	Border level 0 only (VBK0)	Switches the border level. (Only valid when BLK0 is 0 and BLK1 is 1.)
		1	Two-stage border level (VBK0 and VBK1)	

Note: All registers are set to 0 when the LC74785/M is reset by the $\overline{RST}$ pin.

COMMAND8 (Display control setup command)

First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 8 identification code Display control setup	
6	—	1		
5	—	1		
4	—	1		
3	—	0	Extended command 1 identification code	
2	—	1		
1	SEL2	0	External synchronizing signal judgment output signal	Switches the $SYNC_{JDG}$ (pin 8) output Valid when HLFTON is low.
		1	O/$\overline{E}$ signal	
0	MOD1	0	Even field line 21 data extraction (VCR)	Switches line 21 data extraction.
		1	Line 21 data extraction on both odd and even fields (NTSC-TV)	

Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	LNA3	0		Specifies the line whose background is to be changed (If the same line is specified to have different background colors with LNA*, LNB*, and LNC*, then the setting specified by the last command issued will be valid. The previously specification registers (LN* and LP*) will all be reset to 0.)
		1		
5	LNA2	0		
		1		
4	LNA1	0		
		1		
3	LNA0	0		
		1		
2	LPA2	0		Specifies the background color.
		1		
1	LPA1	0		
		1		
0	LPA0	0		
		1		

LNA3	LNA2	LNA1	LNA0	Specified line
0	0	0	0	Do not change the line background
0	0	0	1	Line 1
0	0	1	0	Line 2
0	0	1	1	Line 3
0	1	0	0	Line 4
0	1	0	1	Line 5
0	1	1	0	Line 6
0	1	1	1	Line 7
1	0	0	0	Line 8
1	0	0	1	Line 9
1	0	1	0	Line 10
1	0	1	1	Line 11
1	1	—	—	Line 12

LPA2	LPA1	LPA0	Background color (phase)
0	0	0	Cyan *
0	0	1	Yellow *
0	1	0	Red *
0	1	1	Blue *
1	0	0	Cyan - blue
1	0	1	Green *
1	1	0	Orange
1	1	1	Magenta *

*: When 2 fsc is used.

Note: All registers are set to 0 when the LC74785/M is reset by the $\overline{RST}$ pin.

COMMAND9 (Display control setup command)

First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 9 identification code Display control setup	
6	—	1		
5	—	1		
4	—	1		
3	—	1	Extended command 2 identification code	
2	—	0		
1	LNBSEL	0	Normal line background color operation	Switches the RV mode background color for the line specified by LNB* for characters specified for RV display.
		1	RV characters have the background color specified by PH* or the RV character background color is white.	
0	MOD2	0	LNBSEL: 1 setting specification	Valid when LNBSEL is high
		1	RV characters have the background color specified by PH*, characters are white.	

Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	LNB3	0		Specifies the line whose background is to be changed (If the same line is specified to have different background colors with LNA*, LNB*, and LNC*, then the setting specified by the last command issued will be valid. The previously specification registers (LN* and LP*) will all be reset to 0.)
		1		
5	LNB2	0		
		1		
4	LNB1	0		
		1		
3	LNB0	0		
		1		

LNB3	LNB2	LNB1	LNB0	Specified line
0	0	0	0	Do not change the line background
0	0	0	1	Line 1
0	0	1	0	Line 2
0	0	1	1	Line 3
0	1	0	0	Line 4
0	1	0	1	Line 5
0	1	1	0	Line 6
0	1	1	1	Line 7
1	0	0	0	Line 8
1	0	0	1	Line 9
1	0	1	0	Line 10
1	0	1	1	Line 11
1	1	—	—	Line 12

2	LPB2	0		Specifies the background color.
		1		
1	LPB1	0		
		1		
0	LPB0	0		
		1		

LPB2	LPB1	LPB0	Background color (phase)
0	0	0	Cyan *
0	0	1	Yellow *
0	1	0	Red *
0	1	1	Blue *
1	0	0	Cyan - blue
1	0	1	Green *
1	1	0	Orange
1	1	1	Magenta *

*: When 2 fsc is used.

Note: All registers are set to 0 when the LC74785/M is reset by the $\overline{\text{RST}}$ pin.

COMMAND10 (Display control setup command)

First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 10 identification code Display control setup	
6	—	1		
5	—	1		
4	—	1		
3	—	1	Extended command 2 identification code	
2	—	0		
1	LNCSEL	0	Normal line background color operation	Switches the RV mode background color for the line specified by LNC* for characters specified for RV display.
		1	RV characters have the background color specified by PH* or the RV character background color is white.	
0	MOD3	0	LNCSEL: 1 setting specification	Valid when LNCSEL is high
		1	RV characters have the background color specified by PH*, characters are white.	

Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	LNC3	0		Specifies the line whose background is to be changed. (If the same line is specified to have different background colors with LNA*, LNB*, and LNC*, then the setting specified by the last command issued will be valid. The previously specification registers (LN* and LP*) will all be reset to 0.)
		1		
5	LNC2	0		
		1		
4	LNC1	0		
		1		
3	LNC0	0		
		1		
2	LPC2	0		Specifies the background color.
		1		
1	LPC1	0		
		1		
0	LPC0	0		
		1		

LNC3	LNC2	LNC1	LNC0	Specified line
0	0	0	0	Do not change the line background
0	0	0	1	Line 1
0	0	1	0	Line 2
0	0	1	1	Line 3
0	1	0	0	Line 4
0	1	0	1	Line 5
0	1	1	0	Line 6
0	1	1	1	Line 7
1	0	0	0	Line 8
1	0	0	1	Line 9
1	0	1	0	Line 10
1	0	1	1	Line 11
1	1	—	—	Line 12

LPC2	LPC1	LPC0	Background color (phase)
0	0	0	Cyan *
0	0	1	Yellow *
0	1	0	Red *
0	1	1	Blue *
1	0	0	Cyan - blue
1	0	1	Green *
1	1	0	Orange
1	1	1	Magenta *

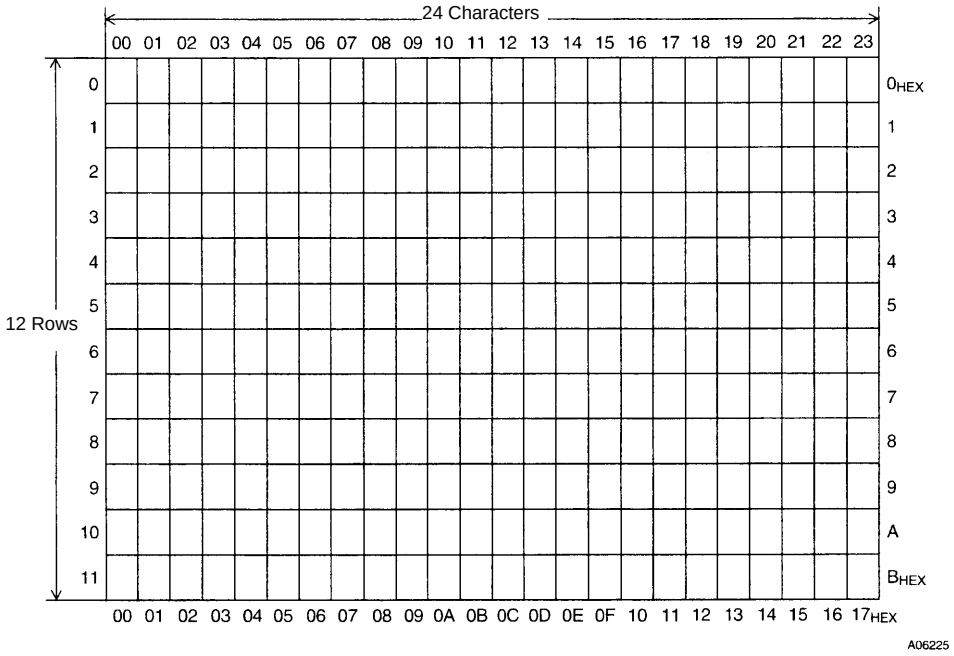
*: When 2 fsc is used.

Note: All registers are set to 0 when the LC74785/M is reset by the $\overline{\text{RST}}$ pin.

Display Screen Structure

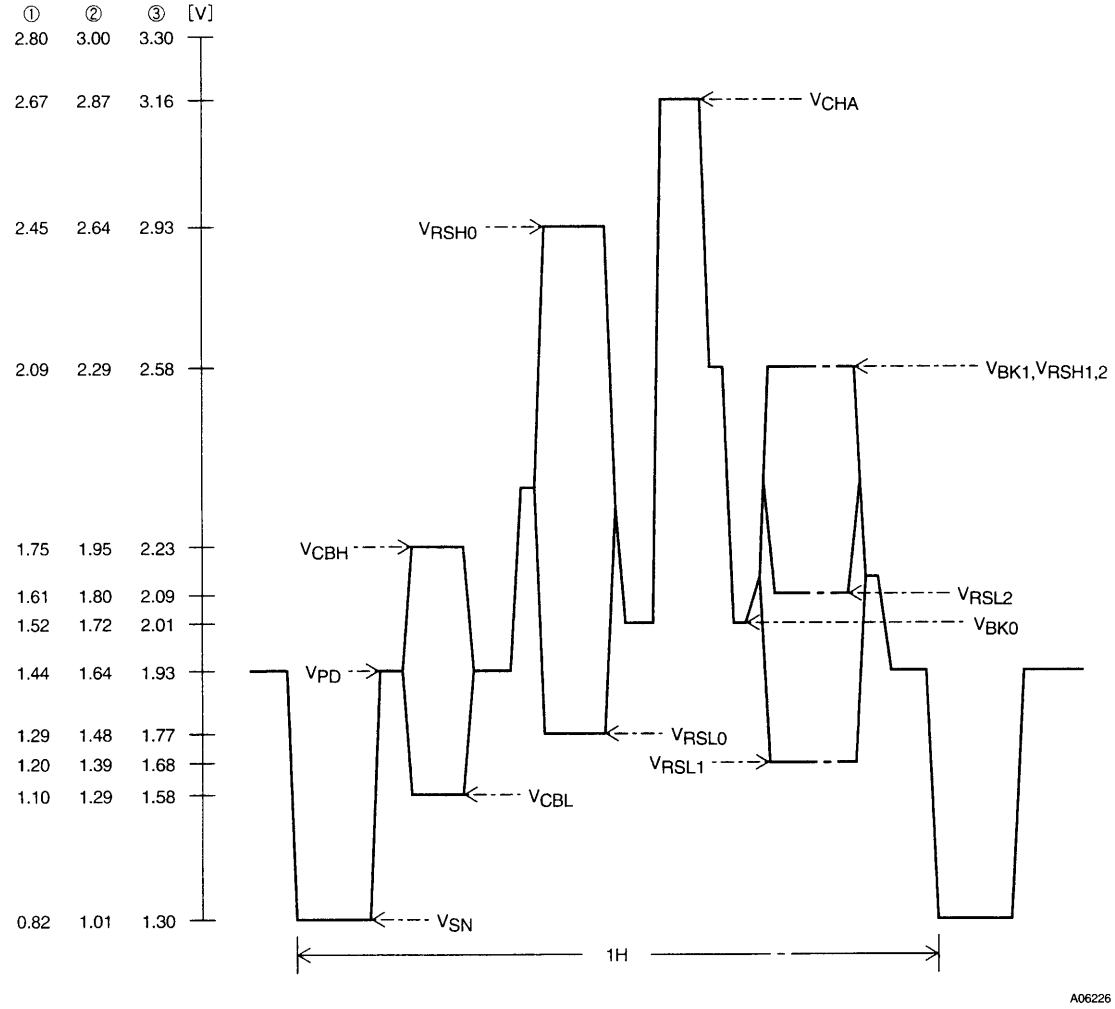
The display consists of 12 lines of 24 characters.
Up to 288 characters can be displayed.
The number of characters that can be displayed is reduced when enlarged characters are displayed.
Display memory addresses are specified as row (0 to 11 decimal) and column (0 to 23 decimal) addresses.

Display Screen Structure (display memory addresses)



Composite Video Signal Output Levels (internally generated levels)

CV_{OUT} output level waveform ($V_{DD}2$ = 5.00 V)

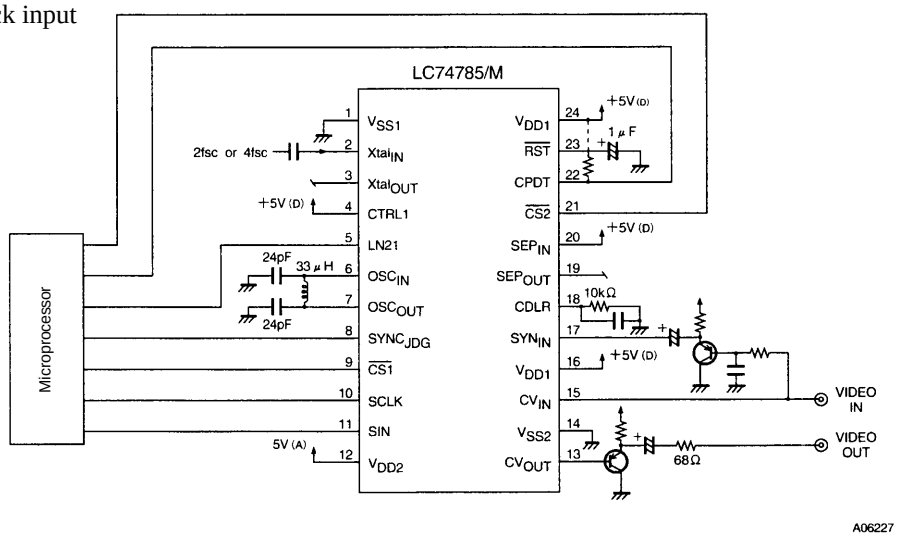


Output level		Output voltage (1) [V]	Output voltage (2) [V]	Output voltage (3) [V]
V_{CHA}:	Character	2.67	2.87	3.16
$V_{RSH}0$:	High for background colors other than blue	2.45	2.64	2.93
$V_{RSH}1,2$	High for blue background colors 1 and 2	2.09	2.29	2.58
$V_{BK}1$:	Border 1	2.09	2.29	2.58
V_{CBH}:	High for the color burst signal	1.75	1.95	2.23
$V_{RSL}2$:	Low for blue background color 2	1.61	1.80	2.09
$V_{BK}0$:	Border 0	1.52	1.72	2.01
V_{PD}:	Pedestal level	1.44	1.64	1.93
$V_{RSL}0$:	Low for background colors other than blue	1.29	1.48	1.77
$V_{RSL}1$	Low for blue background color 1	1.20	1.39	1.68
V_{CBL}:	Low for the color burst signal	1.10	1.29	1.58
V_{SN}:	Sync	0.82	1.01	1.30

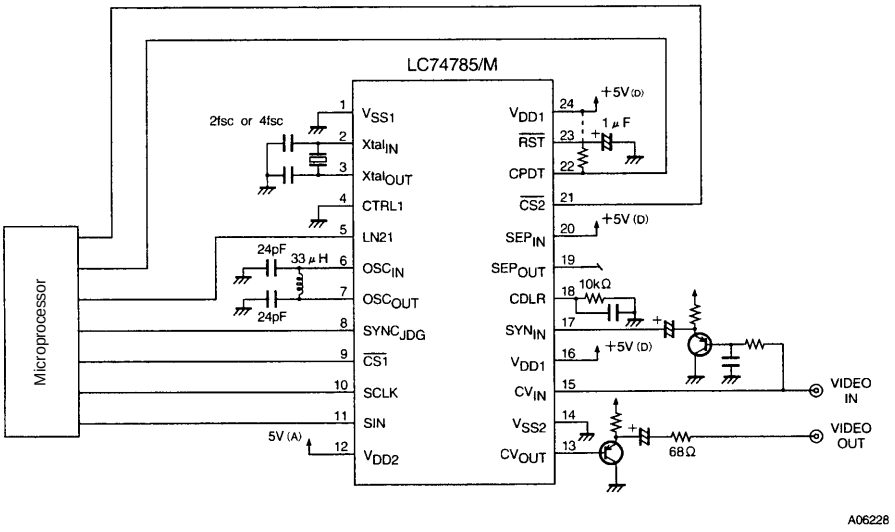
Note: $V_{DD}2$ = 5.0 V.

Sample Application Circuit (When the LC74785/M is used in conjunction with a single-chip Y/C circuit.)

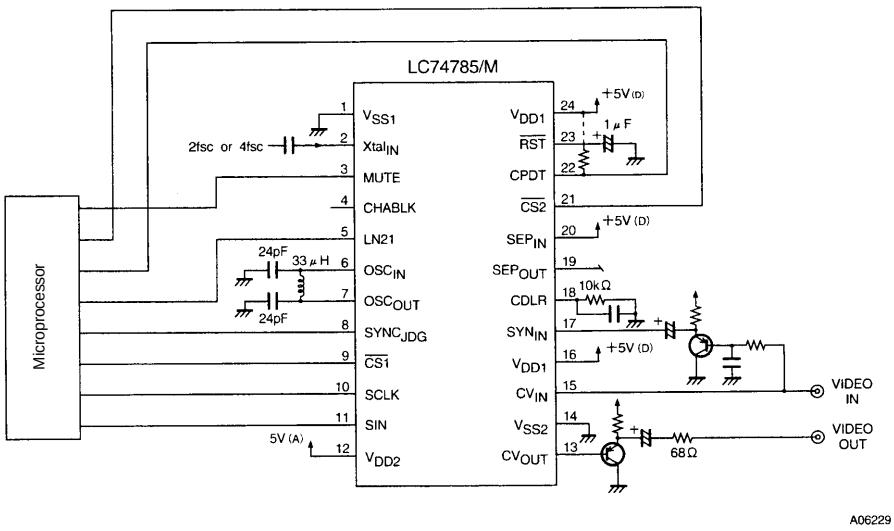
External system clock input



Crystal oscillator



External system clock input (when the pin 3 and 4 functions are modified by mask options)



Note: When a sync tip level of 1.3 V DC (CV_{IN} input signal: sync tip = 1.3 V) is selected for the internal generated video signals by option settings, the electrolytic capacitor connected to SYN_{IN} must be connected with the correct polarity.
When $V_{DD}1$ is 5.0 V, the SYN_{IN} input video signal pedestal level is clamped at about 2.5 V DC.