Ordering number: EN 4978

CMOS LSI

SANYO No. 4978

LC7458B-04

Closed-Caption Decoder LSI

Overview

The LC7458B-04 is a closed-caption system (CCS) decoder and OSD display LSI that conforms to the most recent American FCC standard issued on April 12, 1991. Together with an LA7945N Front End IC it forms a complete 2-chip system.

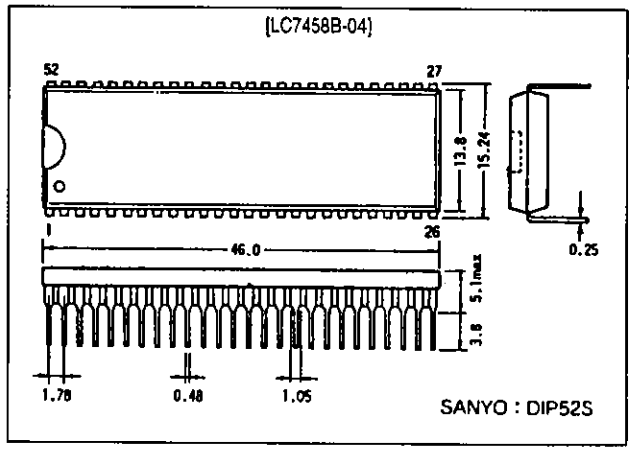
Features

- FCC Standard Conforming Signal Demodulation
  - Caption optional line display (new function)
  - Color character display
  - Lower-case character display
  - Underline display
  - Flashing
  - Italic display
  - Channel 1/Channel 2 mode switching and display
  - Field 1/Field 2 mode switching and display
  - Caption/Text mode switching and display
- Control System
  - Serial/Parallel signal mode switching
  - 5 parallel inputs or serial mode (PWM) interface selectable
- Miscellaneous
  - Supports 16 characters from the EIA-608 Optional Extended Character set
  - Automatic display ON/OFF
  - On-Screen Display positioning input pins
  - 5V supply voltage

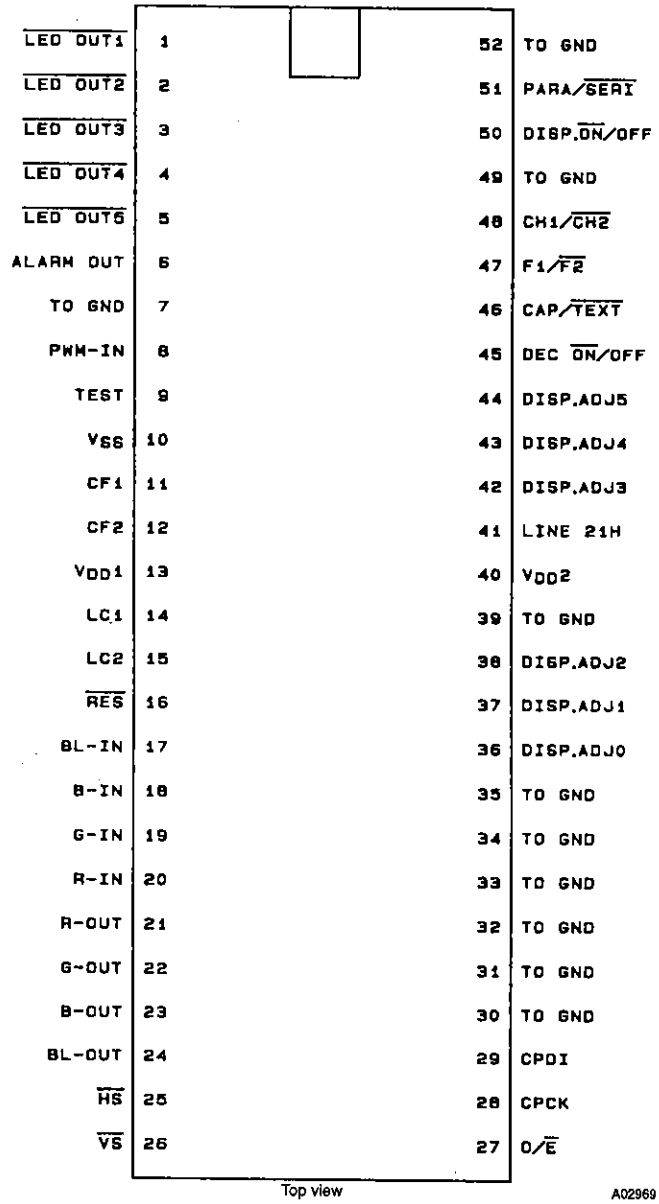
Package Dimensions

unit: mm

3128-DIP52S



Pin Assignment



Pin Functions

Number	Name	I/O	After reset[1]	Built-in resistance	Function description	Connection when not in use
1	$\overline{\text{LED OUT1}}$	O	Hi-Z	Nch-OD	Caption ON output (active low)	GND
2	$\overline{\text{LED OUT2}}$	O	Hi-Z	Nch-OD	Text ON output (active low)	GND
3	$\overline{\text{LED OUT3}}$	O	Hi-Z	Nch-OD	Channel 1 ON output (active low)	GND
4	$\overline{\text{LED OUT4}}$	O	Hi-Z	Nch-OD	Channel 2 ON output (active low)	GND
5	$\overline{\text{LED OUT5}}$	O	Hi-Z	Nch-OD	Field 2 mode output (active low)	GND
6	ALARM OUT	O	Hi-Z	Nch-OD	Alarm signal output (active high)	GND
7	–	–	–	–	Not used (tied to GND)	GND
8	PWM-IN	I	Hi-Z	Nch-OD	PWM control signal input	GND
9	TEST	O	–	Pull-up	Test pin (normally open)	Open
10	V_{SS}	–	–	–	Supply negative pin	

Number	Name	I/O	After reset[1]	Built-in resistance	Function description	Connection when not in use
11	CF1	I	–	–	12MHz ceramic filter oscillator element, system clock connection	
12	CF2	O	–	–	12MHz ceramic filter oscillator element, system clock connection	
13	$V_{DD}1$	–	–	–	Supply positive pin	
14	LC1	I	–	–	LC oscillator circuit input pin	
15	LC2	O	–	–	LC oscillator circuit output pin	
16	$\overline{RES}$	I	–	–	System reset input pin	
17	BL-IN	I	Hi-Z	–	Blanking signal input pin (active high)	GND
18	B-IN	I	Hi-Z	–	RGB signal input pin (active high)	GND
19	G-IN	I	Hi-Z	–	RGB signal input pin (active high)	GND
20	R-IN	I	Hi-Z	–	RGB signal input pin (active high)	GND
21	R-OUT	O	Low	–	RGB signal output pin (active high)	Open
22	G-OUT	O	Low	–	RGB signal output pin (active high)	Open
23	B-OUT	O	Low	–	RGB signal output pin (active high)	Open
24	BL-OUT	O	Low	–	Blanking signal output pin (active high)	Open
25	$\overline{HS}$	I	Hi-Z	–	Horizontal sync signal input pin (active low)	
26	$\overline{VS}$	I	Hi-Z	–	Vertical sync signal input pin (active low)	
27	O/$\overline{E}$	I	Hi-Z	–	Field control pin (connects to LA7945)	
28	CPCK	I	Hi-Z	–	Caption clock input pin (connects to LA7945)	
29	CPDI	I	Hi-Z	–	Caption data input pin (connects to LA7945)	
30	–	–	–	–	Not used (tied to GND)	GND
31	–	–	–	–	Not used (tied to GND)	GND
32	–	–	–	–	Not used (tied to GND)	GND
33	–	–	–	–	Not used (tied to GND)	GND
34	–	–	–	–	Not used (tied to GND)	GND
35	–	–	–	–	Not used (tied to GND)	GND
36	DISP ADJ0	I	Hi-Z	Nch-OD	OSD display start position adjust	
37	DISP ADJ1	I	Hi-Z	Nch-OD	OSD display start position adjust	
38	DISP ADJ2	I	Hi-Z	Nch-OD	OSD display start position adjust	
39	–	–	–	–	Not used (tied to GND)	GND
40	$V_{DD}2$	–	–	–	Supply positive pin	
41	LINE 21H	I	Hi-Z	Nch-OD	Line 21H sync signal input (connects to LA7945)	
42	DISP ADJ3	I	Hi-Z	Nch-OD	OSD display start position adjust	
43	DISP ADJ4	I	Hi-Z	Nch-OD	OSD display start position adjust	
44	DISP ADJ5	I	Hi-Z	Nch-OD	OSD display start position adjust	
45	DEC $\overline{ON}$/OFF	I	High	Pull-up	Parallel signal control, caption decode ON/OFF	Open
46	CAP/$\overline{TEXT}$	I	High	Pull-up	Parallel signal control, caption/text switching	Open
47	F1/$\overline{F2}$	I	High	Pull-up	Parallel signal control, field 1/field 2 switching	Open
48	CH1/$\overline{CH2}$	I	High	Pull-up	Parallel signal control, channel 1/channel 2 switching	Open
49	–	–	–	–	Not used (tied to GND)	Open
50	DISP $\overline{ON}$/OFF	I	High	Pull-up	Parallel signal control, caption display ON/OFF	Open
51	PARA/$\overline{SERI}$	I	Hi-Z	Nch-OD	Parallel/serial control select	
52	–	–	–	–	Not used (tied to GND)	GND

1. Hi-Z = high impedance, Nch-OD = N-channel open-drain

Specifications

Maximum Ratings at Ta = 25°C, V_{SS} = 0V

Parameter	Symbol	Conditions	min	typ	max	Unit
Maximum supply voltage	V_{DD} max	V_{DD}, $V_{DD}V_{pp}$: $V_{DD} = V_{DD}V_{pp}$	–0.3	–	+7.0	V
Input voltage	V_{I1}	$\overline{RES}$, $\overline{HS}$, $\overline{VS}$, CPCK, CPDI, O/$\overline{E}$, DISP ADJ0 to 5, BL-IN, R-IN, G-IN, B-IN, PARA/$\overline{SERI}$, DISP $\overline{ON}$/OFF, CH1/$\overline{CH2}$, F1/$\overline{F2}$, CAP/$\overline{TEXT}$, DEC $\overline{ON}$/OFF, PWM-IN	–0.3	–	V_{DD} + 0.3	V
Output voltage	V_{O1}	BL-OUT, R-OUT, G-OUT, B-OUT	–0.3	–	V_{DD} + 0.3	V
Output high-level current						
Peak output current (per pin)	I_{OPH1}	$\overline{LED\ OUT1}$ to 5, ALARM OUT (per pin)	–2	–	–	mA
	I_{OPH2}	BL-OUT, R-OUT, G-OUT, B-OUT, (per CMOS output)	–5	–	–	mA
Total output current (total for all pins)	ΣI_{OAH1}	$\overline{LED\ OUT1}$ to 5, ALARM OUT (sum of all pins)	–10	–	–	mA
	ΣI_{OAH2}	BL-OUT, R-OUT, G-OUT, B-OUT (sum of all pins)	–12	–	–	mA
Output low-level current						
Peak output current (per pin)	I_{OPL1}	$\overline{LED\ OUT1}$ to 5, ALARM OUT (per pin)	–	–	20	mA
	I_{OPL2}	BL-OUT, R-OUT, G-OUT, B-OUT (per pin)	–	–	5	mA
Total output current (total for all pins)	ΣI_{OAL1}	$\overline{LED\ OUT1}$ to 5, ALARM OUT (sum of all pins)	–	–	40	mA
	ΣI_{OAL2}	BL-OUT, R-OUT, G-OUT, B-OUT (sum of all pins)	–	–	12	mA
Maximum power dissipation	Pd max	DIP52S; Ta = –30 to +70°C	–	–	430	mW
Operating temperature	Topr		–30	–	+70	°C
Storage temperature	Tstg		–55	–	+150	°C

Allowable Operating Ranges at Ta = –30 to +70°C, V_{SS} = 0V

Parameter	Symbol	Conditions	min	typ	max	Unit
Operating supply voltage	V_{DD}	V_{DD}	4.5	–	5.5	V
Input high-level voltage	V_{IH1}	PARA/$\overline{SERI}$, DISP $\overline{ON}$/OFF, CAP/$\overline{TEXT}$, F1/$\overline{F2}$, DEC $\overline{ON}$/OFF, CH1/$\overline{CH2}$ (Schmitt); V_{DD} = 4.5 to 5.5V	$0.6V_{DD}$	–	V_{DD}	V
	V_{IH2}	DISP ADJ0 to 5, $\overline{HS}$, $\overline{VS}$, O/$\overline{E}$, CPCK, CPDI, LINE21, $\overline{RES}$ (Schmitt); V_{DD} = 4.5 to 5.5V	$0.75V_{DD}$	–	V_{DD}	V
	V_{IH3}	BL-IN, B-IN, G-IN, R-IN; V_{DD} = 4.5 to 5.5V	$0.7V_{DD}$	–	V_{DD}	V
Input low-level voltage	V_{IL1}	PARA/$\overline{SERI}$, DISP $\overline{ON}$/OFF, CAP/$\overline{TEXT}$, F1/$\overline{F2}$, DEC $\overline{ON}$/OFF, CH1/$\overline{CH2}$ (Schmitt); V_{DD} = 4.5 to 5.5V	V_{SS}	–	$0.2V_{DD}$	V
	V_{IL2}	DISP ADJ0 to 5, $\overline{HS}$, $\overline{VS}$, O/$\overline{E}$, CPCK, CPDI, LINE21, $\overline{RES}$ (Schmitt); V_{DD} = 4.5 to 5.5V	V_{SS}	–	$0.25V_{DD}$	V
	V_{IL3}	BL-IN, B-IN, G-IN, R-IN; V_{DD} = 4.5 to 5.5V	V_{SS}	–	$0.3V_{DD}$	V
Oscillator frequency range[1]	FmCF	CF1, CF2; 12MHz ceramic oscillator, see Figure 1, V_{DD} = 4.5 to 5.5V	11.76	12	12.24	MHz
	FmLC	LC1, LC2; 12MHz LC oscillator, V_{DD} = 4.5 to 5.5V	–	12	–	MHz
Oscillator stabilization time[2]	TmsCF	CF1, CF2; 12MHz ceramic oscillator, see Figure 3, V_{DD} = 4.5 to 5.5V	–	0.02	0.2	ms

1. Oscillator constants are shown in Tables 1 and 2.
2. The oscillator stabilization time is the time from the moment the supply is applied or main clock oscillation is resumed after a stop until the oscillations stabilize. See Figure 3.

Electrical Characteristics at Ta = –30 to +70°C, V_{SS} = 0V

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high-level current	I_{IH1}	PARA/$\overline{SERI}$, DISP $\overline{ON}$/OFF, CAP/$\overline{TEXT}$, CH1/$\overline{CH2}$, F1/$\overline{F2}$, DEC $\overline{ON}$/OFF, DISP ADJ0 to 5, BL-IN, LINE21, B-IN, G-IN, R-IN, $\overline{RES}$, $\overline{HS}$, $\overline{VS}$, O/$\overline{E}$, CPCK, CPDI; V_{IN} = V_{DD}, V_{DD} = 4.5 to 5.5V	–	–	1	µA
Input low-level current	I_{IL1}	PARA/$\overline{SERI}$, DISP $\overline{ON}$/OFF, CAP/$\overline{TEXT}$, CH1/$\overline{CH2}$, F1/$\overline{F2}$, DEC $\overline{ON}$/OFF, DISP ADJ0 to 5, BL-IN, LINE21, B-IN, G-IN, R-IN, $\overline{RES}$, $\overline{HS}$, $\overline{VS}$, O/$\overline{E}$, CPCK, CPDI; V_{IN} = V_{SS}, V_{DD} = 4.5 to 5.5V	–1	–	–	µA
Output high-level voltage	V_{OH1}	R-OUT, G-OUT, B-OUT, BL-OUT, $\overline{LED\ OUT1}$ to 5, ALARM OUT; I_{OH} = –1.0mA, V_{DD} = 4.5 to 5.5V	V_{DD} – 1	–	–	V
	V_{OH2}	R-OUT, G-OUT, B-OUT, BL-OUT, $\overline{LED\ OUT1}$ to 5, ALARM OUT; I_{OH} = –0.1mA, V_{DD} = 4.5 to 5.5V	V_{DD} – 0.5	–	–	V
Output low-level voltage	V_{OL1}	$\overline{LED\ OUT1}$ to 5, ALARM OUT; I_{OL} = 10mA, V_{DD} = 4.5 to 5.5V	–	–	1.5	V
	V_{OL2}	$\overline{LED\ OUT1}$ to 5, ALARM OUT; I_{OL} = 1.6mA, V_{DD} = 4.5 to 5.5V	–	–	0.4	V
	V_{OL3}	R-OUT, G-OUT, B-OUT, BL-OUT; I_{OL} = 3.0mA, V_{DD} = 4.5 to 5.5V	–	–	0.4	V
Pull-up MOS transistor resistance		PARA/$\overline{SERI}$, DISP $\overline{ON}$/OFF, CAP/$\overline{TEXT}$, CH1/$\overline{CH2}$, F1/$\overline{F2}$, DEC $\overline{ON}$/OFF; V_{OH} = 0.9V_{DD}, V_{DD} = 4.5 to 5.5V	13	38	80	kΩ
Hysteresis voltage	V_{HIS}	$\overline{RES}$, $\overline{HS}$, $\overline{VS}$, O/$\overline{E}$, CPCK, CPDI, PARA/$\overline{SERI}$, DISP $\overline{ON}$/OFF, CAP/$\overline{TEXT}$, CH1/$\overline{CH2}$, F1/$\overline{F2}$, DEC $\overline{ON}$/OFF, DISP ADJ0 to 5, LINE21; V_{DD} = 4.5 to 5.5V	–	0.1V_{DD}	–	V
Pin capacitance	C_P	All pins[1]; f = 1MHz, V_{DD} = 4.5 to 5.5V	–	10	–	pF

1. All pins other than the pin measured have V_{IN} = V_{SS}, Ta = 25°C.

Pulse Input Conditions at Ta = –30 to +70°C, V_{SS} = 0V

Parameter	Symbol	Conditions	min	typ	max	Unit
High/low-level pulse width	TP_{IH1} TP_{IL1}	LINE21; interrupt status flags can be set, timer/counter 0 can count pulses, V_{DD} = 4.5 to 5.5V	1	–	–	Tcyc
	TP_{IL2}	$\overline{RES}$; device can be reset, V_{DD} = 4.5 to 5.5V	200	–	–	µs
	TP_{IH2} TP_{IL3}	$\overline{HS}$, $\overline{VS}$; display position can be controlled. $\overline{HS}$ and $\overline{VS}$ active edges > 1Tcyc apart, see Figure 5, V_{DD} = 4.5 to 5.5V	2	–	–	Tcyc
Rise/fall transition time	TT_{HL}/TT_{LH}	$\overline{HS}$; see Figure 6, V_{DD} = 4.5 to 5.5V	–	–	500	ns

Current Consumption Characteristics at Ta = –30 to +70°C, V_{SS} = 0V

Parameter	Symbol	Conditions	min	typ	max	Unit
Normal operating current consumption[1]	I_{DDOP1}	V_{DD}; FmCF = 12MHz ceramic oscillator, FmLC = 12MHz LC oscillator, system clock:main clock, V_{DD} = 4.5 to 5.5V	–	15	25	mA

1. The current consumption does not include the output transistor and pull-up MOS transistor current.

Table 1. Ceramic oscillator guaranteed constants (main clock)

Oscillator type	Manufacturer	Oscillator element	C1[1]	C2[1]
12 MHz ceramic oscillator	Murata	CSA12.0MTZ	33pF	33pF
		CSA12.0MT	33pF	33pF
		CST12.0MT	Built-in	
	Kyocera	KBR-12.0M	33pF	33pF

1. C1 and C2 should be ±10% K tolerance types with SL characteristics.

Table 2. LC oscillator recommended constants (OSD clock)

Oscillator type	L	C3	C4
12 MHz LC oscillator	12μH	18pF	18pF

Note that the parts making up the oscillator should be mounted as close as possible with circuit patterns as short as possible to reduce the effects of the circuit pattern.

The oscillator characteristics above are not guaranteed for oscillator elements other than those listed.

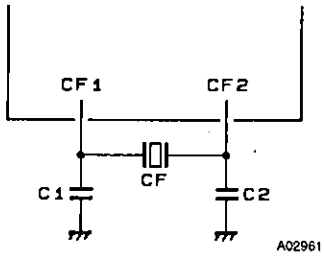


Figure 1. Main clock (ceramic oscillator)

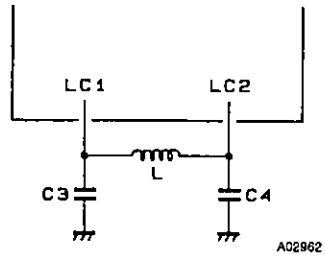


Figure 2. OSD clock (LC oscillator)

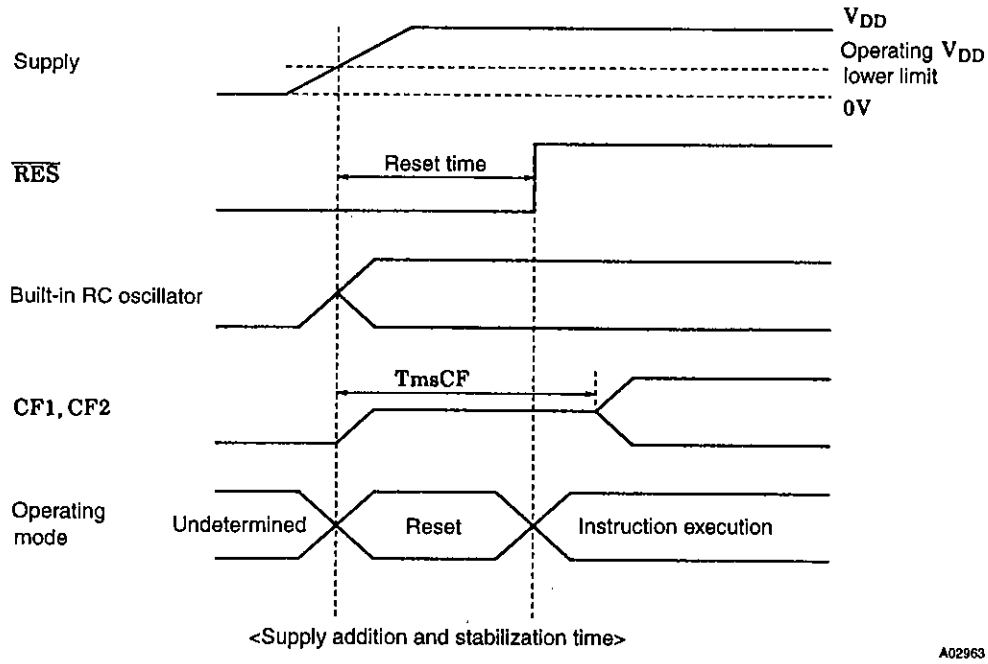
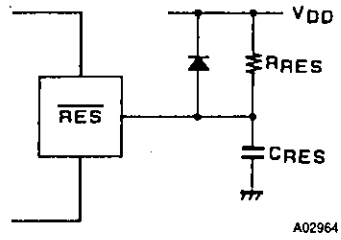
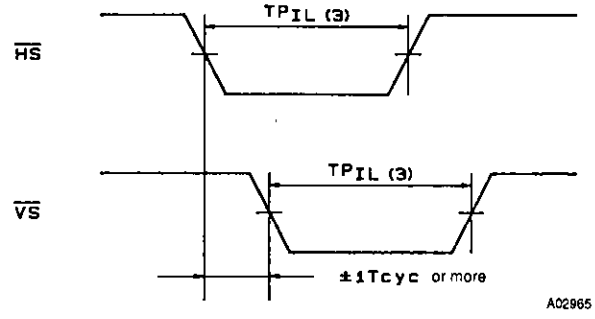


Figure 3. Oscillator stabilization time

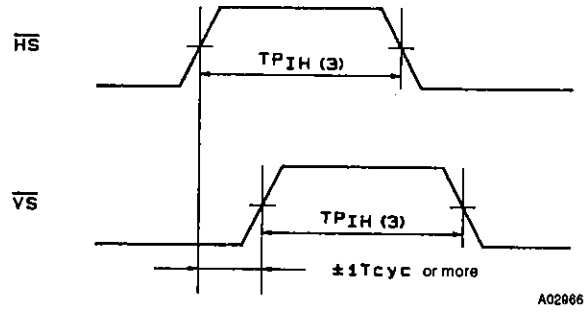


Note. Choose values for C_{RES} and R_{RES} such that the reset time is > 200µs.

Figure 4. Reset circuit



(a) Falling-edge sync (active low)



(b) Rising-edge sync (active high)

Figure 5. Pulse input timing conditions 1

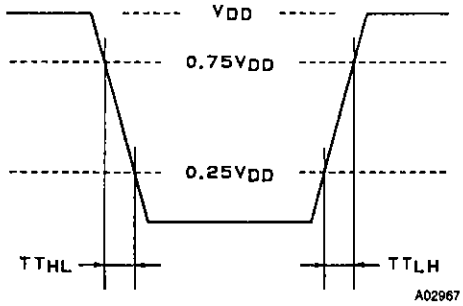


Figure 6. Pulse input timing conditions 2

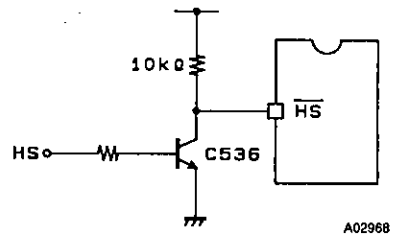
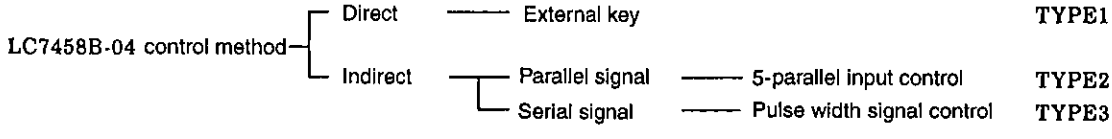


Figure 7. Recommended interface circuit

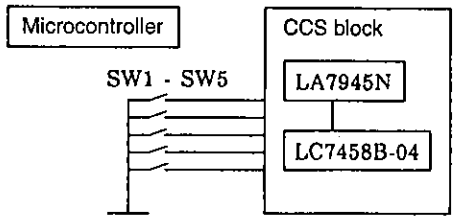
Mode Control

The LC7458B-04 allows, using a simple interface, a CCS function to be added to any of the existing television systems. The degree of freedom of using microcontroller input/output pins and different program changes mean that any one of three possible interfaces can be selected to best match design requirements. The LC7458B-04 interface methods can broadly be classified into two categories—direct control by external keys and indirect control using signals from a microcontroller.



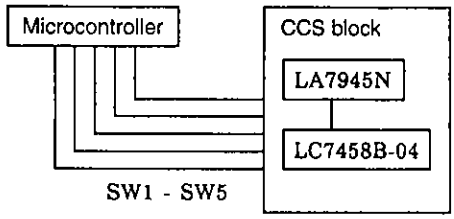
The control method, parallel signal control (types 1 and 2) or pulse width signal (PWM) control (type 3), is selected by the level on pin 51 when power is applied.
High: Parallel signal control (types 1 and 2)
Low: Pulse width signal (PWM) control (type 3)

Type 1: External Key Control



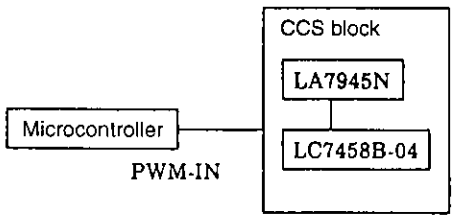
Changed microcontroller parameters:
1. Hardware
None
2. Software
None
If pin 50 (DISP $\overline{\text{ON}}$/OFF) is tied to GND, then 4-key control is also possible.
Note that pin 51 (PARA/$\overline{\text{SERI}}$) is used pull-up.

Type 2: 5 Parallel Input Control



Changed microcontroller parameters:
1. Hardware
5 output pins required
2. Software
Parallel signal generation
Note that pin 51 (PARA/$\overline{\text{SERI}}$) is used pull-up.

Type 3: Pulse Width Signal (PWM)



Changed microcontroller parameters:
1. Hardware
1 output pin required
2. Software
PWM control signal generation
Note that pin 51 (PARA/$\overline{\text{SERI}}$) and pin 52 are connected to GND.

Parallel Input Control

DEC $\overline{\text{ON}}$/OFF (pin 45)

Caption system decoder function ON/OFF switching
High: Caption OFF
Low: Caption ON

CAP/$\overline{\text{TEXT}}$ (pin 46)

Caption/text switching
High: Caption
Low: Text

F1/$\overline{\text{F2}}$ (pin 47)

Caption field switching
High: Field 1
Low: Field 2

CH1/$\overline{\text{CH2}}$ (pin 48)

Caption channel switching
High: Channel 1
Low: Channel 2

DISP $\overline{\text{ON}}$/OFF (pin 50)

Caption display ON/OFF switching
High: Caption display OFF
Low: Caption display ON

Each switch should be lock-type with a chattering rejection time of 60ms.

Parallel Input Mode Transitions

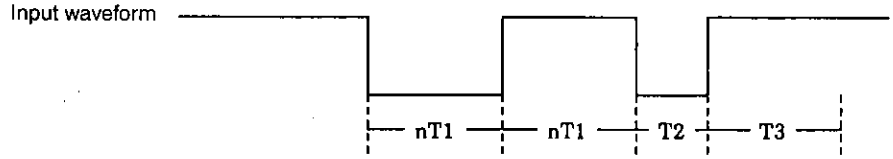
Input	Mode				
	TV mode (caption OFF)[1]	Caption CH1	Caption CH2	Text CH1	Text CH2
DEC $\overline{ON}$/OFF	High	Low	Low	Low	Low
CAPTION/$\overline{TEXT}$	×	High	High	Low	Low
FIELD1/$\overline{FIELD2}$	×	FIELD1 = High and FIELD2 = Low for each mode			
CHANNEL1/$\overline{CHANNEL2}$	×	High	Low	High	Low

1. × = don't care

Decoding commences when DEC $\overline{ON}$/OFF is ON. While DISP $\overline{ON}$/OFF is not ON, the caption is not displayed on the screen. Also if DISP $\overline{ON}$/OFF goes from ON to OFF while decoding, then decoding continues and the screen display is removed.

TV mode is restored after a reset.

Pulse Width Signal (PWM) Control



PWM Timing

$2 \leq n \leq 10$

T1: Command time (490 to 510µs)
T2: Command decision time (300 to 500µs)
T3: Input prohibit time (33ms)

PWM Command Summary

2T: Display stop
3T: Display re-start
4T: Caption channel 1
5T: Text channel 1
6T: Caption channel 2
7T: Text channel 2
8T: TV mode
9T: Field 1
10T: Field 2

LED Display Functions

The LC7458B-04 has 5 built-in LED driver circuits which are used to indicate the different modes of operation.

$\overline{LED\ OUT1}$ (pin 1)

Caption mode when ON. Text mode or decoder when OFF.

$\overline{LED\ OUT2}$ (pin 2)

Text mode when ON. Caption mode or decoder when OFF.

$\overline{LED\ OUT3}$ (pin 3)

Channel 1 selected when ON. Channel 2 selected or decoder when OFF.

$\overline{LED\ OUT4}$ (pin 4)

Channel 2 selected when ON. Channel 1 selected or decoder when OFF.

$\overline{LED\ OUT5}$ (pin 5)

Field 2 selected when ON. Field 1 selected or decoder when OFF.

Automatic Display ON/OFF

The LC7458B-04 uses the presence of valid data on line 21H to automatically switch display ON/OFF to prevent the inadvertent display of erroneous captions. If 45 continuous instances of invalid data (parity error) are detected, the display is automatically removed. Then if 15 continuous instances of valid data is received, the display is re-started.

Alarm Function

If the caption data on line 21H is the alarm ON code, then ALARM OUT (pin 6) goes high. This condition is maintained until either an alarm OFF code is received or a decoder reset occurs.

OSD Display Start Positioning Function

After a reset, the levels on DISP ADJ0 to DISP ADJ5 (pins 36 to 38 and 42 to 44) at the next horizontal sync signal $\overline{HS}$ rising edge determine the horizontal display start position out of a possible 64 positions.

The display start position is given by

Start Position = [DISP ADJ5 to 0] $\times 2 \times T_{LC}$

where T_{LC} is the LC oscillator period.

Extended Characters

Of the 64 EIA-608 Optional Extended Characters, the following 16 are supported.

Data channel 1	Data channel 2	Symbol	Description	Also used for:
12 20	1A 20	Á	Capital 'A' with acute accent	Portuguese
12 21	1A 21	É	Capital 'E' with acute accent	French, Portuguese
12 22	1A 22	Ó	Capital 'O' with acute accent	Portuguese
12 23	1A 23	Ú	Capital 'U' with acute accent	Portuguese
12 24	1A 24	Ü	Capital 'U' with diaeresis or umlaut	French, German, Portuguese
12 25	1A 25	ü	Small 'u' with diaeresis or umlaut	French, German, Portuguese
12 26	1A 26	‘	Opening single quote	
12 27	1A 27	¡	Inverted exclamation mark	
12 28	1A 28	*	Asterisk	ASCII
12 29	1A 29	'	Plain single quote	
12 2A	1A 2A	—	em dash	
12 2B	1A 2B	©	Copyright symbol	
12 2C	1A 2C	SM	Service mark symbol	
12 2D	1A 2D	°	Round bullet	
12 2E	1A 2E	“	Opening double quotes	
12 2F	1A 2F	”	Closing double quotes	

Sample Application Circuits

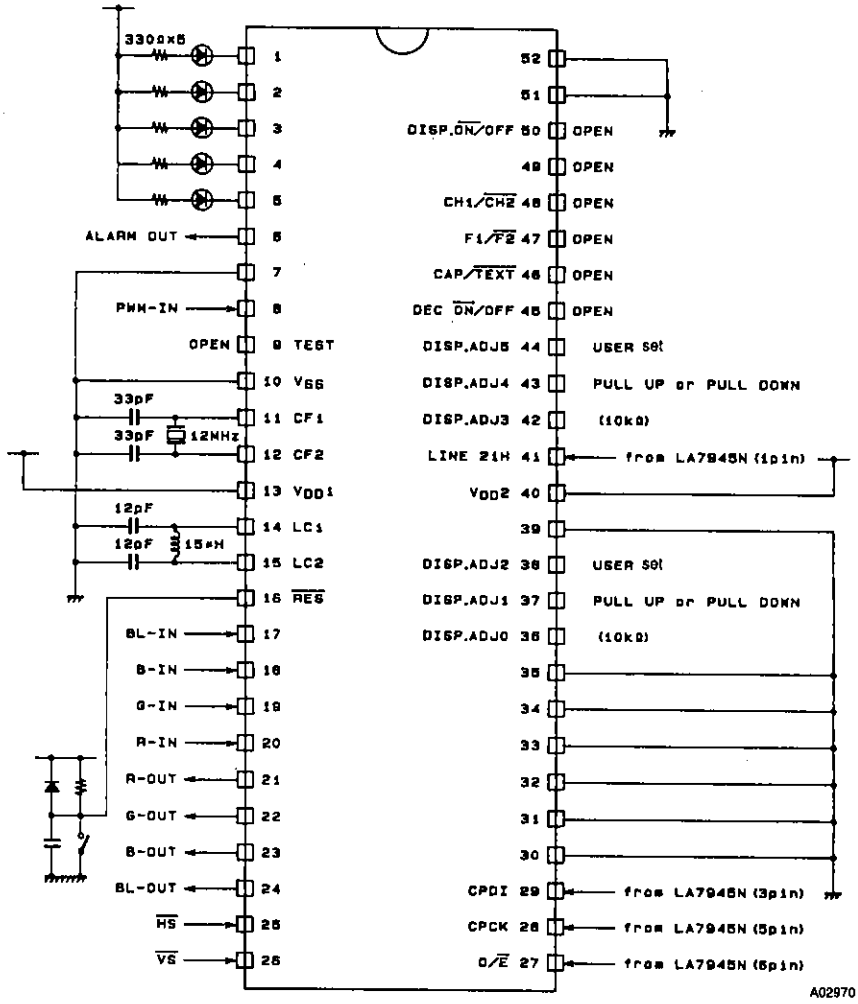


Figure 8. Serial (PWM) control interface

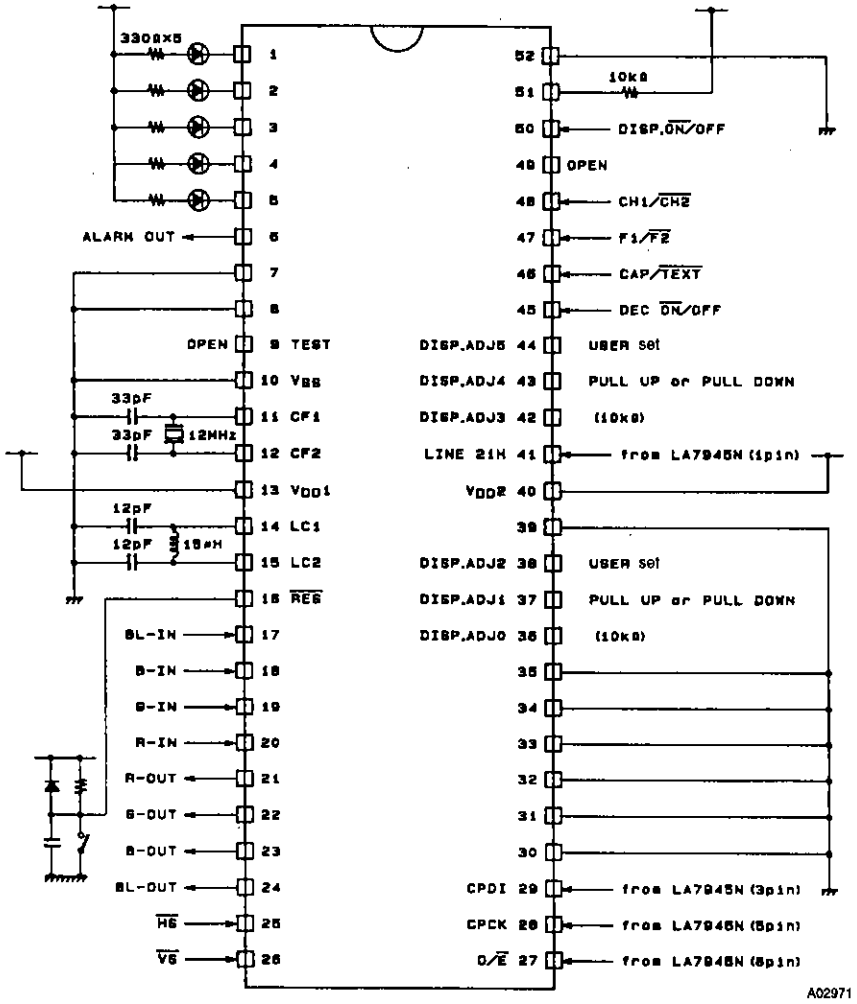


Figure 9. Parallel control selected

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