

SANYO

No.2362

LC7431,7431M,7432

CMOS IC
VHS VTR CHROMA SIGNAL
RECORDING/PLAYBACK PROCESSOR

The LC7431 is a VHS VTR chroma signal processor LSI that can be used in conjunction with the LA7315 to perform all the signal processing functions required for recording/playback. The LC7432 is an RF switch pulse input polarity-reversed version of the LC7431. The LC7431M is a miniflat package version of the LC7431.

Functions

- . Burst gate pulse generator
- . 4-phase shift circuit
- . PB side lock detector
- . ID phase select circuit (NTSC: Inversion, PAL: 90° phase shift)
- . 1/2H killer
- . REC AFC
- . 320(321) f_H VCO automatic adjust system

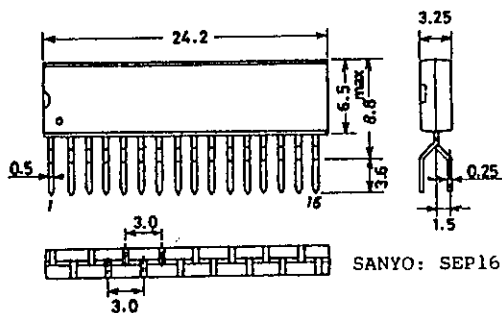
Features

- . Adjustment-free 320/321f_H VCO
- . On-chip REC/PB low-pass filter and its automatic adjust system
- . CCD delay clock pulse generator (2f_{sc})
- . Adjustment-free 3.58/4.43MHz VCO, PB output level (No adjustment required for other than REC chroma level)
- . NTSC/PAL/SECAM use
- . Minimum number of external parts required
- . Low power dissipation

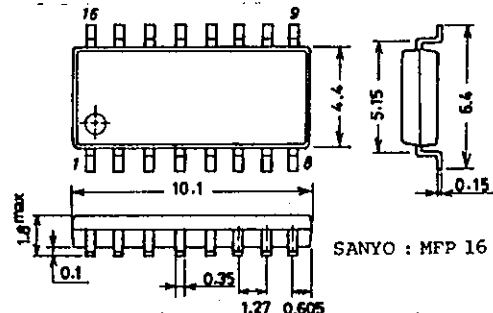
Absolute Maximum Ratings at Ta=25°C

			unit
Maximum Supply Voltage	V _{DD} max	-0.3 to +7.0	V
Input Voltage	V _I	-0.3 to V _{DD} +0.3	V
Output Voltage	V _O	-0.3 to V _{DD} +0.3	V
Allowable Power Dissipation	P _d max	150	mW
Operating Temperature	T _{opg}	-30 to +75	°C
Storage Temperature	T _{stg}	-55 to +125	°C

Case Outline 3020A-S16IC
(unit:mm) [LC7431,7432]



Case Outline 3035A-M16IC
(unit:mm) [LC7431M]



Specifications and information herein are subject to change without notice.

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(1097TA, TS No.2362-1/3)

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Allowable Operating Conditions at Ta=-30°C to +75°C, VSS=0V

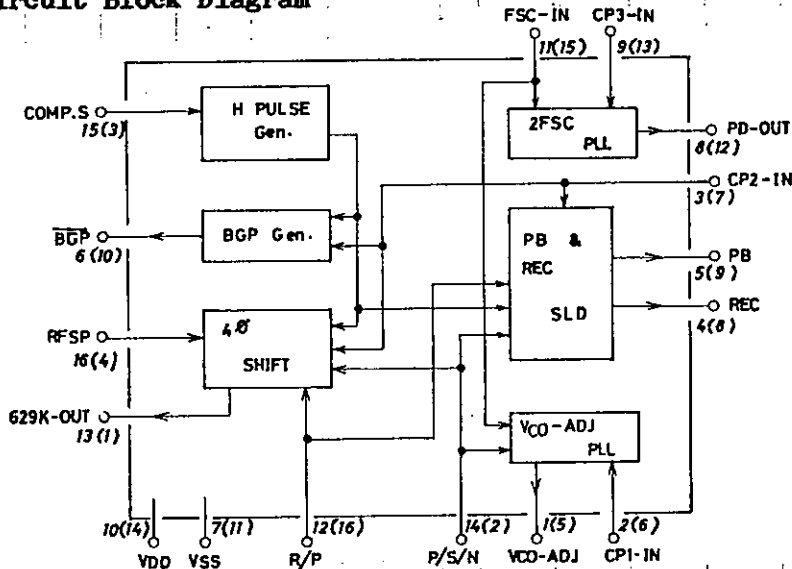
			min	typ	max	unit
Supply Voltage	V _{DD}	V _{DD}	4.5	5.0	5.6	V
"H"-Level Input Voltage	V _{IH} (1)	COMP.S	0.7V _{DD}		V _{DD}	V
"L"-Level Input Voltage	V _{IH} (2)	R/P, P/S/N	0.8V _{DD}		V _{DD}	V
	V _{IH} (3)	REC	0.6V _{DD}		V _{DD}	V
	V _{IH} (4)	RFSP	2		V _{DD}	V
	V _{IH} (1)	REC, COMP.S	V _{SS}	0.2V _{DD}	V _{DD}	V
"M"-Level Input Voltage	V _{IH} (2)	P/S/N	V _{SS}		0.5	V
	V _{IH} (3)	R/P	V _{SS}	0.2V _{DD}	V _{DD}	V
	V _{IH} (4)	RFSP	V _{SS}		0.5	V
	V _{IM}	P/S/N	1.5		2.6	V
Hysteresis Width Allowable	V _{HYS}	COMP.S		0.2V _{DD}		V
Operating Frequency	*F _{IN} (1)	CP3-IN	1		20	MHz
Input Amplitude	F _{IN} (2)	CP1-IN, CP2-IN, FSC-IN	1		7	MHz
	V _{IN} p-p	CP1-IN, CP2-IN, CP3-IN, FSC-IN	0.3		V _{DD}	Vp-p

* Capacitive coupling V_{IN}=0.3Vp-p

Electrical Characteristics at Ta=25°C, V_{DD}=4.5 to 5.6V

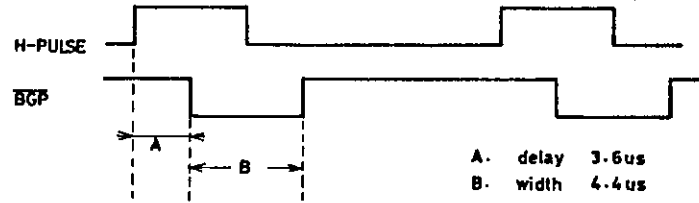
			min	typ	max	unit
"H"-Level Input Current	I _{IH} (1)	REC, R/P, P/S/N, COMP.S, RFSP: V _{IN} =V _{DD}			1.0	uA
	I _{IH} (2)	CP1-IN, CP2-IN, CP3-IN, FSC-IN: V _{IN} =V _{DD}		5.0		uA
"L"-Level Input Current	I _{IL} (1)	Same as I _{IH} (1), V _{IN} =V _{SS}	-1.0			uA
	I _{IL} (2)	Same as I _{IH} (2), V _{IN} =V _{SS}		-5.0		uA
"H"-Level Output Voltage	V _{OH} (1)	BGP, PD-out, 629K-out : I _{OH} =-0.5mA	V _{DD} -0.5			V
	V _{OH} (2)	VCO-ADJ: I _{OH} =-0.1mA	V _{DD} -0.65V	V _{DD} -0.5V	V _{DD} -0.35	V
	V _{OH} (3)	REC, PB: I _{OH} =-0.5mA	V _{DD} -0.25			V
"L"-Level Output Voltage	V _{OL} (1)	Same as V _{OH} (1), I _{OL} =0.5mA			0.5	V
	V _{OL} (2)	Same as V _{OH} (2), I _{OL} =0.1mA	0.35	0.5	0.65	V
	V _{OL} (3)	Same as V _{OH} (3), I _{OL} =0.5mA			0.25	V
Output OFF-State Leakage Current	I _{OFF}	VCO-ADJ, REC, PD-out, PB	-0.1		0.1	uA
Current Dissipation	I _{DD}	V _{DD} : F _{IN} (1)=7MHz, F _{IN} (2)=20MHz, V _{IN} =0.3Vp-p, V _{DD} =5.0V		2.5	7	mA

Equivalent Circuit Block Diagram



(): Pin No. of the LC7431M

Pin Description

Pin Name	Pin No.	I/O	Functions
V _{DD} V _{SS}	10(14) 7(11)		Power supply V _{DD} =4.5V to 5.6V V _{SS} =0V
P/S/N	14(2)	I	"H"-level=PAL, "M"-level=SECAM, "L"-level=NTSC.
CP1-IN	2(6)	I	The ref VCO-out signal of the LA7315 is applied. When locked, 5.369MHz is provided for NTSC and 5.320MHz for PAL, SECAM.
CP2-IN	3(7)	I	The 320f _h VCO-out signal of the LA7315 is applied. NTSC 320f _h , PAL, SECAM 321f _h
CP3-IN	9(13)	I	The 2fscVCO-out signal of the LA7315 is applied.
FSC-IN	11(15)	I	The VXO(Fsc) of the LA7315 is applied. Provides the reference clock for internal control.
COMP.S	15(3)	I	The composite sync signal is applied.
RFSP	16(4)	I	The channel select signal of the cylinder head is applied.
VCO-ADJ	1(5)	O	Output pin for 320/321f _h VCO adjust phase comparison signal. When the CP1-IN is locked, the output is brought to a high-impedance state.
BGP	6(10)	O	Gate pulse used to take out the burst signal synchronously with the H-PULSE signal.  A. delay 3.6us B. width 4.4us
629K-out	13(1)	O	The CP2-IN signal is divided by 8 and the signal being 90° phase shifted is output. In the PLAY mode, receives the ID pulse from the REC pin to shift the phase.
PD-out	8(12)	O	Configures the PLL with the 2fscVCO in the LA7315.
PB	5(9)	O	Connected to the PB-AFC pin of the LA7315. Prevents side lock of the 320/321f _h VCO in the P.B. mode.
REC	4(8)	I/O	Connected to the REC-AFC pin of the LA7315. Configures the PPL of the 320/321f _h VCO in the REC mode. The output is the AND of the CP2-IN signal divided by 320(321) and the H-PULSE signal. Used as the input pin for the ID pulse in the P.B. mode.

(): Pin No. of the LC7431M

The application circuit diagrams and circuit constants herein are included as an example and provide no guarantee for designing equipment to be mass-produced.
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