No. 1852

LC7410, 7411, 7415

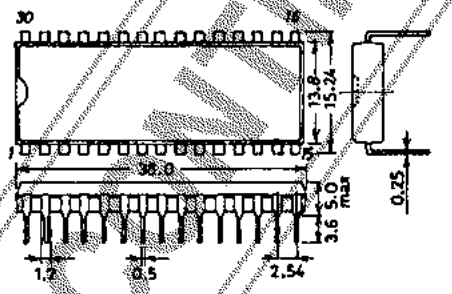
C MOS LSI
VTR (ß/VHS) SERVO CIRCUIT

The LC7410, 7411, 7415 are digital controller CMOS LSI's for VTR (ß/VHS) servo circuit use. Since any servo characteristics can be achieved by coding the on-chip mask ROM's and externally addressing the ROM's, they can be applied to any multifunctional VTR's. The LC7410, 7411, 7415 can be used in conjunction with interface IC LA7110 to form a servo system with a good cost performance.

Features

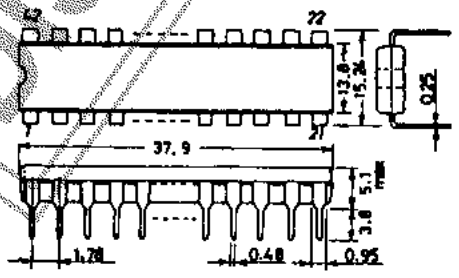
- Speed/phase control of drum unit
- Speed/phase control of capstan unit (For speed control, mask option permits 2FG application also.)
- Color subcarrier signal (f_{SC}) is programmable-divided to generate internal reference signal (REF30).
- Tape speed (recording time mode) detection (ßI/ßII/ßIII, SP/LP/EP)
- Control signal phasing capability during edit recording
- Mode (PB, REC, special PB, etc.) selection (max. 16 modes) is made by 4-bit binary data.
- A wide variety of stepwise search (1/2, 1, 2, 3, 4, 5, ----, 15max.)
- Destination (NTSC/PAL) is pin-selectable.
- The on-chip input amp acts to permit color subcarrier signal (V_{IN}≥0.35V_{P-P}) to be interfaced.
- Operating voltage (V_{DD}=4.5 to 5.5V)/operating current dissipation (I_{DD} typ.=3mA)
- Operating temperature (T_a=−30 to +70°C)
- Package: DIP30 (LC7410-XX), DIP42S (LC7411-XX), or QIP48 (LC7415-XX)

LC7410
Case Outline 3051
(unit: mm)



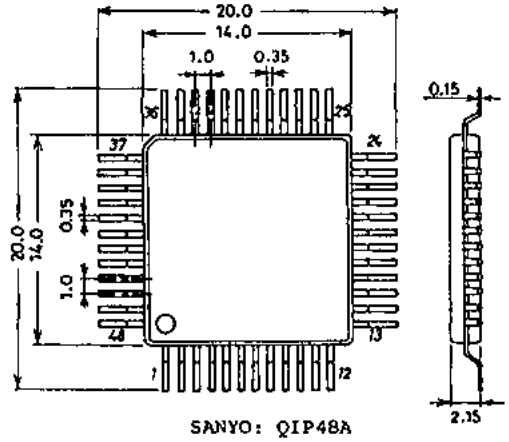
SANYO: DIP 30

LC7411
Case Outline 3025B-D42SIC
(unit: mm)



SANYO: DIP42S

LC7415
Case Outline 3052A-Q48AIC
(unit: mm)

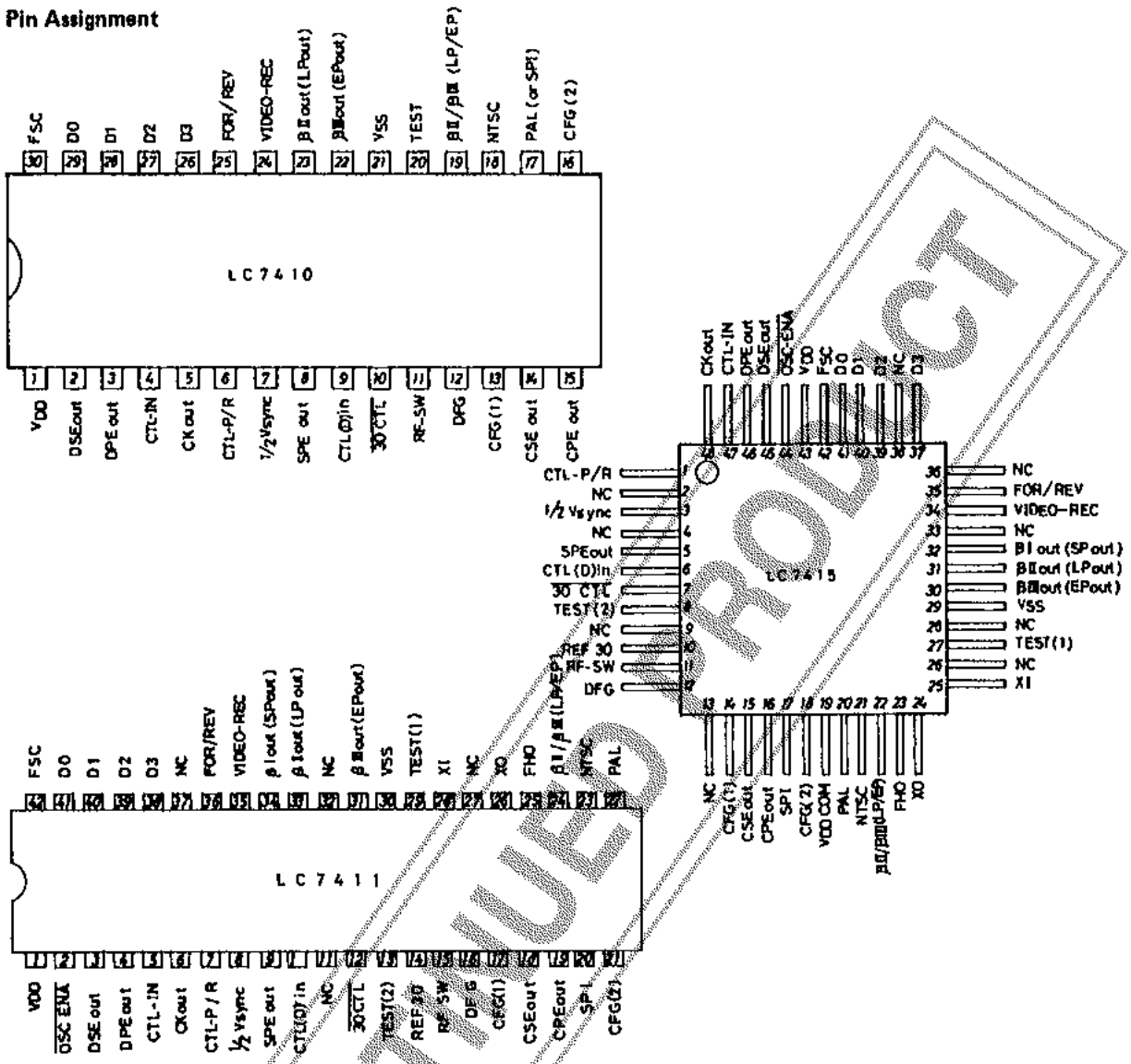


SANYO: QIP48A

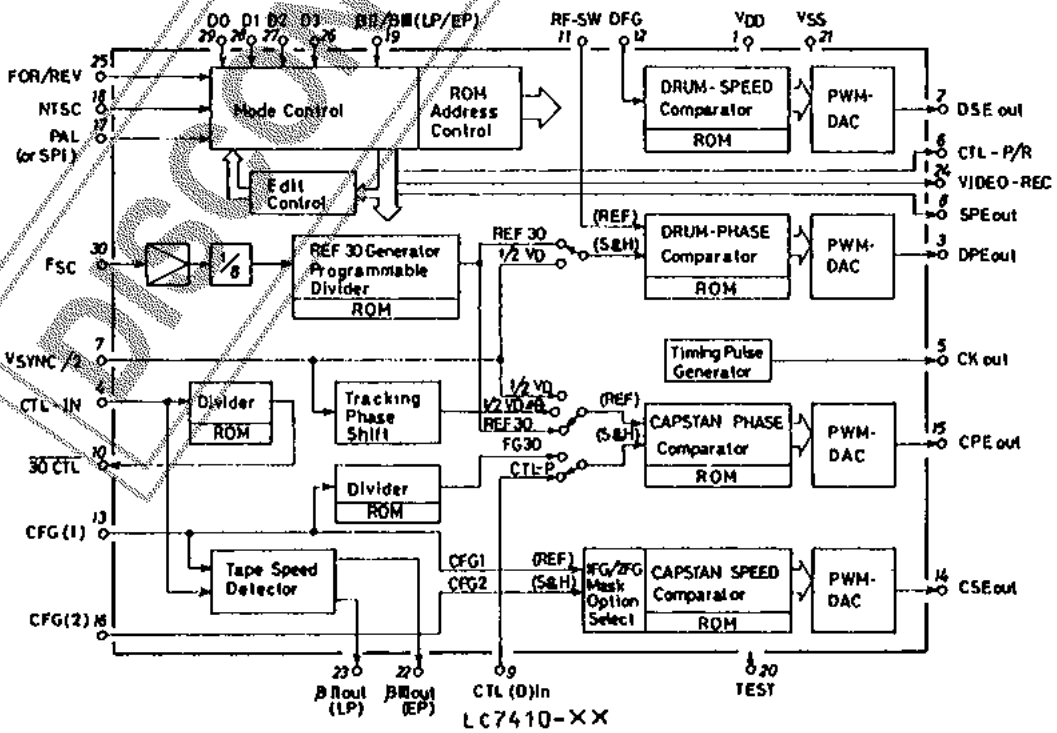
These specifications are subject to change without notice.

TOKYO SANYO ELECTRIC CO., LTD. SEMICONDUCTOR DIVISION
15-13, 6-CHOME, SOTOKANDA, CHIYODA-KU, TOKYO 101 JAPAN

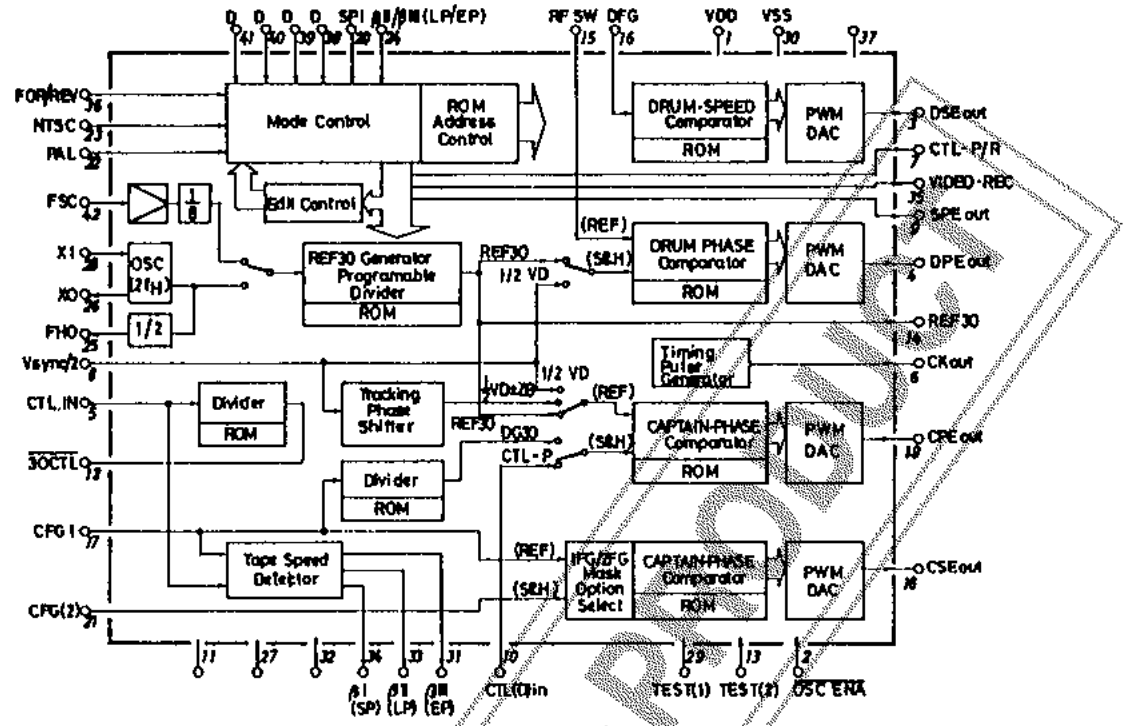
Pin Assignment



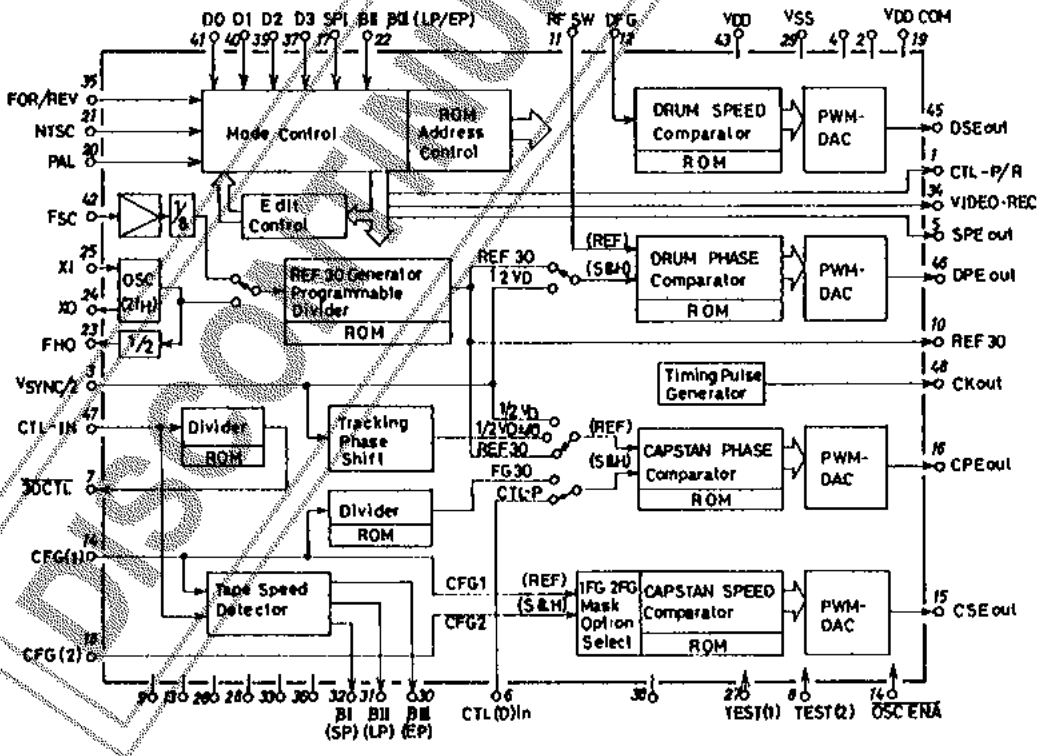
Internal Block Diagram



Internal Block Diagram

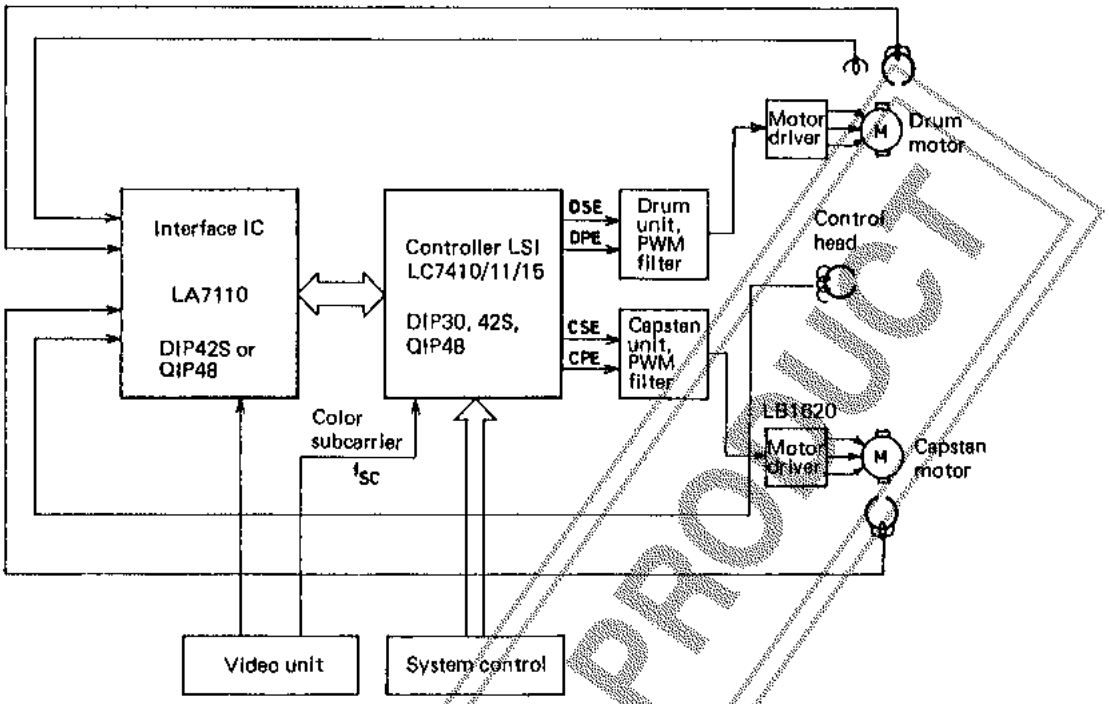


LC7411-XX

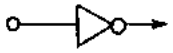
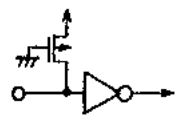
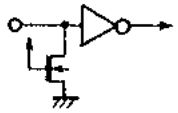


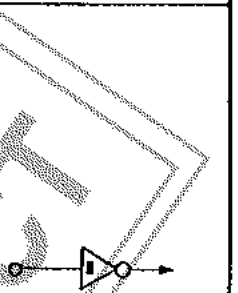
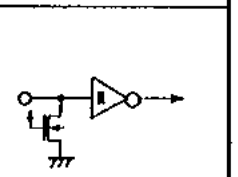
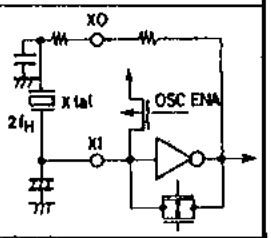
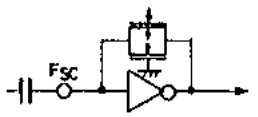
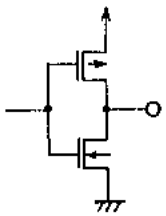
LC7415-XX

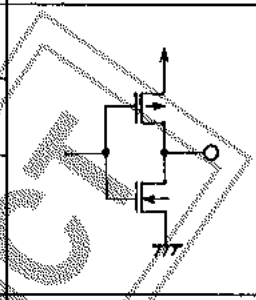
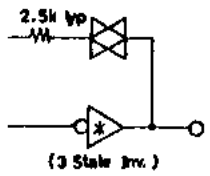
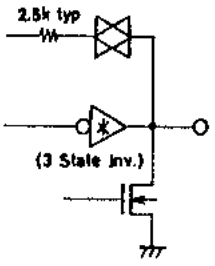
Application Block Diagram



Pin Description

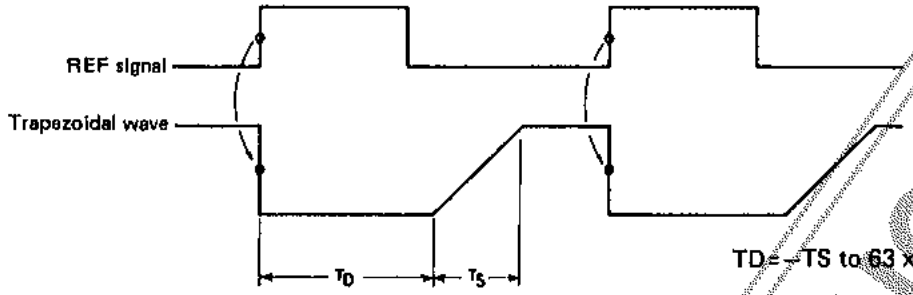
Pin Name	Pin No.			Functions	Input/Output Configuration
	LC7410	LC7411	LC7415		
V_{DD}	1	1	43	Supply Voltage V_{DD}=+4.5 to +5.5V V_{SS}=0V	
V_{SS}	21	30	29		
D0, D1, D2, D3	29, 28 27, 26	41, 40 39, 38	41, 40 39, 37	Mode selection (16 modes) is made by 4-bit binary data. Latch function must be provided externally.	
FOR/REV	25	36	35	Forward/reverse selection. "H" level=Forward, "L" level=Reverse.	
NTSC/PAL (LC7410), NTSC (LC7411, 7415)	18	23	21	Destination selection "H" level=NTSC (LC7410: "L" level=PAL)	
PAL (or SPI)	17	22	20	Destination selection. "H" level (LC7410 VHS: SPI)	
ßII/ßIII (LP/EP)	19	24	22	Tape speed (recording time) at REC mode is specified. ßII/ßIII (ß), LP/EP (VHS)	
OSC-ENA	—	2	44	In applications where on-chip $2f_H$ OSC circuit is used, this pin is set to "L" level.	
TEST (1)	20	29	27	Test pin	
TEST (2)	—	13	8	Test pin	
SPI	—	20	17	REC tape speed in VHS applications is specified. SP mode selection (VHS).	

Pin Name	Pin No.			Functions	Input/Output Configuration
	LC7410	LC7411	LC7415		
1/2 V sync	7	8	3	1/2 (30Hz) of vertical sync signal is applied as external reference signal at REC mode.	
RF-SW	11	15	11	Channel select signal of drum (cylinder) head is applied. Phase comparison, control in drum unit.	
DFG	12	16	12	FG signal (rotational speed detect signal) for drum unit is applied to perform speed control.	
CFG (1)	13	17	14	FG signal for capstan unit is applied. Speed control, phase control, tape speed detection.	
CFG (2)	16	21	18	2nd FG signal is applied when controlling capstan unit in 2FG application.	
CTL-in	4	5	47	Control signal is applied. CTL/n=30Hz=$\overline{30CTL}$ at n-fold high-speed search mode.	
CTL (D) In	9	10	6	Control signal after tracking delay processing is applied. Phase control in capstan unit.	
XI XO	–	28 26	25 24	OSC circuit is formed by connecting $2f_H$ (31.5kHz) crystal resonator externally. $2f_H$ OSC signal is 1/2 divided and delivered at FHO pin ($\overline{OSC\text{-}ENA}$="L").	
FSC	30	42	42	Color subcarrier signal to be used for internal system clock of LSI is applied through capacitive coupling. On-chip input amp acts to permit color subcarrier signal of 0.35Vp-p or greater to be applied.	
CTL-P/R	6	7	1	PB/REC mode control signal of control head is delivered. PB="H", REC="L".	
$\overline{30CTL}$	10	12	7	Control signal applied through CTL-IN pin is divided to deliver 30Hz signal at high-speed search mode.	
REF30	–	14	10	30Hz reference signal obtained by dividing FSC signal is delivered. REF30=FSCx1/8x1/Nx1/2=30Hz	
FHO	–	25	23	f_H signal obtained by 1/2 dividing $2f_H$ OSC signal is delivered. ($\overline{OSC\text{-}ENA}$="L")	
ßI (ß) SP (VHF)	–	34	32	REC time mode detect output. ßI="H", SP="H".	

Pin Name	Pin No. LC7410	Pin No. LC7411	Pin No. LC7415	Functions	Input/Output Configuration
ßII (ß) LP (VHS)	23	33	31	REC time mode detect output. ßII="H", EP="H"	
ßIII (ß) EP (VHS)	22	31	30	REC time mode detect output. ßIII="H", EP="H"	
VIDEO-REC	24	35	34	Video unit REC mode control output. Pin voltage changes on the positive transition of RF-SW signal after mode selection (D0 to D3).	
DPE out	3	4	46	Low-order 3 bits and high-order 5 to 8 bits of error output of drum unit phase control are delivered in the form of analog signal and PWM signal respectively. Signal of duty 50% is delivered at the time of mode selection, stop mode, other than speed slope.	
CPE out	15	19	16	Low-order 3 bits and high-order 5 to 8 bits of error output of capstan unit phase control are delivered in the form of analog signal and PWM signal respectively. Signal of duty 50% is delivered at the time of mode selection, stop mode, other than speed slope.	
DSE out	2	3	45	Low-order 3 bits and high-order 5 to 8 bits of error output of drum unit speed control are delivered in the form of analog signal and PWM signal respectively. At drum stop mode N-channel transistor is turned ON and this pin is set to "L" level.	
CSE out	14	18	15	Low-order 3 bits and high-order 4 to 8 bits of error output of capstan unit speed control are delivered in the form of analog signal and PWM signal respectively. At capstan stop mode N-channel transistor is turned ON and this pin is set to "L" level.	
SPE out	8	9	5	Control output to change tracking constant. Normal mode="L" 2 or 3-fold fast mode="H" 1/2 slow mode="Hi-Z"	
CK out	5	6	48	Superposed signal of 1/8FSC signal and 1/240FSC signal (NTSC) or 1/10FSC signal and 1/360FSC signal (PAL) is delivered.	3 State (L, Hi-Z, H) out

Items for ROM coding

(1) Trapezoidal wave for speed, phase control



TD = TS to 63 x TS

CAP (F): TS=2/SC, 4/SC, 8/SC, 16/SC x (7 to 11 bits)
Mode selection

Other than CAP (F): TS=4/SC, 8/SC, 16/SC x (8 to 11 bits)
To be separately selected for each unit by mask option
Mode selection

Trapezoidal Wave Slope Select Table

Number of Bits of Trapezoidal Wave Slope	Ts (ms) Clock of Trapezoidal Wave Slope			
	$1/2f_{SC}$	$1/4f_{SC}$	$1/8f_{SC}$	$1/16f_{SC}$
7 bits	0.076ms	0.143ms	0.286ms	0.572ms
8 bits	0.143ms	0.286ms	0.572ms	1.144ms
9 bits	0.286ms	0.572ms	1.144ms	2.288ms
10 bits	0.572ms	1.144ms	2.288ms	4.577ms
11 bits	1.144ms	2.288ms	4.577ms	9.154ms

NTSC: f_{SC}=3.58MHz

(2) Frequency division for REF30 signal generation (N=10 to 16,383)

- For color subcarrier (f_{SC})

$$f_{REF30} = f_{SC} \times 1/8 \times 1/N \times 1/2 \text{ (Hz)}$$

- For $2f_H$ OSC signal

$$f_{REF30} = 2f_H \times 1/N \times 1/2 \text{ (Hz)}$$

(3) Frequency division for FG30 signal generation (M=1 to 31)

$$f_{FG30} = f_{CFG}(1) \times 1/M \times 1/2 \text{ (Hz)}$$

Note: If a limitation is put on maximum operating frequency of CFG(1) signal, odd-numbered frequency division is available.

(4) Frequency division for CTL signal special PB preprocessing (L=1 to 15)

$$f_{30CTL} = f_{CTL} \times 1/L \text{ (Hz)}$$

(5) Control output for 16 modes (D0 to D3, selection by 4 bits)

- CTL-P/B "H", "L" coding
- VIDEO-REC "H", "L" coding
- SPE out "H", "L", "high Z"

PWM frequency of PWM-DAC

For low-order 3 bits, R-2R type DAC is used. Therefore, 8-fold PWM frequency is available with the accuracy for 3 bits left unaffected.

PWM Frequency

Mask Option	Clock	t_{LSB} (f_{SC}=3.58MHz)	Number of Bits of Trapezoidal Wave Slope (=Number of Bits of DAC)			
			11 bits	10 bits	9 bits	8 bits
I	$f_{SC}/8$	2.2us	1.7kHz	3.4kHz	6.8kHz	13.6kHz
II	$f_{SC}/4$	1.1us	3.4kHz	6.8kHz	13.6kHz	27.2kHz
III	$f_{SC}/2$	0.55us	6.8kHz	13.6kHz	27.2kHz	54.4kHz

Absolute Maximum Ratings/T_a=25°C

				unit
Maximum Supply Voltage	V_{DD} max		−0.3 to +6.0	V
Input Voltage	V_I		−0.3 to V_{DD}+0.3	V
Output Voltage	V_O		−0.3 to +V_{DD}+0.3	V
Allowable Power Dissipation	P_d max	$T_a \leq 70°C$	150	mW
Operating Temperature	T_{opg}		−30 to +70	°C
Storage Temperature	T_{stg}		−55 to +125	°C

Allowable Operating Conditions/T_a=−30 to +70°C, V_{SS}=0V

			min	typ	max	unit
Supply Voltage	V_{DD}		4.5		5.5	V
Input "H"-Level Voltage	$V_{IH(1)}$	D0 to D3, FOR/REV, 8II/III, PAL, $\overline{OSC\text{-}ENA}$, SPI, TEST (2)	0.7V_{DD}		V_{DD}	V
	$V_{IH(2)}$	CTL-IN, CTL(D) in, DFG, RF-SW, CFG(1), CFG(2), 1/2V sync	0.8V_{DD}		V_{DD}	V
	$V_{IH(3)}$	NTSC, TEST(1)	0.9V_{DD}		V_{DD}	V
Input "L"-Level Voltage	$V_{IL(1)}$	Pins for $V_{IH(1)}$	V_{SS}		0.3V_{DD}	V
	$V_{IL(2)}$	Pins for $V_{IH(2)}$	V_{SS}		0.2V_{DD}	V
	$V_{IL(3)}$	Pins for $V_{IH(3)}$	V_{SS}		0.1V_{DD}	V
Input Amplitude	$V_{INP\text{-}P}$	FSC: Sine wave capacitive coupling			0.35	$V_{P\text{-}P}$
Operating Frequency	$f_{IN(1)}$	FSC: Sine wave capacitive coupling V_{IN}=0.35$V_{p\text{-}p}$	1.0		5.0	MHz
	$f_{IN(2)}$	CFG(1), CFG(2), DFG: $t_{IWH} \geq 92us$	30		5400	Hz
	$f_{IN(3)}$	CTL-IN: $t_{IWH} \geq 50us$	5		1000	Hz
	$f_{IN(4)}$	RF-SW, CTL(D) in, 1/2V sync: $t_{IWH} \geq 1ms$	5		500	Hz
"H"-Level Pulse Width	t_{IWH1}	CTL-IN	50			us
	t_{IWH2}	CFG(1), CFG(2), DFG	92			us
	t_{IWH3}	RF-SW, CTL(D) in, 1/2V sync	1000			us

Electrical Characteristics/T_a=25±2°C, V_{DD}=5V±10%, V_{SS}=0V			min	typ	max	unit
Input "H"-Level Current	$I_{IH(1)}$	D0 to D3, F/R, ßII/III, NTSC, PAL, DFG, RF-SW, CFG(1), CFG(2), 1/2V sync: $V_{IN}=V_{DD}$			1.0	uA
	$I_{IH(2)}$	CTL-IN, CTL(D) in, SPI: $V_{IN}=V_{DD}$	2.5		20	uA
	$I_{IH(3)}$	TEST(1), TEST(2): $V_{IN}=V_{DD}$	6.0		50	uA
Input "L"-Level Current	$I_{IL(1)}$	Pins for $I_{IH(1)}$: $V_{IN}=V_{SS}$	−1.0			uA
	$I_{IL(2)}$	OSC-ENA, XI (at $\overline{\text{OSC-ENA}}$="L") : $V_{IN}=V_{SS}$	−20		−2.5	uA
Input "H"-Level Floating Voltage	V_{IFH}	$\overline{\text{OSC-ENA}}$, ßII/III, XI (at $\overline{\text{OSC-ENA}}$="H"): Input pin open	V_{IH}+0.5		V_{DD}	V
Input "L"-Level Floating Voltage	V_{IFL}	CTL-IN, CTL(D) in, SPI, TEST(2) : Input pin open	V_{SS}		V_{IL}−0.5	V
Output "H"-Level Voltage	$V_{OH(1)}$	CTL-P/R, SPEout, $\overline{\text{30CTL}}$, REF30, FHO, ßI, ßII, ßIII, VIDEO-REC: I_{OH}=−0.3mA	V_{DD}−0.6			V
	$V_{OH(2)}$	CKout, PWM output driver of DSE, DPE, CSE, CPE pins: I_{OH}=−0.3mA	V_{DD}−0.3			V
Output "L"-Level Voltage	$V_{OL(1)}$	Pins for $V_{OH(1)}$, OD-TR of DSE, CSE : I_{OL}=0.3mA			0.6	V
	$V_{OL(2)}$	Pins for $V_{OH(2)}$: I_{OL}=0.3mA			0.3	V
R-2R DA Characteristics						
Bit Error	ΔV_{LSB}	DSE, DPE, CSE, CPE	−1/2LSB	1LSB (2^{-3}, V_{DD})	1LSB+1/2LSB	V
Output Impedance	Z_{OUT}	DSE, DPE, CSE, CPE: R_L=100kohm	2.1	3.0	3.9	kΩ
R-2R Ladder Composite Resistance	Ro(LAD)	DSE, DPE, CSE, CPE		2.5		kΩ
DA Output Analog Switch ON-State Resistance	Ron(SW)	DSE, DPE, CSE, CPE: R_L=100kohm		500		Ω
Output OFF-State Leakage Current	$I_{OFF(1)}$	DSE, DPE, CSE, CPE	−2.0		2.0	uA
	$I_{OFF(2)}$	CKout, SPEout	−1.0		1.0	uA
Dynamic Current Dissipation	I_{DD}	V_{DD}: fin=4.43MHz, Vinp-p=0.35Vp-p			5.0	mA
OSC Characteristics						
OSC Frequency	f_{OSC}	XI, XO		31.5		kHz