Ordering number : EN※4968

CMOS LSI

SANYO

No. ※4968

LC72P321

Single-Chip Microcontroller + PLL with On-Chip One-Time PROM

Preliminary

Overview

The LC72P321 is a one-time programmable PROM version of the LC72321/322/323 single-chip microcontroller plus PLL products. The LC72P321 features the same functions, pin assignment and package as the mask ROM LC72321/322/323 and provides an 8K-byte* (4K × 16 bits) PROM on chip. The LC72P321 is optimal for the first phases of end product production when production is ramping up and for reducing the switchover time when specifications change.

Features

- PROM data option switching
  The LC72321/322/323 optional functions can be specified with PROM data. This allows trial evaluations with the printed circuit board used in the mass-produced end product.
- 8K-byte* (4K × 16 bits) on-chip PROM
  This is a one-time programmable 8K-byte* (4K × 16 bits) PROM.
- Pin assignment and package identical to those in the mask ROM version (pin compatibility)

  Note * Keep in mind that the LC72323 has only a 6K byte (3K × 16 bits) ROM size when using the LC72P321.

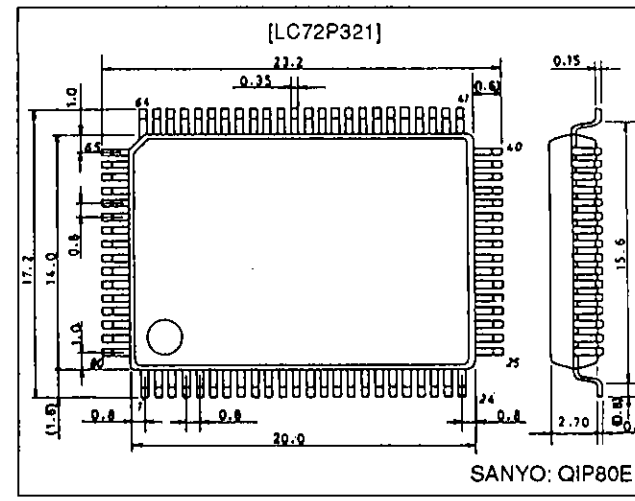
Concerning Sanyo's ROM writing service

Sanyo provides a for-fee PROM writing service for Sanyo on-chip one-time PROM type microcontrollers. This service includes writing the PROM, package printing, screening and data readout confirmation. Contact your Sanyo sales representative for details.

Package Dimensions

unit: mm

3174-QIP80E



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		−0.3 to +6.5	V
Input voltage	$V_{IN}1$	$\overline{HOLD}$, $\overline{INT}$, $\overline{RES}$, AD1, $\overline{SNS}$, G port	−0.3 to +13	V
	$V_{IN}2$	Inputs other than $V_{IN}1$	−0.3 to V_{DD} + 0.3	V
Output voltage	$V_{OUT}1$	H port	−0.3 to +15	V
	$V_{OUT}2$	Outputs other than $V_{OUT}1$	−0.3 to V_{DD} + 0.3	V
Output current	$I_{OUT}1$	Each pin in the D and H ports	0 to 5	mA
	$I_{OUT}2$	Each pin in the E and F ports	0 to 3	mA
	$I_{OUT}3$	Each pin in the B and C ports	0 to 1	mA
	$I_{OUT}4$	S1 to S28, each pin in the I port	0 to 1	mA
Allowable power dissipation	Pd max	Topr = −30 to +70°C	400	mW
Operating temperature	Topr		−30 to +70	°C
Storage temperature	Tstg		−45 to +125	°C

Note: This IC has an increased susceptibility to destruction from static discharges and requires special care in handling.

SANYO Electric Co., Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

Allowable Operating Ranges at Ta = –30 to +70°C, V_{DD} = 3.5 to 5.5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	$V_{DD}1$	CPU and PLL operating	4.5		5.5	V
	$V_{DD}2$	CPU operating	4.0		5.5	V
	$V_{DD}3$	Memory retention	1.3		5.5	V
Input high level voltage	$V_{IH}1$	G port	0.7 V_{DD}		8.0	V
	$V_{IH}2$	$\overline{RES}$, $\overline{INT}$, $\overline{HOLD}$	0.8 V_{DD}		8.0	V
	$V_{IH}3$	$\overline{SNS}$	2.5		8.0	V
	$V_{IH}4$	A port	0.6 V_{DD}		V_{DD}	V
	$V_{IH}5$	E and F ports	0.7 V_{DD}		V_{DD}	V
	$V_{IH}6$	LCTR (period measurement), $V_{DD}1$	0.8 V_{DD}		V_{DD}	V
Input low level voltage	$V_{IL}1$	G port	0		0.3 V_{DD}	V
	$V_{IL}2$	$\overline{RES}$, $\overline{INT}$	0		0.2 V_{DD}	V
	$V_{IL}3$	$\overline{SNS}$	0		1.3	V
	$V_{IL}4$	A port	0		0.2 V_{DD}	V
	$V_{IL}5$	E and F ports	0		0.3 V_{DD}	V
	$V_{IL}6$	LCTR (period measurement), $V_{DD}1$	0		0.2 V_{DD}	V
	$V_{IL}7$	$\overline{HOLD}$	0		0.4 V_{DD}	V
Input frequency	$f_{IN}1$	XIN	4.0	4.5	5.0	MHz
	$f_{IN}2$	FMIN, $V_{IN}2$, $V_{DD}1$	10		130	MHz
	$f_{IN}3$	FMIN, $V_{IN}3$, $V_{DD}1$	10		150	MHz
	$f_{IN}4$	AMIN (L), $V_{IN}4$, $V_{DD}1$	0.5		10	MHz
	$f_{IN}5$	AMIN (H), $V_{IN}5$, $V_{DD}1$	2.0		40	MHz
	$f_{IN}6$	HCTR, $V_{IN}6$, $V_{DD}1$	0.4		12	MHz
	$f_{IN}7$	LCTR (frequency), $V_{IN}7$, $V_{DD}1$	100		500	kHz
	$f_{IN}8$	LCTR (period), $V_{IH}6$, $V_{IL}6$, $V_{DD}1$	1		20×10^3	Hz
Input amplitude	$V_{IN}1$	XIN	0.50		1.5	Vrms
	$V_{IN}2$	FMIN	0.10		1.5	Vrms
	$V_{IN}4$	FMIN	0.15		1.5	Vrms
	$V_{IN}4$, $V_{IN}5$	AMIN	0.10		1.5	Vrms
	$V_{IN}6$, $V_{IN}7$	LCTR, HCTR	0.10		1.5	Vrms
Input voltage range	$V_{IN}8$	ADI	0		V_{DD}	V

Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Conditions	min	typ	max	Unit
Hysteresis	V_H	LCTR (period), $\overline{RES}$, $\overline{INT}$	0.1 V_{DD}			V
Rejected pulse width	P_{REJ}	$\overline{SNS}$			50	µs
Power down detection voltage	V_{DET}		3.0	3.5	4.0	V
Input high level current	$I_{IH}1$	$\overline{INT}$, $\overline{HOLD}$, $\overline{RES}$, ADI, $\overline{SNS}$, G port: V_I = 5.5 V			3.0	µA
	$I_{IH}2$	A, E and F ports, with the E and F port outputs off, A port without RDP: $V_I = V_{DD}$			3.0	µA
	$I_{IH}3$	XIN: $V_I = V_{DD}$ = 5.0 V	2.0	5.0	15	µA
	$I_{IH}4$	FMIN, AMIN, LCTR, HCTR: $V_I = V_{DD}$ = 5.0 V	4.0	10	30	µA
	$I_{IH}5$	A port with PDR: $V_I = V_{DD}$ = 5.0 V		50		µA
Input low level current	$I_{IL}1$	$\overline{INT}$, $\overline{HOLD}$, $\overline{RES}$, ADI, $\overline{SNS}$, G port: $V_I = V_{SS}$			3.0	µA
	$I_{IL}2$	A, E and F ports, with the E and F port outputs off, A port without PDR: $V_I = V_{SS}$			3.0	µA
	$I_{IL}3$	XIN: $V_{IN} = V_{SS}$	2.0	5.0	15	µA
	$I_{IL}4$	FMIN, AMIN, LCTR, HCTR: $V_I = V_{SS}$	4.0	10	30	µA
Input floating voltage	V_{IF}	A port with RDP			0.05 V_{DD}	V
Pull-down resistor	R_{PD}	A port with RDP, V_{DD} = 5.0 V	75	100	200	kΩ
Output high level off leakage current	$I_{OFFH}1$	EO1, EO2: $V_O = V_{DD}$		0.01	10	nA
	$I_{OFFH}2$	B, C, D, E, F and I ports: $V_O = V_{DD}$			3.0	µA
	$I_{OFFH}3$	H port: V_O = 13 V			5.0	µA
Output low level off leakage current	$I_{OFFL}1$	EO1, EO2: $V_O = V_{SS}$		0.01	10	nA
	$I_{OFFL}2$	B, C, D, E, F and I ports: $V_O = V_{SS}$			3.0	µA

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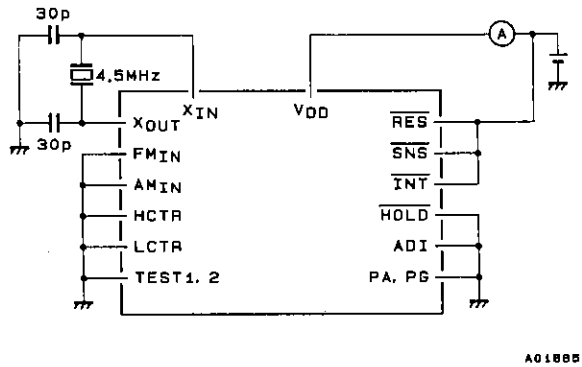
Parameter	Symbol	Conditions	min	typ	max	Unit
Output high level voltage	$V_{OH}1$	B and C ports: I_O = 1 mA	V_{DD} – 2.0	V_{DD} – 1.0	V_{DD} – 0.5	V
	$V_{OH}2$	E and F ports: I_O = 1 mA	V_{DD} – 1.0			V
	$V_{OH}3$	EO1, EO2: I_O = 500 µA	V_{DD} – 1.0			V
	$V_{OH}4$	XOUT: I_O = 200 µA	V_{DD} – 1.0			V
	$V_{OH}5$	S1 to S28, I port: I_O = –0.1 mA	V_{DD} – 1.0			V
	$V_{OH}6$	D port: I_O = 5 mA	V_{DD} – 1.0			V
	$V_{OH}7$	COM1, COM2: I_O = 25 µA	V_{DD} – 0.75	V_{DD} – 0.5	V_{DD} – 0.3	V
Output low level voltage	$V_{OL}1$	B and C ports: I_O = 50 µA	0.5	1.0	2.0	V
	$V_{OL}2$	E and F ports: I_O = 1 mA			1.0	V
	$V_{OL}3$	EO1, EO2: I_O = 500 µA			1.0	V
	$V_{OL}4$	XOUT: I_O = 200 µA			1.0	V
	$V_{OL}5$	S1 to S28, I port: I_O = 0.1 mA			1.0	V
	$V_{OL}6$	D port: I_O = 5 mA			1.0	V
	$V_{OL}7$	COM1, COM2: I_O = 25 µA	0.3	0.5	0.75	V
	$V_{OL}8$	H port: I_O = 5 mA	(150 Ω) 0.75		(400 Ω) 2.0	V
Output middle level voltage	V_M1	COM1, COM2: V_{DD} = 5.0 V, I_O = 20 µA	2.0	2.5	3.0	V
A/D conversion error		ADI: $V_{DD}1$	–1/2		+1/2	LSB
Supply current	$I_{DD}1$	$V_{DD}1$, $f_{IN}2$: 130 MHz		15	20	mA
	$I_{DD}2$	V_{DD} = 5.0 V, PLL stopped, CT = 2.67 µs (hold mode, Figure 1)		2.7		mA
	$I_{DD}3$	V_{DD} = 5.0 V, PLL stopped, CT = 13.33 µs (hold mode, Figure 1)		1.7		mA
	$I_{DD}4$	V_{DD} = 5.0 V, PLL stopped, CT = 40.00 µs (hold mode, Figure 1)		1.5		mA
	$I_{DD}5$	V_{DD} = 5.5 V, PLL stopped, Ta = 25°C (backup mode, Figure 2)			5	µA
		V_{DD} = 2.5 V, PLL stopped, Ta = 25°C (backup mode, Figure 2)			1	µA

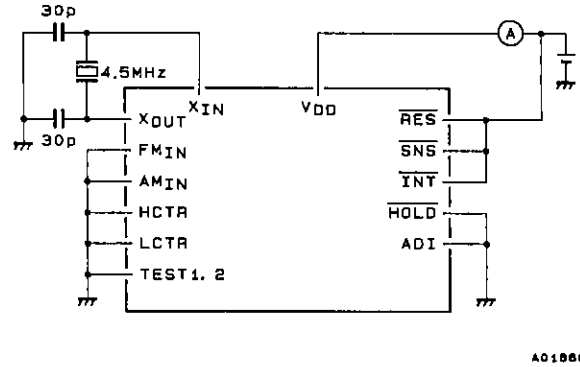
Test Circuit

Unit (capacitance: F)



Note: PB to PF, PH and PI are all open. However, PE and PF must be output selected.

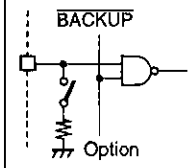
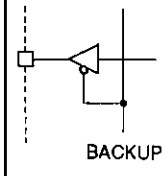
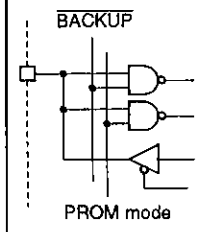
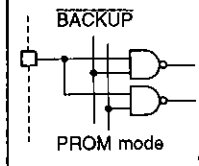
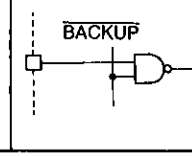
Figure 1 $I_{DD}2$ to 4 in Hold Mode



Note: PA to PI, S1 to S24, COM1 and COM2 are all open.

Figure 2 $I_{DD}5$ in Backup Mode

Pin Functions

Pin No.	Symbol	Function	I/O	I/O circuit	PROM mode function
35 34 33 32	PA0 PA1 PA2 PA3	Low threshold type input-only ports These pins can be used for key data acquisition. Pull-down resistors can be specified as an option. This specification is in 4-pin units and cannot be made for individual pins. Input is disabled in backup mode.	Input		
30 29 28 27 26 25 24 23	PB0 PB1 PB2 PB3 PC0 PC1 PC2 PC3	Output-only ports Since the output transistor impedance is due to an unbalanced type CMOS circuit these pins can be used effectively for key scan timing. These pins go to the high-impedance output state in backup mode. These pins go to the low level on a reset ($\overline{RES}$ = low).	Output		
22 21 20 19	PD0 PD1 PD2 PD3	Output-only ports These are normal CMOS outputs. These pins go to the high-impedance output state in backup mode. These pins go to the low level on a reset ($\overline{RES}$ = low).			
18 17 16 15	PE0*1 PE1/$\overline{SCK}$ PE2/SO PE3/SI	I/O ports These ports are switched between input and output mode as follows. The execution of an input instruction (IN, TPT or TPF) locks the corresponding port in input mode and an output instruction (OUT, SPB or RPB) locks the port in output mode. These pins go to input mode on a reset ($\overline{RES}$ = low). In backup mode, these pins go to input mode with input disabled.	I/O		Data I/O PE0: D0 PE1: D1 PE2: D2 PE3: D3 PF0: D4 PF1: D5 PF2: D6 PF3: D7
14 13 12 11	PF0 PF1 PF2 PF3	I/O ports These ports are switched between input and output by the FPC instruction. These ports can be set to input or output in single-pin units. These pins go to input mode on a reset ($\overline{RES}$ = low). In backup mode, these pins go to input mode with input disabled.			
6 5	PG0 PG1	Input-only ports Input is disabled in backup mode.	Input		PROM control signal inputs PG0: $\overline{CE}$ PG1: $\overline{OE}$
4 3	PG2 PG3				

Note: 1. $\overline{SCK}$, SO and SI can only be used when the LC72321 is used.

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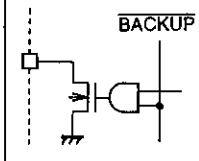
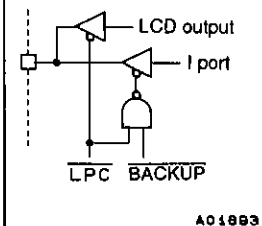
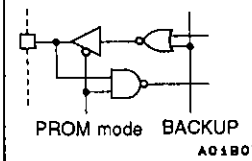
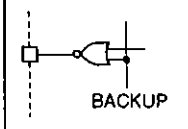
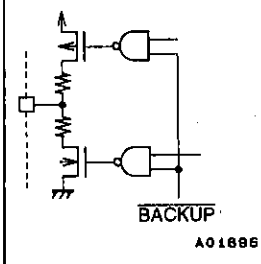
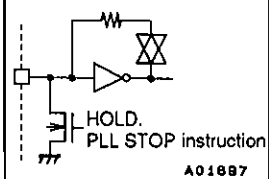
Pin No.	Symbol	Function	I/O	I/O circuit	PROM mode function
10 9 8 7	PH0 PH1/BEEP*2 PH2/DAC1*3 PH3/DAC2	Output-only ports Since these ports are high breakdown voltage open drain n-channel transistor outputs, they can be used effectively for band power supply switching. Note that PH2 and PH3 are also used as the DAC1 and DAC2 outputs. These outputs go to the high-impedance state on a reset ($\overline{RES}$ = low) and in backup mode.	Output		
39 38 37 36	PI0/S25 PI1/S26 PI2/S27 PI3/S28	Output-only ports Although these ports are CMOS outputs they can be switched to use as LCD drivers. The SS and RS instructions are used to switch the pin functions. These pins cannot be switched in single-pin units. These pins are selected as LCD drivers when $\overline{RES}$ is low and when power is first applied and output an LCD off signal at that time. These pins are held at the low level in backup mode. Note that when these pins are used as general-purpose ports under option specification, they output the content of IPORT when LPC is 1 and the content of the general-purpose output port latch when LPC is 0.	Output		
63 to 50	S1 to S14	LCD driver segment outputs The frame frequency is 100 Hz. The drive technique is 1/2 duty - 1/2 bias. These pins output an LCD off signal when $\overline{RES}$ is low and when power is first applied. These pins are held at the low level in backup mode. These ports can be used a general-purpose output ports under option specification.	I/O		Address inputs S1: A0 to S14: A13
49 to 40	S15 to S24		Output		
65 64	COM1 COM2	LCD driver common outputs The drive technique is 1/2 duty - 1/2 bias. These pins output the same signals when $\overline{RES}$ is low and when power is first applied as they do in normal operation. These pins are held at the low level in backup mode.	Output		
74	FMIN	FM VCO (local oscillator) input Input must be applied using capacitor coupling. Input frequency range: 10 to 130 MHz	Input		
75	AMIN	AM VCO (local oscillator) input Input must be applied using capacitor coupling. The bandwidth accepted by this pin can be selected by the PLL instruction CW1 bit as follows. High (2 to 40 MHz) → SW Low (0.5 to 10 MHz → LW, MW			

Note: 2. The BEEP pin can only be used when the LC72321 is used.
3. DAC1 and DAC2 cannot be used in the LC72323.

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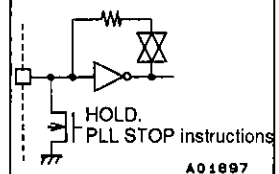
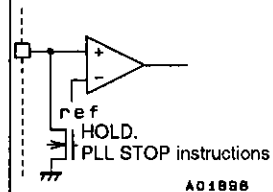
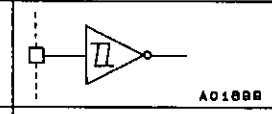
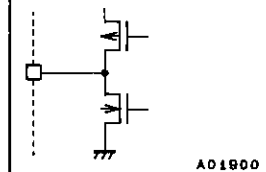
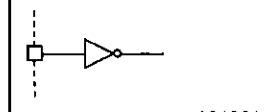
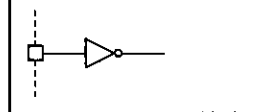
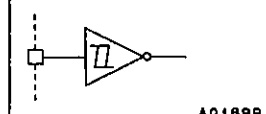
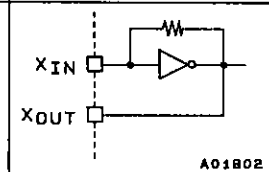
Pin No.	Symbol	Function	I/O	I/O circuit	PROM mode function
70	HCTR	Universal counter input Input must be applied using capacitor coupling. Input frequency range: 0.4 to 12 MHz This counter is effective for FM IF and AM IF counting.	Input		
71	LCTR	Universal counter input Input must be applied using capacitor coupling for inputs in the 100 to 150 kHz range. Capacitor coupling is not required for inputs in the 1 to 20 Hz range. This counter can be used for AM IF counting.			
69	ADI	A/D converter input A 6-bit successive-approximation conversion requires 1.28 ms. Full scale (the voltage for which the result is 3FH) is 63/96 of V_{DD}.	Input		
66	$\overline{INT}$	Interrupt request input An interrupt occurs when the INTEN flag is set (by the SS instruction) and a falling edge signal is applied.	Input		
77 78	EO1 EO2	Reference frequency and programmable divider output phase comparator error outputs These pin circuits include a charge pump. EO1 and EO2 are identical.	Output		
72	$\overline{SNS}$	Input used to determine whether a power failure has occurred in backup mode This pin can also be used as a normal input port.	Input		
67	$\overline{HOLD}$	Input that sets the LC72P321 to hold mode The LC72P321 goes to hold mode when the HOLDEN flag is set (with an SS instruction) and $\overline{HOLD}$ is set to low. A high breakdown voltage circuit is used here so that this pin can be used in conjunction with a normal power switch.	Input		
68	$\overline{RES}$	System reset input A low level that lasts at least 75 ms must be provided to assure a power-up reset. The reset starts after at least 6 master clock cycles have been input.	Input		
1 80	XIN XOUT	Crystal oscillator connections (4.5 MHz) A feedback resistor is built in.	Input Output		
79 2	TEST1 TEST2	LSI test pins. These pins must be connected to V_{SS} in normal operation.			
31, 73	V_{DD}	Power supply + connections. Both pins must be connected to the power supply.			Write power supply V_{PP}
76	V_{SS}	Power supply – connection			

Options

No.	Description	Selections
1	WDT (watchdog timer) inclusion selection	WDT included
		No WDT
2	Port A pull-down resistor inclusion selection	Pull-down resistors included
		No pull-down resistors
3	Cycle time selection	2.67 µs
		13.33 µs
		40.00 µs
4	LCD port/general purpose port selection	LCD ports
		General purpose output ports

Usage Notes

The LC72P321 is provided for early production of end products based on the Sanyo LC72321/322/323 microcontrollers. Keep the following points in mind when using this product.

1. Differences between the LC72P321 and the LC72321/322/323

Parameter		LC72P321	LC72321/322/323
Operating temperature (Topg)		–30 to +70 °C	–40 to +85°C
Operation immediately following power-on		After the 75 ms power on reset period, the LSI internal option settings are set up during a period of about 1 ms. After that operation completes, program execution starts with the program counter set to location 0.	After the 75 ms power on reset period, program execution starts with the program counter set to location 0.
Input type of the A port immediately following power on*		No pull-down resistors	Pull-down resistors are included or not according to the option specifications.
Output type of the S1 to S28 outputs immediately following power-on*		LCD ports	These pins function as either LCD ports or general-purpose output ports according to the option specifications.
Power-down detection voltage (V_{DET})		Minimum: 3.0 V Typical 3.5 V Maximum: 4.0 V	Minimum: 2.7 V Typical: 3.0 V Maximum: 3.3 V
Current drain	$I_{DD}2$	Conditions: V_{DD} = 5.0 V, PLL stopped CT = 2.67 µs (HOLD mode, figure 1) Typical: 2.7 mA	Conditions: $V_{DD}2$, PLL stopped CT = 2.67 µs (HOLD mode, Figure 1) Typical: 1.5 mA
	$I_{DD}3$	Conditions: V_{DD} = 5.0 V, PLL stopped CT = 13.33 µs (HOLD mode, figure 1) Typical: 1.7 mA	Conditions: $V_{DD}2$, PLL stopped CT = 13.33 µs (HOLD mode, Figure 1) Typical: 1.0 mA
	$I_{DD}4$	Conditions: V_{DD} = 5.0 V, PLL stopped CT = 40.00 µs (HOLD mode, figure 1) Typical: 1.5 mA	Conditions: $V_{DD}2$, PLL stopped CT = 40.00 µs (HOLD mode, Figure 1) Typical: 0.7 mA
The TEST1 and TEST2 pins		These are LSI test pins and must be connected to V_{SS}.	These are LSI test pins and must be either left open or connected to V_{SS}.

Note: This refers to the option setup time of about 1 ms that occurs following the period of about 75 ms from power application.

2. PLA and options

The LC72P321 uses address 2000H to 201FH in the same address space as program memory for the PLA pattern and addresses 2020H to 2033H for specifying the options. This option specification allows the LC72P321 to implement the same option setup as the target LC72321/322/323 product.

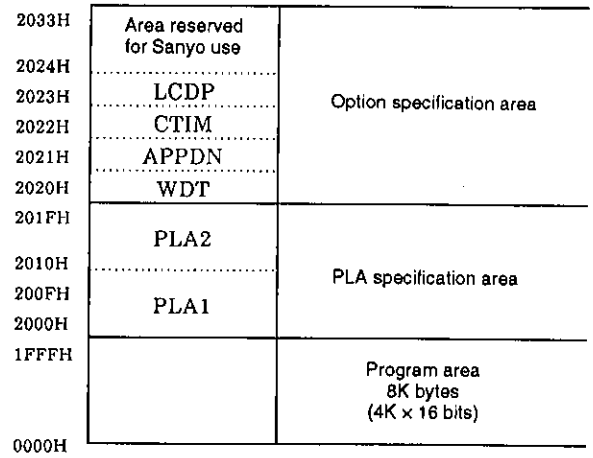
- LC72P321 option types

Symbol	Option Type	Selections
WDT	WDT (watchdog timer) inclusion selection	WDT included
		No WDT
APPDN	A port pull-down resistor inclusion selection	Pull-down resistors included
		No pull-down resistors
CTIM	Cycle time selection	2.67 µs
		13.33 µs
		40.00 µs
LCDP	LCD port/general purpose port selection	LCD ports
		General purpose output ports

Note that these options are not set up until the 1 ms option setup period, which follows 75 ms after power is first applied, has passed.

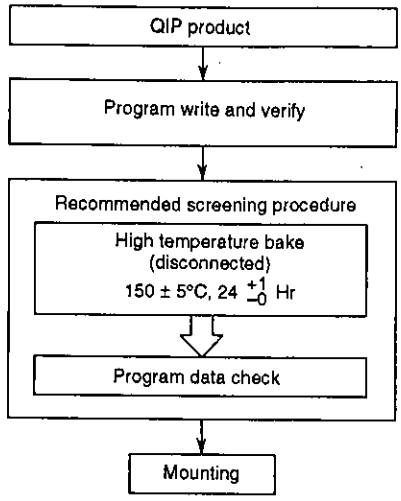
3. Mass production product printed circuit board
When using the LC72P321 with the mass production product printed circuit board used with the LC72321/322/323 end product, always connect both the TEST1 and TEST2 pins to V_{SS} and always connect both V_{DD} pins 31 and 73 to the + side of the power supply.

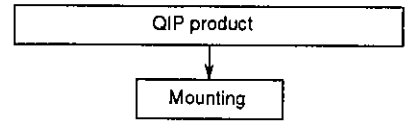
4. PROM space



5. ROM ordering techniques when using the Sanyo (for-fee) PROM writing service
- When ordering one-time versions and mask ROM versions at the same time
Provide a filled-out one-time version order form along with a PROM to which the mask ROM version program and option data have been written and the mask ROM order form.
- When ordering one-time versions only
Provide a filled-out one-time version order form along with a PROM to which the program and option data have been written.

6. Conditions prior to mounting
   - Products written by the user
     When the LC72P321 is purchased before the PROM has been written, it must be mounted according to the following procedure.





   - Products written by Sanyo
     When the LC72P321 is purchased after the PROM has been written, it must be mounted according to the following procedure.

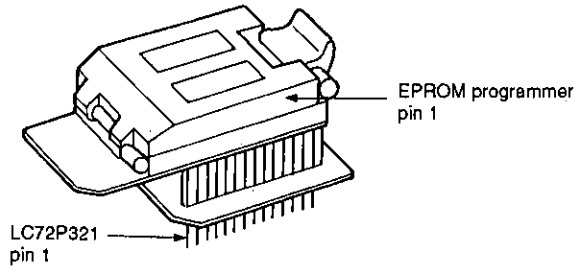
Note: Since it is not possible to perform a full test of one-time PROM microcontrollers (i.e., products in which the PROM has not been written) before shipment, there will be some reduction in the writing yield.

Usage Techniques

1. Techniques for writing the on-chip PROM
   There are two techniques for writing to the LC72P321 on-chip PROM as follows.
   - Using a general-purpose EPROM programmer
     If a general-purpose EPROM programmer is to be used, the PROM can be written by using a special-purpose PROM writing socket, the LC72E32 ADAPTER FOR EPROM PROGRAMMER. The EPROM programmer should be set to use the "27512 (Vpp = 12.5 V) Intel high-speed write" technique. The address range should be set to locations 0 to 2033H.

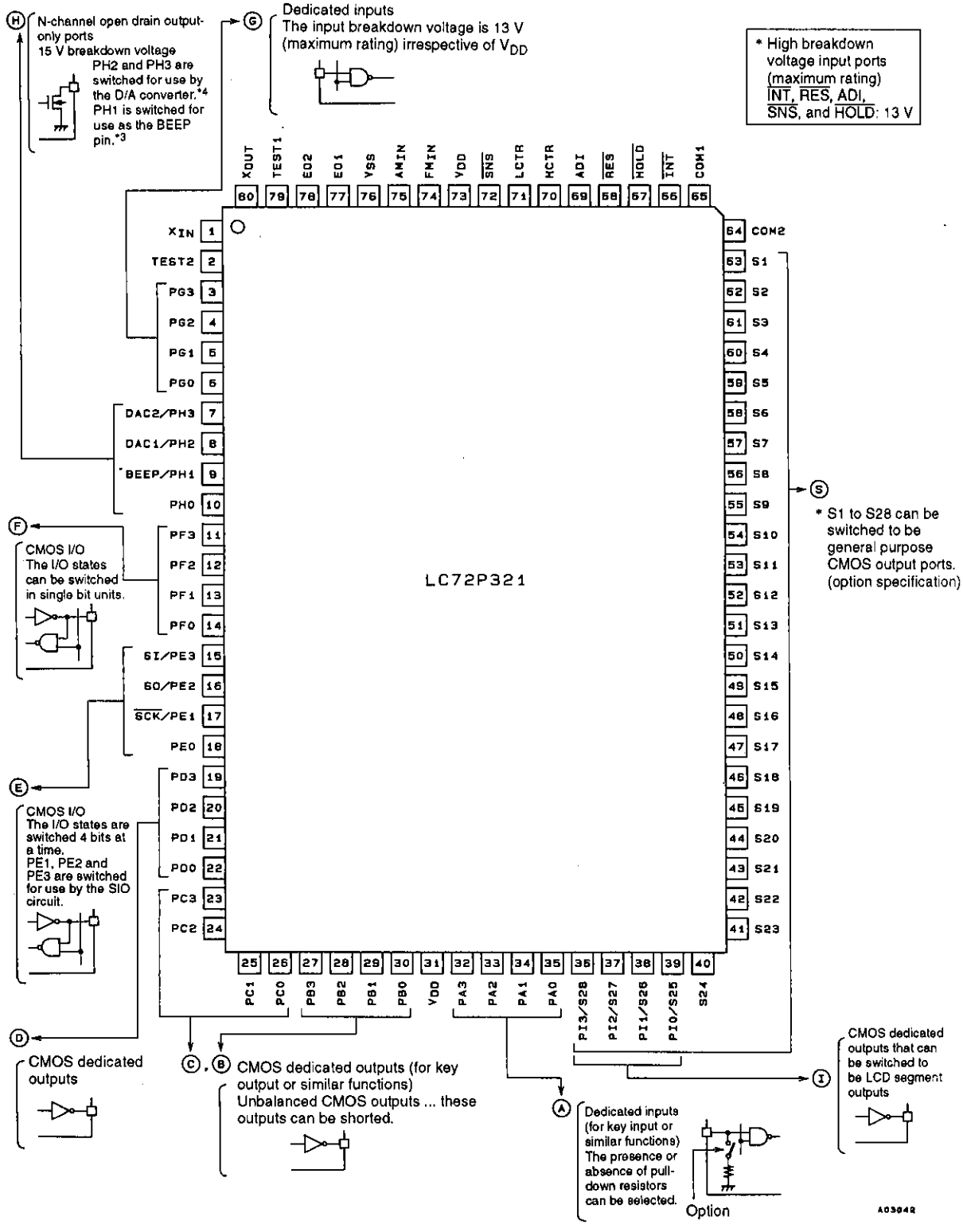
   - Using the RE32 in-circuit emulator
     If the RE32 in-circuit emulator is to be used for PROM writing, the PROM can be written by using a special-purpose PROM writing socket, the LC72E32 Adapter for RE32 Programmer. Use the PGOTP command as the writing technique.

2. Special-purpose PROM writing socket
   As mentioned above, there are two special-purpose PROM writing sockets. These sockets must only be used for their intended writing technique.

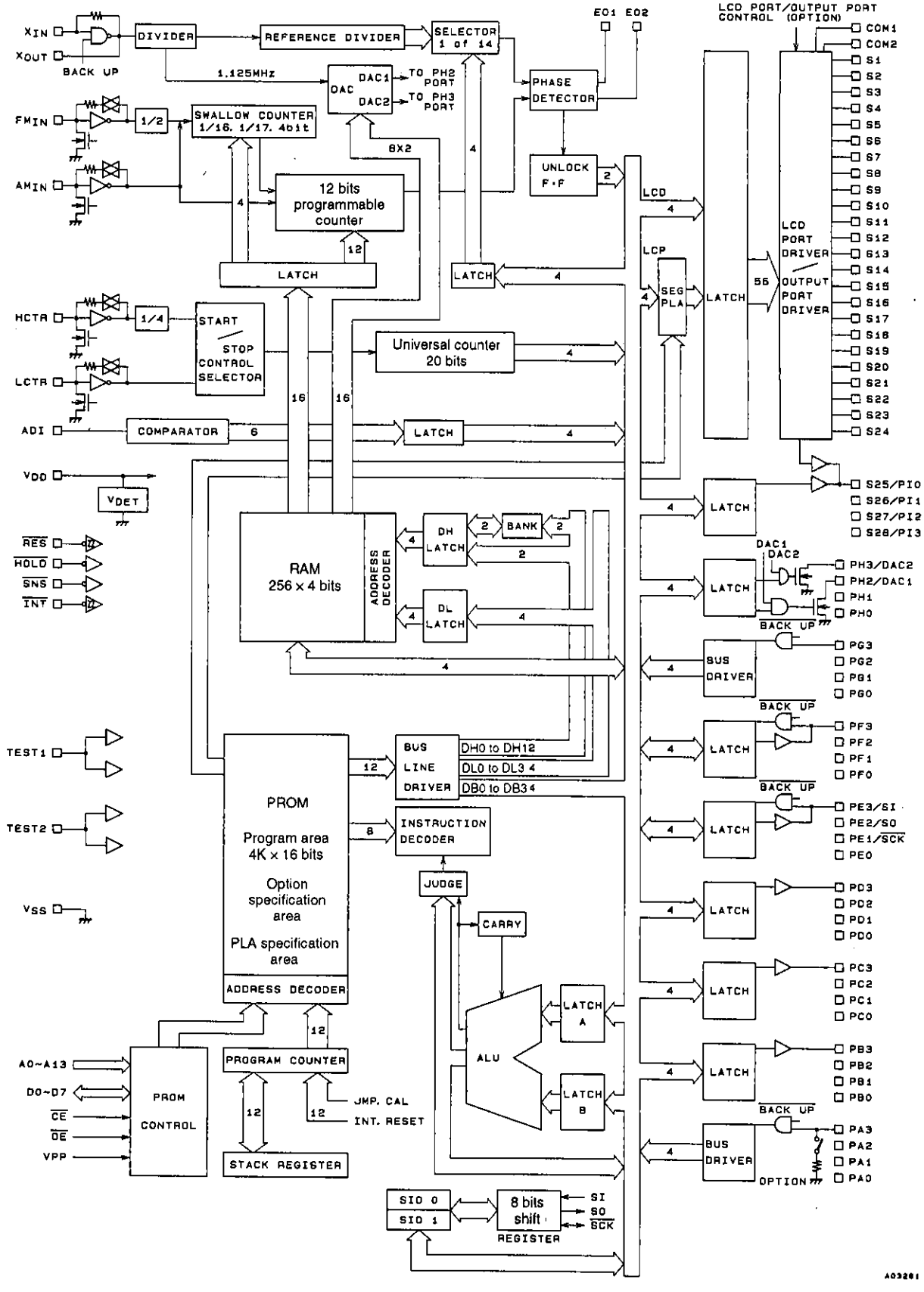


General-purpose EPROM programmer adapter:
Product name: LC72E32 Adapter for EPROM Programmer
Product code: NDK-DC-001-A
RE32 in-circuit emulator adapter:
Product name: LC72E32 Adapter for RE32
Product code: NDK-DC-003-A

Pin Assignment



Block Diagram



LC72P321 Instruction Table

Abbreviations:

ADDR: Program memory address [12 bits]
b: Borrow
B: Bank number [2 bits]
C: Carry
DH: Data memory address high (row address) [2 bits]
DL: Data memory address low (column address) [4 bits]
I: Immediate data [4 bits]
M: Data memory address
N: Bit position [4 bits]
Pn: Port number [4 bits]
r: General register (one of the locations 00 to 0FH in bank 0)
Rn: Register number [4 bits]
( ): Contents of register or memory
( )n: Contents of bit N of register or memory

Instruction Group	Mnemonic	Operand		Function	Operation	Machine code													
		1st	2nd			D15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	D0
Addition instructions	AD	r	M	Add M to r	r ← (r) + (M)	0	1	0	0	0	0	DH		DL				Rn			
	ADS	r	M	Add M to r, then skip if carry	r ← (r) + (M) skip if carry	0	1	0	0	0	1	DH		DL				Rn			
	AC	r	M	Add M to r with carry	r ← (r) + (M) + C	0	1	0	0	1	0	DH		DL				Rn			
	ACS	r	M	Add M to r with carry, then skip if carry	r ← (r) + (M) + C skip if carry	0	1	0	0	1	1	DH		DL				Rn			
	AI	M	I	Add I to M	M ← (M) + I	0	1	0	1	0	0	DH		DL				I			
	AIS	M	I	Add I to M, then skip if carry	M ← (M) + I skip if carry	0	1	0	1	0	1	DH		DL				I			
	AIC	M	I	Add I to M with carry	M ← (M) + I + C	0	1	0	1	1	0	DH		DL				I			
	AICS	M	I	Add I to M with carry, then skip if carry	M ← (M) + I + C skip if carry	0	1	0	1	1	1	DH		DL				I			
Subtraction instructions	SU	r	M	Subtract M from r	r ← (r) − (M)	0	1	1	0	0	0	DH		DL				Rn			
	SUS	r	M	Subtract M from r, then skip if borrow	r ← (r) − (M) skip if borrow	0	1	1	0	0	1	DH		DL				Rn			
	SB	r	M	Subtract M from r with borrow	r ← (r) − (M) − b	0	1	1	0	1	0	DH		DL				Rn			
	SBS	r	M	Subtract M from r with borrow, then skip if borrow	r ← (r) − (M) − b skip if borrow	0	1	1	0	1	1	DH		DL				Rn			
	SI	M	I	Subtract I from M	M ← (M) − I	0	1	1	1	0	0	DH		DL				I			
	SIS	M	I	Subtract I from M, then skip if borrow	M ← (M) − I skip if borrow	0	1	1	1	0	1	DH		DL				I			
	SIB	M	I	Subtract I from M with borrow	M ← (M) − I − b	0	1	1	1	1	0	DH		DL				I			
	SIBS	M	I	Subtract I from M with borrow, then skip if borrow	M ← (M) − I − b skip if borrow	0	1	1	1	1	1	DH		DL				I			
Comparison instructions	SEQ	r	M	Skip if r equals M	r − M skip if zero	0	0	0	0	0	1	DH		DL				Rn			
	SGE	r	M	Skip if r is greater than or equal to M	r − M skip if not borrow (r) ≥ (M)	0	0	0	0	1	1	DH		DL				Rn			
	SEQI	M	I	Skip if M equal to I	M − I skip if zero	0	0	1	1	0	1	DH		DL				I			
	SGEI	M	I	Skip if M is greater than or equal to I	M − I skip if not borrow (M) ≥ I	0	0	1	1	1	1	DH		DL				I			

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Instruction Group	Mnemonic	Operand 1st	Operand 2nd	Function	Operation	Machine code D15 14 13 12	11 10	9 8	7 6 5 4	3 2 1 D0
Logical operation instructions	AND	M	I	AND I with M	M ← (M) ∧ I	0 0 1 1	0 0	DH	DL	I
	OR	M	I	OR I with M	M ← (M) ∨ I	0 0 1 1	1 0	DH	DL	I
	EXL	r	M	Exclusive OR M with r	r ← (r) ⊕ (M)	0 0 1 0	0 0	DH	DL	Rn
Transfer instructions	LD	r	M	Load M to r	r ← (M)	1 0 0 0	0 0	DH	DL	Rn
	ST	M	r	Store r to M	M ← (r)	1 0 0 0	0 1	DH	DL	Rn
	MVRD	r	M	Move M to destination M referring to r in the same row	[DH, Rn] ← (M)	1 0 0 0	1 0	DH	DL	Rn
	MVRS	M	r	Move source M referring to r to M in the same row	M ← [DH, Rn]	1 0 0 0	1 1	DH	DL	Rn
	MVSR	M1	M2	Move M to M in the same row	[DH, DL1] ← [DH, DL2]	1 0 0 1	0 0	DH	DL1	DL2
	MVI	M	I	Move I to M	M ← I	1 0 0 1	0 1	DH	DL	I
	PLL	M	r	Load M to PLL registers	PLL r ← PLL DATA	1 0 0 1	1 0	DH	DL	Rn
Bit test instructions	TMT	M	N	Test M bits, then skip if all bits specified are true	if M (N) = all "1", then skip	1 0 1 0	0 1	DH	DL	N
	TMF	M	N	Test M bits, then skip if all bits specified are false	if M (N) = all "0", then skip	1 0 1 0	1 1	DH	DL	N
Jump and subroutine call instructions	JMP	ADDR		Jump to the address	PC ← ADDR	1 0 1 1	ADDR (12 bits)			
	CAL	ADDR		Call subroutine	PC ← ADDR Stack ← (PC) + I	1 1 0 0	ADDR (12 bits)			
	RT			Return from subroutine	PC ← Stack	1 1 0 1	0 1 0 0	0 0 0 0	0 0 0 0	
	RTI			Return from interrupt	PC ← Stack	1 1 0 1	0 1 0 1	0 0 0 0	0 0 0 0	
F/F test instructions	TTM	N		Test timer F/F then skip if it has not been set	if timer F/F = "0", then skip	1 1 0 1	0 1 1 0	0 0 0 0	N	
	TUL	N		Test unlock F/F then skip if it has not been set	if UL F/F = "0", then skip	1 1 0 1	0 1 1 1	0 0 0 0	N	
Status register instructions	SS	N		Set status register	(Status register 1) N ← 1	1 1 0 1	1 1 0 0	0 0 0 0	N	
	RS	N		Reset status register	(Status register 1) N ← 0	1 1 0 1	1 1 0 1	0 0 0 0	N	
	TST	N		Test status register true	if (Status register 2) N = all "1", then skip	1 1 0 1	1 1 1 0	0 0 0 0	N	
	TSF	N		Test status register false	if (Status register 2) N = all "0", then skip	1 1 0 1	1 1 1 1	0 0 0 0	N	
Bank switching instructions	BANK	B		Select bank	BANK ← B	1 1 0 1	0 0	B	0 0 0 0	0 0 0 0

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Instruction Group	Mnemonic	Operand 1st	Operand 2nd	Function	Operation	Machine code D15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 D0	
I/O instructions	LCD	M	I	Output segment pattern to LCD digit direct	LCD (DIGIT) ← M	1 1 1 0	0 0 DH	DL	DIGIT	
	LCP	M	I	Output segment pattern to LCD digit through PLA	LCD (DIGIT) ← PLA ← M	1 1 1 0	0 1 DH	DL	DIGIT	
	IN	M	P	Input port data to M	M ← (Port (P))	1 1 1 0	1 0 DH	DL	P	
	OUT	M	P	Output contents of M to port	(Port (P)) ← M	1 1 1 0	1 1 DH	DL	P	
	SPB	P	N	Set port bits	(Port (P)) N ← 1	1 1 1 1	0 0 0 0	P	N	
	RPB	P	N	Reset port bits	(Port (P)) N ← 0	1 1 1 1	0 1 0 1	P	N	
	TPT	P	N	Test port bits, then skip if all bits specified are true	if (Port (P)) N = all "1", then skip	1 1 1 1	1 0 1 0	P	N	
	TPF	P	N	Test port bits, then skip if all bits specified are false	if (Port (P)) N = all "0", then skip	1 1 1 1	1 1 1 1	P	N	
Universal counter instructions	UCS	I		Set I to UCCW1	UCCW1 ← I	0 0 0 0	0 0 0 1	0 0 0 0	I	
	UCC	I		Set I to UCCW2	UCCW2 ← I	0 0 0 0	0 0 1 1	0 0 0 0	I	
Other instructions	FPC	N		F port I/O control	FPC latch ← N	0 0 0 1	0 0 0 0	0 0 0 0	N	
	CKSTP			Clock stop	Stop clock if $\overline{HOLD}$ = 0	0 0 0 1	0 0 0 1	0 0 0 0	0 0 0 0	
	DAC	I		Load M to D/A registers	DA reg ← DAC DATA	0 0 0 0	0 0 1 0	0 0 0 0	I	*3
	SIO	I1	I2	Serial I/O control	SIOCW ← I1, I2	0 0 0 1	0 0 1 1	I1	I2	
	SIOL	M	I	Load SIO reg to M	M ← SIO reg	0 0 0 1	1 0 DH	DL	I	*1
	SIOS	M	I	Store M to SIO reg	SIO reg ← M	0 0 0 1	0 1 DH	DL	I	
	BEEP	I		Beep control	BEEP reg ← I	0 0 0 1	0 0 1 0	0 0 0 0	I	*2
	NOP			No operation		0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	