Ordering number: EN ※4118

SANYO

No.※4118

LC7232N

CMOS LSI

Single-chip PLL and Microcontroller with LCD Driver

Preliminary

OVERVIEW

The LC7232N is a single-chip microcontroller that incorporates a 0.5 to 150 MHz phase-locked loop (PLL) and a liquid-crystal display (LCD) driver, making it ideal for digital tuners. It incorporates frequency and period measurement circuits, and a large number of input/output ports on-chip.

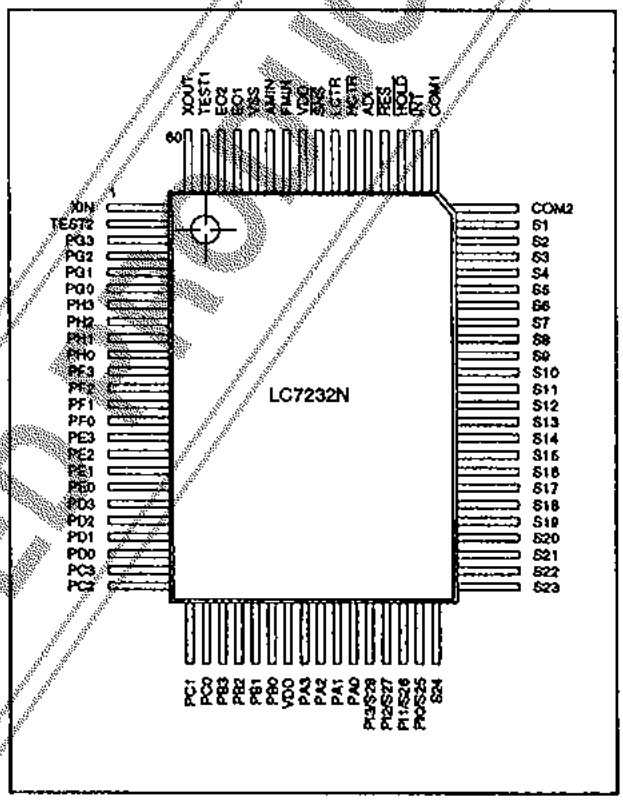
The LC7232N comprises on-chip RAM and ROM, a programmable high-speed divider, a 6-bit analog-to-digital converter, two 8-bit digital-to-analog converters and a low-voltage detection reset circuit.

The LC7232N operates from a 5 V supply and is available in 80-pin QIPs.

FEATURES

- 0.5 to 150 MHz phase-locked loop
- LCD driver
- 6-bit analog-to-digital converter
- Two 8-bit PWM digital-to-analog converters
- Two 4-bit input/output ports
- Two 4-bit input ports
- One 4-bit output port
- 8-bit keypad matrix scan output port
- 4-bit open-drain, high-voltage output port
- 28 mask-selectable output drivers
- 20-bit universal counter
- 4096 × 16-bit program ROM (001H to FFFH user-addressable memory)
- 256 × 4-bit data RAM
- Low-voltage detection reset circuit
- Programmable high-speed divider
- Single-word instructions
- Four-level stack
- PLL-unlocked flip-flop
- Timer flip-flop
- External interrupt
- Programmable watchdog interrupt address
- Standby mode
- CPU operates down to 3.5 V and retains data down to 1.3 V.
- 5 V supply
- 80-pin QIP

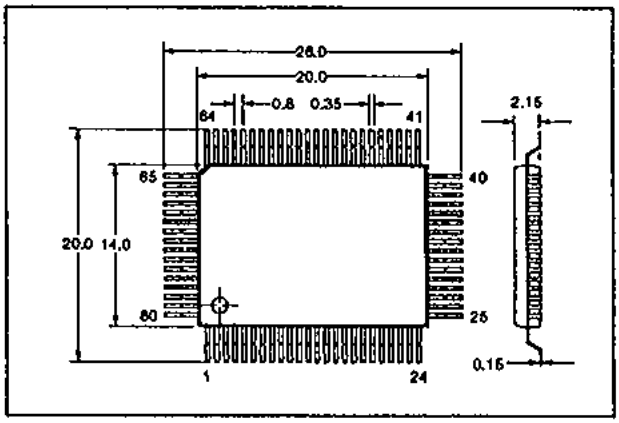
PINOUT



PACKAGE DIMENSIONS

Unit: mm

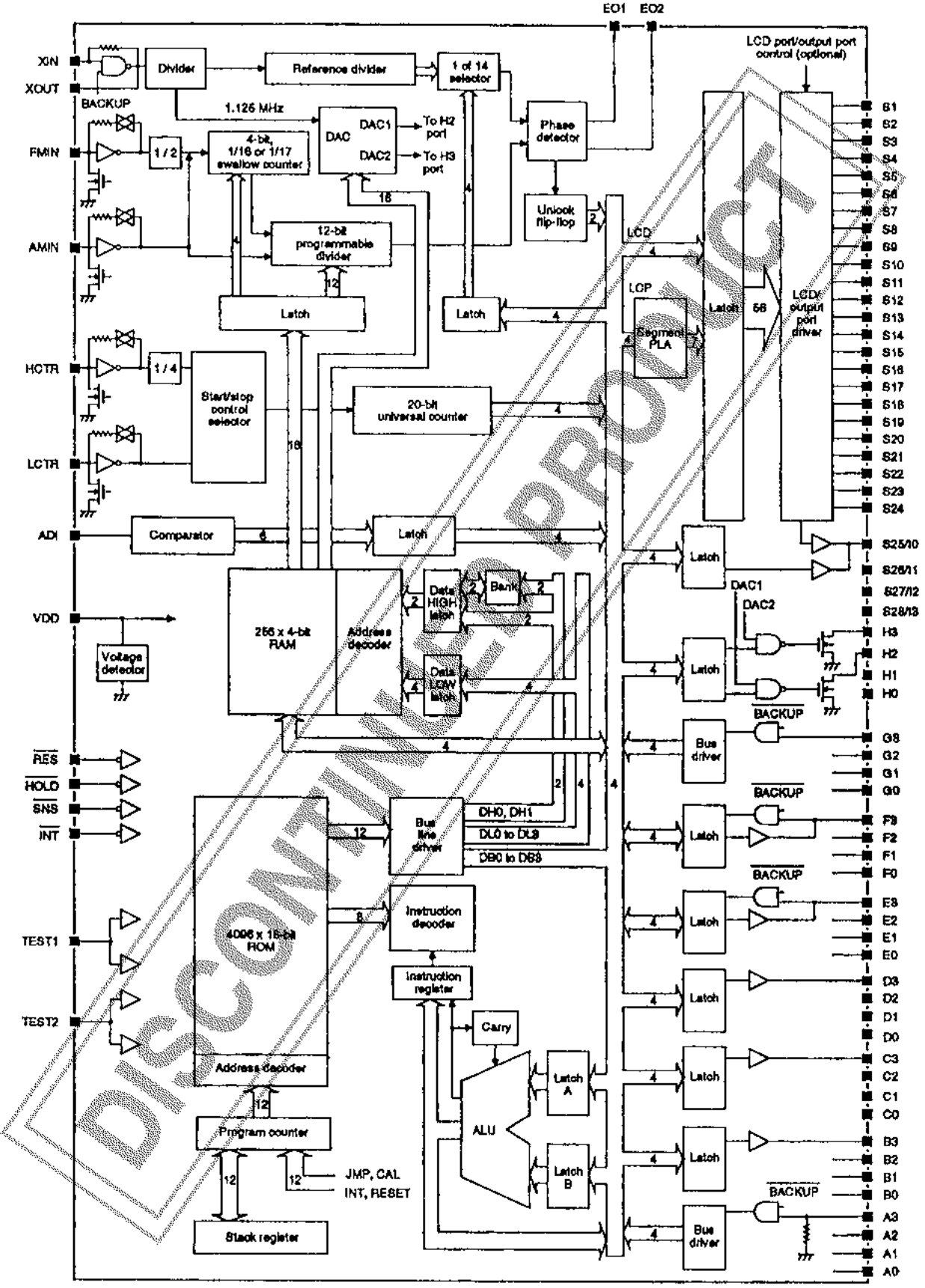
3044B-QIP80A



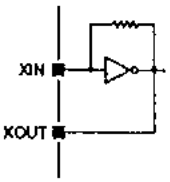
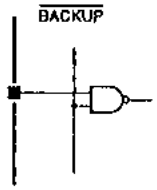
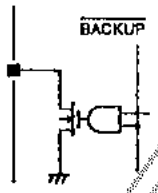
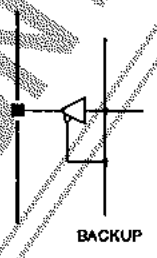
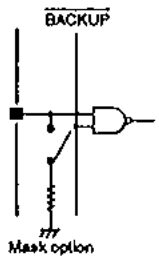
Specifications and information herein are subject to change without notice.

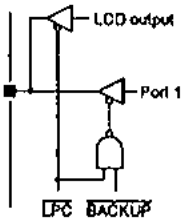
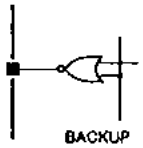
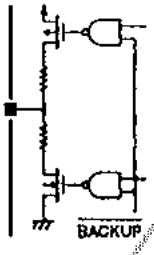
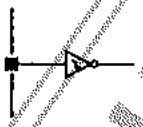
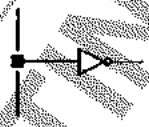
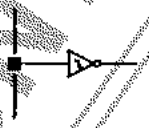
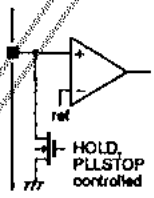
SANYO Electric Co., Ltd. Semiconductor Division
Natsume Bldg., 18-6, 2-chome, Yushima, Bunkyo-ku, TOKYO 113 JAPAN

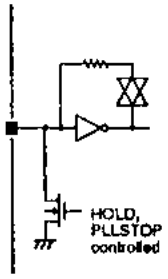
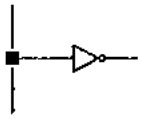
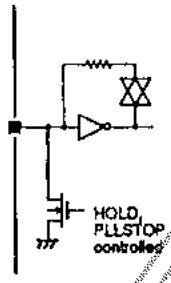
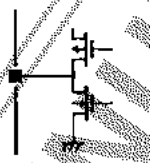
BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	Equivalent Circuit	Description
1	XIN		Crystal oscillator connections
80	XOUT		
2	TEST2		Test pins
79	TEST1		
3 to 6	PG3 to PG0		Input port G
7 to 10	PH3 to PH0		Output port H
11 to 14	PF3 to PF0		Input/output port F
15 to 18	PE3 to PE0		Input/output port E
19 to 22	PD3 to PD0		Output port D
23 to 26	PC3 to PC0		Output port C
27 to 30	PB3 to PB0		Output port B
31, 73	VDD		5 V supply
32 to 35	PA3 to PA0		Input port A

Number	Name	Equivalent Circuit	Description
36 to 39	PI3/S28 to PI0/S25		Input port I
40 to 63	S24 to S1		LCD segment outputs
64, 65	COM2, COM1		LCD common driver outputs
66	$\overline{INT}$		Interrupt request input
67	$\overline{HOLD}$		Hold-mode control input
68	$\overline{RES}$		Device reset input
69	ADI		A/D converter input

Number	Name	Equivalent Circuit	Description
70	HCTR		Universal counter input 1
71	LCTR		Universal counter input 2
72	$\overline{SNS}$		Power-fail detect
74	FMIN		FM VCO input
75	AMIN		AM VCO input
76	VSS		Ground
77, 78	EO1 and EO2		Phase comparator outputs

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	−0.3 to 6.5	V
Port G, $\overline{HOLD}$, ADI, $\overline{INT}$, $\overline{RES}$ and $\overline{SNS}$ input voltage range	V_{I1}	−0.3 to 13	V
Input voltage range for all other inputs	V_{I2}	−0.3 to V_{DD} + 0.3	V
Port H output voltage range	V_{O1}	−0.3 to 15	V
Output voltage range for all other outputs	V_{O2}	−0.3 to V_{DD} + 0.3	V
Ports D and H output current range	I_{O1}	0 to 5	mA
Ports E and F output current range	I_{O2}	0 to 3	mA
Ports B and C output current range	I_{O3}	0 to 1	mA
Port I and S1 to S28 output current range	I_{O4}	0 to 1	mA
Power dissipation	P_D	400	mW

Parameter	Symbol	Rating	Unit
Operating temperature range	T_{opg}	−40 to 85	°C
Storage temperature range	T_{stg}	−45 to 125	°C

Recommended Operating Conditions

T_a = 25 °C

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	5	V
Supply voltage range (PLL and CPU)	V_{DD1}	4.5 to 5.5	V
Supply voltage range (CPU)	V_{DD2}	3.5 to 5.5	V
Supply voltage range for data retention	V_{DDS}	1.3 to 5.5	V

Electrical Characteristics

V_{DD} = 3.5 to 5.5 V, T_a = −40 to 85 °C unless otherwise noted.

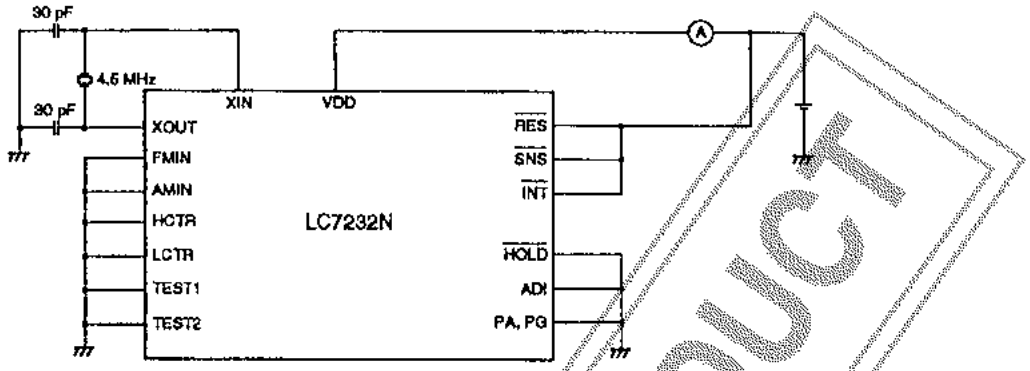
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply current	I_{DD1}	f_i = 130 MHz, V_{DD} = 4.5 to 5.5 V	–	15	20	mA
Hold-mode supply current	I_{DD2}	PLL halted, t_{cyc} = 2.57 µs, V_{DD} = 3.5 to 5.5 V	–	1.6	–	mA
		PLL halted, t_{cyc} = 13.33 µs, V_{DD} = 3.5 to 5.5 V	–	1.0	–	
		PLL halted, t_{cyc} = 40.00 µs, V_{DD} = 3.5 to 5.5 V	–	0.7	–	
Standby-mode supply current	I_{DDS}	V_{DD} = 5.5 V, oscillator halted, T_a = 25 °C	–	–	5	µA
		V_{DD} = 2.5 V, oscillator halted, T_a = 25 °C	–	–	1	
Port A LOW-level input voltage	V_{IL1}		0	–	0.2V_{DD}	V
Ports E and F LOW-level input voltage	V_{IL2}		0	–	0.3V_{DD}	V
Port G LOW-level input voltage	V_{IL3}		0	–	0.3V_{DD}	V
$\overline{HOLD}$ LOW-level input voltage	V_{IL4}		0	–	0.4V_{DD}	V
LCTR LOW-level input voltage	V_{IL5}	V_{DD} = 4.5 to 5.5 V	0	–	0.2V_{DD}	V
$\overline{RES}$ and $\overline{INT}$ LOW-level input voltage	V_{IL6}		0	–	0.2V_{DD}	V
$\overline{SNS}$ LOW-level input voltage	V_{IL7}		0	–	1.3	V
Port A HIGH-level input voltage	V_{IH1}		0.6V_{DD}	–	V_{DD}	V
Ports E and F HIGH-level input voltage	V_{IH2}		0.7V_{DD}	–	V_{DD}	V
Port G HIGH-level input voltage	V_{IH3}		0.7V_{DD}	–	6.0	V
LCTR HIGH-level input voltage	V_{IH4}	V_{DD} = 4.5 to 5.5 V	0.6V_{DD}	–	V_{DD}	V
$\overline{RES}$, $\overline{INT}$ and $\overline{HOLD}$ HIGH-level input voltage	V_{IH5}		0.8V_{DD}	–	6.0	V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
$\overline{SNS}$ HIGH-level input voltage	V_{IH6}		2.5	–	8.0	V
XIN rms input amplitude	V_{I1}		0.5	–	1.5	V
FMIN rms input amplitude	V_{I2}		0.1	–	1.5	V
AMIN rms input amplitude	V_{I3}		0.1	–	1.5	V
LCTR and HCTR rms input amplitude	V_{I4}		0.1	–	1.5	V
ADI input voltage	V_{I5}		0	–	V_{DD}	V
LCTR, $\overline{RES}$ and $\overline{INT}$ input hysteresis width	V_{HYS}		$0.1V_{DD}$	–	–	V
Standby threshold voltage	V_{DET}		2.7	3.0	3.3	V
Port A input voltage	V_{IF}	Port A is high impedance. Port A has R_{PD}.	–	–	$0.05V_{DD}$	V
XIN input frequency	f_{I1}	V_I = 0.5 to 1.5 V	4.0	4.5	5.0	MHz
FMIN input frequency	f_{I2}	V_I = 0.1 to 1.5 V, V_{DD} = 4.5 to 5.5 V	10	–	130	MHz
		V_I = 0.15 to 1.5 V, V_{DD} = 4.5 to 5.5 V	10	–	150	
AMIN input frequency (low range)	f_{I3}	V_I = 0.1 to 1.5 V, V_{DD} = 4.5 to 5.5 V	0.5	–	10.0	MHz
AMIN input frequency (high range)	f_{I4}	V_I = 0.1 to 1.5 V, V_{DD} = 4.5 to 5.5 V	2	–	40	MHz
HCTR input frequency	f_{I5}	V_I = 0.1 to 1.5 V, V_{DD} = 4.5 to 5.5 V	0.4	–	12.0	MHz
LCTR input frequency	f_{I7}	V_I = 0.1 to 1.5 V, V_{DD} = 4.5 to 5.5 V	100	–	500	kHz
		V_{IL} = 0 V to $0.2V_{DD}$, V_{IH} = $0.8V_{DD}$ to V_{DD}	0.001	–	20	
$\overline{SNS}$ reject pulsewidth	P_{W6}		–	–	50	µs
Ports A, E and F LOW-level input current	I_{IL1}	Ports E and F are high impedance. Port A has no R_{PD}. V_I = V_{SS}	–	–	3.0	µA
$\overline{INT}$, $\overline{RES}$, $\overline{HOLD}$, ADI, $\overline{SNS}$ and port G LOW-level input current	I_{IL2}	V_I = V_{SS}	–	–	3.0	µA
LCTR, FMIN, AMIN and HCTR LOW-level input current	I_{IL3}	V_I = V_{SS}	4	10	30	µA
XIN LOW-level input current	I_{IL4}	V_I = V_{SS}	2	5	15	µA
Ports A, E and F HIGH-level input current	I_{IH1}	Ports E and F are high impedance. Port A has no R_{PD}. V_I = V_{DD}	–	–	3.0	µA
Port A HIGH-level input current	I_{IH2}	V_I = V_{DD} = 5.0 V, Port A has R_{PD}.	–	50	–	µA
$\overline{INT}$, $\overline{RES}$, $\overline{HOLD}$, ADI, $\overline{SNS}$ and port G HIGH-level input current	I_{IH3}	V_{IN} = 5.5 V	–	–	3.0	µA
LCTR, FMIN, AMIN and HCTR HIGH-level input current	I_{IH4}	V_I = V_{DD} = 5.0 V	4	10	30	µA
XIN HIGH-level input current	I_{IH5}	V_I = V_{DD} = 5.0 V	2	5	15	µA
Ports B and C LOW-level output voltage	V_{OL1}	I_O = 50 µA	0.5	1.0	2.0	V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Port D LOW-level output voltage	V_{OL2}	I_O = 5 mA	–	–	1.0	V
Ports E and F LOW-level output voltage	V_{OL3}	I_O = 1 mA	–	–	1.0	V
Port H LOW-level output voltage	V_{OL4}	I_O = 5 mA	0.75 (150 Ω)	–	2.0 (400 Ω)	V
COM1 and COM2 LOW-level output voltage	V_{OL5}	I_O = 25 μA	0.3	0.5	0.75	V
EO1 and EO2 LOW-level output voltage	V_{OL6}	I_O = 500 μA	–	–	1.0	V
Port I and S1 to S28 LOW-level output voltage	V_{OL7}	I_O = 0.1 mA	–	–	1.0	V
XOUT LOW-level output voltage	V_{OL8}	I_O = 200 μA	–	–	1.0	V
COM1 and COM2 mid-level output voltage	V_{M1}	V_{DD} = 6 V, I_O = 20 μA	2.0	2.5	3.0	V
Ports B and C HIGH-level output voltage	V_{OH1}	I_O = 1 mA	V_{DD} – 2.0	V_{DD} – 1.0	V_{DD} – 0.5	V
Port D HIGH-level output voltage	V_{OH2}	I_O = 5 mA	V_{DD} – 1.0	–	–	V
Ports E and F HIGH-level output voltage	V_{OH3}	I_O = 1 mA	V_{DD} – 1.0	–	–	V
COM1 and COM2 HIGH-level output voltage	V_{OH4}	I_O = 25 μA	V_{DD} – 0.75	V_{DD} – 0.5	V_{DD} – 0.3	V
EO1 and EO2 HIGH-level output voltage	V_{OH5}	I_O = 500 μA	V_{DD} – 1.0	–	–	V
Port I and S1 to S28 HIGH-level output voltage	V_{OH6}	I_O = –0.1 mA	V_{DD} – 1.0	–	–	V
XOUT HIGH-level output voltage	V_{OH7}	I_O = 200 μA	V_{DD} – 1.0	–	–	V
Ports B, C, E, F and I LOW-level output leakage current	I_{OFFL1}	V_O = V_{SS}	–	–	3.0	μA
EO1 and EO2 LOW-level output leakage current	I_{OFFL2}	V_O = V_{SS}	–	0.01	10.0	nA
Ports B, C, E, F and I HIGH-level output leakage current	I_{OFFH1}	V_O = V_{DD}	–	–	3.0	μA
Port H HIGH-level output leakage current	I_{OFFH2}	V_O = 13 V	–	–	5.0	μA
EO1 and EO2 HIGH-level output leakage current	I_{OFFH3}	V_O = V_{DD}	–	0.01	10.0	nA
A/D converter error	ε	V_{DD} = 4.5 to 5.5 V	–½	–	½	lsb
Port A pull-down resistance	R_{PD}	V_{DD} = 6 V	75	100	200	kΩ

Measurement Circuits

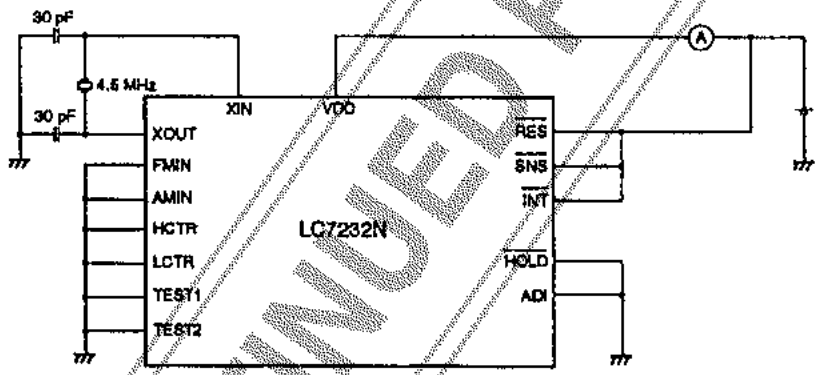
Hold mode



Notes

1. Ports E and F are selected as output ports.
2. Ports B to H are open.

Standby mode



Note

Ports A to I, S1 to S24, COM1 and COM2 are open.

FUNCTIONAL DESCRIPTION

LCD Driver

The LC7232N can drive LCD segments. The LCP and LCD instructions transfer data to the LCD outputs. The LCD instruction transfers data directly to the LCD outputs whereas the LCP instruction converts data to 7-segment format before transfer to the outputs.

S1 to S28 are the driver outputs. The LCD frame rate is 100 Hz with a 50% duty cycle. After reset or power-up, a blank signal is present on all outputs. In standby mode, all outputs are LOW. They can be used as general-purpose outputs if the appropriate mask option is selected.

COM1 and COM2 are the LCD common driver outputs. Output drive is 50% duty with 50% bias. Upon reset or after power-up, the normal drive signals are present on these outputs. In standby mode, all outputs are LOW.

Frequency and Period Measurement

AM IF frequencies are measured at HCTR and LCTR by the 20-bit universal counter using an input frequency range of 0.4 to 12 MHz. FM IF frequencies are measured at HCTR only. Capacitative coupling should be used at HCTR for all input frequencies, and at LCTR, for input frequencies in the range 100 to 500 KHz.

Period measurement is performed at LCTR by the 20-bit universal counter using an input frequency range of 1 Hz to 20 KHz. Capcitative coupling is not required.

Phase-locked Loop

The FMIN or AMIN input signal is divided down by a programmable divider, and then compared with the crystal frequency, which is also divided down using 14

selectable ratios. The phase difference between the two signals is measured using a phase detector and output on EO1 and EO2.

FMIN is the input pin for the FM VCO input signal. The input frequency range is 10 to 130 MHz. Capacitive coupling should be used.

AMIN is the AM VCO input. The bandwidth is adjustable in two ranges by using the PLL instruction—HIGH (2 to 40 MHz) for the SW band, and LOW (0.5 to 10 MHz), for the LW and MW bands. Capacitive coupling should be used.

Input/Output Ports

Port A

This input port has a low switching threshold, which is used for keypad matrix inputs. Pull-down resistors for all pins are available as a mask option. Note that either all or none of the pins should have pull-down resistors. In standby mode, inputs are ignored.

Ports B and C

These output ports have unbalanced CMOS outputs which are used as keypad matrix scan outputs. Upon reset, outputs are set LOW, and in standby mode, outputs are high impedance. The outputs can be short-circuited.

Port D

Port D is an output port only. Upon reset, outputs are LOW, and in standby mode, outputs are high impedance.

Port E

The transfer direction of this input/output port is selected automatically under software control. When an input instruction (IN, TPT, or TPF) is executed, port E is configured for input operation, and an output instruction (OUT, SPB or RPB), for output operation. Upon reset, all pins become inputs. In standby mode, the output drivers are high impedance and the input signals are ignored. All bits should either be inputs or outputs.

Port F

The transfer direction of this input/output port is selected by the FPC instruction. Each pin of this port can be set independently to be an input or output. Upon reset, all pins become inputs. In standby mode, the output drivers are high impedance and the input signals are ignored.

Port G

This is an input port only. In standby mode, inputs are ignored.

Port H

These output ports are high-voltage, n-channel open-drain drivers, which are used for switching power supplies. Upon reset and in standby mode, outputs are high impedance.

Port I

Port I is a 4-bit general purpose output port. The outputs PI0 to PI3 are multiplexed with four of the LCD driver outputs, S25 to S28. The bits can be configured as either standard outputs or LCD driver outputs by using the SS and RS instructions. Upon power-on or after reset, they are configured as LCD drivers and output a blank display signal. In standby mode these pins are LOW.

A/D Converter

The A/D converter is a 6-bit successive approximation type. The conversion cycle time is 1.28 ms. Full-scale output data is 3FH for an input of (63/96) × V_{DD}.

PWM Outputs

Bits 2 and 3 of port H are the outputs of DAC1 and DAC2, respectively. The outputs are pulsewidth modulation (PWM) encoded, with the width of the output pulse determined by the value loaded into the 8-bit register for the corresponding DAC. The output frequency is 4394.5 Hz for a cycle time of 2.67 µs.

Power-fail Detection

When connected to the supply, $\overline{SNS}$ is used as a power-fail detector. $\overline{SNS}$ can also be used as a standard input port.

Interrupt Request

This input generates a device interrupt when a HIGH-to-LOW transition occurs. The corresponding INTEN flag should be set by the SS instruction before an interrupt can be generated.

Reset

This input can be used to re-initialize the LC7232N. Upon power-up, this pin should be held LOW for at least 75 ms after the supply stabilizes. Thereafter, it should be held LOW for at least six clock cycles to reset the device.

Crystal Oscillator

The master crystal oscillator, which has a feedback resistor on-chip, requires only the connection of a 4.5 MHz crystal.

Low-power Modes

Hold mode

When the hold mode control pin, $\overline{HOLD}$, is driven LOW and the HOLDEN (hold enable) flip-flop has previously been set by an SS instruction, the LC7232N enters hold mode.

$\overline{HOLD}$ has a high-voltage input (V_{IH}(max) = 8.0 V) which can be connected directly to the power supply.

Standby mode

When the LC7232N is in hold mode and $\overline{HOLD}$ is LOW, standby mode can be set by the CKSTP instruction.

Test Pins

Two device test pins are provided—TEST1 and TEST2. These should either be tied to V_{SS} or left open.

INSTRUCTION SET

ADDR	Program memory address [12 bits]
b	Borrow
B	Bank number [2 bits]
C	Carry
DH	Data memory address high-order bits (row address) [2 bits]
DL	Data memory address low-order bits (column address) [4 bits]
I	Immediate data [4 bits]
M	Data memory address
N	Bit position [4 bits]
P*n*	Port number [4 bits]
r	General register (Bank 0 addresses 00H to 0FH)
R*n*	Register number [4 bits]
( )	Contents of register or memory
( )*n*	Contents of bit N of register or memory

Mnemonic	Operand		Operation	Instruction format																Notation	Description	Skip condition
	1st	2nd		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0			
Add																						
AD	r	M	Add M to r.	0	1	0	0	0	0	DH			DL			Rn				r ← (r) + (M)	Adds the contents of M to the contents of r and stores the result in r.	
ADS	r	M	Add M to r and skip if carry.	0	1	0	0	0	1	DH			DL			Rn				r ← (r) + (M), skip if carry.	Adds the contents of M to the contents of r then stores the result in r. Skips if a carry is generated.	Carry
AC	r	M	Add M to r with carry.	0	1	0	0	1	0	DH			DL			Rn				r ← (r) + (M) + C	Adds the contents of M to the contents of r and C then stores the result in r.	
ACS	r	M	Add M to r with carry and skip if carry.	0	1	0	0	1	1	DH			DL			Rn				r ← (r) + (M) + C, skip if carry	Adds the contents of M to the contents of r and C then stores the result in r. Skips if a carry is generated.	Carry
AI	M	I	Add I to M.	0	1	0	1	0	0	DH			DL			I				M ← (M) + I	Adds the immediate data to the contents of M then stores the result in M.	
AIS	M	I	Add I to M and skip if carry.	0	1	0	1	0	1	DH			DL			I				M ← (M) + I, skip if carry	Adds the immediate data to the contents of M then stores the result in M. Skips if a carry is generated.	Carry
AIC	M	I	Add I to M with carry.	0	1	0	1	1	0	DH			DL			I				M ← (M) + I + C	Adds the immediate data to the contents of M and C then stores the result in M.	
AICS	M	I	Add I to M with carry and skip if carry.	0	1	0	1	1	1	DH			DL			I				M ← (M) + I + C, skip if carry	Adds the immediate data to the contents of M and C then stores the result in M. Skips if a carry is generated.	Carry
Subtract																						
SU	r	M	Subtract M from r.	0	1	1	0	0	0	DH			DL			Rn				r ← (r) − (M), skip if carry	Subtracts the contents of M from the contents of r then stores the result in r.	
SUS	r	M	Subtract M from r and skip if borrow.	0	1	1	0	0	1	DH			DL			Rn				r ← (r) − (M), skip if borrow	Subtracts the contents of M from the contents of r then stores the result in r. Skips if a borrow is generated.	Borrow
SB	r	M	Subtract M from r with borrow.	0	1	1	0	1	0	DH			DL			Rn				r ← (r) − (M) − b	Subtracts the contents of M from the contents of r with borrow then stores the result in r.	
SBS	r	M	Subtract M from r with borrow and skip if borrow.	0	1	1	0	1	1	DH			DL			Rn				r ← (r) − (M) − b, skip if borrow	Subtracts the contents of M from the contents of r with borrow then stores the result in r. Skips if a borrow is generated.	Borrow
SI	M	I	Subtract I from M.	0	1	1	1	0	0	DH			DL			I				M ← (M) − I	Subtracts the immediate data from the contents of M then stores the result in M.	
SIS	M	I	Subtract I from M and skip if borrow.	0	1	1	1	0	1	DH			DL			I				M ← (M) − I, skip if borrow	Subtracts the immediate data from the contents of M then stores the result in M. Skips if a borrow is generated.	Borrow
SIB	M	I	Subtract I from M with borrow.	0	1	1	1	1	0	DH			DL			I				M ← (M) − I − b	Subtracts the immediate data from the contents of M with borrow, then stores the result in M.	
SIBS	M	I	Subtract I from M with borrow and skip if borrow.	0	1	1	1	1	1	DH			DL			I				M ← (M) − I − b, skip if borrow	Subtracts the immediate data from the contents of M with borrow, then stores the result in M. Skips if a borrow is generated.	Borrow

Mnemonic	Operand		Operation	Instruction format																Notation	Description	Skip condition
	1st	2nd		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0			
Compare																						
SEQ	r	M	Skip if r equals M.	0	0	0	0	0	1	DH		DL				Rn				(r) − (M), skip if zero	Compares the contents of r and M then skips if they are equal.	(r) = (M)
SGE	r	M	Skip if r is greater than or equal to M.	0	0	0	0	1	1	DH		DL				Rn				(r) − (M), skip if (r) ≥ (M)	Compares the contents of r and M then skips if r is greater than or equal to M.	(r) ≥ (M)
SEQI	M	I	Skip if M equals I.	0	0	1	1	0	1	DH		DL				I				(M) − I, skip if zero	Compares the immediate data to the contents of M then skips if they are equal.	(M) − I = 0
SGEI	M	I	Skip if M is greater than or equal to I.	0	0	1	1	1	1	DH		DL				I				(M) − I, skip if (M) ≥ I	Compares the contents of M with the immediate data then skips if M is greater than or equal to I.	(M) ≥ I
Logic																						
AND	M	I	AND I with M.	0	0	1	1	0	0	DH		DL				I				M ← (M) · I	Calculates the logical AND of the immediate data and the contents of M then stores the result in M.	
OR	M	I	OR I with M.	0	0	1	1	1	0	DH		DL				I				M ← (M) + I	Calculates the logical OR of the immediate data and the contents of M then stores the result in M.	
EXL	r	M	Exclusive-OR M with r.	0	0	1	0	0	0	DH		DL				Rn				r ← (r) ⊕ (M)	Calculates the logical Exclusive-OR of the contents of r and the contents of M then stores the result in r.	
Load and store																						
LD	r	M	Load M into r.	1	0	0	0	0	0	DH		DL				Rn				r ← (M)	Moves the contents of M to r.	
ST	M	r	Store r in M.	1	0	0	0	0	1	DH		DL				Rn				M ← (r)	Moves the contents of r to M.	
MVRD	r	M	Move M to M addressed by Rn.	1	0	0	0	1	0	DH		DL				Rn				[DH, Rn] ← (M)	Moves the contents of M to the address referenced by DH and Rn.	
MVRS	M	r	Move M addressed by Rn to M.	1	0	0	0	1	1	DH		DL				Rn				M ← [DH, Rn]	Moves the contents of the memory location referenced by DH and Rn to M.	
MVSR	M_1	M_2	Move M to M.	1	0	0	1	0	0	DH		DL_1				DL_2				[DH,DL_1] ← [DH,DL_2]	Moves the contents of memory location 2 to memory location 1.	
MVI	M	I	Move I to M.	1	0	0	1	0	1	DH		DL				I				M ← I	Moves the immediate data to M.	
PLL	M	r	Load M to PLL registers.	1	0	0	1	1	0	DH		DL				Rn				PLL ← (M)	Moves the contents of M to the PLL registers.	
Bit test																						
TMT	M	N	Test bits of M and skip if true.	1	0	1	0	0	1	DH		DL				N				Skip if M(N) = all 1	Tests the bits of memory location M specified by N. Skips if all bits are logic 1.	All bits specified = 1
TMF	M	N	Test bits of M and skip if false.	1	0	1	0	1	1	DH		DL				N				Skip if M(N) = all 0	Tests the bits of memory location M specified by N. Skips if all bits are logic 0.	All bits specified = 0

Mnemonic	Operand		Operation	Instruction format																Notation	Description	Skip condition
	1st	2nd		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0			
Jump and subroutine																						
JMP	ADDR		Jump to address.	1	0	1	1	ADDR (12 bits)												PC ← ADDR	Jumps to the address specified by ADDR.	
CAL	ADDR		Call subroutine.	1	1	0	0	ADDR (12 bits)												Stack ← (PC) + 1, PC ← ADDR	Jumps to the subroutine specified by ADDR.	
RT			Return from subroutine.	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	PC ← stack	Returns from a subroutine.	
RTI			Return from interrupt.	1	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	PC ← stack	Returns from an interrupt.	
Flag test																						
TTM	N		Test timer flip-flop.	1	1	0	1	0	1	1	0	0	0	0	0	N				Skip if timer F/F = 0	Tests the timer flip-flop and skips if zero.	Timer F/F = 0
TUL	N		Test PLL flip-flop.	1	1	0	1	0	1	1	1	0	0	0	0	N				Skip if PLL F/F = 0	Tests the PLL-unlocked flip-flop and skips if zero.	PLL F/F = 0
Status register test and set																						
SS	N		Set status register bits.	1	1	0	1	1	1	0	0	0	0	0	0	N				(Status register 1) N ← 1	Sets the bits of status register 1 specified by N.	
RS	N		Reset status register bits.	1	1	0	1	1	1	0	1	0	0	0	0	N				(Status register 1) N ← 0	Resets the bits of status register 1 specified by N.	
TST	N		Test status register bits and skip if true.	1	1	0	1	1	1	1	0	0	0	0	0	N				Skip if (status register 2) N = all 1	Tests the bits of status register 2 specified by N. Skips if all bits are 1.	All bits specified = 1
TSF	N		Test status register bits and skip if false.	1	1	0	1	1	1	1	1	0	0	0	0	N				Skip if (status register 2) N = all 0	Tests the bits of status register 2 specified by N. Skips if all bits are 0.	All bits specified = 0
Bank select																						
BANK	B		Select bank.	1	1	0	1	0	0	B		0	0	0	0	0	0	0	0	BANK ← B	Selects one of four memory banks.	
Input/output																						
LCD	M	I	Move data to LCD segments.	1	1	1	0	0	0	DH		DL			DIGIT					LCD (DIGIT) ← I	Loads the immediate data directly to the LCD driver.	
LCP	M	I	Move 7-segment data to LCD.	1	1	1	0	0	1	DH		DL			DIGIT					LCD (DIGIT) ← PLA ← I	Converts the immediate data to 7-segment format using a PLA then transfers it to the LCD driver.	
IN	M	Pn	Move port data to M.	1	1	1	0	1	0	DH		DL			P					M ← (port (Pn))	Moves the data from input port Pn to M.	
OUT	M	Pn	Move data to port.	1	1	1	0	1	1	DH		DL			P					(Port (Pn)) ← M	Moves the contents of memory location M to port Pn.	
SPB	Pn	N	Set port bits.	1	1	1	1	0	0	0	0	P			N					(Port (Pn)) N ← 1	Sets the bits of port Pn specified by N to logic 1.	
RPB	Pn	N	Reset port bits.	1	1	1	1	0	1	0	1	P			N					(Port (Pn)) N ← 0	Sets the bits of port Pn specified by N to logic 0.	

Mnemonic	Operand		Operation	Instruction format																Notation	Description	Skip condition
	1st	2nd		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0			
TPT	Pn	N	Test bits of port and skip if true.	1	1	1	1	1	0	1	0	P				N				Skip if (port (Pn)) N = all 1	Tests the bits of port Pn specified by N. Skips if all bits are logic 1.	All bits specified = 1
TPF	Pn	N	Test bits of port and skip if false.	1	1	1	1	1	1	1	1	P				N				Skip if (port (Pn)) N = all 0	Tests the bits of port Pn specified by N. Skips if all bits are logic 0.	All bits specified = 0
Universal counter																						
UCS	I		Set UCCW1.	0	0	0	0	0	0	0	1	0	0	0	0	I				UCCW1 ← I	Sets the universal counter flag 1.	
UCC	I		Set UCCW2.	0	0	0	0	0	0	1	1	0	0	0	0	I				UCCW2 ← I	Sets the universal counter flag 2.	
Miscellaneous																						
FPC	N		Port F direction control	0	0	0	1	0	0	0	0	0	0	0	0	N				FPC latch ← N	Defines the direction of individual pins of port F. If a bit in the port F direction register is set by FPC, the corresponding pin of port F becomes an output.	
CKSTP			Stop clock.	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	Stop clock if $\overline{HOLD}$ = 0	Stops the processor clock if $\overline{HOLD}$ = 0.	
DAC	I		Move data to DAC registers.	0	0	0	0	0	0	1	0	0	0	0	0	I				DACr ← I	Loads the immediate data to the DAC registers.	
NOP			No operation	0	0	0	0	0	0	0	0	0	0	0	0						No operation	

MASK OPTIONS

Parameter	Options
Watchdog timer (WDT)	Yes
	No
Pull-down resistors on port A (the keypad matrix input port)	Yes
	No
Instruction cycle time	2.67 µs

Parameter	Options
Instruction cycle time	13.33 µs
	40.00 µs
S1 to S28 configuration	LCD driver output port
	General-purpose output port

DEVELOPMENT SYSTEM

The LC7232N development environment is shown in the following figure. It uses an LC72EV32 evaluation chip mounted on a TB-72EV32 target board and a multifunctional emulator (RE32), which is controlled by a personal computer, to provide full debugging facilities.