CMOS LSI

No. 3114A

SANYO

LC66P516

4-bit Microcontroller with Built-in PROM

OVERVIEW

The LC66P516 is a 4-bit microcontroller with a built-in 16 Kbyte PROM. It is compatible with the LC665XX series mask ROM devices, making it ideal for prototyping and software development and testing.
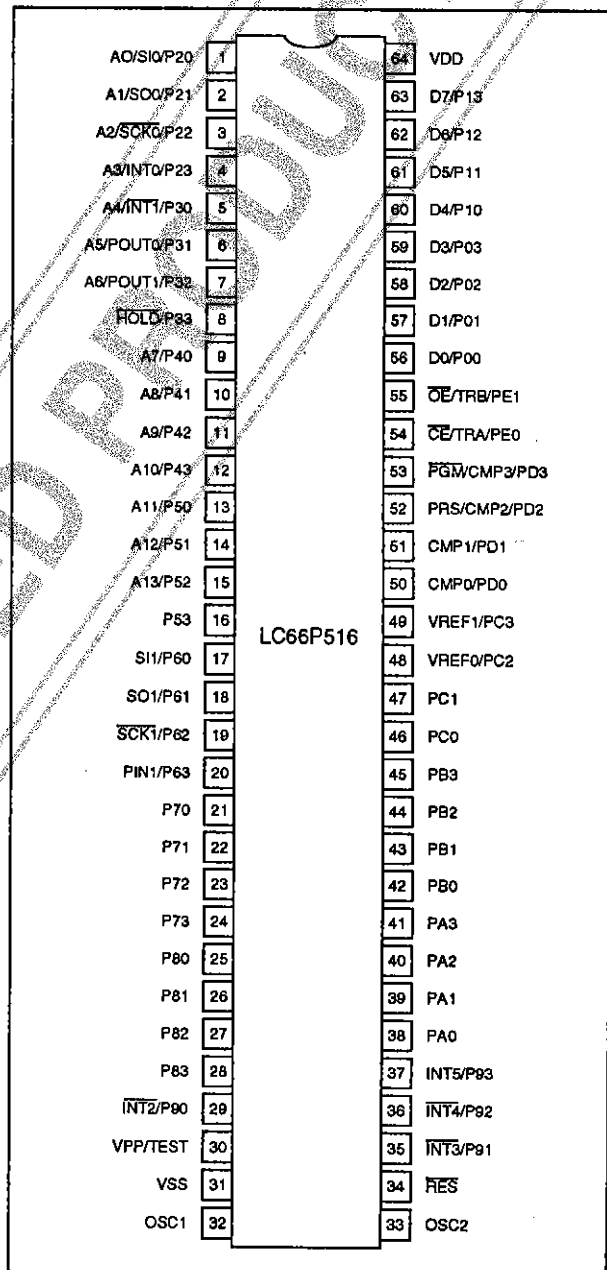
The LC66P516 features 56 user-defined options comprising output configuration, output level after reset, watchdog timer and oscillator configuration options. The output configuration options are open-drain, open-drain with pull-up, and p-channel open-drain with pull-down. The oscillator options are ceramic resonator, RC oscillator and external clock.

The LC66P516 operates from a 5 V supply and is available in 64-pin DIPs and 64-pin QIPs.
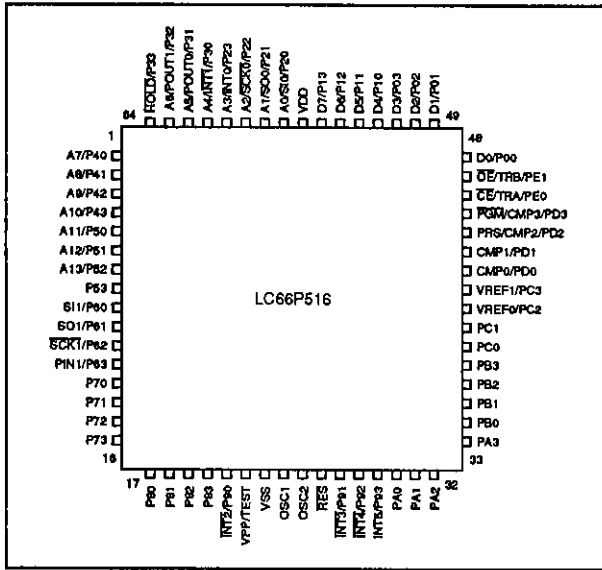
FEATURES

- 56 user-defined options including port output configuration, output level after reset and watchdog timer options
- Ceramic resonator, RC oscillator or external clock option
- 16 Kbyte PROM (0000H to 3FFF user addressable)
- Compatible with the LC665XX series mask ROM devices
- 0.92 to 10.0 μs instruction cycle time
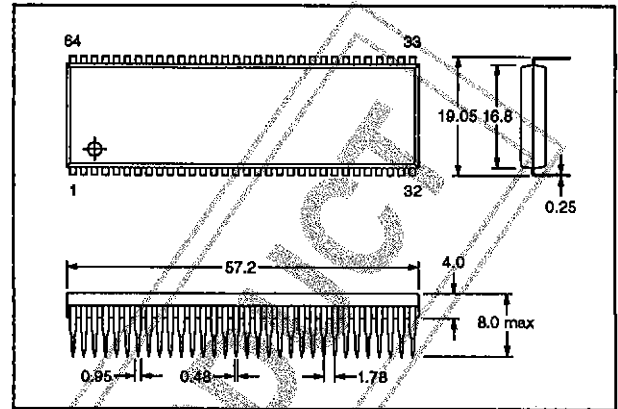- 5 V supply
- 64-pin DIP and 64-pin QIP

PINOUTS

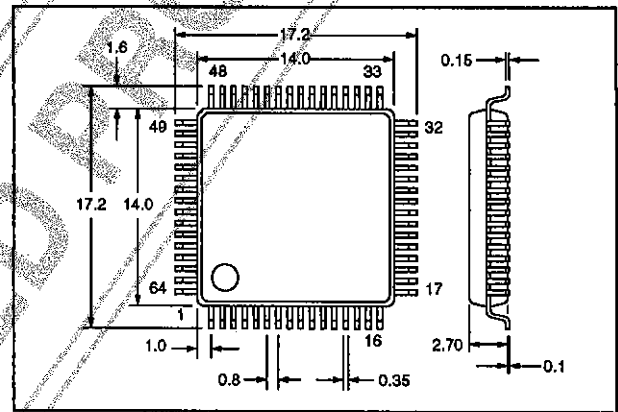| Pin	Name		Pin	Name
1	AO/SIO/P20		64	VDD
2	A1/SOO/P21		63	D7/P13
3	A2/SCKO/P22		62	D6/P12
4	A3/INTO/P23		61	D5/P11
5	A4/INT1/P30		60	D4/P10
6	A5/POUTO/P31		59	D3/P03
7	A6/POUT1/P32		58	D2/P02
8	HOLD/P33		57	D1/P01
9	A7/P40		56	DO/P00
10	A8/P41		55	OE/TRB/PE1
11	A9/P42		54	CE/TRA/PE0
12	A10/P43		53	PGM/CMP3/PD3
13	A11/P50		52	PRS/CMP2/PD2
14	A12/P51		51	CMP1/PD1
15	A13/P52		50	CMP0/PD0
16	P53		49	VREF1/PC3
17	SI1/P60		48	VREF0/PC2
18	SO1/P61		47	PC1
19	SCK1/P62		46	PC0
20	PIN1/P63		45	PB3
21	P70		44	PB2
22	P71		43	PB1
23	P72		42	PB0
24	P73		41	PA3
25	P80		40	PA2
26	P81		39	PA1
27	P82		38	PA0
28	P83		37	INT5/P93
29	INT2/P90		36	INT4/P92
30	VPP/TEST		35	INT3/P91
31	VSS		34	RES
32	OSC1		33	OSC2

LC66P516

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PACKAGE DIMENSIONS

Unit: mm

3071-DIP64S

3159-QIP64E

BLOCK DIAGRAM

RES
TEST
OSC1
OSC2
HOLD

System control

512-byte RAM stack
Flag

C Z

16 Kbyte EPROM

EPROM controller

A0 to A13
D0 to D7
OE
CE
PGM
PRS
VPP

SP | E M R | D P P H | D P X Y

E | A

ALU

PC

TRA/PE0 — PE
TRB/PE1
CMP0/PD0 — PD
CMP1/PD1
CMP2/PD2
CMP3/PD3
VREF0/PC2 — PC
VREF1/PC3
PC0, PC1
PB0 to PB3 — PB
PA0 to PA3 — PA

Prescaler
Multiplexer
Timer 0
Serial input/output port 0

POUT0
SIO
SO0
SCK0
INT0

Multiplexer

INT1 to INT4, INT5

Interrupt control
Multiplexer
Timer 1
Serial input/output port 1

SI1
SO1
SCK1
PIN1, POUT1

P0 | P1 | P2 | P3 | P4 | P5 | P6 | P7 | P8 | P9

P00 to P03 | P10 to P13 | P20 to P23 | P30 to P33 | P40 to P43 | P50 to P53 | P60 to P63 | P70 to P73 | P80 to P83 | P90 to P93

PIN DESCRIPTION

Number		Name	Description
DIP64S	QIP64E		
1	57	A0/SIO/P20	Multiplexed 4-bit input/output port P2 (P20 to P23), serial input 0 (SIO), serial output 0 (SO0), serial clock 0 (SCK0), interrupt request 0 (INT0) and PROM address bus lines (A0 to A3)
2	58	A1/SO0/P21	
3	59	A2/SCK0/P22	
4	60	A3/INT0/P23	
5	61	A4/INT1/P30	Multiplexed 4-bit input/output port P3 (P30 to P33), interrupt request 1 (INT1), timer outputs (POUT0 and POUT1), hold-mode control input (HOLD) and PROM address bus lines (A4 to A6)
6	62	A5/POUT0/P31	
7	63	A6/POUT1/P32	
8	64	HOLD/P33	
9	1	A7/P40	Multiplexed 4-bit input/output port P4 (P40 to P43) and PROM address bus lines (A7 to A10)
10	2	A8/P41	
11	3	A9/P42	
12	4	A10/P43	
13	5	A11/P50	Multiplexed 4-bit input/output port P5 (P50 to P53) and PROM address bus lines (A11 to A13)
14	6	A12/P51	
15	7	A13/P52	
16	8	P53	

Number		Name	Description
DIP64S	QIP64E		
17	9	SI1/P60	Multiplexed 4-bit input/output port P6 (P60 to P63), serial input 1 (SI1), serial output 1 (SO1), serial clock 1 (SCK1) and event counter input (PIN1)
18	10	SO1/P61	
19	11	$\overline{SCK1}$/P62	
20	12	PIN1/P63	
21	13	P70	4-bit output port P7 (P70 to P73)
22	14	P71	
23	15	P72	
24	16	P73	
25	17	P80	4-bit output port P8 (P80 to P83)
26	18	P81	
27	19	P82	
28	20	P83	
29	21	$\overline{INT2}$/P90	Multiplexed 4-bit input/output port P9 (P90 to P93) and interrupt requests ($\overline{INT2}$ to $\overline{INT4}$ and INT5)
35	27	$\overline{INT3}$/P91	
36	28	$\overline{INT4}$/P92	
37	29	INT5/P93	
30	22	VPP/TEST	CPU test input
31	23	VSS	Ground
32	24	OSC1	External oscillator connections
33	25	OSC2	
34	26	$\overline{RES}$	Reset input
38	30	PA0	4-bit output port PA (PA0 to PA3)
39	31	PA1	
40	32	PA2	
41	33	PA3	
42	34	PB0	4-bit output port PB (PB0 to PB3)
43	35	PB1	
44	36	PB2	
45	37	PB3	
46	38	PC0	Multiplexed 4-bit input/output port PC (PC0 to PC3), comparator 0 reference voltage input (VREF0) and comparators 1, 2 and 3 reference voltage input (VREF1)
47	39	PC1	
48	40	VREF0/PC2	
49	41	VREF1/PC3	
50	42	CMP0/PD0	Multiplexed 4-bit input port PD (PD0 to PD3), comparator inputs (CMP0 to CMP3) and PROM program control inputs (PRS and $\overline{PGM}$).
51	43	CMP1/PD1	
52	44	PRS/CMP2/PD2	
53	45	$\overline{PGM}$/CMP3/PD3	

Number		Name	Description
DIP64S	QIP64E		
54	46	CE/TRA/PE0	Multiplexed 2-bit input port PE (PE0 to PE1), ternary inputs (TRA and TRB), PROM chip enable (CE) and output enable (OE)
55	47	OE/TRB/PE1	
56	48	D0/P00	Multiplexed 4-bit input/output port P0 (P00 to P03) and PROM data bus lines (D0 to D3)
57	49	D1/P01	
58	50	D2/P02	
59	51	D3/P03	
60	52	D4/P10	Multiplexed 4-bit input/output port P1 (P10 to P13) and PROM data bus lines (D4 to D7)
61	53	D5/P11	
62	54	D6/P12	
63	55	D7/P13	
64	56	VDD	5 V supply

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	−0.3 to 7.0	V
Ports P2, P3 (excluding P33) and P6 input voltage range. See note 1.	V_{I1}	−0.3 to 15.0	V
Input voltage range for all inputs. See note 2.	V_{I2}	−0.2 to V_{DD} + 0.3	V
Ports P2, P3 (excluding P33), P6, P7 and PA output voltage range. See note 1.	V_{O1}	−0.3 to 15.0	V
Output voltage range for all outputs. See note 2.	V_{O2}	−0.3 to V_{DD} + 0.3	V
Ports P0 to P6 (excluding P33), P8, P9 and PC output sink current	I_{ON1}	4	mA
Ports P7, PA and PB output sink current	I_{ON2}	20	mA
Ports P0, P1, P4, P5, P7, PA and PB output source current	$-I_{OP1}$	2	mA
Ports P2, P3 (excluding P33), P6, P8, P9 and PC output source current	$-I_{OP2}$	4	mA
Ports P2 to P8 (excluding P33) total sink current	ΣI_{ON1}	75	mA
Ports P0, P1 and P9 to PC total sink current	ΣI_{ON2}	75	mA
Ports P2 to P8 (excluding P33) total source current	$-\Sigma I_{OP1}$	25	mA
Ports P0, P1 and P9 to PC total source current	$-\Sigma I_{OP2}$	25	mA
Power dissipation (DIP64S)	P_{D1}	600	mW
Power dissipation (QIP64E)	P_{D2}	430	mW
Operating temperature range	T_{opr}	−30 to 70	°C
Storage temperature range	T_{stg}	−55 to 125	°C

Notes

1. Open-drain output configuration option
2. All output configuration options
3. Heat-soak the QIP package before mounting. Do not immerse the package in the solder dip tank when mounting the QIP on the substrate, and avoid prolonged contact with the solder.

Recommended Operating Conditions

$T_a = 25 \; °C$, $V_{SS} = 0 \; V$

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	5	V
Supply voltage range	V_{DD}	4.5 to 5.5	V
Hold-mode supply voltage range for data retention	V_{DD}	1.8 to 5.5	V

Electrical Characteristics

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = −30 to 70 °C unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply current	I_{DD}	4 MHz ceramic resonator	–	4.5	8.0	mA
		4 MHz external clock	–	6.5	11.0	
		RC oscillator	–	4.0	8.0	
Halt-mode supply current	I_{DDHT}	4 MHz ceramic resonator	–	3.0	5.0	mA
		4 MHz external clock	–	3.5	6.0	
		RC oscillator	–	3.0	5.0	
Hold-mode supply current	I_{DDHD}	V_{DD} = 1.8 to 5.5 V	–	0.01	10.0	μA
Ports P2, P3 (excluding P33), P6 and P9, $\overline{RES}$ and OSC1 LOW-level input voltage	V_{IL1}	Output n-channel transistor OFF. See note 1.	V_{SS}	–	$0.25V_{DD}$	V
$\overline{HOLD}$/P33 LOW-level input voltage	V_{IL2}	V_{DD} = 1.8 to 5.5 V	V_{SS}	–	$0.25V_{DD}$	V
Ports P0, P1, P4, P5, PC, PD and PE, and TEST LOW-level input voltage	V_{IL3}	Output n-channel transistor OFF. See note 1.	V_{SS}	–	$0.3V_{DD}$	V
Port PE LOW-level input voltage	V_{IL4}	Ternary input levels	V_{SS}	–	$0.2V_{DD}$	V
Port PE MID-level input voltage	V_{IM}	Ternary input levels	$0.4V_{DD}$	–	$0.6V_{DD}$	V
Ports P2, P3 (excluding P33) and P6 HIGH-level input voltage	V_{IH1}	Output n-channel transistor OFF. See notes 1 and 2.	$0.75V_{DD}$	–	13.5	V
$\overline{HOLD}$/P33, P9, $\overline{RES}$ and OSC1 HIGH-level input voltage	V_{IH2}	Output n-channel transistor OFF. See note 1.	$0.75V_{DD}$	–	V_{DD}	V
Ports P0, P1, P4, P5, PC, PD and PE HIGH-level input voltage	V_{IH3}	Output n-channel transistor OFF. See note 1.	$0.7V_{DD}$	–	V_{DD}	V
Port PE HIGH-level input voltage	V_{IH4}	Ternary input levels	$0.8V_{DD}$	–	V_{DD}	V
Ports P0 to P6 (excluding P33), P8 (CMOS), P9 and PC LOW-level output voltage	V_{OL1}	I_{OL} = 1.6 mA	–	–	0.4	V
Ports P7, PA and PB LOW-level output voltage	V_{OL2}	I_{OL} = 10 mA	–	–	1.5	V
Ports P2, P3 (excluding P33), P6, P8, P9 and PC HIGH-level output voltage	V_{OH1}	I_{OH} = −1 mA. See note 3.	V_{DD} − 1.0	–	–	V
		I_{OH} = −0.1 mA. See note 3.	V_{DD} − 0.5	–	–	
Ports P0, P1, P4, P5, P7, PA and PB HIGH-level output voltage	V_{OH2}	I_{OH} = −200 μA. V_{DD} = 4.5 V. See note 4.	2.4	–	–	V
		I_{OH} = −130 μA. See note 4.	V_{DD} − 1.35	–	–	

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Ports PD, PC2 and PC3 comparator input voltage range	V_{CMM}		1.0	–	$V_{DD} - 1.5$	V
Port PD comparator offset voltage	V_{OFF}	$V_I = 1.0$ to $V_{DD} - 1.5$ V	–	±50	±300	mV
Ports P2, P3, P6 and P9, and $\overline{RES}$ and OSC1 Schmitt-trigger LOW-level threshold voltage	V_{IL}		$0.25V_{DD}$	–	$0.5V_{DD}$	V
Ports P2, P3, P6 and P9, and $\overline{RES}$ and OSC1 Schmitt-trigger HIGH-level threshold voltage	V_{IH}		$0.5V_{DD}$	–	$0.75V_{DD}$	V
Ports P2, P3, P6 and P9, $\overline{RES}$ and OSC1 Schmitt-trigger hysteresis voltage	V_{HYS}		–	$0.1V_{DD}$	–	V
Ports PC2, PC3, PD and PE LOW-level input current	I_{IL1}	$V_I = V_{SS}$, output n-channel transistor OFF. See note 2.	–1.0	–	–	μA
LOW-level input current for all other inputs	I_{IL2}	$V_I = V_{SS}$, output n-channel transistor OFF. See note 2.	–1.0	–	–	μA
Ports P2, P3 (excluding P33) and P6 HIGH-level input current	I_{IH1}	$V_I = 13.5$ V, output n-channel transistor OFF. See notes 1 and 2.	–	–	5.0	μA
Ports P0, P1, P33, P4, P5, P9, PC (excluding PC2 and PC3), $\overline{RES}$ and OSC1 HIGH-level input current	I_{IH2}	$V_I = V_{DD}$, output n-channel transistor OFF. See notes 1 and 2.	–	–	1.0	μA
Ports PC2, PC3, PD and PE HIGH-level input current	I_{IH3}	$V_I = V_{DD}$, output n-channel transistor OFF. See notes 1 and 2.	–	–	1.0	μA
Ports P2, P3, P6, P7 and PA output leakage current	I_{OFF1}	$V_I = 13.5$ V, output n-channel transistor OFF. See note 2.	–	–	5.0	μA
Ports P0, P1, P4, P5, P9, PB and PC output leakage current	I_{OFF2}	$V_I = V_{DD}$, output n-channel transistor OFF. See note 2.	–	–	1.0	μA
Port P8 output leakage current	I_{OFF3}	$V_I = V_{SS}$, output p-channel transistor OFF. See note 2.	–1.0	–	–	μA
Ports P0, P1, P4, P5, P7, PA and PB output current with pull-up option	I_{PO}	$V_I = V_{SS}$, $V_{DD} = 5.5$ V, output n-channel transistor OFF. See note 4.	–1.6	–	–	mA
Ceramic resonator input frequency	f_{CF}	4 MHz resonator	–	4.0	–	MHz
Ceramic resonator input stabilization time	t_{CFS}	4 MHz resonator	–	–	10	ms
RC oscillator input frequency	f_{ext}	$R_{ext} = 2.2$ kΩ ±1%, $C_{ext} = 100$ pF ±5%	2	3	4	MHz
External RC oscillator capacitance	C_{ext}		–	100	–	pF
External RC oscillator resistance	R_{ext}		–	2.2	–	kΩ

Notes

1. Ports with CMOS output configuration option cannot be used as input ports.
2. Open-drain output configuration option
3. CMOS output configuration option
4. Pull-up output configuration option

## Timing Characteristics

Serial input/output timing
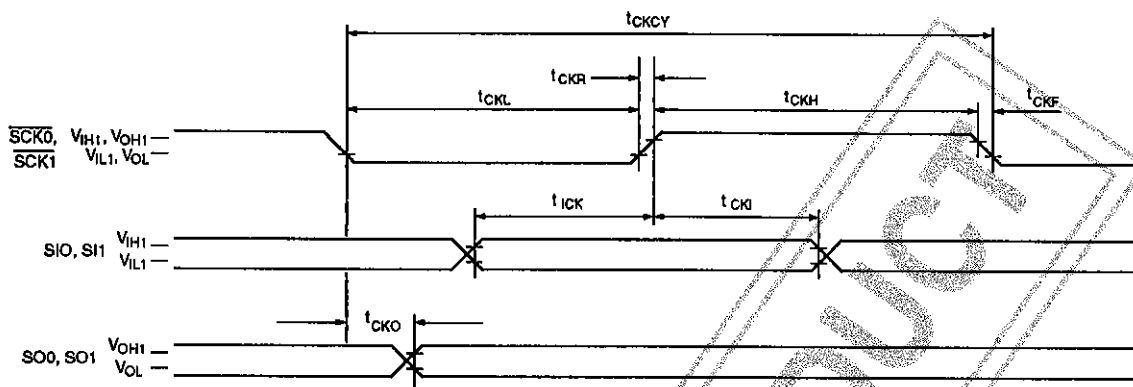
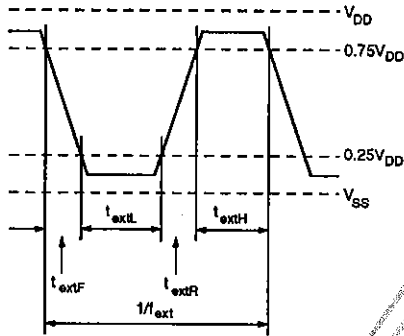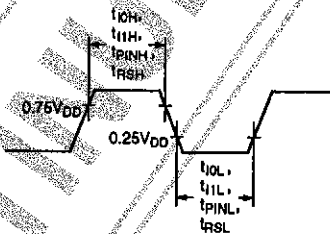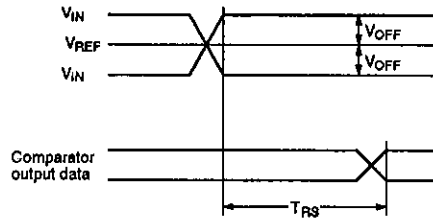V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = −30 to 70 °C

Parameter	Symbol	Rating			Unit
		min	typ	max	
Instruction cycle time	t_{CYC}	0.92	–	10	μs
$\overline{SCK0}$ and $\overline{SCK1}$ serial clock input cycle time	t_{CKCY}	0.9	–	–	μs
$\overline{SCK0}$ and $\overline{SCK1}$ serial clock output cycle time	t_{OCY}	$2t_{CYC}$	–	–	μs
$\overline{SCK0}$ and $\overline{SCK1}$ serial clock input pulsewidth	t_{CKL}	0.4	–	–	μs
$\overline{SCK0}$ and $\overline{SCK1}$ serial clock output pulsewidth	t_{CKH}	t_{CYC}	–	–	μs
$\overline{SCK0}$ and $\overline{SCK1}$ serial clock output rise time	t_{CKR}	–	–	0.1	μs
$\overline{SCK0}$ and $\overline{SCK1}$ serial clock output fall time	t_{CKF}	–	–	0.1	μs
SI0 and SI1 serial data setup time	t_{ICK}	0.3	–	–	μs
SI0 and SI1 serial data hold time	t_{CKI}	0.3	–	–	μs
SO0 and SO1 serial data output delay	t_{CKO}	–	–	0.3	μs

Note

Each test input and output has an RC load as shown in the following figure.
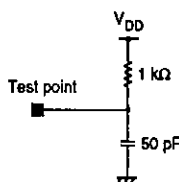
External clock timing

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –30 to 70 °C

Parameter	Symbol	Rating			Unit
		min	typ	max	
OSC1 external clock input frequency	f_{ext}	0.4	–	4.35	MHz
OSC1 external clock LOW-level input pulsewidth	t_{extL}	70	–	–	ns
OSC1 external clock HIGH-level input pulsewidth	t_{extH}	70	–	–	ns
OSC1 external clock input rise time	t_{extR}	–	–	30	ns
OSC1 external clock input fall time	t_{extF}	–	–	30	ns

Interrupt and reset timing

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –30 to 70 °C

Parameter	Symbol	Rating			Unit
		min	typ	max	
INT0 LOW-level pulsewidth	t_{I0L}	$2t_{CYC}$	–	–	μs
INT0 HIGH-level pulsewidth	t_{I0H}	$2t_{CYC}$	–	–	μs
INT1 to INT4 and INT5 LOW-level pulsewidth	t_{I1L}	$2t_{CYC}$	–	–	μs
INT1 to INT4 and INT5 HIGH-level pulsewidth	t_{I1H}	$2t_{CYC}$	–	–	μs
PIN1 LOW-level input pulsewidth	t_{PINL}	$2t_{CYC}$	–	–	μs
PIN1 HIGH-level input pulsewidth	t_{PINH}	$2t_{CYC}$	–	–	μs
RES LOW-level input pulsewidth	t_{RSL}	$3t_{CYC}$	–	–	μs
RES HIGH-level input pulsewidth	t_{RSH}	$3t_{CYC}$	–	–	μs

Comparator output timing

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = −30 to 70 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Port PD comparator response time	t_{RS}		–	–	30	ms

INPUT AND OUTPUT FUNCTIONS

The LC66P516 has many multiplexed pins whose function is controlled by software. The function of each of these pins is shown in the following table.

Table 1. Pin functions

Name	Function
D0/P00	Ports P00 to P03 can be addressed as either a 4-bit port or four, single-bit ports. They function as data bus lines when memory is addressed. They also have halt-mode control functions. Level after reset is set by user option.
D1/P01	
D2/P02	
D3/P03	
D4/P10	Ports P10 to P13 can be addressed as either a 4-bit port or four, single-bit ports. They function as data bus lines when memory is addressed. Level after reset is set by user option.
D5/P11	
D6/P12	
D7/P13	
A0/SI0/P20	Ports P20 to P23 can be addressed as either a 4-bit port or four, single-bit ports. They function as address bus inputs when memory is addressed. Port P20 also functions as a serial data input, P21 as a serial data output, P22 as a serial data clock and P23 as an interrupt request, pulsewidth measurement and event counter input using timer 0.
A1/SO0/P21	
A2/SCK0/P22	
A3/INT0/P23	
A4/INT1/P30	Ports P30 to P32 can be addressed as either a 3-bit port, a 4-bit port with P33 or three, single-bit ports. They function as address bus inputs when memory is addressed. Port P30 also functions as an interrupt request input, P31 as a square-wave output from timer 0, and P32 as a square-wave output and a PWM output from timer 1.
A5/POUT0/P31	
A6/POUT1/P32	
HOLD/P33	Port P33 can be addressed as either a 4-bit port with P30 to P32 or a single-bit port. It functions as the hold-mode control input when P33 is LOW and the HOLD instruction is executed. The CPU restarts when P33 goes HIGH again. Reset signals are ignored whenever HOLD/P33 is LOW, including when not in hold mode.
A7/P40	Ports P40 to P43 can be addressed as either a 4-bit port, four, single-bit ports or an 8-bit port with P50 to P53. They function as address bus inputs when memory is addressed.
A8/P41	
A9/P42	
A10/P43	

Table 1. Pin functions—continued

Name	Function
A11/P50	Ports P50 to P53 can be addressed as either a 4-bit port, four, single-bit ports or an 8-bit port with P40 to P43. Ports P50 to P52 function as address bus inputs when memory is addressed.
A12/P51	
A13/P52	
P53	
SI1/P60	Ports P60 to P63 can be addressed as either a 4-bit port or four, single-bit ports. Port P60 also functions as a serial data input, P61 as a serial data output, P62 as a serial data clock and P63 as the timer 1 event counter input.
SO1/P61	
$\overline{SCK1}$/P62	
PIN1/P63	
P70	Ports P70 to P73 can be addressed as either a 4-bit port or four, single-bit ports. Input instructions read the contents of the output latch.
P71	
P72	
P73	
P80	Ports P80 to P83 can be addressed as either a 4-bit port or four, single-bit ports. Input instructions read the contents of the output latch. Note that the open-drain option for P8 is p-channel.
P81	
P82	
P83	
$\overline{INT2}$/P90	Ports P90 to P93 can be addressed as either a 4-bit port or four, single-bit ports. P90 also functions as interrupt request 2, P91 as interrupt request 3, P92 as interrupt request 4 and P93 as interrupt request 5.
$\overline{INT3}$/P91	
$\overline{INT4}$/P92	
INT5/P93	
PA0	Ports PA0 to PA3 can be addressed as either a 4-bit port or four, single-bit ports. Input instructions read the contents of the output latch.
PA1	
PA2	
PA3	
PB0	Ports PB0 to PB3 can be addressed as either a 4-bit port or four, single-bit ports. Input instructions read the contents of the output latch.
PB1	
PB2	
PB3	
PC0	Ports PC0 to PC3 can be addressed as either a 4-bit port or four, single-bit ports. Port PC2 also functions as the reference voltage input for comparator 0, and PC3, as the reference voltage input for comparators 1, 2 and 3.
PC1	
VREF0/PC2	
VREF1/PC3	
CMP0/PD0	Ports PD0 to PD3 can be addressed as either a 4-bit port or four, single-bit ports. They also function as comparator inputs. Port PD3 also functions as the memory program control input, and PD2 as PRS (program mode select).
CMP1/PD1	
PRS/CMP2/PD2	
$\overline{PGM}$/CMP3/PD3	
TRA/PE0	Ports PE0 to PE1 can be addressed as either a 2-bit port or two, single-bit ports. They also function as ternary-level inputs. They also function as chip enable and write enable respectively, when memory is addressed.
TRB/PE1	

Table 1. Pin functions—continued

Name	Function
OSC1	OSC1 and OSC2 function as the external ceramic resonator or RC oscillator connections. When an external clock is used, OSC2 is left open.
OSC2	
$\overline{\text{RES}}$	When $\overline{\text{RES}}$ goes LOW while $\overline{\text{HOLD}}$/P33 is HIGH, the CPU is reset.
VPP/TEST	CPU test input. Normally connected to ground

USER OPTIONS

Oscillator Options

There are three user options for the oscillator—an external clock, an RC oscillator and a ceramic resonator. The internal circuits of OSC1 and OSC2 for the external clock, RC oscillator and ceramic resonator options are shown in figures 1, 2 and 3, respectively. Note the Schmitt-trigger inputs for both the external clock and RC oscillator options.

Figure 1. External clock option
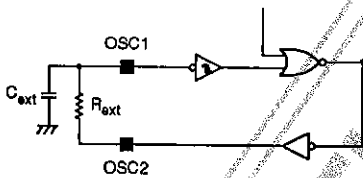
Figure 2. RC oscillator option
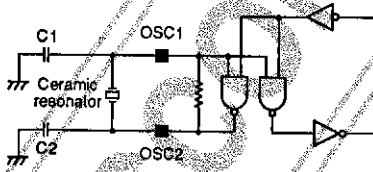
Figure 3. Ceramic resonator option

Output Options

There are two user options for the output configuration of each port. The options for all ports, excluding P8, PD and PE, are shown in figures 4 and 6, and for P8, in figures 5 and 7. Ports P2, P3, P6 and P9 have Schmitt-trigger inputs in both output configurations.
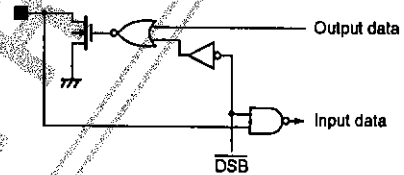
Figure 4. N-channel open-drain option for all ports except P8
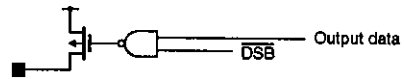
Figure 5. P-channel open-drain option for port P8

The p-channel pull-up option for ports P0, P1, P4, P5, P7, PA and PB results in an n-channel sink transistor with a p-channel, active pull-up transistor configuration, and for ports P2, P3, P6 and PC, a CMOS configuration.
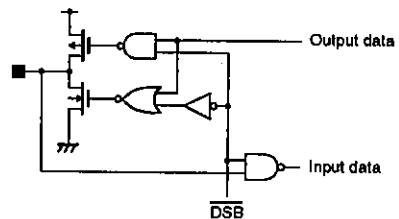
Figure 6. P-channel pull-up option for all ports except P8, PD and PE
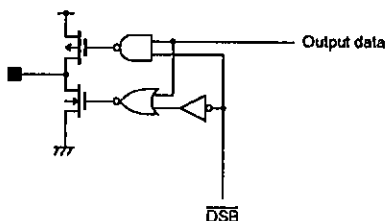
Figure 7. N-channel pull-down option for port P8

Port PD comparator input and port PE ternary input modes are selected by the user program.

PROM SPECIFICATION

Specifying Programs and Options

The user-addressable memory is 0000H to 3FFFH. Addresses 0000H to 3FF7H are for user programs, and addresses 3FF8H to 3FFFH, for option specification.

Note that the n-channel open-drain outputs for ports P2, P3, P6, P7 and PA have a maximum withstand voltage of 15 V.

Output Level After Reset Option

The output level of ports P0, P1 and P8 after a CPU reset is user selectable.

Watchdog Timer Option

A watchdog timer is available to prevent program runaway.

The option specification is coded using the information shown in the following table.

Address	Data bit	Parameter	Option	
			0	1
3FF8H	D0	Watchdog timer function	No	Yes
	D1	Port P0 level after reset	LOW	HIGH
	D2	Port P1 level after reset	LOW	HIGH
	D3	Port P8 level after reset	LOW	HIGH
	D4	Oscillator	RC oscillator or external clock	Ceramic resonator
	D5 to D7	No function	Set to 0	
3FF9H	D0	Port P00 output configuration	Open-drain	Pull-up
	D1	Port P01 output configuration		
	D2	Port P02 output configuration		
	D3	Port P03 output configuration		
	D4	Port P10 output configuration	Open-drain	Pull-up
	D5	Port P11 output configuration		
	D6	Port P12 output configuration		
	D7	Port P13 output configuration		
3FFAH	D0	Port P20 output configuration	Open-drain	CMOS
	D1	Port P21 output configuration		
	D2	Port P22 output configuration		
	D3	Port P23 output configuration		
	D4	Port P30 output configuration	Open-drain	CMOS
	D5	Port P31 output configuration		
	D6	Port P32 output configuration		
	D7	No function	Set to 0	

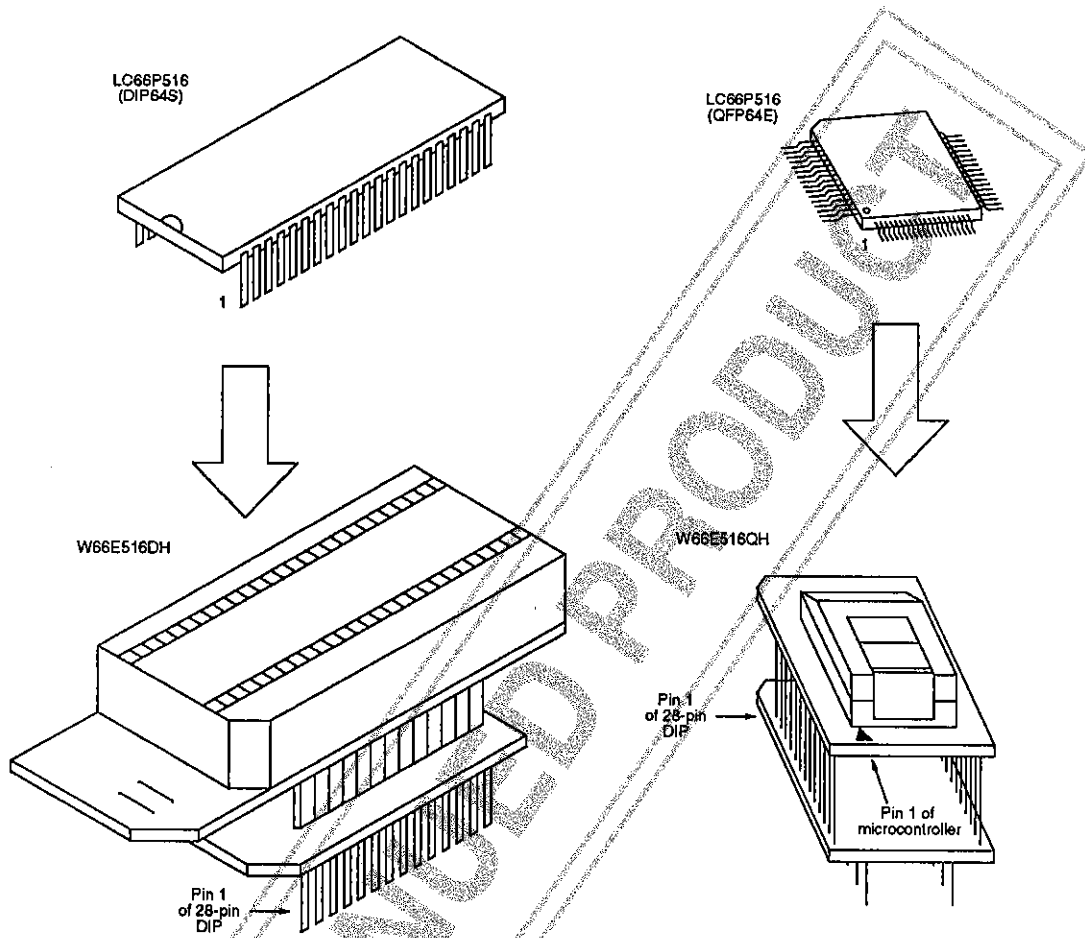| Address	Data bit	Parameter	Option	
			0	1
3FFBH	D0	Port P40 output configuration	Open-drain	Pull-up
	D1	Port P41 output configuration		
	D2	Port P42 output configuration		
	D3	Port P43 output configuration		
	D4	Port P50 output configuration	Open-drain	Pull-up
	D5	Port P51 output configuration		
	D6	Port P52 output configuration		
	D7	Port P53 output configuration		
3FFCH	D0	Port P60 output configuration	Open-drain	CMOS
	D1	Port P61 output configuration		
	D2	Port P62 output configuration		
	D3	Port P63 output configuration		
	D4	Port P70 output configuration	Open-drain	Pull-up
	D5	Port P71 output configuration		
	D6	Port P72 output configuration		
	D7	Port P73 output configuration		
3FFDH	D0	Port P80 output configuration	Open-drain	Pull-down
	D1	Port P81 output configuration		
	D2	Port P82 output configuration		
	D3	Port P83 output configuration		
	D4	Port P90 output configuration	Open-drain	CMOS
	D5	Port P91 output configuration		
	D6	Port P92 output configuration		
	D7	Port P93 output configuration		
3FFEH	D0	Port PA0 output configuration	Open-drain	Pull-up
	D1	Port PA1 output configuration		
	D2	Port PA2 output configuration		
	D3	Port PA3 output configuration		
	D4	Port PB0 output configuration	Open-drain	Pull-up
	D5	Port PB1 output configuration		
	D6	Port PB2 output configuration		
	D7	Port PB3 output configuration		
3FFFH	D0	Port PC0 output configuration	Open-drain	CMOS
	D1	Port PC1 output configuration		
	D2	Port PC2 output configuration		
	D3	Port PC3 output configuration		
	D4 to D7	No function	Set to 0	

The assembler execute command when specifying programs and options using a Sanyo cross assembler is LC66S.EXE. Cross-assemble the programs for an LC66516 target CPU.

PROM Programming

The PROM can be programmed using a special adapter board, W66E516DH for the 64-pin DIP and W66E516QH for the 64-pin QIP as shown in the following figure, and a universal EPROM programmer.

LC66P516
(DIP64S)

1

W66E516DH

Pin 1
of 28-pin
DIP

LC66P516
(QFP64E)

1

W66E516QH

Pin 1
of 28-pin
DIP

Pin 1 of
microcontroller

Program the PROM using the M mode of the PV command of the EVA800 or EVA850. The EPROM programmer should be Intel 27128 compatible with V_{PP} = 21 V. The recommended programmers are shown in the following table. Please contact your nearest Sanyo representative if you intend to use an alternative EPROM programmer.

Note

The PV command is the EVA800/850 programmer mode command.

Manufacturer	Model
ADVANTEST	TR4943, R4944A, R4945 or equivalent
Sanyo	EVA850 or EVA800 special-purpose programmers

Notes

1. Intel is a registered trademark of Intel Corporation.
2. ADVANTEST is a registered trademark of ADVANTEST Corporation.

APPLICATION NOTES

Reset Timing

The reset signal on $\overline{\text{RES}}$ should be held LOW for a minimum of three instruction cycles after the oscillator has stabilized to ensure correct operation, as shown in the following figure.
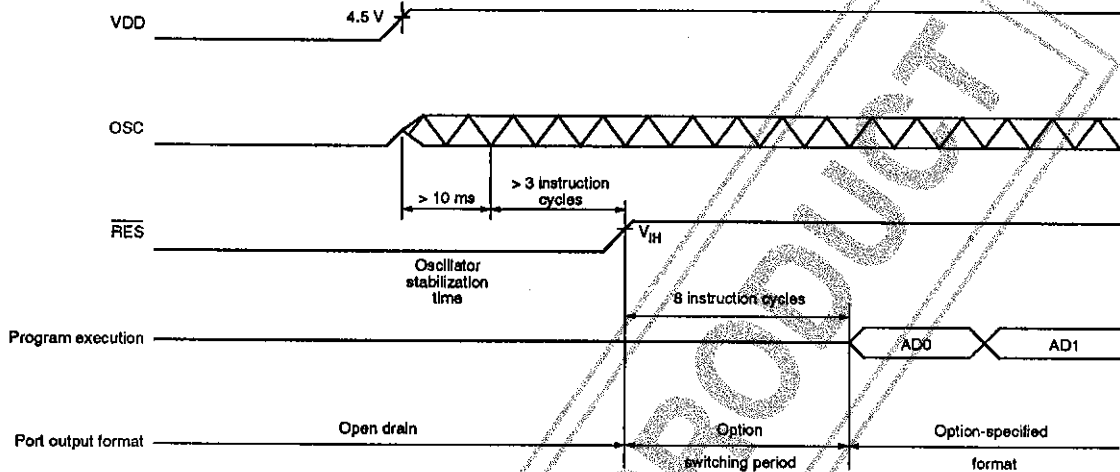
After a reset occurs, all I/O ports are reset to open-drain output configuration with floating outputs, except for ports P0 and P1 which both have an output level after reset option. The output configuration of each port is then set using the specified options during the eight instruction cycles after $\overline{\text{RES}}$ goes HIGH. Program execution then begins from address 0000H.

The LC66E516/P516 can be reset while in hold mode ($\overline{\text{HOLD}}$/P33 is LOW). When $\overline{\text{RES}}$ goes LOW in hold mode, $\overline{\text{HOLD}}$/P33 must go HIGH before $\overline{\text{RES}}$ goes HIGH again.

Reference Clock

The external circuit for a ceramic resonator is shown in figure 8, and the recommended resonator and component values, in the following table. The oscillator stabilization characteristics are shown in figure 9.
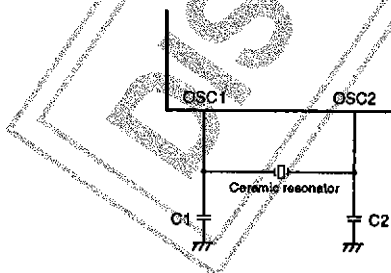
Figure 8. Ceramic resonator

| Ceramic resonator	Capacitance	
	C1	C2
4 MHz Murata CSA-4.00MG	33 pF ±10%	33 pF ±10%
4 MHz Kyocera KBR-4.0MS	33 pF ±10%	33 pF ±10%
4 MHz Murata CST-4.00MG with internal capacitor	N/A	N/A
4 MHz Kyocera KBR-4.0MES with internal capacitor	N/A	N/A
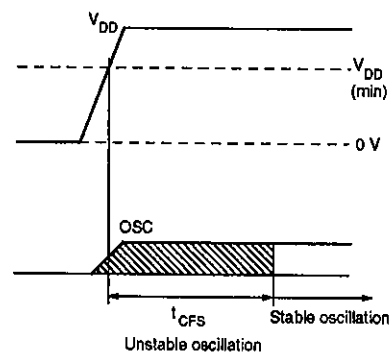
Figure 9. Ceramic resonator stabilization time

The external circuit for an RC oscillator is shown in the following figure.
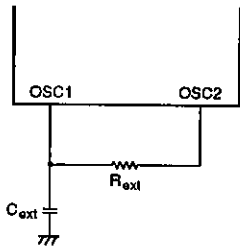
The external clock input connection is OSC1. The remaining oscillator connection, OSC2, should be left open as shown in the following figure.
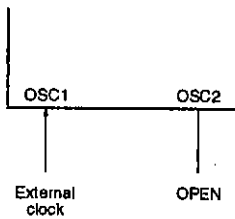

The RC oscillator frequency is determined by the external resistor and capacitor and has only been specified for $R_{ext} = 2.2$ kΩ and $C_{ext} = 100$ pF. The frequency for other values of R_{ext} and C_{ext} can be determined from the graph in the following figure.
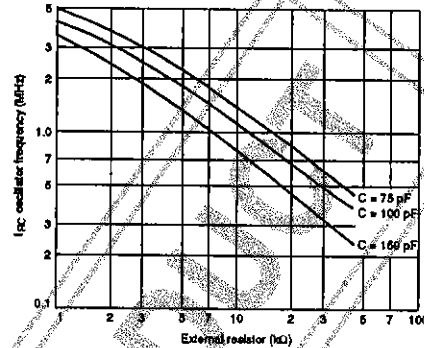
Preparation Procedure

The preparation procedures shown in the following figure for DIP and QIP packages should always be followed prior to mounting the packages on the substrate. Note that the QIP package should be heat-soaked for 24 hours at 125 °C immediately prior to mounting.
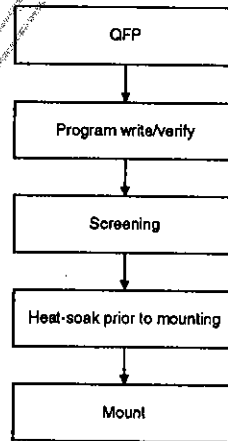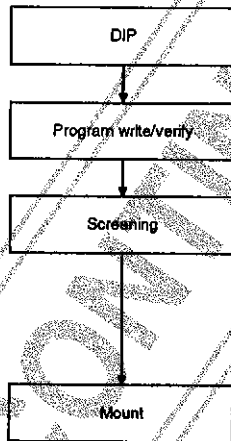
Screening procedure

The construction of the microcontroller with a blank built-in PROM makes it impossible for Sanyo to completely factory-test it before shipping. To prove reliability of the programmed devices, the screening procedure shown in the following figure should always be followed.
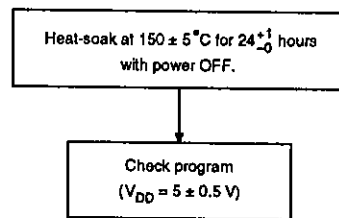
Note that it is not possible to perform a write test on the blank PROM. 100% yield, therefore, cannot be guaranteed.

ORDERING INFORMATION

When ordering identical mask ROM and PROM devices simultaneously, provide an EPROM containing the target memory contents together with separate order forms for each of the mask ROM and PROM versions.

When ordering a PROM device, provide an EPROM containing the target memory contents together with an order form.

When ordering either an LC66506/556 6 Kbyte, LC66508/558 8 Kbyte or LC66512/562 12 Kbyte mask

ROM device, insert a jump command, or any similar command, to avoid executing an address beyond the range of the target device. In addition, write a 0 into all locations above 3FFFH.

A comparison of the LC66516 characteristics with those of the LC665XX mask ROM devices is shown in the following table.

Parameter	Symbol	Condition	LC66P516	LC665XX series		Unit
				LC6650X series	LC6655X series	
Supply voltage range	V_{DD}	t_{CYC} = 0.92 to 10 μs	4.5 to 5.5	4.0 to 6.0	–	V
		t_{CYC} = 3.92 to 10 μs	–	–	2.2 to 5.5	
		t_{CYC} = 1.96 to 10 μs	–	–	3.0 to 5.5	
Maximum halt-mode supply current	I_{DDHT}	4 MHz ceramic resonator	6.0	2.5	2.5	mA
		4 MHz external clock	6.0	3.5	3.5	
		3 MHz (typ) RC oscillator	5.0	2.5	–	
Hold-mode release hardware delay	N_{HOLD}		65,536	65,536	16,384	Cycles
Hold-mode release time	I_{HOLD}	f_{osc} = 4 MHz (t_{CYC} = 1 μs)	≈64	≈64	–	ms
		f_{osc} = 2 MHz (t_{CYC} = 2 μs)	–	–	≈32	
		f_{osc} = 1 MHz (t_{CYC} = 4 μs)	–	–	≈64	
External RC oscillator capacitance	C_{ext}		100	100	–	pF
External RC oscillator resistance	R_{ext}		2.2	2.7	–	kΩ
Timer 0 contents after reset or hold-mode release			FF0	FF0	FFC	Hex
Port output configuration after reset			See note.	Specified by user option	Specified by user option	
Package type			DIP64S or QIP64E	DIP64S or QIP64A	DIP64S or QIP64E	

Note

- Ports P2 to PC are open-drain and floating.
- Ports P0 and P1 have pull-up resistances and are HIGH or LOW.
- LC6650X series is LC66506, LC66508, LC66512, LC66516
- LC6655X series is LC66556, LC66558, LC66562, LC66566

A breakdown of the LC66 series devices, which includes the LC66516B and LC665XX devices, is shown in the following table.

Device	Pins	ROM capacity	RAM capacity	Package type
LC66304A/306A/308A	42/48	4/6/8 Kbyte ROM	512 bytes	DIP42S or QIP48E
LC66354A/356A/358A	42/48	4/6/8 Kbyte ROM	512 bytes	DIP42S or QIP48E
LC66354S$^\nabla$/356S$^\nabla$/358S$^\nabla$	44	4/6/8 Kbyte ROM	512 bytes	QIP44M
LC66E308	42/48	8 Kbyte EPROM	512 bytes	DIC42S or QIC48
LC66P308	42/48	8 Kbyte PROM	512 bytes	DIP42S or QIP48E
LC66404A/406A/408A	42/48	4/6/8 Kbyte ROM	512 bytes	DIP42S or QIP48E
LC66E408	42/48	8 Kbyte EPROM	512 bytes	DIC42S or QIC48
LC66P408	42/48	8 Kbyte PROM	512 bytes	DIP42S or QIP48E
LC66506B/508B/512B/516B	64	6/8/12/16 Kbyte ROM	512 bytes	DIP64S or QIP64A
LC66556A/558A/562A/566A	64	6/8/12/16 Kbyte ROM	512 bytes	DIP64S or QIP64E
LC66E516	64	16 Kbyte EPROM	512 bytes	DIC64S or QIC64
LC66P516	64	16 Kbyte PROM	512 bytes	DIP64S or QIP64E

Note

∇ = under development

Sanyo ROM Services

Sanyo offers various services at nominal charges. These include ROM writing, ROM reading, and package stamping and screening. Contact your local Sanyo representative for further information.