CMOS LSI

No. 3491A | **LC66404A, 66406A, 66408A**

SANYO

4K/6K/8K-BYTE ROM-CONTAINED SINGLE-CHIP 4-BIT MICROCOMPUTER FOR CONTROL-ORIENTED APPLICATIONS

General Description

The LC66404A, 66406A, 66408A are 42-pin package type CMOS 4-bit single-chip microcomputers. They contain a ROM, a RAM, I/O ports, a dual 8-bit serial interface, A/D converter input, a 12-bit timer, an 8-bit timer, and provide 8 interrupt sources with 8 vector addresses.
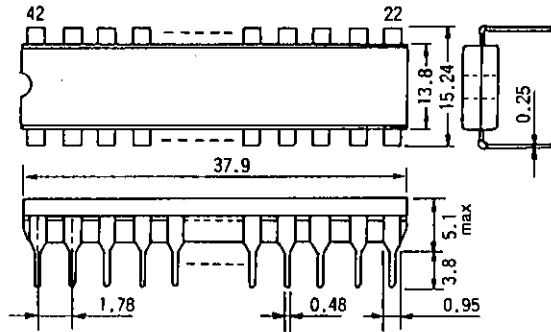
Features

(1) On-chip 4K-byte/6K-byte/8K-byte ROM, 512x4-bit RAM
(2) Instruction set with 128 instructions common with the LC665XX series
(3) I/O ports ----- 36 pins
(4) 8-bit serial interface ----- 2 lines (16-bit cascade connection available)
(5) Minimum instruction cycle time ----- 0.92µs (4.3MHz external clock input mode)
(6) Powerful timer function and prescaler
    12-bit timer-used interval timer, event counter, pulse width measurement, burst pulse output
    8-bit timer-used interval timer, event counter, PWM output, burst pulse output
    12-bit prescaler-used time base function
(7) A/D converter
    6-bit, 6-channel
(8) Powerful 8-source 8-vector interrupt function
    External interrupt: 3 sources, 3 vector addresses
    Internal iterrupt: 5 sources, 5 vector addresses (timer: 2 sources, serial I/O: 2 sources, prescaler)
(9) Flexible I/O function
    A/D converter input, 20mA drive output, 15V breakdown voltage, pull-up/open drain selectable by option
(10) Runaway detection function (option)
(11) 8-bit input/output function
(12) HALT/HOLD mode-used power-down function
(13) Package: DIP42S, QFP48E (QIP48E)
(14) Evaluation LSI: LC66599 (evaluation chip) + EVA850/800-TB6640X, LC66E408 (microcomputer with EPROM)

Series Lineup

Type No.	Pins	ROM capacity	RAM capacity	Package	Remark
LC66304A/306A/308A	42,48	4K/6K/8KB	512W	DIP42S, QFP48E	Available
LC66354A/356A/358A	42,48	4K/6K/8KB	512W	DIP42S, QFP48E	Available
LC66354S/356S/358S	44	4K/6K/8KB	512W	QFP44M	Under development
LC66E308	42,48	EPROM 8KB	512W	DIC42S, QFC48 with window	Available
LC66P308	42,48	OTPROM 8KB	512W	DIP42S, QFP48E	Available
LC66404A/406A/408A	42,48	4K/6K/8KB	512W	DIP42S, QFP48E	Available
LC66E408	42,48	EPROM 8KB	512W	DIC42S, QFC48 with window	Available
LC66P408	42,48	OTPROM 8KB	512W	DIP42S, QFP48E	Available
LC66506B/508B/512B/516B	64	6K/8K/12K/16KB	512W	DIP64S, QFP64A	Available
LC66556A/558A/562A/566A	64	6K/8K/12K/16KB	512W	DIP64S, QFP64E	Available
LC66354B/356B/358B	42,48	4K/6K/8KB	512W	DIP42S, QFP48E	Available
LC66556B/558B	64	6K/8K	512W	DIP64S, QFP64E	Under development
LC66562B/566B	64	12K/16KB	512W	DIP64S, QFP64E	Available
LC66E516	64	EPROM 16KB	512W	DIC64S, QFC64 with window	Available
LC66P516	64	OTPROM 16KB	512W	DIP64S, QFP64E	Available

SANYO Electric Co.,Ltd. Semiconductor Business Headquarters

Package Dimensions 3025B
(unit : mm)

42   22

13.8
15.24
0.25

37.9

5.1 max
3.8

1.78   0.48   0.95

SANYO : DIP42S

Pin Assignment

DIP42S

P00	1	42	PE1/AN6
P01	2	41	PE0/AN5
P02	3	40	VDD
P03	4	39	PD3/AN4
P10	5	38	PD2/AN3
P11	6	37	PD1/AN2
P12	7	36	PD0/AN1
P13	8	35	PC3
SI0/P20	9	34	PC2
SO0/P21	10	33	P63/PIN1
$\overline{SCK0}$/P22	11	32	P62/$\overline{SCK1}$
INT0/P23	12	31	P61/SO1
$\overline{INT1}$/P30	13	30	P60/SI1
POUT0/P31	14	29	P53/$\overline{INT2}$
POUT1/P32	15	28	P52
$\overline{HOLD}$/P33	16	27	P51
P40	17	26	P50
P41	18	25	P43
TEST	19	24	P42
Vss	20	23	$\overline{RES}$
OSC1	21	22	OSC2

LC66404A
LC66406A
LC66408A
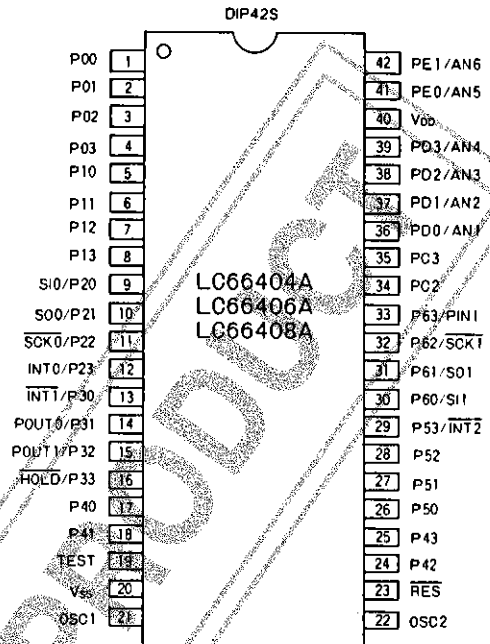
Package Dimensions 3156
(unit : mm)

17.2
14.0   1.6
1.5   1.0   1.5   0.15
1.6
1.5
1.5
17.2   14.0
1.0
48
0.35
2.70   0.1
MAX3.0
0.8   15.6
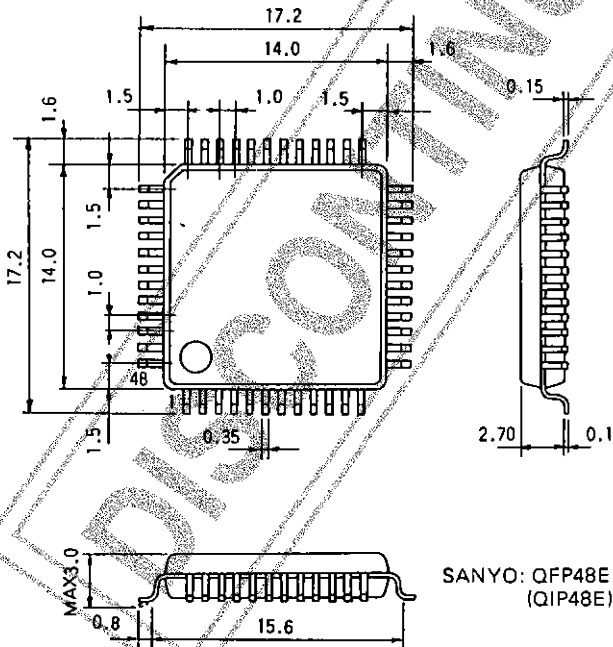
SANYO: QFP48E
(QIP48E)

Pin Assignment

PD1/AN2 PD0/AN1 PC3 PC2 P63/PIN1 P62/$\overline{SCK1}$ NC P61/SO1 P60/SI1 P53/$\overline{INT2}$ P52 P51
36 35 34 33 32 31 30 29 28 27 26 25

PD2/AN3	37	24	P50
PD3/AN4	38	23	P43
VDD	39	22	P42
PE0/AN5	40	21	$\overline{RES}$
PE1/AN6	41	20	OSC2
NC	42	19	NC
NC	43	18	NC
P00	44	17	OSC1
P01	45	16	Vss
P02	46	15	TEST
P03	47	14	P41
P10	48	13	P40

LC66404A
LC66406A
LC66408A

1 2 3 4 5 6 7 8 9 10 11 12

P11 P12 P13 SI0/P20 SO0/P21 NC $\overline{SCK0}$/P22 INT0/P23 $\overline{INT1}$/P30 POUT0/P31 POUT1/P32 $\overline{HOLD}$/P33

Note) Reflow soldering is recommended for QFP (QIP) packages.
Please consult your local representative for information on solder-bath immersion of the device.

System Block Diagram
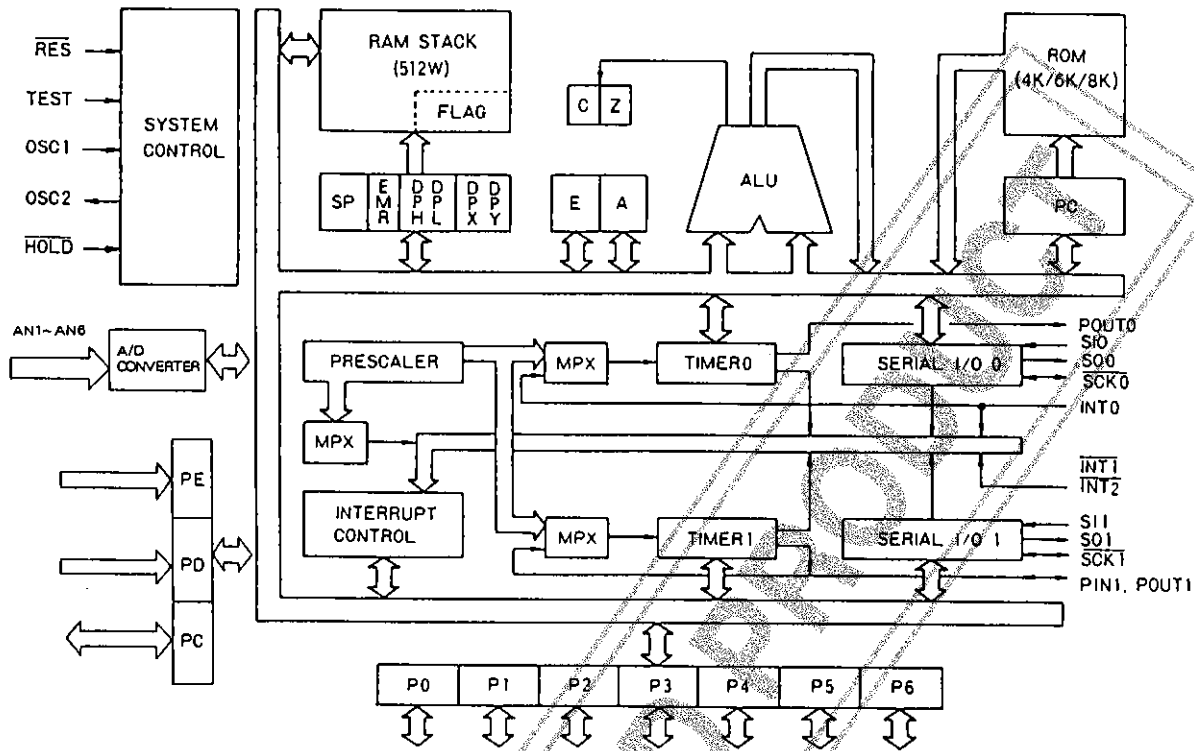
Pin Description

Pin Name	I/O	Functions	Output Driver Type	Option	During Reset
P00 P01 P02 P03	I/O	Input/output common port P00 to P03 • 4-bit and single-bit input/output • P00 to P03: Provided with HALT mode control function	• Pch: Pu MOS type • Nch: Sink medium current type	• With Pu MOS or Nch OD output • Output level during reset	H or L (option)
P10 P11 P12 P13	I/O	Input/output common port P10 to P13 • 4-bit and single-bit input/output	• Pch: Pu MOS type • Nch: Sink medium current type	• With Pu MOS or Nch OD output • Output level during reset	H or L (option)
P20/SIO P21/SOO P22/SCKO P23/INTO	I/O	Input/output common port P20 to P23 • 4-bit and single-bit input/output • P20: Common with serial input SIO • P21: Common with serial output SOO • P22: Common with serial clock SCKO • P23: Common with INTO interrupt and timer 0-used event count, pulse width measurement input	• Pch: CMOS type • Nch: Sink medium current type • +15V breakdown voltage at Nch OD configuration	• CMOS or Nch OD output	H

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Pin Name	I/O	Functions	Output Driver Type	Option	During Reset
P30/$\overline{INT1}$ P31/POUT0 P32/POUT1	I/O	Input/output common port P30 to P32 • 3-bit and single-bit input/output • P30: Common with $\overline{INT1}$ interrupt request • P31: Common with burst pulse output from timer 0 • P32: Common with burst pulse output, PWM output from timer 1	• Pch: CMOS type • Nch: Sink medium current type • +15 breakdown voltage at Nch OD configuration	• CMOS or Nch OD output	H
P33/$\overline{HOLD}$	I	HOLD mode control input • The HOLD mode is entered by executing the HOLD instruction at $\overline{HOLD}$=L. • The CPU is restarted by setting the $\overline{HOLD}$ to H level at the HOLD mode. • Usable as input port P33 with P30 to P32 • Even if the $\overline{RES}$ is brought to L level when the P33/$\overline{HOLD}$ is at L level, the CPU is not reset. So this pin must be H level when V$_{DD}$ has risen to a point where the CPU can operate properly.			
P40 P41 P42 P43	I/O	Input/output port P40 to P43 • 4-bit and single-bit input/output • 8-bit input/output with P50 to P53 • 8-bit output of ROM data with P50 to P53	• Pch: Pu MOS type • Nch: Sink medium current type • +15 breakdown voltage at Nch OD configuration	• With Pu MOS or Nch OD output	H
P50 P51 P52 P53/$\overline{INT2}$	I/O	Input/output port P50 to P53 • 4-bit and single-bit input/output • 8-bit input/output with P40 to P43 • 8-bit output of ROM data with P40 to P43 • P53: Common with $\overline{INT2}$ interrupt request	• Pch: Pu MOS type • Nch: Sink medium current type • +15 breakdown voltage at Nch OD configuration	• With Pu MOS or Nch OD output	H

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Pin Name	I/O	Functions	Output Driver Type	Option	During Reset
P60/SI1 P61/SO1 P62/SCK1 P63/PIN1	I/O	Input/output common port P60 to P63 • 4-bit and single-bit Input/output • P60: Common with serial Input SI1 • P61: Common with serial output SO1 • P62: Common with serial clock SCK1 • P63: Common with event counter input of timer 1	• Pch: CMOS type • Nch: Sink medium current type • +15V breakdown voltage at Nch OD configuration	• CMOS or Nch OD output	H
PC2 PC3	I/O	Input/output common port PC2 to PC3 • 2-bit and single-bit input/output	• Pch: CMOS type • Nch: Sink medium current type	• CMOS or Nch OD output	H
PD0/AN1 PD1/AN2 PD2/AN3 PD3/AN4	I	Input-only port PD0 to PD3 • The AD input is software-selectable. • AN1: AD converter input channel 1 • AN2: AD converter input channel 2 • AN3: AD converter input channel 3 • AN4: AD converter input channel 4			Normal input
PE0/AN5 PE1/AN6	I	Input-only port • The AD input is software-selectable.			Normal input
OSC1 OSC2	I O	Pins for externally connecting R, C or a ceramic resonator for system clock generation. For the external clock mode, the OSC2 pin is left open and the OSC1 pin is used for input.		• Ceramic resonator OSC, RC OSC, or external clock	
RES	I	System reset input pin • When the RES is brought to L level at P33/HOLD=H, the CPU is initialized.			
TEST	I	CPU test pin Connected to Vss at the operating mode			
VDD VSS		Power supply pins			

Remarks: Output with Pu MOS ------------------ Output with pull-up MOS transistor
CMOS output -------------------------------- Complementary output
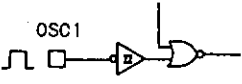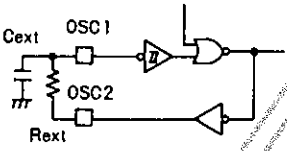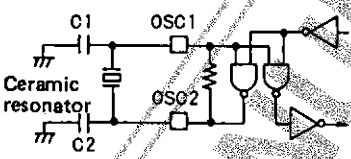OD output --------------------------------- Open drain output

User Options

(1) Options of ports 0, 1 output level during reset

For input/output ports 0, 1 either of the following two output levels may be selected in a group of 4 bits during reset by option

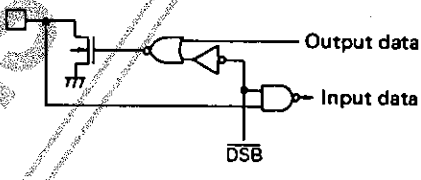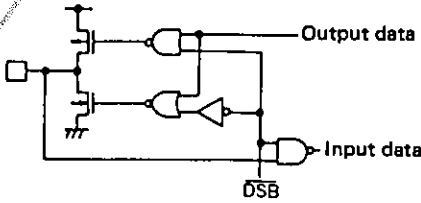| Option Name	Conditions, etc.
1. Output during reset: "H" level	All of 4 bits of ports 0, 1
2. Output during reset: "L" level	All of 4 bits of ports 0, 1

(2) Oscillator Circuit Options

Option Name	Circuit	Conditions, etc.
1. External clock		• Input: Schmitt type
2. 2-pin RC OSC		• Input: Schmitt type
3. Ceramic resonator OSC		

(3) Watchdog timer option

The presence or absence of the runaway detection function (watchdog timer) may be selected by option.

(4) Options of port output configuration

For each port of P0, P1, P2, P3 (except P33/$\overline{\text{HOLD}}$), P4, P5, P6, PC, either of the following two output configurations may be selected by option (in bit units).

Option Name	Circuit	Conditions, etc.
1. Open drain type output		P2, P3, P5, P6: Schmitt input
2. Output with pull-up resistance		P2, P3, P5, P6: Schmitt input CMOS output (P2, P3, P6, PC) or Pu MOS output (P0, P1, P4, P5) is selected according to Pch Tr drive capacity.

Main Specifications

(1) Absolute Maximum Ratings at Ta=25°C, V$_{SS}$=0V

Parameter	Symbol	Applicable Pins, Remarks	Conditions	Limits	Unit	Note
Maximum Supply Voltage	V$_{DD}$ max	V$_{DD}$		-0.3 to $+7.0$	V	
Input Voltage	V$_{IN}$(1)	P2,P3(except P33/$\overline{HOLD}$), P4,P5,P6		-0.3 to $+15.0$	V	1
	V$_{IN}$(2)	Other Inputs		-0.3 to V$_{DD}$+0.3	V	2
Output Voltage	V$_{OUT}$(1)	P2,P3(except P33/$\overline{HOLD}$), P4,P5,P6		-0.3 to $+15.0$	V	1
	V$_{OUT}$(2)	Other outputs		-0.3 to V$_{DD}$+0.3	V	2
Output Current per Pin	I$_{ON}$	P0,P1,P2,P3(except P33/$\overline{HOLD}$),PC,P4 P5,P6		20	mA	3
	$-$I$_{OP}$(1)	P0,P1,P4,P5		2	mA	4
	$-$I$_{OP}$(2)	P2,P3(except P33/$\overline{HOLD}$), P6,PC		4	mA	4
Total Pin Current	ΣI$_{ON}$(1)	P0,P1,P2,P3(except P33/$\overline{HOLD}$),P40,P41		75	mA	3
	ΣI$_{ON}$(2)	P5,P6,P42,P43,PC		75	mA	3
	$-\Sigma$I$_{OP}$(1)	P0,P1,P2,P3(except P33/$\overline{HOLD}$),P40,P41		25	mA	4
	$-\Sigma$I$_{OP}$(2)	P5,P6,P42,P43,PC		25	mA	4
Allowable Power Dissipation	Pd max	Ta=-30 to $+70$°C	DIP 42S (QFP48)	600 (430)	mW	5
Operating Temperature	Topr			-30 to $+70$	°C	
Storage Temperature	Tstg			-55 to $+125$	°C	

(Note 1) Applicable only when the open drain output type is selected. If other type than the open drain output is selected, the specification indicated in the column for other pins applies.

(Note 2) For OSC input/output, up to self OSC level is allowable.

(Note 3) Sink current

(Note 4) Source current (applicable only when the pull-up output type or CMOS output type is selected)

(Note 5) Reflow soldering is recommended for QFP packages.
Please consult your local representative for information on solder-bath immersion of the device.

(2) Allowable Operating Conditions at Ta=-30 to $+70$°C, V$_{SS}$=0V unless otherwise specified

Parameter	Symbol	Applicable Pins	Conditions	Limits				Unit	Note
				V$_{DD}$(V)	min	typ	max		
Operating Voltage	V$_{DD}$	V$_{DD}$			4.0	5.0	6.0	V	
Data Retention Voltage	V$_{DD}$(H)	V$_{DD}$	HOLD mode		1.8		6.0	V	
"H"-Level Input Voltage	V$_{IH}$(1)	P2,P3(except P33/$\overline{HOLD}$),P4,P5,P6	Output Nch Tr OFF	4.0 to 6.0	0.75V$_{DD}$		$+13.5$	V	1
	V$_{IH}$(2)	P33/$\overline{HOLD}$, $\overline{RES}$, OSC1	Output Nch Tr OFF	4.0 to 6.0	0.75V$_{DD}$		V$_{DD}$	V	2
	V$_{IH}$(3)	P0,P1,PC,PD,PE	Output Nch Tr OFF	4.0 to 6.0	0.7V$_{DD}$		V$_{DD}$	V	3

Continued from preceding page.

Parameter		Symbol	Applicable Pins	Conditions	Limits				Unit	Note
					VDD(V)	min	typ	max		
"L"-Level Input Voltage		VIL(1)	P2,P3(except P33/HOLD), P5,P6, RES,OSC1	Output Nch Tr OFF	4.0 to 6.0	VSS		0.25VDD	V	2
		VIL(2)	P33/HOLD		1.8 to 6.0	VSS		0.25VDD	V	
		VIL(3)	P0, P1, P4, PC, PD, PE, TEST	Output Nch Tr OFF	4.0 to 6.0	VSS		0.3VDD	V	3
Operating Frequency (Instruction Cycle Time)		fOP (TCYC)			4.0 to 6.0	0.4 (10)		4.35 (0.92)	MHz (μs)	
External Clock Input Conditions	Frequency	fext	OSC1	See Fig. 1. The OSC1 is used for input and the OSC2 is left open. (OSC option: External clock input)	4.0 to 6.0	0.4		4.35	MHz	
	Pulse Width	textH textL		See Fig. 1. The OSC1 is used for input and the OSC2 is left open. (OSC option: External clock input)	4.0 to 6.0	70			ns	
	Rise/Fall Time	textR textF		See Fig. 1. The OSC1 is used for input and the OSC2 is left open. (OSC option: External clock input)	4.0 to 6.0			30	ns	
Self OSC Conditions	External Constants for RC OSC	Cext Rext	OSC1, OSC2	See Fig. 3.	4.0 to 6.0		100 2.7		pF kΩ	

(Note 1) Applicable to pins of open drain type. For P33/HOLD, VIH(2) applies.
 P2, P3, P6 of CMOS output type cannot be used as input pin.
(Note 2) Applicable to pins of open drain type.
(Note 3) PC of CMOS output type cannot be used as input pin.

(3) Electrical Characteristics at Ta=−30 to +70°C, VSS=0V unless otherwise specified

Parameter	Symbol	Applicable Pins	Conditions		VDD(V)	min	typ	max	Unit	Note
"H"-Level Input Current	IIH(1)	P2,P3 (except P33/HOLD), P4,P5,P6	VIN=13.5V Output Nch Tr OFF		4.0to6.0			5.0	μA	1
	IIH(2)	P0, P1, OSC1, RES, P33/HOLD	VIN=VDD Output Nch Tr OFF		4.0to6.0			1.0	μA	1
	IIH(3)	PC2,PC3,PD,PE	VIN=VDD Output Nch Tr OFF		4.0to6.0			1.0	μA	1
"L"-Level Input Current	IIL(1)	Inputs other than PC2,PC3,PD,PE	VIN=VSS Output Nch Tr OFF		4.0to6.0	−1.0			μA	2
	IIL(2)	PC2, PC3, PD, PE	VIN=VSS Output Nch Tr OFF		4.0to6.0	−1.0			μA	2
"H"-Level Output Voltage	VOH(1)	P2, P3 (except P33/HOLD), P6, PC	IOH=−1mA		4.0to6.0	VDD−1.0			V	3
			IOH=−0.1mA		4.0to6.0	VDD−0.5			V	3
	VOH(2)	P0, P1, P4, P5	IOH=−200μA		4.5	2.4			V	4
			IOH=−130μA		4.5to5.5	VDD−1.35			V	
Output Pull-up Current	IPO	P0, P1, P4, P5	VIN=VSS		5.5	−1.6			mA	4
"L"-Level Output Voltage	VOL(1)	P0, P1, P2, P3, P4, P5, P6, PC (except P33/HOLD)	IOL=1.6mA		4.0to6.0			0.4	V	
	VOL(2)	P0,P1,P2,P3,P4,P5, P6(except P33/HOLD)	IOL=10mA		4.0to6.0			1.5	V	
Output OFF-State Leakage Current	IOFF(1)	P2,P3,P4,P5,P6	VIN=13.5V		4.0to6.0			5.0	μA	5
	IOFF(2)	P0, P1, PC	VIN=VDD		4.0to6.0			1.0	μA	5
Schmitt Characteristics — Hysteresis Voltage	VHYS	P2,P3,P5,P6,RES, OSC1 (RC,EXT)			4.0to6.0		0.1VDD		V	
"H"-Level Threshold Voltage	Vt H					0.5VDD		0.75VDD	V	
"L"-Level Threshold Voltage	Vt L					0.25VDD		0.5VDD	V	
Ceramic Resonator OSC — OSC Frequency	fCF	OSC1, OSC2	See Fig. 2.	4MHz	4.0to6.0		4.0		MHz	
OSC Stabilizing Period	tCFS		See Fig. 3.	4MHz	4.0to6.0			10	ms	
RC OSC Frequency	fRC	OSC1, OSC2	See Fig. 4. C=100pF±5% R=2.7kΩ±1%		4.0to6.0	2.0	3.0	4.0	MHz	

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Parameter			Symbol	Applicable Pins	Conditions	Limits				Unit	Note
						VDD(V)	min	typ	max		
Serial Clock	Cycle Time	Input	tCKCY	SCK0, SCK1	Timing of Fig. 5 and timing load of Fig. 6.	4.0to6.0	0.9			μS	
		Output				4.0to6.0	2.0			TCYC	
	"L"/"H"-Level Pulse Width	Input	tCKL			4.0to6.0	0.4			μS	
		Output	tCKH			4.0to6.0	1.0			TCYC	
	Rise/Fall Time	Output	tCKR tCKF			4.0to6.0			0.1	μS	
Serial Input	Data Setup Time		tICK	SI0, SI1	Timing of Fig. 5, specified for SCK0, SCK1 rise (↑)	4.0to6.0	0.3			μS	
	Data Hold Time		tCKI			4.0to6.0	0.3			μS	
Serial Output	Output Delay Time		tCKO	SO0, SO1	Timing of Fig. 5 and timing load of Fig. 6, specified for SCK0, SCK1 fall (↓)	4.0to6.0			0.3	μS	
Pulse Input Conditions	"H"/"L"-Level Pulse Width at INT0		tI0H tI0L	INT0	See Fig.7. • Condition under which the INT0 interrupt is accepted • Condition under which the event counter/pulse width measure input by timer 0 is accepted	4.0to6.0	2			TCYC	
	Interrupt Input "H"/"L"-Level Pulse Width at Other than INT0		tI1H tI1L	INT1, INT2	• Condition under which each interrupt is accepted		2			TCYC	
	"H"/"L"-Level Pulse Width at PIN1		tPINH tPINL	PIN1	• Condition under which the event counter input by timer 1 is accepted		2			TCYC	
	"H"/"L"-Level Pulse Width at RES		tRSH tRSL	RES	• Condition under which a reset is caused		3			TCYC	
Current Dissipation at Operating Mode			IDD OP	VDD	4MHz ceramic resonator OSC	4.0to6.0		4.5	8	mA	
					4MHz external clock			6.5	11	mA	6
					RC OSC			4.0	8	mA	

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Parameter	Symbol	Applicable Pins	Conditions	Limits				Unit	Note
				VDD(V)	min	typ	max		
Current Dissipation at HALT Mode	IDDHALT	VDD	4MHz ceramic resonator OSC	4.0 to 6.0		1.0	3.0	mA	
			4MHz external clock			2.0	3.5	mA	
			RC OSC			1.2	3.0	mA	
Current Dissipation at HOLD Mode	IDDHOLD	VDD		1.8 to 6.0		0.01	10.0	μA	

A/D Conversion Characteristics at Ta=−30 to +70°C, V_{SS}=0V (A/D conversion is used in A/D mode.)

Parameter	Symbol	Applicable Pins	Conditions	Limits				unit	Note
				VDD(V)	min	typ	max		
Resolution				4.0 to 6.0		6		Bit	
Absolute Accuracy						+1	+1.5	LSB	
Linearity Error						+0.5	+1	LSB	
Conversion Time	TCAD		ADSPEED=H			64	128	Tcyc	
			ADSPEED=L			128	256		
Analog Input Voltage	VINAD	AN1 to AN6			VSS		VDD	V	

Comparator Characteristics at Ta=−30 to +70°C, V_{SS}=0V (A/D conversion is used in comparator mode.)

Parameter	Symbol	Applicable Pins	Conditions	Limits				unit	Note
				VDD(V)	min	typ	max		
Comparison Accuracy	VCECM	AN1 to AN6		4.0 to 6.0		+1	+1.5	LSB	
Threshold Voltage	VTHCM				VSS		VDD	V	
Input Voltage	VINCM	AN1 to AN6			VSS		VDD	V	
Conversion Time	TCCM						30	μS	

(Note 1) The input/output common ports are of open drain output type with output Nch transistor OFF. When the CMOS output type is selected, the input/output common ports cannot be used as the input pins.

(Note 2) The input/output common ports are of open drain output type with output Nch transistor OFF. The specification for pull-up output type is specified by output pull-up current IPO. When CMOS output type is selected, the input/output common ports cannot be used as the input pins.

(Note 3) CMOS output type and output Nch transistor OFF.

(Note 4) Pull-up output type and output Nch transistor OFF.

(Note 5) Open drain output type and output Nch transistor OFF.

(Note 6) Reset mode.
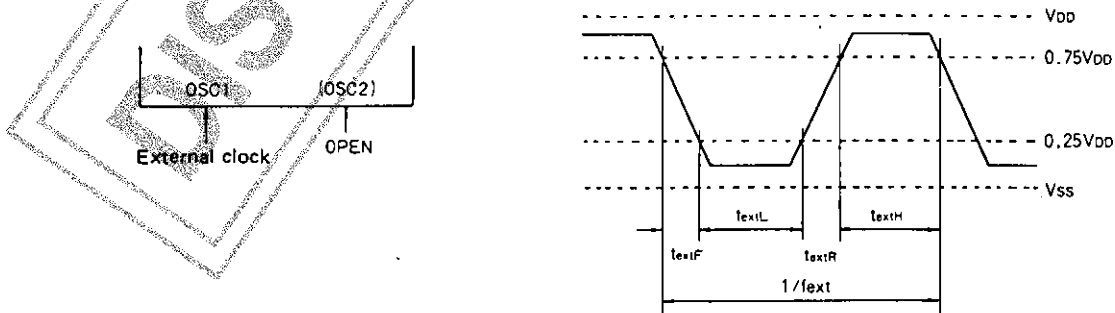
Fig. 1   External Clock Input Waveform
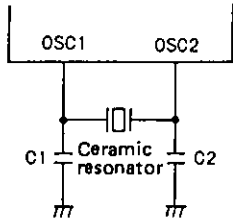
Fig. 2   Ceramic Resonator OSC Circuit
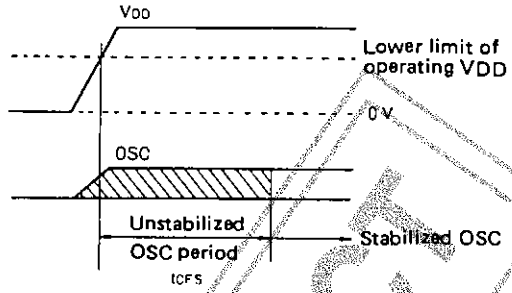
Fig. 3   OSC Stabilizing Period

External capacitor type	4 MHz (Murata) CSA4.00MG	C1	33pF ±10%
		C2	33pF ±10%
	4 MHz (Kyocera) KBR4.0MS	C1	33pF ±10%
		C2	33pF ±10%
On-chip capacitor type	4 MHz (Murata) CST4.00MG		
	4 MHz (kyocera) KBR-4.0MES		

Table 1   Ceramic Resonator OSC-Guaranteed Constants
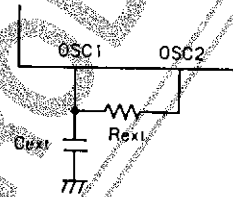
Fig. 4   RC OSC
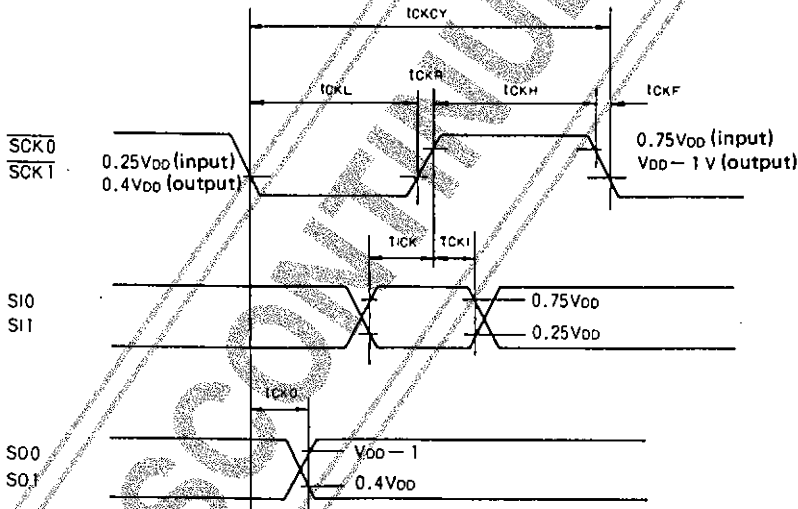
Fig. 5   Serial Input/Output Timing
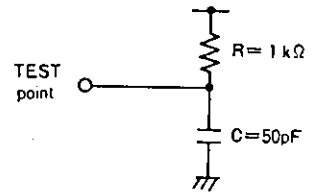
Fig. 6   Timing Load
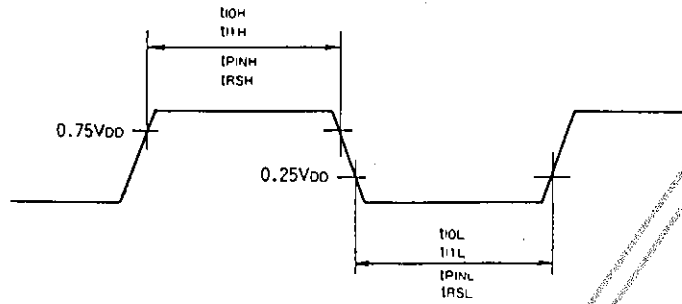
Fig. 7 INT0, INT1, INT2, PIN1, RES Input Timing

RC OSC Characteristic of the LC66404A, 66406A, 66408A

Fig. 8 shows the RC OSC characteristic of the LC66404A, 66406A, 66408A. For the variation range of RC OSC frequency of the LC66404A, 66406A, 66408A, the following are guaranteed at the external constants only shown below.

External constants   Cext=100pF, Rext=2.7kΩ
2.0MHz$\leqq$f$_{RC}\leqq$4.0MHz (Ta=−30°C to +70°C, V$_{DD}$=4.0 to 6.0V)

If any other constants than specified above are used, RC oscillation frequency data (typ.) must be observed. (See Fig. 8.)

(Note 10)   The OSC frequency at V$_{DD}$=4.0 to 6.0V, Ta=−30 to +70°C must be within the operation clock frequency range (0.4 to 4.3MHz).

f$_{RC}$−Rext Characteristic
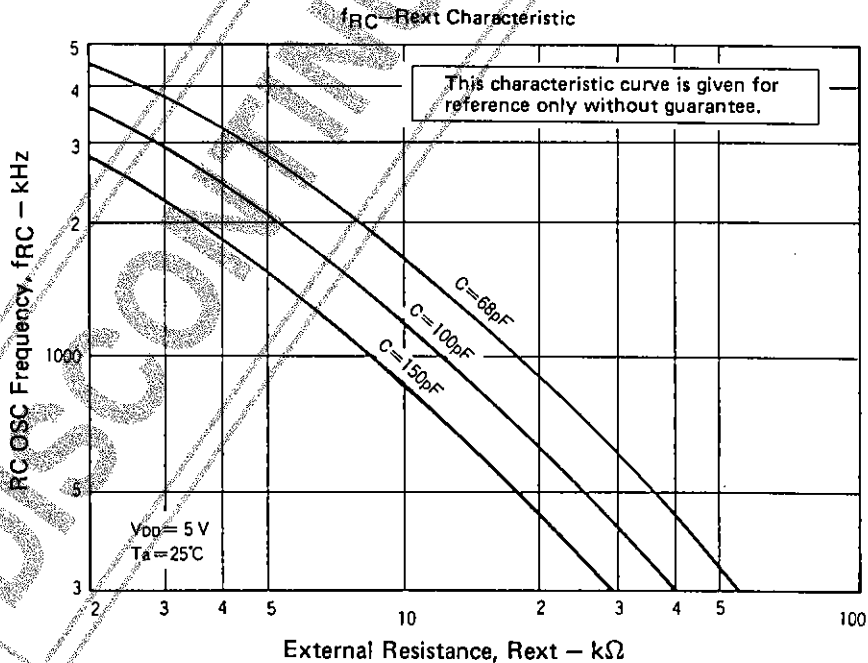
Fig. 8   RC OSC Frequency Data (Typ.)

Application Development Tools

The programs for the LC66404A, 66406A, 66408A microcomputers can be developed on the MS-DOS personal computer system (IBM-PC model system). Cross assembler for this system is provided. To help the user develop programs for the LC66404A, 66406A, 66408A microcomputers, the following development tools are prepared:
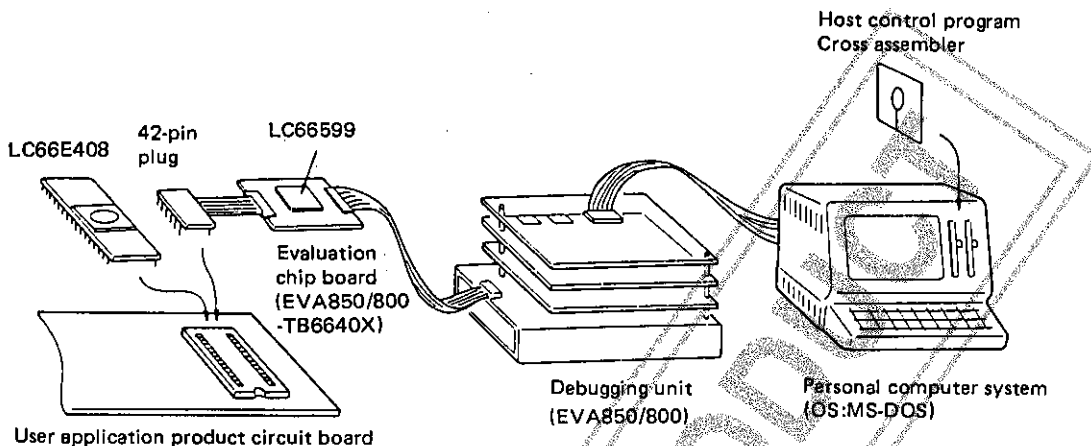
Appearance of Application Development Tools

(1) Program debugging unit (EVA850/800)

The program debugging unit (EVA850/800) is an emulator that includes the EPROM WRITE function and the serial data communications interface function between the unit itself and external systems (host computer, etc.). Application programs can be developed, corrected, and debugged at the machine language level. The debugging function can be carried out through break, step and trace operations. (Use the MPM6640X as the monitor ROM on the EVA850/800 debugging unit.)

(2) Evaluation chip board (EVA850/800-TB6640X)

The evaluation chip board sends control signals to the user application board through the 42-pin connector. Data is transferred between the I/O ports on the evaluation chip board and the user application board through the 42-pin connector. If the LC66599 evaluation chip is connected to the 42-pin plug by the output cable, the data from the LC66599 microcomputer is converted into the LC66404A, 66406A, 66408A-bound data by the plug. There are jumper connectors on the evaluation chip board. They are used to select options and status levels. Therefore, using these jumper connectors, the same input/output formats and functions as those of the LC66404A, 66406A, 66408A microcomputers can be selected on the evaluation chip board.

Jumpers

Type	OSC		Reset type selection		Power supply to the user application board through the evaluation chip board	
Jumper name	Jumper 1 (J1)		Jumper 2 (J2)		Jumper 3 (J3)	
Jumper setting and mode	EXT	External clock	INT	Reset by the RUN instruction from the host computer.	ON	VDD supply to the user application board through the evaluation chip board output.
	RC	RC OSC				
	CF	CF OSC	EXT	Reset by the reset circuit on the user application board	OFF	Power supply to the user application board from an independent power source (from the evaluation chip board)

Switch 9 to 11 (SW9 to SW11)

Type	Output level selection for ports 0,1 at the reset				Watchdog timer function selection	
Switch name	POHL (SW11)		P1HL(SW10)		WDC (SW9)	
Switch setting and mode	+5V	Port 0 "H"	+5V	Port 1 "H"	+5V	Watchdog timer function selected
	GND	Port 0 "L"	GND	Port 1 "L"	GND	Watchdog timer function not selected

(Note) There are many other switches on the evaluation chip board. For further details, refer to the description of "Section 4. Operation" in "EVA 850/800-LC6640X Development Tool Manual".

Switches SW1 to SW8: Pull-up resistor option select

① Set to ON when on-chip pull-up resistor is used. Set to OPEN when open drain output type is selected.

② Selectable for each pin.

(3) Cross assembler

Cross assembler name (File name)	Target machine	Restriction on program development
LC66S.EXE	LC66404A, 66406A, 66408A(LC66E408/P408) (LC66599)	Restriction on SB instruction • LC66404A : SB 0 only usable • LC66406A/408A : SB 0, SB 1 usable (LC66E408/P408) • (LC66599) : SB 0, SB 1, SB 2, SB 3 usable

(4) Simulation chip (For details, refer to the catalog of the LC66E408.)

The simulation chip (LC66E408) is an EPROM-contained microcomputer. Using the dedicated conversion board (DIP: W66EP308D/408D, FLP: W66EP308Q/408Q), you can write programs in the EPROM with a commercially available PROM writer. Then, you can incorporate the simulation chip into an application product to monitor actual operations.

① Case outline

The LC66E408 is the same as the LC66404A, 66406A, 66408A in pin assignment and functions. The pin assignment is shown below.

② Option

Using the on-chip EPROM data (option data area and definition are shown on the next page), you can specify the options (level at port 0, 1 reset mode, watchdog timer, port output configuration) of a microcomputer to be evaluated. Thus, you can perform evaluation using the same peripheral as the board of the equipment to be mass-produced.

Pin Assignment

DIC42S with window

Pin	Left		Pin	Right
1	D0/P00		42	PE1/AN6/$\overline{OE}$
2	D1/P01		41	PE0/AN5/$\overline{CE}$
3	D2/P02		40	VDD
4	D3/P03		39	PD3/AN4/$\overline{PGM}$
5	D4/P10		38	PD2/AN3
6	D5/P11		37	PD1/AN2
7	D6/P12		36	PD0/AN1
8	D7/P13		35	PC3
9	A0/SI0/P20		34	PC2
10	A1/SO0/P21		33	P63/PIN1/DASEC
11	A2/SCK0/P22		32	P62/$\overline{SCK1}$
12	A3/INT0/P23		31	P61/SO1
13	A4/INT1/P30	LC66E408	30	P60/SI1
14	A5/POUT0/P31		29	P53/$\overline{INT2}$
15	A6/POUT1/P32		28	P52/A13
16	$\overline{HOLD}$/P33		27	P51/A12
17	A7/P40		26	P50/A11
18	A8/P41		25	P43/A10
19	VPP/TEST		24	P42/A9
20	Vss		23	$\overline{RES}$
21	OSC1		22	OSC2

Option Data Area and Definition

ROM Area	Bit	Option		Relation between Option and Data
2 0 0 0 H	7	Unused		Fixed at 0
	6			
	5			
	4	OSC option		1=Ceramic resonator OSC 0=RC OSC, external clock
	3	Unused		Fixed at 0
	2	P1	Level at reset mode	1="H" level
	1	P0		0="L" level
	0	Watchdog timer option		1=Available, 0=Unavailable
2 0 0 1 H	7	P13	Output configuration	1 =PU、 0 =OD
	6	P12		
	5	P11		
	4	P10		
	3	P03	Output configuration	1 =PU、 0 =OD
	2	P02		
	1	P01		
	0	P00		
2 0 0 2 H	7	Unused		Fixed at 0
	6	P32	Output configuration	1 =PU、 0 =OD
	5	P31		
	4	P30		
	3	P23	Output configuration	1 =PU、 0 =OD
	2	P22		
	1	P21		
	0	P20		
2 0 0 3 H	7	P53	Output configuration	1 =PU、 0 =OD
	6	P52		
	5	P51		
	4	P50		
	3	P43	Output configuration	1 =PU、 0 =OD
	2	P42		
	1	P41		
	0	P40		
2 0 0 4 H	7~4	Unused		
	3	P63	Output configuration	1 =PU、 0 =OD
	2	P62		
	1	P61		
	0	P60		
2 0 0 5 H	7~0	Unused		Fixed at 0
2 0 0 6 H	7~0	Unused		Fixed at 0
2 0 0 7 H	7~4	Unused		Fixed at 0
	3	PC3	Output configuration	1 =PU、 0 =OD
	2	PC2		
	1	Unused		Fixed at 0
	0			

Remarks:

PU --- Pull-up MOS type resistance output

OD --- Open drain output

Note: The pull-up MOS type resistance output represents the pull-up MOS (PU MOS) type resistor output circuit and the complementary MOS (CMOS) type output circuit.

LC6640X SERIES INSTRUCTION SET (BY FUNCTION)

Symbol	Description
AC	: Accumulator
E	: E register
CF	: Carry flag
ZF	: Zero flag
HL	: Data pointer DPH, DPL
XY	: Data pointer DPX, DPY
M	: Data memory
M (HL)	: Data memory contents specified by data pointer DPH, DPL
M (XY)	: Data memory contents specified by supplementary data pointer DPX, DPY
M2 (HL)	: 2-word data memory contents specified by data pointer DPH, DPL.
	In this case, the accessed data memory area address must be multiples of 2 (even address).
SP	: Stack pointer
M2 (SP)	: 2-word data memory contents specified by stack pointer
M4 (SP)	: 4-word data memory contents specified by stack pointer
in	: n-bit immediate data
t2	: Bit specification

t2	11	10	01	00
Bit	2^3	2^2	2^1	2^0

PCh	: Bits 8 to 11 of PC
PCm	: Bits 4 to 7 of PC
PCl	: Bits 0 to 3 of PC
Fn	: User's flag n=0 to 15
TIMER0	: Timer 0
TIMER1	: Timer 1
SIO	: Serial register
P	: Port
P (i4)	: Port contents specified by 4-bit immediate data
INT	: Interrupt enable flag
( ),[ ]	: Contents
←	: Transfer direction and operation result
∀	: Exclusive logical sum
∧	: Logical product
∨	: Logical sum
+	: Addition
−	: Subtraction
‾	: 1's complement

Instruction type	Mnemonics		Instruction code D7D6D5D4	D3D2D1D0	Bytes	Cycles	Function	Description	Status flags affected	Remarks
Accumulator manipulation instructions	CLA	Clear AC	1 0 0 0	0 0 0 0	1	1	AC←0 (Equivalent to LAI 0)	Clears AC.	ZF	Only the first instruction is effective if executed continuously (skip function)
	DAA	Decimal adjust AC in addition	1 1 0 0 / 0 0 1 0	1 1 1 1 / 0 1 1 0	2	2	AC←(AC) + 6 (Equivalent to ADI 6)	Adds 6 to AC.	ZF	
	DAS	Decimal adjust AC in subtraction	1 1 0 0 / 0 0 1 0	1 1 1 1 / 1 0 1 0	2	2	AC←(AC) – 10 (Equivalent to ADI 0AH)	Adds 10 to AC.	ZF	
	CLC	Clear CF	0 0 0 1	1 1 1 0	1	1	CF←0	Clears CF.	CF	
	STC	Set CF	0 0 0 1	1 1 1 1	1	1	CF←1	Sets CF.	CF	
	CMA	Complement AC	0 0 0 1	1 0 0 0	1	1	AC←$\overline{(AC)}$	Gives 1's complement of (invert) AC.	ZF	
	IA	Increment AC	0 0 0 1	0 1 0 0	1	1	AC←(AC) + 1	Adds 1 to AC.	ZF, CF	
	DA	Decrement AC	0 0 1 0	0 1 0 0	1	1	AC←(AC) – 1	Subtracts 1 from AC.	ZF, CF	
	RAR	Rotate AC right through CF	0 0 0 1	0 0 0 0	1	1	AC_3←(CF), ACn←(ACn + 1) , CF←(AC_0)	Rotates AC right through CF.	CF	
	RAL	Rotate AC left through CF	0 0 0 0	0 0 0 1	1	1	AC_0←(CF), ACn + 1←(ACn), CF←(AC_3)	Rotates AC left through CF.	CF, ZF	
	TAE	Transfer AC to E	0 1 0 0	0 1 0 1	1	1	E←(AC)	Transfers the AC contents to the E register.		
	TEA	Transfer E to AC	0 1 0 0	0 1 1 0	1	1	AC←(E)	Transfers the E register contents to AC.	ZF	
	XAE	Exchange AC with E	0 1 0 0	0 1 0 0	1	1	(AC)←→(E)	Exchanges the contents of the AC and E register.		
Memory manipulation instructions	IM	Increment M	0 0 0 1	0 0 1 0	1	1	M(HL)←(M(HL)) + 1	Adds 1 to M(HL).	ZF, CF	
	DM	Decrement M	0 0 1 0	0 0 1 0	1	1	M(HL)←(M(HL)) – 1	Subtracts 1 from M(HL).	ZF, CF	
	IMDR i8	Increment M direct	1 1 0 0 / I7 I6 I5 I4	0 1 1 1 / I3 I2 I1 I0	2	2	M(i8)←(M(i8)) + 1	Adds 1 to M(i8).	ZF, CF	
	DMDR i8	Decrement M direct	1 1 0 0 / I7 I6 I5 I4	0 0 1 1 / I3 I2 I1 I0	2	2	M(i8)←(M(i8)) – 1	Subtracts 1 from M(i8).	ZF, CF	
	SMB t2	Set M data bit	0 0 0 0	1 1 t1 t0	1	1	(M(HL), t2)←1	Sets a bit specified by t1,t0 of M(HL).		
	RMB t2	Reset M data bit	0 0 1 0	1 1 t1 t0	1	1	(M(HL), t2)←0	Resets a bit specified by t1,t0 of M(HL).	ZF	
Operation/Comparison instructions	AD	Add M to AC	0 0 0 0	0 1 1 0	1	1	AC←(AC) + (M(HL))	Adds together the contents of AC and M(HL) in binary and stores the result in AC.	ZF, CF	
	ADDR i8	Add M direct to AC	1 1 0 0 / I7 I6 I5 I4	1 0 0 1 / I3 I2 I1 I0	2	2	AC←(AC) + (M(i8))	Adds together the contents of AC and M(i8) in binary and stores the result in AC.	ZF, CF	
	ADC	Add M to AC with CF	0 0 0 0	0 0 1 0	1	1	AC←(AC) + (M(HL)) + (CF)	Adds together the contents of AC, M(HL), and CF in binary and stores the result in AC.	ZF, CF	
	ADI i4	Add immediate data to AC	1 1 0 0 / 0 0 1 0	1 1 1 1 / I3 I2 I1 I0	2	2	AC←(AC) + I3,I2,I1,I0	Adds together the contents of AC and immediate data in binary and stores the result in AC.	ZF	
	SUBC	Subtract AC from M with CF	0 0 0 1	0 1 1 1	1	1	AC←(M(HL)) – (AC) – $\overline{(CF)}$	Subtracts the contents of AC from M(HL) with CF in binary and stores the result in AC.	ZF, CF	CF=0 if there is a borrow while CF=1 if there is no borrow.
	ANDA	AND M with AC then store AC	0 0 0 0	0 1 1 1	1	1	AC←(AC)∧(M(HL))	Performs a logical AND operation between AC and M(HL) and stores the result in AC.	ZF	
	ORA	OR M with AC then store AC	0 0 0 0	0 1 0 1	1	1	AC←(AC)∨(M(HL))	Performs a logical OR operation between AC and M(HL) and stores the result in AC.	ZF	
	EXL	Exclusive OR M with AC then store AC	0 0 0 1	0 1 0 1	1	1	AC←(AC)$\veebar$(M(HL))	Performs a logical exclusive OR operation between AC and M(HL) and stores the result in AC.	ZF	
	ANDM	AND M with AC then store M	0 0 0 0	0 0 1 1	1	1	M(HL)←(AC)∧(M(HL))	Performs a logical AND operation between AC and M(HL) and stores the result in M(HL).	ZF	
	ORM	OR M with AC then store M	0 0 0 0	0 1 0 0	1	1	M(HL)←(AC)∨(M(HL))	Performs a logical OR operation between AC and M(HL) and stores the results in M(HL).	ZF	

Instruction type	Mnemonics		Instruction code D7D6D5D4	D3D2D1D0	Bytes	Cycles	Function	Description	Status flags affected	Remarks
Operation/Comparison instructions	CM	Compare AC with M	0 0 0 1	0 1 1 0	1	1	$\overline{(M(HL))} + (AC) + 1$	Compares the contents of AC and M(HL) and then sets/resets the carry flag (CF) and zero flag (ZF). Comparison relations / CF / ZF (M(HL)) > (AC) / 0 / 0 (M(HL)) = (AC) / 1 / 1 (M(HL)) < (AC) / 1 / 0	ZF, CF	
	CI i4	Compare AC with immediate data	1 1 0 0 / 1 0 1 0	1 1 1 1 / $I_3 I_2 I_1 I_0$	2	2	$\overline{I_3 I_2 I_1 I_0} + (AC) - 1$	Compares the contents of the accumulator (AC) and immediate data I3I2I1I0 and sets/resets the zero flag (ZF) and carry flag (CF). Comparison relations / CF / ZF $I_3 I_2 I_1 I_0 > AC$ / 0 / 0 $I_3 I_2 I_1 I_0 = AC$ / 1 / 1 $I_3 I_2 I_1 I_0 < AC$ / 1 / 0	ZF, CF	
	CLI i4	Compare DPL with immediate data	1 1 0 0 / 1 0 1 1	1 1 1 1 / $I_3 I_2 I_1 I_0$	2	2	$ZF \leftarrow 1$ if$(DP_L) = I_3 I_2 I_1 I_0$ $ZF \leftarrow 0$ if$(DP_L) \neq I_3 I_2 I_1 I_0$	Compares the contents of DPL and immediate data and sets the zero flag (ZF) if they are equal, or resets the flag if not equal.	ZF	
	CMB t2	Compare AC bit with M data bit	1 1 0 0 / 1 1 0 1	1 1 1 1 / 0 0 $t_1 t_0$	2	2	$ZF \leftarrow 1$ if(AC, t2) = (M(HL), t2); $ZF \leftarrow 0$ if(AC, t2) ≠ (M(HL), t2)	Compares the contents of AC and M(HL) bit specified by the 2 bits (t1 and t2) of the instruction and sets the zero flag (ZF) if they are equal, or resets the flag if not equal.	ZF	
Load/store instructions	LAE	Load AC and E from M2 (HL)	0 1 0 1	1 1 0 0	1	1	AC←M(HL) E←M(HL+1)	Loads the contents of M2(HL) into the AC and the E register.		
	LAI i4	Load AC with immediate data	1 0 0 0	$I_3 I_2 I_1 I_0$	1	1	AC← $I_3 I_2 I_1 I_0$	Loads immediate data into AC.	ZF	Only the first instruction is effective if executed continuously (skip function).
	LADR i8	Load AC from M direct	1 1 0 0 / $I_7 I_6 I_5 I_4$	0 0 0 1 / $I_3 I_2 I_1 I_0$	2	2	AC←(M(i8))	Loads the contents of M(i8) into AC.	ZF	
	S	Store AC to M	0 1 0 0	0 1 1 1	1	1	M(HL)←(AC)	Stores the contents of AC into M(HL).		
	SAE	Store AC and E to M2 (HL)	0 1 0 1	1 1 1 0	1	1	M(HL)←(AC) M(HL+1)←(E)	Stores the contents of AC and the E register into M2(HL).		
	LA reg	Load AC from M(reg)	0 1 0 0	1 0 t_0 0	1	1	AC←(M(reg))	Loads the contents of M(reg) into AC. reg is either an HL or XY. reg / t0 HL / 0 XY / 1	ZF	
	LA reg,I	Load AC from M(reg) then increment reg	0 1 0 0	1 0 t_0 1	1	2	AC←(M(reg)) $DP_L \leftarrow (DP_L) + 1$ or $DP_Y \leftarrow (DP_Y) + 1$	Loads the contents of M(reg) into the accumulator (AC). reg is either an HL or XY. After loading, increments the contents of DPL or DPY. Refer to the LA reg instruction for the relationship between reg and t0.	ZF	ZF status depends on DPLorDPY increment result.
	LA reg,D	Load AC from M(reg) then decrement reg	0 1 0 1	1 0 t_0 1	1	2	AC←(M(reg)) $DP_L \leftarrow (DP_L) - 1$ or $DP_Y \leftarrow (DP_Y) - 1$	Loads the contents of M(reg) into AC. reg is either an HL or XY. After loading, decrements the contents of DPL or DPY. Refer to the LA reg instruction for the relationship between reg and t0.	ZF	ZF status depends on DPLorDPY decrement result.
	XA reg	Exchange AC with M(reg)	0 1 0 0	1 1 t_0 0	1	1	(AC)↔(M(reg))	Exchanges the contents of AC and M(reg). reg is either an HL or XY. reg / t0 HL / 0 XY / 1		
	XA reg,I	Exchange AC with M(reg) then increment reg	0 1 0 0	1 1 t_0 1	1	2	(AC)↔(M(reg)) $DP_L \leftarrow (DP_L) + 1$ or $DP_Y \leftarrow (DP_Y) + 1$	Exchanges the contents of AC and M(reg). reg is either an HL or XY. After exchanging, increments the contents of DPL or DPY. Refer to the XA reg instruction for the relationship between reg and t0.	ZF	ZF status depends on DPLorDPY increment result.
	XA reg,D	Exchange AC with M(reg) then decrement reg	0 1 0 1	1 1 t_0 1	1	2	(AC)↔(M(reg)) $DP_L \leftarrow (DP_L) - 1$ or $DP_Y \leftarrow (DP_Y) - 1$	Exchanges the contents of AC and M(reg). reg is either an HL or XY. After exchanging, decrements the contents of DPL or DPY. Refer to the XA reg instruction for the relationship between reg and t0.	ZF	ZF status depends on DPLorDPY decrement result.
	XADR i8	Exchange AC with M direct	1 1 0 0 / $I_7 I_6 I_5 I_4$	1 0 0 0 / $I_3 I_2 I_1 I_0$	2	2	(AC)↔(M(i8))	Exchanges the contents of AC and M(i8).		

Instruction type	Mnemonics		Instruction code D7D6D5D4	Instruction code D3D2D1D0	Bytes	Cycles	Function	Description	Status flags affected	Remarks
Load/store instructions	LEAI i8	Load E & AC with immediate data	1 1 0 0 / $I_7 I_6 I_5 I_4$	0 1 1 0 / $I_3 I_2 I_1 I_0$	2	2	$E \leftarrow I_7 I_6 I_5 I_4$, $AC \leftarrow I_3 I_2 I_1 I_0$	Loads immediate data i8 into the E register and the accumulator (AC).		
	RTBL	Read table data from program ROM	0 1 0 1	1 0 1 0	1	2	E, AC←(ROM(PCh, E, AC))	First, replace the contents of lower 8 bits of PC with the E register and AC contents. Then, loads the ROM data at an address specified by the new contents of the lower 8 bits of PC into the E register and AC.		
	RTBLP	Read table data from program ROM then output to P4,5	0 1 0 1	1 0 0 0	1	2	Port 4, 5←(ROM(PCh, E, AC))	First, replaces the contents of lower 8 bits of AC with the E register and AC contents. Then, outputs the ROM data at an address specified by the new contents of the lower 8 bits of PC to ports 4 and 5.		
Data pointer manipulation instructions	LDZ i4	Load DPH with zero and DPL with immediate data respectively	0 1 1 0	$I_3 I_2 I_1 I_0$	1	1	$DP_H \leftarrow 0$, $DP_L \leftarrow I_3 I_2 I_1 I_0$	Loads the data of 0 (zero) and immediate data i4 into the DPH and DPL respectively.		
	LHI i4	Load DPH with immediate data	1 1 0 0 / 0 0 0 0	1 1 1 1 / $I_3 I_2 I_1 I_0$	2	2	$DP_H \leftarrow I_3 I_2 I_1 I_0$	Loads immediate data i4 into the DPH.		
	LLI i4	Load DPL with immediate data	1 1 0 0 / 0 0 0 1	1 1 1 1 / $I_3 I_2 I_1 I_0$	2	2	$DP_L \leftarrow I_3 I_2 I_1 I_0$	Loads immediate data i4 into the DPL.		
	LHLI i8	Load DPH, DPL with immediate data	1 1 0 0 / $I_7 I_6 I_5 I_4$	0 0 0 0 / $I_3 I_2 I_1 I_0$	2	2	$DP_H \leftarrow I_7 I_6 I_5 I_4$, $DP_L \leftarrow I_3 I_2 I_1 I_0$	Loads immediate data into the DPH and DPL.		
	LXYI i8	Load DPX, DPY with immediate data	1 1 0 0 / $I_7 I_6 I_5 I_4$	0 0 1 0 / $I_3 I_2 I_1 I_0$	2	2	$DP_X \leftarrow I_7 I_6 I_5 I_4$, $DP_Y \leftarrow I_3 I_2 I_1 I_0$	Loads immediate data into the DPX and DPY.		
	IL	Increment DPL	0 0 0 1	0 0 0 1	1	1	$DP_L \leftarrow (DP_L) + 1$	Increments the contents of the DPL by 1.	ZF	
	DL	Decrement DPL	0 0 1 0	0 0 0 1	1	1	$DP_L \leftarrow (DP_L) - 1$	Decrements the contents of the DPL by 1.	ZF	
	IY	Increment DPY	0 0 0 1	0 0 1 1	1	1	$DP_Y \leftarrow (DP_Y) + 1$	Increments the contents of the DPY by 1.	ZF	
	DY	Decrement DPY	0 0 1 0	0 0 1 1	1	1	$DP_Y \leftarrow (DP_Y) - 1$	Decrements the contents of the DPY by 1.	ZF	
	TAH	Transfer AC to DPH	1 1 0 0 / 1 1 1 1	1 1 1 1 / 0 0 0 0	2	2	$DP_H \leftarrow (AC)$	Transfers the contents of the accumulator (AC) to the DPH.		
	THA	Transfer DPH to AC	1 1 0 0 / 1 1 1 0	1 1 1 1 / 0 0 0 0	2	2	$AC \leftarrow (DP_H)$	Transfers the contents of the DPH to the AC.	ZF	
	XAH	Exchange AC with DPH	0 1 0 0	0 0 0 0	1	1	$(AC) \leftrightarrow (DP_H)$	Exchanges the contents of the accumulator (AC) and the DPH.		
	TAL	Transfer AC to DPL	1 1 0 0 / 1 1 1 1	1 1 1 1 / 0 0 0 1	2	2	$DP_L \leftarrow (AC)$	Transfers the contents of the accumulator (AC) to the DPL.		
	TLA	Transfer DPL to AC	1 1 0 0 / 1 1 1 0	1 1 1 1 / 0 0 0 1	2	2	$AC \leftarrow (DP_L)$	Transfers the contents of the DPL to the accumulator (AC).	ZF	
	XAL	Exchange AC with DPL	0 1 0 0	0 0 0 1	1	1	$(AC) \leftrightarrow (DP_L)$	Exchanges the contents of the AC and DPL.		
	TAX	Transfer AC to DPX	1 1 0 0 / 1 1 1 1	1 1 1 1 / 0 0 1 0	2	2	$DP_X \leftarrow (AC)$	Transfers the contents of the accumulator (AC) to the DPX.		
	TXA	Transfer DPX to AC	1 1 0 0 / 1 1 1 0	1 1 1 1 / 0 0 1 0	2	2	$AC \leftarrow (DP_X)$	Transfers the contents of DPX to the AC.	ZF	
	XAX	Exchange AC with DPX	0 1 0 0	0 0 1 0	1	1	$(AC) \leftrightarrow (DP_X)$	Exchanges the contents of the AC and DPX.		
	TAY	Transfer AC to DPY	1 1 0 0 / 1 1 1 1	1 1 1 1 / 0 0 1 1	2	2	$DP_Y \leftarrow (AC)$	Transfers the contents of the accumulator (AC) to the DPY.		
	TYA	Transfer DPY to AC	1 1 0 0 / 1 1 1 0	1 1 1 1 / 0 0 1 1	2	2	$AC \leftarrow (DP_Y)$	Transfers the contents of the DPY to the AC.	ZF	
	XAY	Exchange AC with DPY	0 1 0 0	0 0 1 1	1	1	$(AC) \leftrightarrow (DP_Y)$	Exchanges the contents of the accumulator (AC) and the DPY.		
Flag manipulation instructions	SFB n4	Set flag bit	0 1 1 1	$n_3 n_2 n_1 n_0$	1	1	$Fn \leftarrow 1$	Sets a flag specified by n4.		
	RFB n4	Reset flag bit	0 0 1 1	$n_3 n_2 n_1 n_0$	1	1	$Fn \leftarrow 0$	Resets a flag specified by n4.	ZF	
Jump/subroutine instructions	JMP addr	Jump in the current bank	1 1 1 0 / $P_7 P_6 P_5 P_4$	$P_{11} P_{10} P_9 P_8$ / $P_3 P_2 P_1 P_0$	2	2	PC12←PC12, PC11-0←$P_{11} \sim P_0$	Jumps to an address specified by immediate data $P_{11} \sim P_0$ in the current bank.		When executed immediately after the BANK instruction, PC12←(PC12)
	JPEA	Jump to the address stored at E and AC in the current page	0 0 1 0	0 1 1 1	1	1	PC12~PC8←PC12~PC8, PC7-4←(E), PC3-0←(AC)	Jumps to an address specified by the contents of the E register and accumulator (AC) which have replaced the contents of lower 8 bits of the program counter (PC).		

Instruction type	Mnemonics		Instruction code		Bytes	Cycles	Function	Description	Status flags affected	Remarks
			$D_7D_6D_5D_4$	$D_3D_2D_1D_0$						
Jump/subroutine instructions	CAL addr	Call subroutine	0 1 0 1 $P_7P_6P_5P_4$	0 $P_{10}P_9P_8$ $P_3P_2P_1P_0$	2	2	PC12~11←0 PC10~0← P_{10}~P_0 M4(SP)←(CF, ZF, PC13~0) SP←(SP)-4	Calls a subroutine.		
	CZP addr	Call subroutine in the zero page	1 0 1 0	$P_3P_2P_1P_0$	1	2	PC12~6, PC1~0←0 PC5~2←P_3~P_0 M4(SP)←(CF, ZF, PC13~0) SP←SP-4	Calls a subroutine in page 0 of bank 0.		
	BANK	Change bank	0 0 0 1	1 0 1 1	1	1		Changes memory banks and register banks.		
	PUSH reg	Push reg on M2(SP)	1 1 0 0 1 1 1 1	1 1 1 1 1 $i_1 i_0$ 0	2	2	M2(SP)←(reg) SP←(SP)-2	Stores the contents of reg into the M2(SP) and then subtracts 2 from the stack pointer (SP). reg / i_1 i_0 — HL / 0 0 — XY / 0 1 — AE / 1 0 — Inhibited / 1 1		
	POP reg	Pop reg off M2(SP)	1 1 0 0 1 1 1 0	1 1 1 1 1 $i_1 i_0$ 0	2	2	SP←(SP)+2 reg←(M2(SP))	Stores the contents of reg into the M2(SP) and then increments the contents of the stack pointer (SP) by 2 and loads the contents of M2(SP) into a reg. Refer to the PUSH reg instruction for the relationship between i1i0 and reg.		
	RT	Return from subroutine	0 0 0 1	1 1 0 0	1	2	SP←(SP)+4 PC←(M4(SP))	Returns execution from a subroutine or interrupt processing routine back to the routine that called it. The contents of the carry flag (CF) and zero flag (ZF) are not returned from the stack area.		
	RTI	Return from interrupt routine	0 0 0 1	1 1 0 1	1	2	SP←(SP)+4 PC←(M4(SP)) CF, ZF←(M4(SP))	Returns execution from a subroutine or interrupt processing routine back to the routine that called it. The contents of the carry flag (CF) and zero flag (ZF) are returned from the stack area.	ZF, CF	
Branch instructions	BAt2 addr	Branch on AC bit	1 1 0 1 $P_7P_6P_5P_4$	0 0 $t_1 t_0$ $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(AC, t2)= 1	Transfers execution to an address specified by the contents of P7 to P0 in the current page if a bit specified by immediate data t1t0 of AC is 1 (program branch).		
	BNAt2 addr	Branch on no AC bit	1 0 0 1 $P_7P_6P_5P_4$	0 0 $t_1 t_0$ $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(AC, t2)= 0	Transfers execution to an address specified by the contents of P7 to P0 in the current page if a bit specified by immediate data t1t0 of AC is 0 (program branch).		
	BMt2 addr	Branch on M bit	1 1 0 1 $P_7P_6P_5P_4$	0 1 $t_1 t_0$ $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(M(HL), t2)=1	Transfers execution to an address specified by the contents of P7 to P0 in the current page if a bit specified by immediate data t1t0 of M(HL) is 1 (program branch).		
	BNMt2 addr	Branch on no M bit	1 0 0 1 $P_7P_6P_5P_4$	0 1 $t_1 t_0$ $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(M(HL), t2)=0	Transfers execution to an address specified by the contents of P7 to P0 in the current page if a bit specified by immediate data t1t0 of M(HL) is 0 (program branch).		
	BPt2 addr	Branch on Port bit	1 1 0 1 $P_7P_6P_5P_4$	1 0 $t_1 t_0$ $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(P(DPL), t2)=1	Transfers execution to an address specified by the contents of P7 to P0 in the current page if a bit specified by immediate data t1t0 of the port accessed by DPL is 1 (program branch).		Used to manipulate internal control registers if executed immediately after the BANK instruction. In this case, the internal control registers must be readable.
	BNPt2 addr	Branch on no Port bit	1 0 0 1 $P_7P_6P_5P_4$	1 0 $t_1 t_0$ $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(P(DPL), t2)=0	Transfers execution to an address specified by the contents of P7 to P0 in the current page if a bit specified by immediate data t1t0 of the port accessed by DPL is 0 (program branch).		Same as above.
	BC addr	Branch on CF	1 1 0 1 $P_7P_6P_5P_4$	1 1 0 0 $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(CF)=1	Transfers execution to an address specified by the contents of P7 to P0 in the current page if the content of the carry flag (CF) is 1 (program branch).		
	BNC addr	Branch on no CF	1 0 0 1 $P_7P_6P_5P_4$	1 1 0 0 $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(CF)=0	Transfers execution to an address specified by the contents of P7 to P0 in the current page if the content of the carry flag (CF) is 0 (program branch).		
	BZ addr	Branch on ZF	1 1 0 1 $P_7P_6P_5P_4$	1 1 0 1 $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(ZF)=1	Transfers execution to an address specified by the contents of P7 to P0 in the current page if the content of the zero flag (ZF) is 1 (program branch).		
	BNZ addr	Branch on no ZF	1 0 0 1 $P_7P_6P_5P_4$	1 1 0 1 $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(ZF)=0	Transfers execution to an address specified by the contents of P7 to P0 in the current page if the content of the zero flag (ZF) is 0 (program branch).		

Instruction type	Mnemonics		Instruction code $D_7D_6D_5D_4$	$D_3D_2D_1D_0$	Bytes	Cycles	Function	Description	Status flags affected	Remarks
Branch instructions	BFn4 addr	Branch on flag bit	1 1 1 1 $P_7P_6P_5P_4$	$n_3n_2n_1n_0$ $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(Fn)=1	Transfers execution to an address specified by the contents of P7 to P0 in the current page if the content of the flag specified by n3n2n1n0 is 1. The flag is one of the 16 flags.		
	BNFn4 addr	Branch on no flag bit	1 0 1 1 $P_7P_6P_5P_4$	$n_3n_2n_1n_0$ $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(Fn)=0	Transfers execution to an address specified by the contents of P7 to P0 in the current page if the content of the flag specified by n3n2n1n0 is 0. The flag is one of the 16 flags.		
Input/output instructions	IP0	Input port 0 to AC	0 0 1 0	0 0 0 0	1	1	AC←(P0)	Inputs the contents of port 0 to the accumulator (AC).	ZF	
	IP	Input port to AC	0 0 1 0	0 1 1 0	1	1	AC←(P(DP$_L$))	Inputs the contents of port accessed by DPL to the accumulator (AC).	ZF	
	IPM	Input port to M	0 0 0 1	1 0 0 1	1	1	M(HL)←(P(DP$_L$))	Inputs the contents of port accessed by DPL to the M(HL).		
	IPDR i4	Input port to AC direct	1 1 0 0 0 1 1 0	1 1 1 1 $I_3 I_2 I_1 I_0$	2	2	AC←(P(i4))	Inputs the contents of port accessed by i4 to the accumulator (AC).	ZF	
	IP45	Input port 4,5 to E, AC respectively	1 1 0 0 1 1 0 1	1 1 1 1 0 1 0 0	2	2	E ←(P(4)) AC←(P(5))	Inputs the contents of ports 4 and 5 to the E register and accumulator (AC) respectively.		
	OP	Output AC to port	0 0 1 0	0 1 0 1	1	1	P(DP$_L$)←(AC)	Outputs the contents of the accumulator (AC) to a port accessed by DPL.		
	OPM	Output M to port	0 0 0 1	1 0 1 0	1	1	P(DP$_L$)←(M(HL))	Outputs the contents of the M(HL) to a port accessed by DPL.		
	OPDR i4	Output AC to port direct	1 1 0 0 0 1 1 1	1 1 1 1 $I_3 I_2 I_1 I_0$	2	2	P(4)←(AC)	Outputs the contents of the accumulator (AC) to a port accessed by i4.		
	OP45	Output E, AC to port 4,5 respectively	1 1 0 0 1 1 0 1	1 1 1 1 0 1 0 1	2	2	P(4)←(E) P(5)←(AC)	Outputs the contents of the E register and accumulator (AC) to ports 4 and 5 respectively.		
	SPB t2	Set port bit	0 0 0 0	1 0 $t_1 t_0$	1	1	(P(DP$_L$), t2)←1	Sets a bit specified by immediate data t1t0 of a port accessed by DPL.		
	RPB t2	Reset port bit	0 0 1 0	1 0 $t_1 t_0$	1	1	(P(DP$_L$), t2)←0	Resets a bit specified by immediate data t1t0 of a port accessed by DPL.	ZF	
	ANDPDR i4, p4	AND port with immediate data then output	1 1 0 0 $I_3 I_2 I_1 I_0$	0 1 0 1 $P_3P_2P_1P_0$	2	2	P(P_3~P_0)←(P(P_3~P_0))∨I_3~I_0	Performs a logical AND operation between the contents of a port specified by P3 to P0 and immediate data I3I2I1I0 and outputs the resulted product to the port.	ZF	
	ORPDR i4, p4	OR port with immediate data then output	1 1 0 0 $I_3 I_2 I_1 I_0$	0 1 0 0 $P_3P_2P_1P_0$	2	2	P(P_3~P_0)←(P(P_3~P_0))∨I_3~I_0	Performs a logical OR operation between the contents of a port specified by P3 to P0 and immediate data I3I2I1I0 and outputs the resulted sum to the port.	ZF	
Timer control instructions	WTTM0	Write timer 0	1 1 0 0	1 0 1 0	1	2	TIMER0←(M2(HL)), (AC)	Writes the contents of the M(HL) and the accumulator (AC) to the timer 0 reload register.		
	WTTM1	Write timer 1	1 1 0 0 1 1 1 1	1 1 1 1 0 1 0 0	2	2	TIMER1←(E), (AC)	Writes the contents of the E register and the accumulator (AC) to the timer 1 reload register.		
	RTIM0	Read timer 0	1 1 0 0	1 0 1 1	1	2	M2(HL), AC← (TIMER0)	Reads the contents of the timer 0 counter into the M2(HL) and the accumulator (AC).		
	RTIM1	Read timer 1	1 1 0 0 1 1 1 1	1 1 1 1 0 1 0 1	2	2	E, AC← (TIMER1)	Reads the contents of the timer 1 counter into the E register and the accumulator (AC).		
	START0	Start timer 0	1 1 0 0 1 1 1 0	1 1 1 1 0 1 1 0	2	2	Start timer 0 counter	Starts the timer 0 counter operation.		
	START1	Start timer 1	1 1 0 0 1 1 1 0	1 1 1 1 0 1 1 1	2	2	Start timer1 counter	Starts the timer 1 counter operation.		
	STOP0	Stop timer 0	1 1 0 0 1 1 1 1	1 1 1 1 0 1 1 0	2	2	Stop timer 0 counter	Stops the timer 0 counter operation.		
	STOP1	Stop timer 1	1 1 0 0 1 1 1 1	1 1 1 1 0 1 1 1	2	2	Stop timer1 counter	Stops the timer 1 counter operation.		

Instruction type	Mnemonics		Instruction code		Bytes	Cycles	Function	Description	Status flags affected	Remarks
			$D_7D_6D_5D_4$	$D_3D_2D_1D_0$						
Interrupt control instructions	MSET	Set Interrupt Master Enable Flag	1100 0101	1101 0000	2	2	MSE←1	Sets the interrupt master enable flag.		
	MRESET	Reset Interrupt Master Enable Flag	1100 1001	1101 0000	2	2	MSE←0	Resets the interrupt master enable flag.		
	EIH i4	Enable interrupt high	1100 0101	1101 $i_3i_2i_1i_0$	2	2	EDIH←(EDIH)∨i4	Sets the interrupt enable flag.		
	EIL i4	Enable interrupt low	1100 0100	1101 $i_3i_2i_1i_0$	2	2	EDIL←(EDIL)∨i4	Sets the interrupt enable flag.		
	DIH i4	Disable interrupt high	1100 1001	1101 $i_3i_2i_1i_0$	2	2	EDIH←(EDIH)∧$\overline{i4}$	Resets the interrupt enable flag.	ZF	
	DIL i4	Disable interrupt low	1100 1000	1101 $i_3i_2i_1i_0$	2	2	EDIL←(EDIL)∧$\overline{i4}$	Resets the interrupt enable flag.	ZF	
	WTSP	Write SP	1100 1101	1111 1010	2	2	SP←(E),(AC)	Transfers the contents of the E register and accumulator (AC) to the stack area.		
	RSP	Read SP	1100 1101	1111 1011	2	2	E,AC←(SP)	Transfers the contents of the stack area to the E register and accumulator (AC).		
Standby control instructions	HALT	HALT	1100 1101	1111 1110	2	2	HALT	Selects the HALT mode.		
	HOLD	HOLD	1100 1101	1111 1111	2	2	HOLD	Selects the HOLD mode.		
Serial I/O control instructions	STARTS	Start serial I/O	1100 1110	1111 1110	2	2	START SIO	Starts the SIO operation mode.		
	WTSIO	Write serial I/O	1100 1110	1111 1111	2	2	SIO←(E),(AC)	Writes the contents of the E register and accumulator (AC) to the SIO register.		
	RSIO	Read serial I/O	1100 1111	1111 1111	2	2	E,AC←(SIO)	Reads the contents of the SIO register into the E register and the accumulator (AC).		
Other instructions	NOP	No operation	0000	0000	1	1	No operation	A dummy instruction that is coded 00H and has no effect when executed. Just one machine cycle signal reaches the CPU.		
	SB i2	Select bank	1100 1100	1111 00i_1i_0	2	2	PC12←i_1i_0	Selects memory banks.		