

**SANYO**

No. 3113B

**LC66304A, 66306A, 66308A**

4K/6K/8K-BYTE ROM-CONTAINED  
SINGLE-CHIP 4-BIT MICROCOMPUTER  
FOR CONTROL-ORIENTED APPLICATIONS

**General Description**

The LC66304A, 66306A, 66308A are 42-pin package type CMOS 4-bit single-chip microcomputers. They contain a ROM, a RAM, I/O ports, a dual 8-bit serial interface, a 4-channel comparator input, a dual 3-level input port, a 12-bit timer, an 8-bit timer, and provide 8 interrupt sources with 8 vector addresses.

**Features**

- (1) On-chip 4K-byte/6K-byte/8K-byte ROM, 512x4-bit RAM
- (2) Instruction set with 128 instructions common with the LC665XX series
- (3) I/O ports ---- 36 pins
- (4) 8-bit serial interface ---- 2 lines (16-bit cascade connection available)
- (5) Minimum instruction cycle time ---- 0.92 $\mu$ s (4.3MHz external clock input mode)
- (6) Powerful timer function and prescaler  
12-bit timer-used interval timer, event counter, pulse width measurement, burst pulse output  
8-bit timer-used interval timer, event counter, PWM output, burst pulse output  
12-bit prescaler-used time base function
- (7) Powerful 8-source 8-vector interrupt function  
External interrupt: 3 sources, 3 vector addresses  
Internal interrupt: 5 sources, 5 vector addresses (timer: 2 sources, serial I/O: 2 sources, prescaler)
- (8) Flexible I/O function  
Comparator input, 3-level input, 20mA drive output, 15V breakdown voltage, pull-up/open drain selectable by option
- (9) Runaway detection function (option)
- (10) 8-bit input/output function
- (11) HALT/HOLD mode-used power-down function
- (12) Package: DIP42S, QFP48E (QIP48E)
- (13) Evaluation LSI: LC66599 (evaluation chip) + EVA850/800-TB6630X, LC66E308 (microcomputer with EPROM)

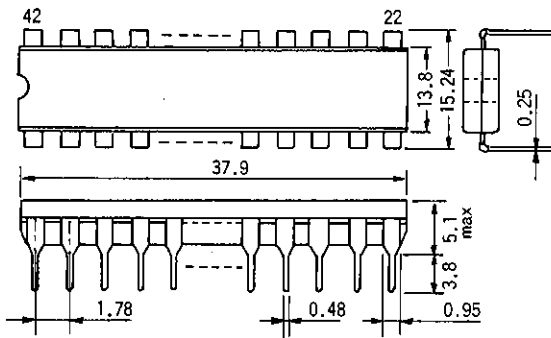
**Series Lineup**

Type No.	Pins	ROM capacity	RAM capacity	Package	Remark
LC66304A/306A/308A	42,48	4K/6K/8KB	512W	DIP42S, QFP48E	Available
LC66354A/356A/358A	42,48	4K/6K/8KB	512W	DIP42S, QFP48E	Available
LC66354S/356S/358S	44	4K/6K/8KB	512W	QFP44M	Under development
LC66E308	42,48	EPROM 8KB	512W	DIC42S, QFC48 with window	Available
LC66P308	42,48	OTPROM 8KB	512W	DIP42S, QFP48E	Available
LC66404A/406A/408A	42,48	4K/6K/8KB	512W	DIP42S, QFP48E	Available
LC66E408	42,48	EPROM 8KB	512W	DIC42S, QFC48 with window	Available
LC66P408	42,48	OTPROM 8KB	512W	DIP42S, QFP48E	Available
LC66506B/508B/512B/516B	64	6K/8K/12K/16KB	512W	DIP64S, QFP64A	Available
LC66556A/558A/562A/566A	64	6K/8K/12K/16KB	512W	DIP64S, QFP64E	Available
LC66354B/356B/358B	42,48	4K/6K/8KB	512W	DIP42S, QFP48E	Available
LC66566B/558B	64	6K/8K	512W	DIP64S, QFP64E	Under development
LC66562B/566B	64	12K/16KB	512W	DIP64S, QFP64E	Available
LC66E516	64	EPROM 16KB	512W	DIC64S, QFC64 with window	Available
LC66P516	64	OTPROM 16KB	512W	DIP64S, QFP64E	Available

**SANYO Electric Co., Ltd. Semiconductor Business Headquarters**  
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

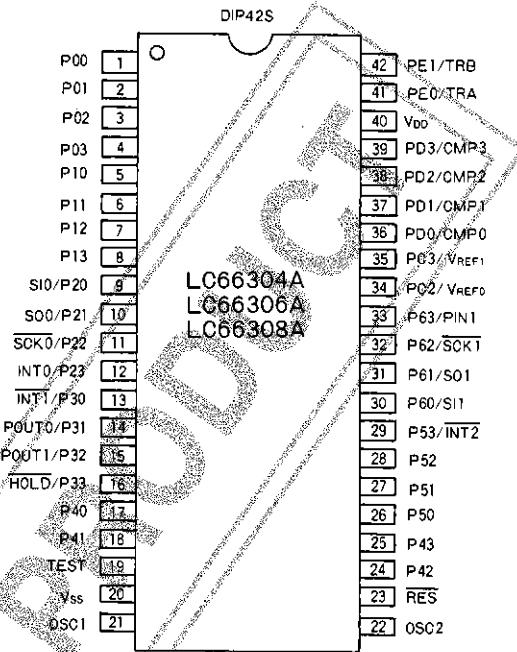
Package Dimensions 3025B

(unit : mm)



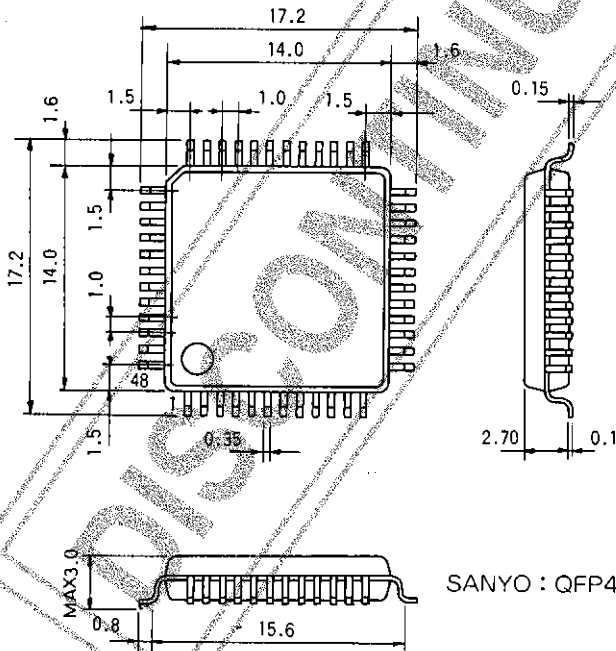
SANYO : DIP42S

Pin Assignment



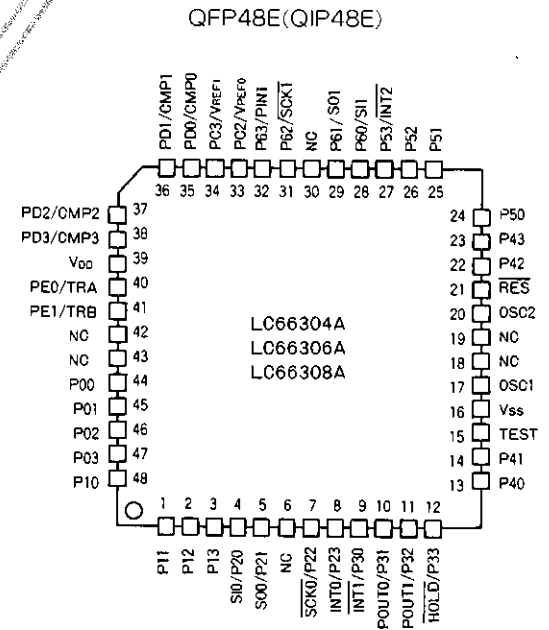
Package Dimensions 3156

(unit : mm)



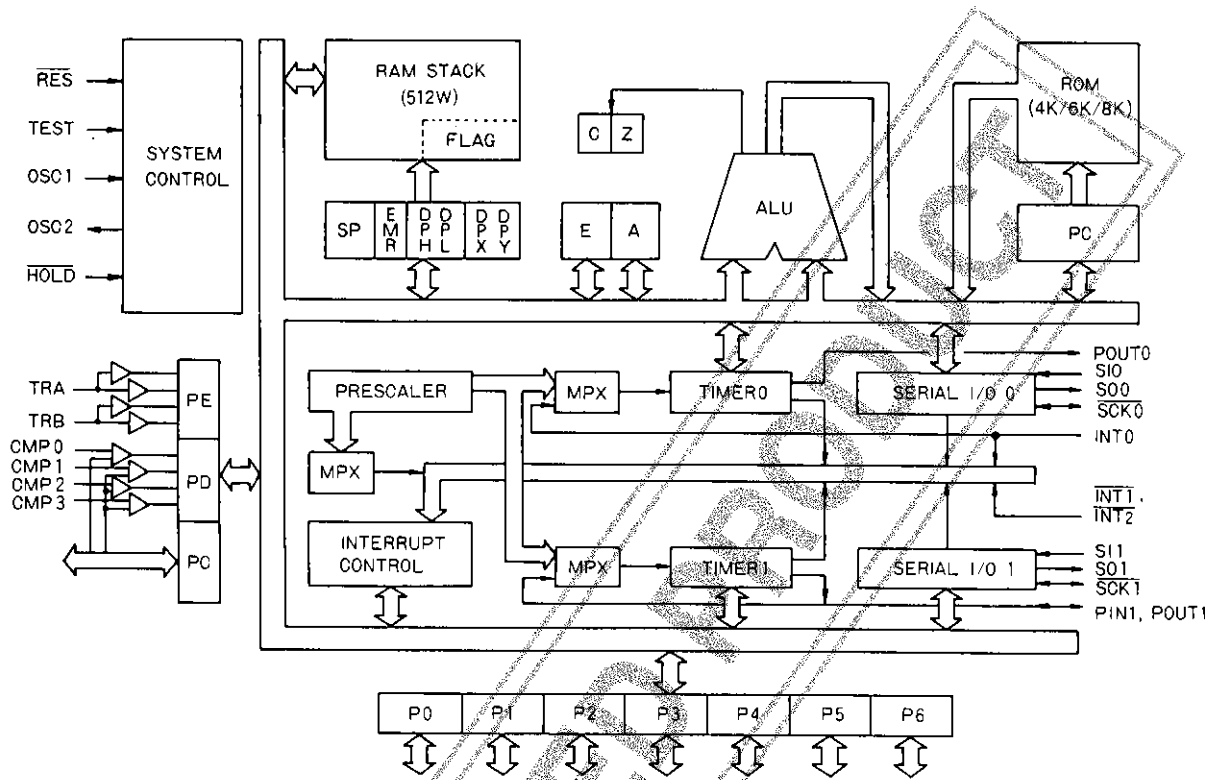
SANYO : QFP48E(QIP48E)

Pin Assignment



Note) Reflow soldering is recommended for QFP (QIP) packages.  
Please consult your local representative for information on solder-bath immersion of the device.

System Block Diagram



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## Pin Description

Pin Name	I/O	Functions	Output Driver Type	Option	During Reset
P00 P01 P02 P03	I/O	Input/output common port P00 to P03 <ul style="list-style-type: none"> <li>4-bit and single-bit input/output</li> <li>P00 to P03: Provided with HALT mode control function</li> </ul>	<ul style="list-style-type: none"> <li>Pch: Pu MOS type</li> <li>Nch: Sink medium current type</li> </ul>	<ul style="list-style-type: none"> <li>With Pu MOS or Nch OD output</li> <li>Output level during reset</li> </ul>	H or L (option)
P10 P11 P12 P13	I/O	Input/output common port P10 to P13 <ul style="list-style-type: none"> <li>4-bit and single-bit input/output</li> </ul>	<ul style="list-style-type: none"> <li>Pch: Pu MOS type</li> <li>Nch: Sink medium current type</li> </ul>	<ul style="list-style-type: none"> <li>With Pu MOS or Nch OD output</li> <li>Output level during reset</li> </ul>	H or L (option)
P20/SI0 P21/SO0 P22/SCK0 P23/INT0	I/O	Input/output common port P20 to P23 <ul style="list-style-type: none"> <li>4-bit and single-bit input/output</li> <li>P20: Common with serial input SI0</li> <li>P21: Common with serial output SO0</li> <li>P22: Common with serial clock SCK0</li> <li>P23: Common with INT0 interrupt and timer 0 used event count, pulse width measurement input</li> </ul>	<ul style="list-style-type: none"> <li>Pch: CMOS type</li> <li>Nch: Sink medium current type</li> <li>+15V breakdown voltage at Nch OD configuration</li> </ul>	<ul style="list-style-type: none"> <li>CMOS or Nch OD output</li> </ul>	H
P30/INT1 P31/POUT0 P32/POUT1	I/O	Input/output common port P30 to P32 <ul style="list-style-type: none"> <li>3-bit and single-bit input/output</li> <li>P30: Common with INT1 interrupt request</li> <li>P31: Common with burst pulse output from timer 0</li> <li>P32: Common with burst pulse output, PWM output from timer 1</li> </ul>	<ul style="list-style-type: none"> <li>Pch: CMOS type</li> <li>Nch: Sink medium current type</li> <li>+15 breakdown voltage at Nch OD configuration</li> </ul>	<ul style="list-style-type: none"> <li>CMOS or Nch OD output</li> </ul>	H
P33/HOLD	I	HOLD mode control input <ul style="list-style-type: none"> <li>The HOLD mode is entered by executing the HOLD instruction at <math>\overline{\text{HOLD}}=\text{L}</math>.</li> <li>The CPU is restarted by setting the <math>\overline{\text{HOLD}}</math> to H level at the HOLD mode.</li> <li>Usable as input port P33 with P30 to P32</li> <li>Even if the <math>\overline{\text{RES}}</math> is brought to L level when the P33/<math>\overline{\text{HOLD}}</math> is at L level, the CPU is not reset. So this pin must be H level when <math>V_{\text{DD}}</math> has risen to a point where the CPU can operate properly.</li> </ul>			

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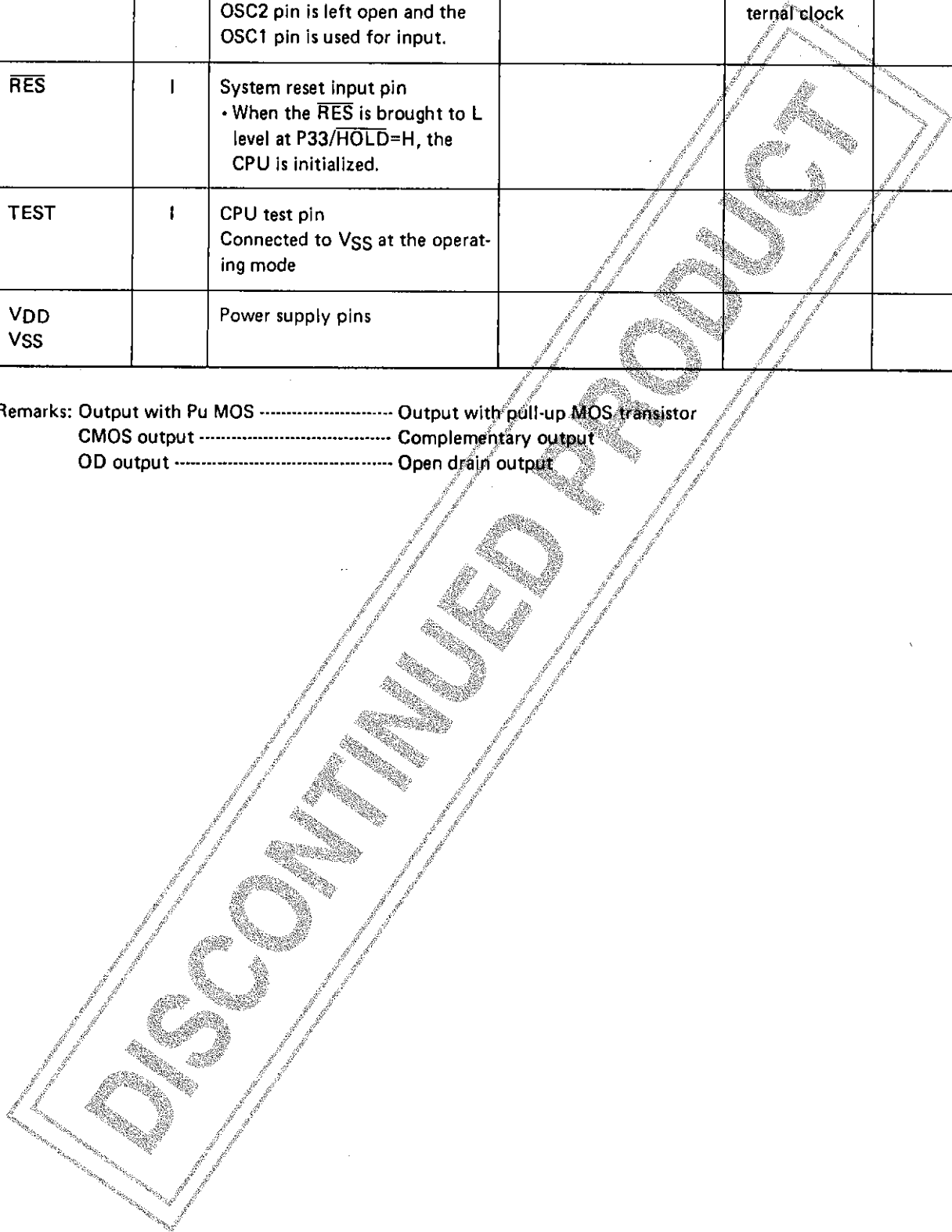
Pin Name	I/O	Functions	Output Driver Type	Option	During Reset
P40 P41 P42 P43	I/O	Input/output port P40 to P43 • 4-bit and single-bit input/output • 8-bit input/output with P50 to P53 • 8-bit output of ROM data with P50 to P53	• Pch: Pu MOS type • Nch: Sink medium current type • +15 breakdown voltage at Nch OD configuration	• With Pu MOS or Nch OD output	H
P50 P51 P52 P53/ $\overline{\text{INT2}}$	I/O	Input/output port P50 to P53 • 4-bit and single-bit input/output • 8-bit input/output with P40 to P43 • 8-bit output of ROM data with P40 to P43 • P53: Common with $\overline{\text{INT2}}$ interrupt request	• Pch: Pu MOS type • Nch: Sink medium current type • +15 breakdown voltage at Nch OD configuration	• With Pu MOS or Nch OD output	H
P60/SI1 P61/SO1 P62/SCK1 P63/PIN1	I/O	Input/output common port P60 to P63 • 4-bit and single-bit input/output • P60: Common with serial input SI1 • P61: Common with serial output SO1 • P62: Common with serial clock SCK1 • P63: Common with event counter input of timer 1	• Pch: CMOS type • Nch: Sink medium current type • +15V breakdown voltage at Nch OD configuration	• CMOS or Nch OD output	H
PC2/VREF0 PC3/VREF1	I/O	Input/output common port PC2 to PC3 • 2-bit and single-bit input/output • PC2: Common with VREF0 comparator comparison voltage pin • PC3: Common with VREF1 comparator comparison voltage pin	• Pch: CMOS type • Nch: Sink medium current type	• CMOS or Nch OD output	H
PD0/CMP0 PD1/CMP1 PD2/CMP2 PD3/CMP3	I	Input-only port PD0 to PD3 • The comparator input is software-selectable. • The comparison voltage of PD0 is VREF0. • The comparison voltage of PD1 to PD3 is VREF1. • The comparator is specified in units of PD0, PD1, (PD2, PD3).			Normal input
PE0/TRA PE1/TRB	I	Input-only port • The 3-level input port is software-selectable.			Normal input

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OSC1 OSC2	I O	Pins for externally connecting R, C or a ceramic resonator for system clock generation. For the external clock mode, the OSC2 pin is left open and the OSC1 pin is used for input.		• Ceramic resonator OSC, RC OSC, or external clock	
RES	I	System reset input pin • When the RES is brought to L level at P33/HOLD=H, the CPU is initialized.			
TEST	I	CPU test pin Connected to VSS at the operating mode			
VDD VSS		Power supply pins			

Remarks: Output with Pu MOS ----- Output with pull-up MOS transistor  
 CMOS output ----- Complementary output  
 OD output ----- Open drain output



**User Options**

(1) Options of ports 0, 1 output level during reset

For input/output ports 0, 1 either of the following two output levels may be selected in a group of 4 bits during reset by option

Option Name	Conditions, etc.
1. Output during reset: "H" level	All of 4 bits of ports 0, 1
2. Output during reset: "L" level	All of 4 bits of ports 0, 1

(2) Oscillator Circuit Options

Option Name	Circuit	Conditions, etc.
1. External clock		• Input: Schmitt type
2. 2-pin RC OSC		• Input: Schmitt type
3. Ceramic resonator OSC		

(3) Watchdog timer option

The presence or absence of the runaway detection function (watchdog timer) may be selected by option.

(4) Options of port output configuration

For each port of P0, P1, P2, P3 (except P33/HOLD), P4, P5, P6, PC, either of the following two output configurations may be selected by option (in bit units).

Option Name	Circuit	Conditions, etc.
1. Open drain type output		P2, P3, P5, P6: Schmitt input
2. Output with pull-up resistance		P2, P3, P5, P6: Schmitt input CMOS output (P2, P3, P6, PC) or Pu MOS output (P0, P1, P4, P5) is selected according to Pch Tr drive capacity.

Main Specifications

(1) Absolute Maximum Ratings at Ta=25°C, VSS=0V

Parameter	Symbol	Applicable Pins, Remarks	Conditions	Limits	Unit	Note
Maximum Supply Voltage	VDD max	VDD		-0.3 to +7.0	V	
Input Voltage	VIN(1)	P2,P3(except P33/HOLD), P4,P5,P6		-0.3 to +15.0	V	1
	VIN(2)	Other inputs		-0.3 to VDD+0.3	V	2
Output Voltage	VOUT(1)	P2,P3(except P33/HOLD), P4,P5,P6		-0.3 to +15.0	V	1
	VOUT(2)	Other outputs		-0.3 to VDD+0.3	V	2
Output Current per Pin	ION	P0,P1,P2,P3(except P33/HOLD),PC,P4,P5,P6		20	mA	3
	-IOP(1)	P0,P1,P4,P5		2	mA	4
	-IOP(2)	P2,P3(except P33/HOLD), P6,PC		4	mA	4
Total Pin Current	ΣION(1)	P0,P1,P2,P3(except P33/HOLD),P40,P41		75	mA	3
	ΣION(2)	P5,P6,P42,P43,PC		75	mA	3
	-ΣIOP(1)	P0,P1,P2,P3(except P33/HOLD),P40,P41		25	mA	4
	-ΣIOP(2)	P5,P6,P42,P43,PC		25	mA	4
Allowable Power Dissipation	Pd max	Ta=-30 to +70°C	DIP-42S (QFP,48E)	600 (430)	mW	5
Operating Temperature	Topr			-30 to +70	°C	
Storage Temperature	Tstg			-55 to +125	°C	

(Note 1) Applicable only when the open-drain output type is selected. If other type than the open drain output is selected, the specification indicated in the column for other pins applies.

(Note 2) For OSC input/output, up to self OSC level is allowable.

(Note 3) Sink current

(Note 4) Source current (applicable only when the pull-up output type or CMOS output type is selected)

(Note 5) Reflow soldering is recommended for QFP packages.

Please consult your local representative for information on solder-bath immersion of the device.

(2) Allowable Operating Conditions at Ta=-30 to +70°C, VSS=0V unless otherwise specified

Parameter	Symbol	Applicable Pins	Conditions	Limits			Unit	Note	
				VDD(V)	min	typ			max
Operating Voltage	VDD	VDD			4.0	5.0	6.0	V	
Data Retention Voltage	VDD(H)	VDD	HOLD mode		1.8		6.0	V	
"H"-Level Input Voltage	VIH(1)	P2,P3(except P33/HOLD), P4,P5,P6	Output Nch Tr OFF	4.0 to 6.0	0.75VDD		+13.5	V	1
	VIH(2)	P33/HOLD, RES, OSC1	Output Nch Tr OFF	4.0 to 6.0	0.75VDD		VDD	V	2
	VIH(3)	P0,P1,PC,PD,PE	Output Nch Tr OFF	4.0 to 6.0	0.7VDD		VDD	V	3
	VIH(4)	PE	3-level input mode	4.0 to 6.0	0.8VDD		VDD	V	

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Parameter	Symbol	Applicable Pins	Conditions	Limits			Unit	Note	
				VDD(V)	min	typ			max
"M"-Level Input Voltage	VIM	PE	3-level input mode	4.0 to 6.0	0.4VDD		0.6VDD	V	
Common-Mode Input Voltage Range	VCMM	PC2, PC3, PD	Comparator input mode	4.0 to 6.0	1.0		VDD - 1.5	V	
"L"-Level Input Voltage	VIL(1)	P2, P3 (except P33/HOLD), P5, P6, RES, OSC1	Output Nch Tr OFF	4.0 to 6.0	VSS		0.25VDD	V	2
	VIL(2)	P33/HOLD		1.8 to 6.0	VSS		0.25VDD	V	
	VIL(3)	PO, P1, P4, PC, PD, PE, TEST	Output Nch Tr OFF	4.0 to 6.0	VSS		0.3VDD	V	3
	VIL(4)	PE	3-level input mode	4.0 to 6.0	VSS		0.2VDD	V	
Operating Frequency (Instruction Cycle Time)	fOP (TCYC)			4.0 to 6.0	0.4 (10)		4.35 (0.92)	MHz (μs)	
External Clock Input Conditions	Frequency	fext	OSC1	See Fig. 1. The OSC1 is used for input and the OSC2 is left open. (OSC option: External clock input)	4.0 to 6.0	0.4		4.35	MHz
	Pulse Width	t <sub>extH</sub> t <sub>extL</sub>		See Fig. 1. The OSC1 is used for input and the OSC2 is left open. (OSC option: External clock input)	4.0 to 6.0	70			ns
	Rise/Fall Time	t <sub>extR</sub> t <sub>extF</sub>		See Fig. 1. The OSC1 is used for input and the OSC2 is left open. (OSC option: External clock input)	4.0 to 6.0			30	ns
Self OSC Conditions	OSC Frequency	f <sub>CF</sub>	OSC1, OSC2	See Fig. 2. 4MHz	4.0 to 6.0		4.0		MHz
	OSC Stabilizing Period	t <sub>CFS</sub>		Fig. 3 4MHz	4.0 to 6.0			10	ms
	External Constants for RC OSC	C <sub>ext</sub> R <sub>ext</sub>	OSC1, OSC2	See Fig. 4.	4.0 to 6.0		100 2.7		pF kΩ

(Note 1) Applicable to pins of open drain type. For P33/HOLD, VIH(2) applies.  
P2, P3, P6 of CMOS output type cannot be used as input pin.

(Note 2) Applicable to pins of open drain type.

(Note 3) When PE is used for 3-level input, VIH(4), VIM, VIL(4) apply. PC of CMOS output type cannot be used as input pin.

(3) Electrical Characteristics at Ta=−30 to +70°C, VSS=0V unless otherwise specified

Parameter	Symbol	Applicable Pins	Conditions	VDD (V)	Limits			Unit	Note
					min	typ	max		
"H"-Level Input Current	I <sub>IH</sub> (1)	P2,P3 (except P33/HOLD), P4,P5,P6	V <sub>IN</sub> =13.5V Output Nch Tr OFF	4.0to6.0			5.0	μA	1
	I <sub>IH</sub> (2)	P0, P1, OSC1, RES, P33/HOLD	V <sub>IN</sub> =V <sub>DD</sub> Output Nch Tr OFF	4.0to6.0			1.0	μA	1
	I <sub>IH</sub> (3)	PC2,PC3,PD,PE	V <sub>IN</sub> =V <sub>DD</sub> Output Nch Tr OFF	4.0to6.0			1.0	μA	1
"L"-Level Input Current	I <sub>IL</sub> (1)	Inputs other than PC2,PC3,PD,PE	V <sub>IN</sub> =V <sub>SS</sub> Output Nch Tr OFF	4.0to6.0	−1.0			μA	2
	I <sub>IL</sub> (2)	PC2, PC3, PD, PE	V <sub>IN</sub> =V <sub>SS</sub> Output Nch Tr OFF	4.0to6.0	−1.0			μA	2
"H"-Level Output Voltage	V <sub>OH</sub> (1)	P2, P3 (except P33/HOLD), P6, PC	I <sub>OH</sub> =−1 mA	4.0to6.0	V <sub>DD</sub> −1.0			V	3
			I <sub>OH</sub> =−0.1mA	4.0to6.0	V <sub>DD</sub> −0.5			V	3
	V <sub>OH</sub> (2)	P0, P1, P4, P5	I <sub>OH</sub> =−200 μA	4.5	2.4			V	4
			I <sub>OH</sub> =−130 μA	4.5to5.5	V <sub>DD</sub> −1.35			V	4
Output Pull-up Current	I <sub>PO</sub>	P0, P1, P4, P5	V <sub>IN</sub> =V <sub>SS</sub>	6.0	−1.6			mA	4
"L"-Level Output Voltage	V <sub>OL</sub> (1)	P0, P1, P2, P3, P4, P5, P6, PC (except P33/HOLD)	I <sub>OL</sub> =1.6mA	4.0to6.0			0.4	V	
	V <sub>OL</sub> (2)	P0,P1,P2,P3,P4,P5,P6 (except P33/HOLD)	I <sub>OL</sub> =10mA	4.0to6.0			1.5	V	
Output OFF-State Leakage Current	I <sub>OFF</sub> (1)	P2,P3,P4,P5,P6	V <sub>IN</sub> =13.5V	4.0to6.0			5.0	μA	5
	I <sub>OFF</sub> (2)	P0, P1, PC	V <sub>IN</sub> =V <sub>DD</sub>	4.0to6.0			1.0	μA	5
Comparator Offset Voltage	V <sub>OFF</sub>	PD	V <sub>IN</sub> =1.0V to V <sub>DD</sub> −1.5V	4.0to6.0		±50	±300	mV	
Schmitt Characteristics	Hysteresis Voltage	V <sub>HYS</sub>	P2,P3,P5,P6, RES, OSC1 (RC,EXT)	4.0to6.0		0.1V <sub>DD</sub>		V	
	"H"-Level Threshold Voltage	V <sub>tH</sub>			0.5V <sub>DD</sub>		0.75V <sub>DD</sub>	V	
	"L"-Level Threshold Voltage	V <sub>tL</sub>			0.25V <sub>DD</sub>		0.5V <sub>DD</sub>	V	
RC OSC Frequency	f <sub>RC</sub>	OSC1, OSC2	See Fig. 4. C=100pF±5% R=2.7kΩ±1%	4.0to6.0	2.0	3.0	4.0	MHz	

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Parameter	Symbol	Applicable Pins	Conditions	Limits			Unit	Note					
				V <sub>DD</sub> (V)	min	typ			max				
Serial Clock	Cycle Time	tCKCY	SCK0, SCK1	Timing of Fig. 5 and timing load of Fig. 6.	4.0 to 6.0	0.9			μs				
					4.0 to 6.0	2.0			T <sub>CKCY</sub>				
	"L"/"H". Level Pulse Width	tCKL			4.0 to 6.0	0.4			μs				
					tCKH	4.0 to 6.0	1.0			T <sub>CKH</sub>			
	Rise/Fall Time	tCKR				tCKF	4.0 to 6.0			0.1	μs		
Serial Input	Data Setup Time	tICK	SIO, SI1	Timing of Fig. 5, specified for SCK0, SCK1 rise (↑)	4.0 to 6.0	0.3			μs				
	Data Hold Time	tCKI			4.0 to 6.0	0.3			μs				
Serial Output	Output Delay Time	tCKO	S00, S01	Timing of Fig. 5 and timing load of Fig. 6, specified for SCK0, SCK1 fall (↓)	4.0 to 6.0			0.3	μs				
Pulse Input Conditions	"H"/"L". Level Pulse Width at INTO	tIOH	INT0	Fig.7. • Condition under which the INTO interrupt is accepted • Condition under which the event counter/pulse width measure input by timer 0 is accepted	4.0 to 6.0	2			T <sub>CYC</sub>				
		tIOL											
	Interrupt Input "H"/"L". Level Pulse Width at Other than INTO	tIIH	INT1, INT2							• Condition under which each interrupt is accepted			
		tIIL											
"H"/"L". Level Pulse Width at PIN1	tPINH	PIN1	• Condition under which the event counter input by timer 1 is accepted										
	tPINL												
"H"/"L". Level Pulse Width at RES	tRSH	RES	• Condition under which a reset is caused	3				T <sub>CYC</sub>					
Comparator Response Time	TRS	PD	Fig.8.		4.0 to 6.0			30	μs				
Current Dissipation at Operating Mode	I <sub>DD</sub> OP	VDD		4MHz ceramic resonator OSC	4.0 to 6.0		4.5	8	mA				
										4MHz external clock	6.5	11	mA
										RC OSC	4.0	8	mA

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Parameter	Symbol	Applicable Pins	Conditions	Limits			Unit	Note	
				VDD(V)	min	typ			max
Current Dissipation at HALT Mode	IDDHALT	VDD	4MHz ceramic resonator OSC	4.0 to 6.0		1.0	2.5	mA	
			4MHz external clock			2	3.5	mA	
			RC OSC			1.2	2.5	mA	
Current Dissipation at HOLD Mode	IDDHOLD	VDD		1.8 to 6.0		0.01	10	$\mu$ A	

- (Note 1) The input/output common ports are of open drain output type with output Nch transistor OFF. When the CMOS output type is selected, the input/output common ports cannot be used as the input pins.
- (Note 2) The input/output common ports are of open drain output type with output Nch transistor OFF. The specification for pull-up output type is specified by output pull-up current IPO. When CMOS output type is selected, the input/output common ports cannot be used as the input pins.
- (Note 3) CMOS output type and output Nch transistor OFF.
- (Note 4) Pull-up output type and output Nch transistor OFF.
- (Note 5) Open drain output type and output Nch transistor OFF.
- (Note 6) Reset mode.

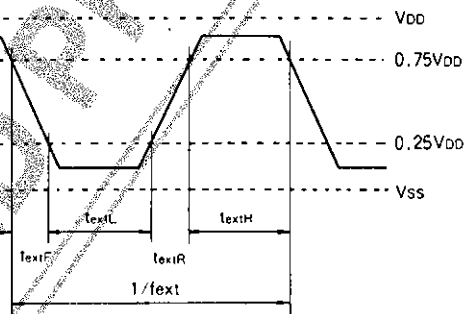
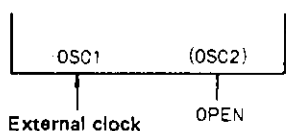


Fig. 1 External Clock Input Waveform

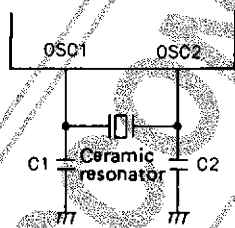


Fig. 2 Ceramic Resonator OSC Circuit

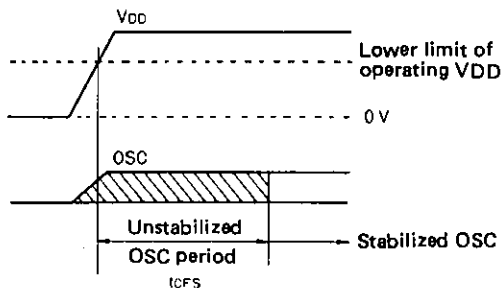


Fig. 3 OSC Stabilizing Period

External capacitor type	4 MHz (Murata) CSA4.00MG	C1	33pF $\pm$ 10%
		C2	33pF $\pm$ 10%
On-chip capacitor type	4 MHz (Murata) CST4.00MG		
	4 MHz (kyocera) KBR-4.0MES		

Table 1 Ceramic Resonator OSC-Guaranteed Constants

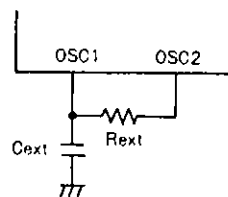


Fig. 4 RC OSC

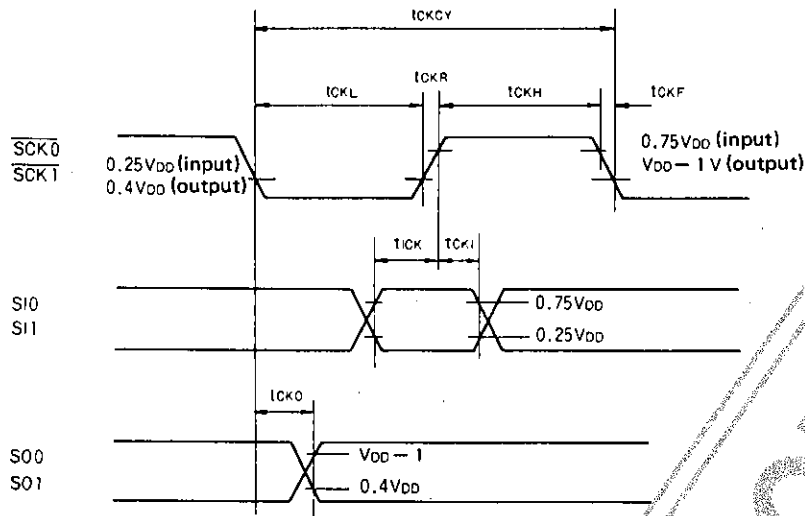


Fig. 5 Serial Input/Output Timing

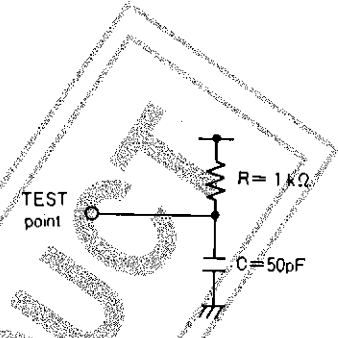


Fig. 6 Timing Load

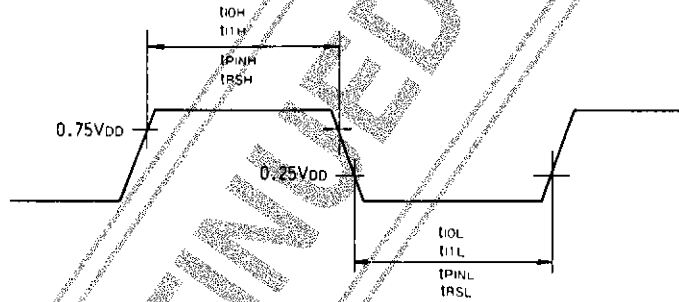


Fig. 7 INT0, INT1, INT2, PIN1, RES Input Timing

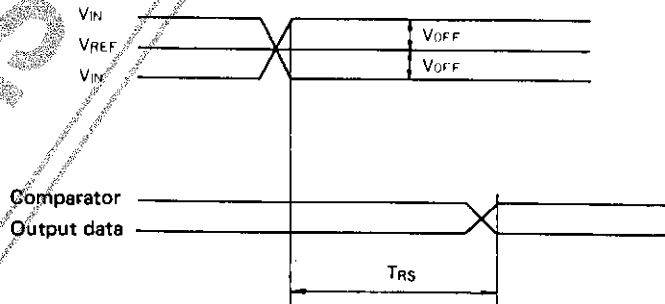


Fig. 8 Timing of Comparator Response Time TRS

DISCONTINUED PRODUCT

RC OSC Characteristic of the LC66304A, 66306A, 66308A

Fig. 9 shows the RC OSC characteristic of the LC66304A, 66306A, 66308A. For the variation range of RC OSC frequency of the LC66304A, 66306A, 66308A, the following are guaranteed at the external constants only shown below.

External constants  $C_{ext}=100\text{pF}$ ,  $R_{ext}=2.7\text{k}\Omega$   
 $2.0\text{MHz} \leq f_{RC} \leq 4.0\text{MHz}$  ( $T_a=-30^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{DD}=4.0$  to  $6.0\text{V}$ )

If any other constants than specified above are used, the range of  $R_{ext}=\text{T.B.Dk}\Omega$  to  $\text{T.B.Dk}\Omega$ ,  $C_{ext}=\text{T.B.DpF}$  to  $\text{T.B.DpF}$  must be observed. (See Fig. 9.)

(Note 10) The OSC frequency at  $V_{DD}=4.0$  to  $6.0\text{V}$ ,  $T_a=-30$  to  $+70^\circ\text{C}$  must be within the operation clock frequency range (0.4 to 4.3MHz).

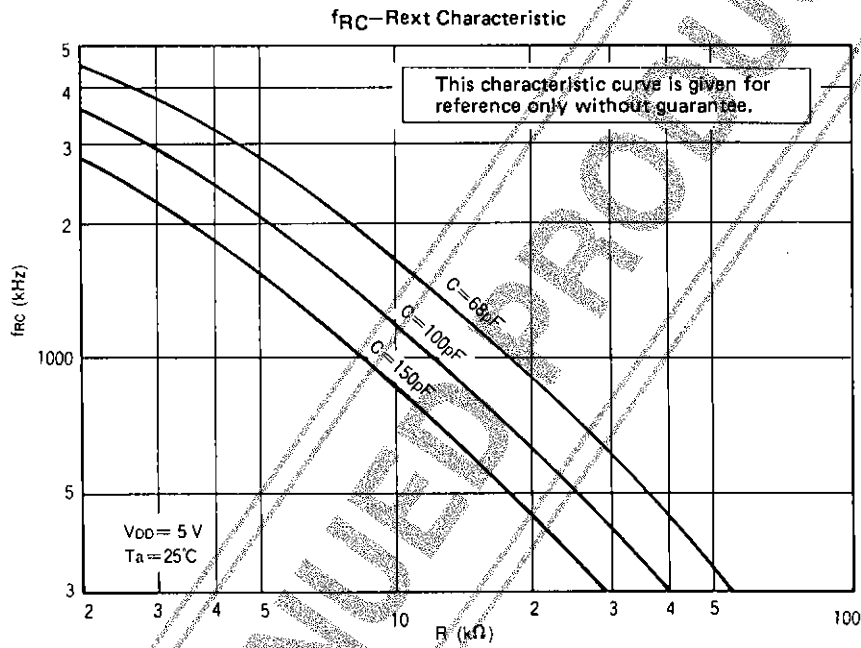
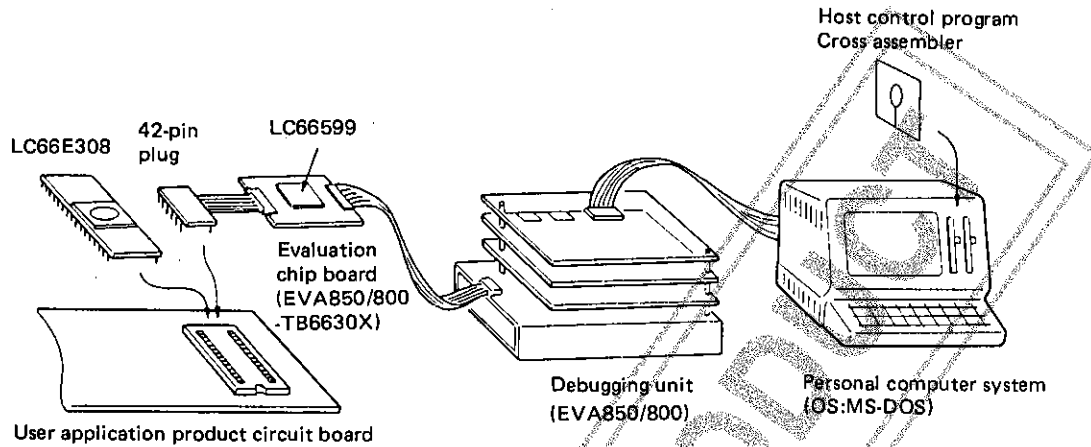


Fig. 9 RC OSC Frequency Data (Typ.)

DISCONTINUED PRODUCT

Application Development Tools

The programs for the LC66304A, 66306A, 66308A microcomputers can be developed on the MS-DOS personal computer system (IBM-PC model system). Cross assembler for this system is provided. To help the user develop programs for the LC66304A, 66306A, 66308A microcomputers, the following development tools are prepared:



Appearance of Application Development Tools

(1) Program debugging unit (EVA850/800)

The program debugging unit (EVA850/800) is an emulator that includes the EPROM WRITE function and the serial data communications interface function between the unit itself and external systems (host computer, etc.). Application programs can be developed, corrected, and debugged at the machine language level. The debugging function can be carried out through break, step and trace operations. (Use the MPM6630X as the monitor ROM on the EVA850/800 debugging unit.)

(2) Evaluation chip board (EVA850/800-TB6630X)

The evaluation chip board sends control signals to the user application board through the 42-pin connector. Data is transferred between the I/O ports on the evaluation chip board and the user application board through the 42-pin connector. If the LC66599 evaluation chip is connected to the 42-pin plug by the output cable, the data from the LC66599 microcomputer is converted into the LC66304A, 66306A, 66308A-bound data by the plug. There are jumper connectors on the evaluation chip board. They are used to select options and status levels. Therefore, using these jumper connectors, the same input/output formats and functions as those of the LC66304A, 66306A, 66308A microcomputers can be selected on the evaluation chip board.

Jumpers

Type	OSC		Reset type selection		Power supply to the user application board through the evaluation chip board	
Jumper name	Jumper 1 (J1)		Jumper 2 (J2)		Jumper 3 (J3)	
Jumper setting and mode	EXT	External clock	INT	Reset by the RUN instruction from the host computer.	ON	VDD supply to the user application board through the evaluation chip board output.
	RC	RC OSC				
	CF	CF OSC	EXT	Reset by the reset circuit on the user application board	OFF	Power supply to the user application board from an independent power source (from the evaluation chip board)

Switch 9 (SW9)

Type	Output level selection for ports 0,1 at the reset				Watchdog timer function selection	
Switch name	P0HL		P1HL		WDC	
Switch setting and mode	+5V	Port 0 "H"	+5V	Port 1 "H"	+5V	Watchdog timer function selected
	GND	Port 0 "L"	GND	Port 0 "L"	GND	Watchdog timer function not selected

Switches SW1 to SW8: Pull-up resistor option select

- ① Set to ON when on-chip pull-up resistor is used. Set to OPEN when open drain output type is selected.
- ② Selectable for each pin.

(3) Cross assembler

Cross assembler name (File name)	Target machine	Restriction on program development
LC663S.EXE	LC66304A, 66306A, 66308A(LC66E308/P308) (LC66599)	Restriction on SB instruction • LC66304A : SB 0 only usable • LC66306A/308A : SB 0, SB 1 usable (LC66E308/P308) • (LC66599) : SB 0, SB 1, SB 2, SB 3 usable

(4) Simulation chip (For details, refer to the catalog of the LC66E308.)

The simulation chip (LC66E308) is an EPROM-contained microcomputer. Using the dedicated conversion board (W66EP308D), you can write programs in the EPROM with a commercially available PROM writer. Then, you can incorporate the simulation chip into an application product to monitor actual operations.

① Case outline

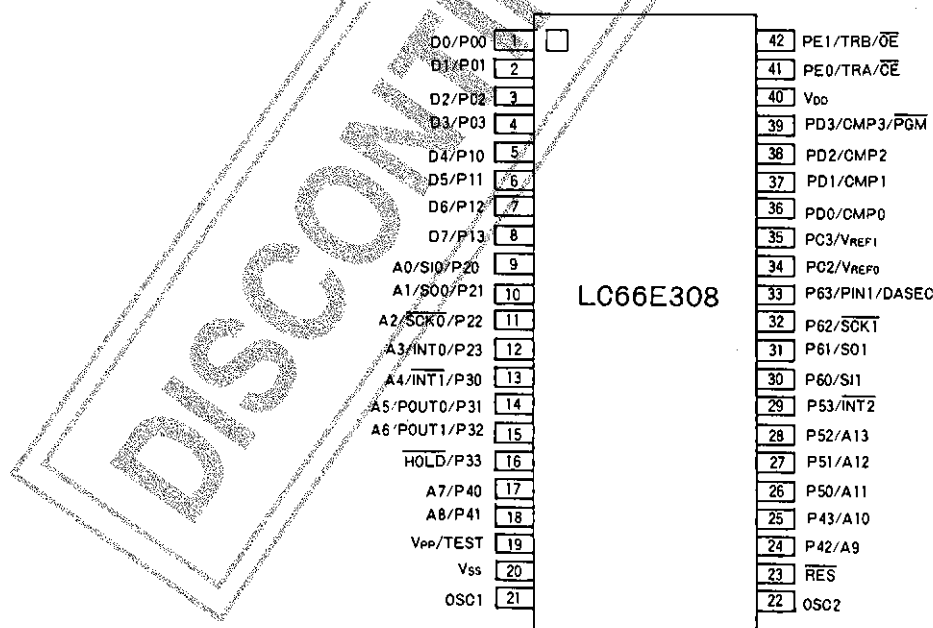
The LC66E308 is the same as the LC66304A, 66306A, 66308A in pin assignment and functions. The pin assignment is shown below.

② Option

Using the on-chip EPROM data (option data area and definition are shown on the next page), you can specify the options (level at port 0, 1 reset mode, watchdog timer, port output configuration) of a microcomputer to be evaluated. Thus, you can perform evaluation using the same peripheral as the board of the equipment to be mass-produced.

Pin Assignment

DIC42S with window





Option Data Area and Definition

ROM Area	Bit	Option	Relation between Option and Data	
2 0 0 0 H	7	Unused	Fixed at 0	
	6			
	5			
	4	OSC option	1=Ceramic resonator OSC 0=RC OSC, external clock	
	3	Unused	Fixed at 0	
	2	P1	Level at reset mode	1="H" level
	1	P0		0="L" level
	0	Watchdog timer option	1=Available, 0=Unavailable	
2 0 0 1 H	7	P13	Output configuration	
	6	P12		
	5	P11		
	4	P10	Output configuration	
	3	P03		
	2	P02		
	1	P01		
0	P00	1=PU, 0=OD		
2 0 0 2 H	7	Unused	Fixed at 0	
	6	P32	Output configuration	
	5	P31		
	4	P30		
	3	P23	Output configuration	
	2	P22		
	1	P21		
0	P20			
2 0 0 3 H	7	P53	Output configuration	
	6	P52		
	5	P51		
	4	P50	Output configuration	
	3	P43		
	2	P42		
	1	P41		
0	P40	1=PU, 0=OD		
2 0 0 4 H	7~4	Unused	Output configuration	
	3	P63		
	2	P62		
	1	P61		
	0	P60		
2 0 0 5 H	7~0	Unused	Fixed at 0	
2 0 0 6 H	7~0	Unused	Fixed at 0	
2 0 0 7 H	7~4	Unused	Output configuration	
	3	PC3		
	2	PC2	1=PU, 0=OD	
	1	0	Unused	Fixed at 0

LC6630X SERIES INSTRUCTION SET (BY FUNCTION)

- Symbol Description
- AC : Accumulator
- E : E register
- CF : Carry flag
- ZF : Zero flag
- HL : Data pointer DPH, DPL
- XY : Data pointer DPX, DPY
- M : Data memory
- M (HL) : Data memory contents specified by data pointer DPH, DPL
- M (XY) : Data memory contents specified by supplementary data pointer DPX, DPY
- M2 (HL) : 2-word data memory contents specified by data pointer DPH, DPL  
 In this case, the accessed data memory area address must be multiples of 2 (even address).
- SP : Stack pointer
- M2 (SP) : 2-word data memory contents specified by stack pointer
- M4 (SP) : 4-word data memory contents specified by stack pointer
- in : n-bit immediate data
- t2 : Bit specification

t2	11	10	01	00
Bit	$2^3$	$2^2$	$2^1$	$2^0$

- PCh : Bits 8 to 11 of PC
- PCm : Bits 4 to 7 of PC
- PCl : Bits 0 to 3 of PC
- F<sub>n</sub> : User's flag n=0 to 15
- TIMER0 : Timer 0
- TIMER1 : Timer 1
- SIO : Serial register
- P : Port
- P (i4) : Port contents specified by 4-bit immediate data
- INT : Interrupt enable flag
- ( ), [ ] : Contents
- ← : Transfer direction and operation result
- ⊖ : Exclusive logical sum
- ∧ : Logical product
- ∨ : Logical sum
- +
- 
- : 1's complement

Instruction type	Mnemonics	Instruction code		Bytes	Cycles	Function	Description	Status flags affected	Remarks	
		D <sub>7</sub> D <sub>6</sub> D <sub>5</sub> D <sub>4</sub>	D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>							
Accumulator manipulation instructions	CLA	Clear AC	1 0 0 0	0 0 0 0	1	1	AC ← 0 (Equivalent to LAI 0)	Clears AC.	ZF	Only the first instruction is effective if executed continuously (skip function).
	DAA	Decimal adjust AC in addition	1 1 0 0	0 0 1 0	2	2	AC ← (AC) + 6 (Equivalent to ADI 6)	Adds 6 to AC.	ZF	
	DAS	Decimal adjust AC in subtraction	1 1 0 0	0 0 1 0	2	2	AC ← (AC) + 10 (Equivalent to ADI 0AH)	Adds 10 to AC.	ZF	
	CLC	Clear CF	0 0 0 1	1 1 1 0	1	1	CF ← 0	Clears CF.	CF	
	STC	Set CF	0 0 0 1	1 1 1 1	1	1	CF ← 1	Sets CF.	CF	
	CMA	Complement AC	0 0 0 1	1 0 0 0	1	1	AC ← $\overline{AC}$	Gives 1's complement of (invert) AC	ZF	
	IA	Increment AC	0 0 0 1	0 1 0 0	1	1	AC ← (AC) + 1	Adds 1 to AC.	ZF, CF	
	DA	Decrement AC	0 0 1 0	0 1 0 0	1	1	AC ← (AC) - 1	Subtracts 1 from AC.	ZF, CF	
	RAR	Rotate AC right through CF	0 0 0 1	0 0 0 0	1	1	AC <sub>7</sub> ← (CF), AC <sub>n</sub> ← (AC <sub>n+1</sub> ), CF ← (AC <sub>0</sub> )	Rotates AC right through CF.	CF	
	RAL	Rotate AC left through CF	0 0 0 0	0 0 0 1	1	1	AC <sub>0</sub> ← (CF), AC <sub>n+1</sub> ← (AC <sub>n</sub> ), CF ← (AC <sub>7</sub> )	Rotates AC left through CF.	CF, ZF	
	TAE	Transfer AC to E	0 1 0 0	0 1 0 1	1	1	E ← (AC)	Transfers the AC contents to the E register.		
	TEA	Transfer E to AC	0 1 0 0	0 1 1 0	1	1	AC ← (E)	Transfers the E register contents to AC.	ZF	
XAE	Exchange AC with E	0 1 0 0	0 1 0 0	1	1	(AC) ↔ (E)	Exchanges the contents of the AC and E register.			
Memory manipulation instructions	IM	Increment M	0 0 0 1	0 0 1 0	1	1	M(HL) ← (M(HL)) + 1	Adds 1 to M(HL).	ZF, CF	
	DM	Decrement M	0 0 1 0	0 0 1 0	1	1	M(HL) ← (M(HL)) - 1	Subtracts 1 from M(HL).	ZF, CF	
	IMDR i8	Increment M direct	1 1 0 0	0 1 1 1	2	2	M(i8) ← (M(i8)) + 1	Adds 1 to M(i8).	ZF, CF	
	DMDR i8	Decrement M direct	1 1 0 0	0 0 1 1	2	2	M(i8) ← (M(i8)) - 1	Subtracts 1 from M(i8).	ZF, CF	
	SMB t2	Set M data bit	0 0 0 0	1 1 t <sub>1</sub> t <sub>0</sub>	1	1	(M(HL), t <sub>2</sub> ) ← 1	Sets a bit specified by t <sub>1</sub> , t <sub>0</sub> of M(HL).		
	RMB t2	Reset M data bit	0 0 1 0	1 1 t <sub>1</sub> t <sub>0</sub>	1	1	(M(HL), t <sub>2</sub> ) ← 0	Resets a bit specified by t <sub>1</sub> , t <sub>0</sub> of M(HL).	ZF	
Operation/Comparison instructions	AD	Add M to AC	0 0 0 0	0 1 1 0	1	1	AC ← (AC) + (M(HL))	Adds together the contents of AC and M(HL) in binary and stores the result in AC.	ZF, CF	
	ADDR i8	Add M direct to AC	1 1 0 0	1 0 0 1	2	2	AC ← (AC) + (M(i8))	Adds together the contents of AC and M(i8) in binary and stores the result in AC.	ZF, CF	
	ADC	Add M to AC with CF	0 0 0 0	0 0 1 0	1	1	AC ← (AC) + (M(HL)) + (CF)	Adds together the contents of AC, M(HL), and CF in binary and stores the result in AC.	ZF, CF	
	ADI i4	Add immediate data to AC	1 1 0 0	1 1 1 1	2	2	AC ← (AC) + i <sub>3</sub> , i <sub>2</sub> , i <sub>1</sub> , i <sub>0</sub>	Adds together the contents of AC and immediate data in binary and stores the result in AC.	ZF	
	SUBC	Subtract AC from M with CF	0 0 0 1	0 1 1 1	1	1	AC ← (M(HL)) - (AC) - (CF)	Subtracts the contents of AC from M(HL) with CF in binary and stores the result in AC.	ZF, CF	CF=0 if there is a borrow while CF=1 if there is no borrow.
	ANDA	AND M with AC then store AC	0 0 0 0	0 1 1 1	1	1	AC ← (AC) ∧ (M(HL))	Performs a logical AND operation between AC and M(HL) and stores the result in AC.	ZF	
	ORA	OR M with AC then store AC	0 0 0 0	0 1 0 1	1	1	AC ← (AC) ∨ (M(HL))	Performs a logical OR operation between AC and M(HL) and stores the result in AC.	ZF	
	EXL	Exclusive OR M with AC then store AC	0 0 0 1	0 1 0 1	1	1	AC ← (AC) ⊕ (M(HL))	Performs a logical exclusive OR operation between AC and M(HL) and stores the result in AC.	ZF	
	ANDM	AND M with AC then store M	0 0 0 0	0 0 1 1	1	1	M(HL) ← (AC) ∧ (M(HL))	Performs a logical AND operation between AC and M(HL) and stores the result in M(HL).	ZF	
ORM	OR M with AC then store M	0 0 0 0	0 1 0 0	1	1	M(HL) ← (AC) ∨ (M(HL))	Performs a logical OR operation between AC and M(HL) and stores the result in M(HL).	ZF		

Instruction type	Mnemonics	Instruction code		Bytes	Cycles	Function	Description	Status flags affected	Remarks												
		D <sub>7</sub> D <sub>6</sub> D <sub>5</sub> D <sub>4</sub>	D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>																		
Operation/Comparison instructions	CM	Compare AC with M	0 0 0 1	0 1 1 0	1	1	(M,HL) ← (AC) - 1 Compares the contents of AC and M(HL) and then sets/resets the carry flag (CF) and zero flag (ZF). <table border="1"> <tr> <th>Comparison relations</th> <th>CF</th> <th>ZF</th> </tr> <tr> <td>(M(HL)) &gt; (AC)</td> <td>0</td> <td>0</td> </tr> <tr> <td>(M(HL)) = (AC)</td> <td>1</td> <td>1</td> </tr> <tr> <td>(M(HL)) &lt; (AC)</td> <td>1</td> <td>0</td> </tr> </table>	Comparison relations	CF	ZF	(M(HL)) > (AC)	0	0	(M(HL)) = (AC)	1	1	(M(HL)) < (AC)	1	0	ZF, CF	
	Comparison relations	CF	ZF																		
	(M(HL)) > (AC)	0	0																		
	(M(HL)) = (AC)	1	1																		
(M(HL)) < (AC)	1	0																			
CI i4	Compare AC with immediate data	1 1 0 0 1 0 1 0	1 1 1 1 i <sub>3</sub> i <sub>2</sub> i <sub>1</sub> i <sub>0</sub>	2	2	i <sub>3</sub> i <sub>2</sub> i <sub>1</sub> i <sub>0</sub> + (AC) + 1 Compares the contents of the accumulator (AC) and immediate data (i <sub>3</sub> i <sub>2</sub> i <sub>1</sub> i <sub>0</sub> ) and sets/resets the zero flag (ZF) and carry flag (CF). <table border="1"> <tr> <th>Comparison relations</th> <th>CF</th> <th>ZF</th> </tr> <tr> <td>i<sub>3</sub> i<sub>2</sub> i<sub>1</sub> i<sub>0</sub> &gt; AC</td> <td>0</td> <td>0</td> </tr> <tr> <td>i<sub>3</sub> i<sub>2</sub> i<sub>1</sub> i<sub>0</sub> = AC</td> <td>1</td> <td>1</td> </tr> <tr> <td>i<sub>3</sub> i<sub>2</sub> i<sub>1</sub> i<sub>0</sub> &lt; AC</td> <td>1</td> <td>0</td> </tr> </table>	Comparison relations	CF	ZF	i <sub>3</sub> i <sub>2</sub> i <sub>1</sub> i <sub>0</sub> > AC	0	0	i <sub>3</sub> i <sub>2</sub> i <sub>1</sub> i <sub>0</sub> = AC	1	1	i <sub>3</sub> i <sub>2</sub> i <sub>1</sub> i <sub>0</sub> < AC	1	0	ZF, CF		
Comparison relations	CF	ZF																			
i <sub>3</sub> i <sub>2</sub> i <sub>1</sub> i <sub>0</sub> > AC	0	0																			
i <sub>3</sub> i <sub>2</sub> i <sub>1</sub> i <sub>0</sub> = AC	1	1																			
i <sub>3</sub> i <sub>2</sub> i <sub>1</sub> i <sub>0</sub> < AC	1	0																			
CLI i4	Compare DP <sub>L</sub> with immediate data	1 1 0 0 1 0 1 1	1 1 1 1 i <sub>3</sub> i <sub>2</sub> i <sub>1</sub> i <sub>0</sub>	2	2	ZF ← 1 if (DP <sub>L</sub> ) = i <sub>3</sub> i <sub>2</sub> i <sub>1</sub> i <sub>0</sub> ZF ← 0 if (DP <sub>L</sub> ) ≠ i <sub>3</sub> i <sub>2</sub> i <sub>1</sub> i <sub>0</sub> Compares the contents of DP <sub>L</sub> and immediate data and sets the zero flag (ZF) if they are equal, or resets the flag if not equal.	ZF														
CMB t2	Compare AC bit with M data bit	1 1 0 0 1 1 0 1	1 1 1 1 0 0 t <sub>1</sub> t <sub>0</sub>	2	2	ZF ← 1 if (AC, t <sub>2</sub> ) = (M(HL), t <sub>2</sub> ) ZF ← 0 if (AC, t <sub>2</sub> ) ≠ (M(HL), t <sub>2</sub> ) Compares the contents of AC and M(HL) bit specified by the 2 bits (t <sub>1</sub> and t <sub>2</sub> ) of the instruction and sets the zero flag (ZF) if they are equal, or resets the flag if not equal.	ZF														
Load/store instructions	LAE	Load AC and E from M2 (HL)	0 1 0 1	1 1 0 0	1	1	AC ← M(HL) E ← M(HL + 1) Loads the contents of M2(HL) into the AC and the E register.														
	LAI i4	Load AC with immediate data	1 0 0 0	i <sub>3</sub> i <sub>2</sub> i <sub>1</sub> i <sub>0</sub>	1	1	AC ← i <sub>3</sub> i <sub>2</sub> i <sub>1</sub> i <sub>0</sub> Loads immediate data into AC.	ZF	Only the first instruction is affected (particularly like function).												
	LADR i8	Load AC from M direct	1 1 0 0 i <sub>7</sub> i <sub>6</sub> i <sub>5</sub> i <sub>4</sub>	0 0 0 1 i <sub>3</sub> i <sub>2</sub> i <sub>1</sub> i <sub>0</sub>	2	2	AC ← (M(i8)) Loads the contents of M(i8) into AC.	ZF													
	S	Store AC to M	0 1 0 0	0 1 1 1	1	1	M(HL) ← (AC) Stores the contents of AC into M(HL).														
	SAE	Store AC and E to M2 (HL)	0 1 0 1	1 1 1 0	1	1	M(HL) ← (AC) M(HL + 1) ← (E) Stores the contents of AC and the E register into M2(HL).														
	LA reg	Load AC from M(reg)	0 1 0 0	1 0 t <sub>1</sub> 0	1	1	AC ← (M(reg)) Loads the contents of M(reg) into AC. reg is either an HL or XY. <table border="1"> <tr> <th>reg</th> <th>to</th> </tr> <tr> <td>HL</td> <td>0</td> </tr> <tr> <td>XY</td> <td>1</td> </tr> </table>	reg	to	HL	0	XY	1	ZF							
	reg	to																			
	HL	0																			
	XY	1																			
LA reg, I	Load AC from M(reg) then increment reg	0 1 0 0	1 0 t <sub>1</sub> 1	1	2	AC ← (M(reg)) DP <sub>L</sub> ← (DP <sub>L</sub> ) + 1 or DP <sub>Y</sub> ← (DP <sub>Y</sub> ) + 1 Loads the contents of M(reg) into the accumulator (AC). reg is either an HL or XY. After loading, increments the contents of DP <sub>L</sub> or DP <sub>Y</sub> . Refer to the LA reg instruction for the relationship between reg and t <sub>0</sub> .	ZF	ZF status depends on DP <sub>L</sub> or DP <sub>Y</sub> increment result.													
LA reg, D	Load AC from M(reg) then decrement reg	0 1 0 1	1 0 t <sub>1</sub> 1	1	2	AC ← (M(reg)) DP <sub>L</sub> ← (DP <sub>L</sub> ) - 1 or DP <sub>Y</sub> ← (DP <sub>Y</sub> ) - 1 Loads the contents of M(reg) into AC. reg is either an HL or XY. After loading, decrements the contents of DP <sub>L</sub> or DP <sub>Y</sub> . Refer to the LA reg instruction for the relationship between reg and t <sub>0</sub> .	ZF	ZF status depends on DP <sub>L</sub> or DP <sub>Y</sub> decrement result.													
XA reg	Exchange AC with M(reg)	0 1 0 0	1 1 t <sub>1</sub> 0	1	1	(AC) ← (M(reg)) Exchanges the contents of AC and M(reg). reg is either an HL or XY. <table border="1"> <tr> <th>reg</th> <th>to</th> </tr> <tr> <td>HL</td> <td>0</td> </tr> <tr> <td>XY</td> <td>1</td> </tr> </table>	reg	to	HL	0	XY	1									
reg	to																				
HL	0																				
XY	1																				
XA reg, I	Exchange AC with M(reg) then increment reg	0 1 0 0	1 1 t <sub>1</sub> 1	1	2	(AC) ← (M(reg)) DP <sub>L</sub> ← (DP <sub>L</sub> ) + 1 or DP <sub>Y</sub> ← (DP <sub>Y</sub> ) + 1 Exchanges the contents of AC and M(reg). reg is either an HL or XY. After exchanging, increments the contents of DP <sub>L</sub> or DP <sub>Y</sub> . Refer to the XA reg instruction for the relationship between reg and t <sub>0</sub> .	ZF	ZF status depends on DP <sub>L</sub> or DP <sub>Y</sub> increment result.													
XA reg, D	Exchange AC with M(reg) then decrement reg	0 1 0 1	1 1 t <sub>1</sub> 1	1	2	(AC) ← (M(reg)) DP <sub>L</sub> ← (DP <sub>L</sub> ) - 1 or DP <sub>Y</sub> ← (DP <sub>Y</sub> ) - 1 Exchanges the contents of AC and M(reg). reg is either an HL or XY. After exchanging, decrements the contents of DP <sub>L</sub> or DP <sub>Y</sub> . Refer to the XA reg instruction for the relationship between reg and t <sub>0</sub> .	ZF	ZF status depends on DP <sub>L</sub> or DP <sub>Y</sub> decrement result.													
XADR i8	Exchange AC with M direct	1 1 0 0 i <sub>7</sub> i <sub>6</sub> i <sub>5</sub> i <sub>4</sub>	1 0 0 0 i <sub>3</sub> i <sub>2</sub> i <sub>1</sub> i <sub>0</sub>	2	2	(AC) ← (M(i8)) Exchanges the contents of AC and M(i8).															

Instruction type	Mnemonics	Instruction code		Bytes	Cycles	Function	Description	Status flags affected	Remarks	
		D <sub>7</sub> D <sub>6</sub> D <sub>5</sub> D <sub>4</sub>	D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>							
Load/store instructions	LEAI i8	Load E & AC with immediate data	1 1 0 0 I <sub>7</sub> I <sub>6</sub> I <sub>5</sub> I <sub>4</sub>	0 1 1 0 I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub>	2	2	E ← I <sub>7</sub> I <sub>6</sub> I <sub>5</sub> I <sub>4</sub> AC ← I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub>			
	RTBL	Read table data from program ROM	0 1 0 1	1 0 1 0	1	2	E, AC ← (ROM(PCh, E, AC))	First, replace the contents of lower 8 bits of PC with the E register and AC contents. Then, loads the ROM data at an address specified by the new contents of the lower 8 bits of PC into the E register and AC.		
	RTBLP	Read table data from program ROM then output to P4,5	0 1 0 1	1 0 0 0	1	2	Port 4, 5 ← (ROM(PCh, E, AC))	First, replaces the contents of lower 8 bits of AC with the E register and AC contents. Then, outputs the ROM data at an address specified by the new contents of the lower 8 bits of PC to ports 4 and 5.		
Data pointer manipulation instructions	LDZ i4	Load DP <sub>H</sub> with zero and DP <sub>L</sub> with immediate data respectively	0 1 1 0	I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub>	1	1	DP <sub>H</sub> ← 0 DP <sub>L</sub> ← I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub>		Loads the data of 0 (zero) and immediate data i4 into the DP <sub>H</sub> and DP <sub>L</sub> respectively.	
	LHI i4	Load DP <sub>H</sub> with immediate data	1 1 0 0 0 0 0 0	1 1 1 1 I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub>	2	2	DP <sub>H</sub> ← I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub>		Loads immediate data i4 into the DP <sub>H</sub> .	
	LLI i4	Load DP <sub>L</sub> with immediate data	1 1 0 0 0 0 0 1	1 1 1 1 I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub>	2	2	DP <sub>L</sub> ← I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub>		Loads immediate data i4 into the DP <sub>L</sub> .	
	LHLI i8	Load DP <sub>H</sub> , DP <sub>L</sub> with immediate data	1 1 0 0 I <sub>7</sub> I <sub>6</sub> I <sub>5</sub> I <sub>4</sub>	0 0 0 0 I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub>	2	2	DP <sub>H</sub> ← I <sub>7</sub> I <sub>6</sub> I <sub>5</sub> I <sub>4</sub> DP <sub>L</sub> ← I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub>		Loads immediate data into the DP <sub>H</sub> and DP <sub>L</sub> .	
	LXYI i8	Load DP <sub>X</sub> , DP <sub>Y</sub> with immediate data	1 1 0 0 I <sub>7</sub> I <sub>6</sub> I <sub>5</sub> I <sub>4</sub>	0 0 1 0 I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub>	2	2	DP <sub>X</sub> ← I <sub>7</sub> I <sub>6</sub> I <sub>5</sub> I <sub>4</sub> DP <sub>Y</sub> ← I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub>		Loads immediate data into the DP <sub>X</sub> and DP <sub>Y</sub> .	
	IL	Increment DP <sub>L</sub>	0 0 0 1	0 0 0 1	1	1	DP <sub>L</sub> ← (DP <sub>L</sub> ) + 1		Increments the contents of the DP <sub>L</sub> by 1.	ZF
	DL	Decrement DP <sub>L</sub>	0 0 1 0	0 0 0 1	1	1	DP <sub>L</sub> ← (DP <sub>L</sub> ) - 1		Decrements the contents of the DP <sub>L</sub> by 1.	ZF
	IY	Increment DP <sub>Y</sub>	0 0 0 1	0 0 1 1	1	1	DP <sub>Y</sub> ← (DP <sub>Y</sub> ) + 1		Increments the contents of the DP <sub>Y</sub> by 1.	ZF
	DY	Decrement DP <sub>Y</sub>	0 0 1 0	0 0 1 1	1	1	DP <sub>Y</sub> ← (DP <sub>Y</sub> ) - 1		Decrements the contents of the DP <sub>Y</sub> by 1.	ZF
	TAH	Transfer AC to DP <sub>H</sub>	1 1 0 0 1 1 1 1	1 1 1 1 0 0 0 0	2	2	DP <sub>H</sub> ← (AC)		Transfers the contents of the accumulator (AC) to the DP <sub>H</sub> .	
	THA	Transfer DP <sub>H</sub> to AC	1 1 0 0 1 1 1 0	1 1 1 1 0 0 0 0	2	2	AC ← (DP <sub>H</sub> )		Transfers the contents of the DP <sub>H</sub> to the AC.	ZF
	XAH	Exchange AC with DP <sub>H</sub>	0 1 0 0	0 0 0 0	1	1	(AC) ↔ (DP <sub>H</sub> )		Exchanges the contents of the accumulator (AC) and the DP <sub>H</sub> .	
	TAL	Transfer AC to DP <sub>L</sub>	1 1 0 0 1 1 1 1	1 1 1 1 0 0 0 1	2	2	DP <sub>L</sub> ← (AC)		Transfers the contents of the accumulator (AC) to the DP <sub>L</sub> .	
	TLA	Transfer DP <sub>L</sub> to AC	1 1 0 0 1 1 1 0	1 1 1 1 0 0 0 1	2	2	AC ← (DP <sub>L</sub> )		Transfers the contents of the DP <sub>L</sub> to the accumulator (AC).	ZF
	XAL	Exchange AC with DP <sub>L</sub>	0 1 0 0	0 0 0 1	1	1	(AC) ↔ (DP <sub>L</sub> )		Exchanges the contents of the AC and DP <sub>L</sub> .	
	TAX	Transfer AC to DP <sub>X</sub>	1 1 0 0 1 1 1 1	1 1 1 1 0 0 1 0	2	2	DP <sub>X</sub> ← (AC)		Transfers the contents of the accumulator (AC) to the DP <sub>X</sub> .	
	TXA	Transfer DP <sub>X</sub> to AC	1 1 0 0 1 1 1 0	1 1 1 1 0 0 1 0	2	2	AC ← (DP <sub>X</sub> )		Transfers the contents of DP <sub>X</sub> to the AC.	ZF
	XAX	Exchange AC with DP <sub>X</sub>	0 1 0 0	0 0 1 0	1	1	(AC) ↔ (DP <sub>X</sub> )		Exchanges the contents of the AC and DP <sub>X</sub> .	
	TAY	Transfer AC to DP <sub>Y</sub>	1 1 0 0 1 1 1 1	1 1 1 1 0 0 1 1	2	2	DP <sub>Y</sub> ← (AC)		Transfers the contents of the accumulator (AC) to the DP <sub>Y</sub> .	
	TYA	Transfer DP <sub>Y</sub> to AC	1 1 0 0 1 1 1 0	1 1 1 1 0 0 1 1	2	2	AC ← (DP <sub>Y</sub> )		Transfers the contents of the DP <sub>Y</sub> to the AC.	ZF
XAY	Exchange AC with DP <sub>Y</sub>	0 1 0 0	0 0 1 1	1	1	(AC) ↔ (DP <sub>Y</sub> )		Exchanges the contents of the accumulator (AC) and the DP <sub>Y</sub> .		
Flag manipulation instructions	SFB n4	Set flag bit	0 1 1 1	n <sub>3</sub> n <sub>2</sub> n <sub>1</sub> n <sub>0</sub>	1	1	F <sub>n</sub> ← 1		Sets a flag specified by n4.	
	RFB n4	Reset flag bit	0 0 1 1	n <sub>3</sub> n <sub>2</sub> n <sub>1</sub> n <sub>0</sub>	1	1	F <sub>n</sub> ← 0		Resets a flag specified by n4.	ZF
Jump/subroutine instructions	JMP addr	Jump in the current bank	1 1 1 0 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	P <sub>11</sub> P <sub>10</sub> P <sub>9</sub> P <sub>8</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC12 ← PC12 PC11-0 ← P <sub>11</sub> -P <sub>0</sub>		Jumps to an address specified by immediate data P <sub>11</sub> - P <sub>0</sub> in the current bank.	When executed immediately after the BANK instruction, PC12 ← (PC12).
	JPEA	Jump to the address stored at E and AC in the current page	0 0 1 0	0 1 1 1	1	1	PC12 ← PC8 - PC12 - PC8 PC7-4 ← (E) PC3-0 ← (AC)		Jumps to an address specified by the contents of the E register and accumulator (AC) which have replaced the contents of lower 8 bits of the program counter (PC).	

Instruction type	Mnemonics	Instruction code		Bytes	Cycles	Function	Description	Status flags affected	Remarks															
		D <sub>7</sub> D <sub>6</sub> D <sub>5</sub> D <sub>4</sub>	D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>																					
Jump/subroutine instructions	CAL addr	Call subroutine	0 1 0 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	0 P <sub>10</sub> P <sub>9</sub> P <sub>8</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC12-11-0 PC10-0--P <sub>10</sub> -P <sub>0</sub> M4(SP)--(CF, ZF, PC13-0) SP--(SP)-4	Calls a subroutine.																
	CZP addr	Call subroutine in the zero page	1 0 1 0	P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	1	2	PC12-6, PC1-0-0 PC5-2--P <sub>3</sub> -P <sub>0</sub> M4(SP)--(CF, ZF, PC13-0) SP--SP-4	Calls a subroutine in page 0 of bank 0.																
	BANK	Change bank	0 0 0 1	1 0 1 1	1	1		Changes memory banks and register banks.																
	PUSH reg	Push reg on M2(SP)	1 1 0 0 1 1 1 1	1 1 1 1 1 i <sub>1</sub> i <sub>0</sub> 0	2	2	M2(SP)--(reg) SP--(SP)-2	Stores the contents of reg into the M2(SP) and then subtracts 2 from the stack pointer (SP). <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>reg</td> <td>if</td> <td>in</td> </tr> <tr> <td>HL</td> <td>0</td> <td>0</td> </tr> <tr> <td>XY</td> <td>0</td> <td>1</td> </tr> <tr> <td>AE</td> <td>1</td> <td>0</td> </tr> <tr> <td>Inhibited</td> <td>1</td> <td>1</td> </tr> </table>	reg	if	in	HL	0	0	XY	0	1	AE	1	0	Inhibited	1	1	
	reg	if	in																					
	HL	0	0																					
XY	0	1																						
AE	1	0																						
Inhibited	1	1																						
POP reg	Pop reg off M2(SP)	1 1 0 0 1 1 1 0	1 1 1 1 1 i <sub>1</sub> i <sub>0</sub> 0	2	2	SP--(SP)+2 reg--(M2(SP))	Stores the contents of reg into the M2(SP) and then increments the contents of the stack pointer (SP) by 2 and loads the contents of M2(SP) into a reg. Refer to the PUSH reg instruction for the relationship between i10 and reg.																	
RT	Return from subroutine	0 0 0 1	1 1 0 0	1	2	SP--(SP)+4 PC--(M4(SP))	Returns execution from a subroutine or interrupt processing routine back to the routine that called it. The contents of the carry flag (CF) and zero flag (ZF) are not returned from the stack area.																	
RTI	Return from interrupt routine	0 0 0 1	1 1 0 1	1	2	SP--(SP)+4 PC--(M4(SP)) CF, ZF--(M4(SP))	Returns execution from a subroutine or interrupt processing routine back to the routine that called it. The contents of the carry flag (CF) and zero flag (ZF) are returned from the stack area.	ZF, CF																
Branch instructions	BAt2 addr	Branch on AC bit	1 1 0 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	0 0 t <sub>1</sub> t <sub>0</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC7-0--P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if(AC.t2)=1	Transfers execution to an address specified by the contents of P7 to P0 in the current page if a bit specified by immediate data t1t0 of AC is 1 (program branch).																
	BNAt2 addr	Branch on no AC bit	1 0 0 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	0 0 t <sub>1</sub> t <sub>0</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC7-0--P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if(AC.t2)=0	Transfers execution to an address specified by the contents of P7 to P0 in the current page if a bit specified by immediate data t1t0 of AC is 0 (program branch).																
	BMt2 addr	Branch on M bit	1 1 0 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	0 1 t <sub>1</sub> t <sub>0</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC7-0--P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if(M(HL), t2)=1	Transfers execution to an address specified by the contents of P7 to P0 in the current page if a bit specified by immediate data t1t0 of M(HL) is 1 (program branch).																
	BNMt2 addr	Branch on no M bit	1 0 0 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	0 1 t <sub>1</sub> t <sub>0</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC7-0--P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if(M(HL), t2)=0	Transfers execution to an address specified by the contents of P7 to P0 in the current page if a bit specified by immediate data t1t0 of M(HL) is 0 (program branch).																
	BPt2 addr	Branch on Port bit	1 1 0 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	1 0 t <sub>1</sub> t <sub>0</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC7-0--P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if(P(DPL), t2)=1	Transfers execution to an address specified by the contents of P7 to P0 in the current page if a bit specified by immediate data t1t0 of the port accessed by DPL is 1 (program branch).	Used to manipulate internal control registers if executed immediately after the BANK instruction. In this case, the internal control registers must be readable.															
	BNPt2 addr	Branch on no Port bit	1 0 0 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	1 0 t <sub>1</sub> t <sub>0</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC7-0--P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if(P(DPL), t2)=0	Transfers execution to an address specified by the contents of P7 to P0 in the current page if a bit specified by immediate data t1t0 of the port accessed by DPL is 0 (program branch).	Same as above.															
	BC addr	Branch on CF	1 1 0 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	1 1 0 0 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC7-0--P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if(CF)=1	Transfers execution to an address specified by the contents of P7 to P0 in the current page if the content of the carry flag (CF) is 1 (program branch).																
	BNC addr	Branch on no CF	1 0 0 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	1 1 0 0 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC7-0--P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if(CF)=0	Transfers execution to an address specified by the contents of P7 to P0 in the current page if the content of the carry flag (CF) is 0 (program branch).																
	BZ addr	Branch on ZF	1 1 0 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	1 1 0 1 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC7-0--P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if(ZF)=1	Transfers execution to an address specified by the contents of P7 to P0 in the current page if the content of the zero flag (ZF) is 1 (program branch).																
	BNZ addr	Branch on no ZF	1 0 0 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	1 1 0 1 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC7-0--P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if(ZF)=0	Transfers execution to an address specified by the contents of P7 to P0 in the current page if the content of the zero flag (ZF) is 0 (program branch).																

Instruction type	Mnemonics	Instruction code		Bytes	Cycles	Function	Description	Status flags affected	Remarks	
		D <sub>7</sub> D <sub>6</sub> D <sub>5</sub> D <sub>4</sub>	D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>							
Branch instructions	BFn4 addr	Branch on flag bit	1 1 1 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	n <sub>3</sub> n <sub>2</sub> n <sub>1</sub> n <sub>0</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC7-0 ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if(Fn) = 1	Transfers execution to an address specified by the contents of P7 to P0 in the current page if the content of the flag specified by n3n2n1n0 is 1. The flag is one of the 16 flags.		
	BNFn4 addr	Branch on no flag bit	1 0 1 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	n <sub>3</sub> n <sub>2</sub> n <sub>1</sub> n <sub>0</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC7-0 ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if(Fn) = 0	Transfers execution to an address specified by the contents of P7 to P0 in the current page if the content of the flag specified by n3n2n1n0 is 0. The flag is one of the 16 flags.		
Input/output instructions	IP0	Input port 0 to AC	0 0 1 0	0 0 0 0	1	1	AC ← (P0)	Inputs the contents of port 0 to the accumulator (AC).	ZF	
	IP	Input port to AC	0 0 1 0	0 1 1 0	1	1	AC ← (P(DPL))	Inputs the contents of port accessed by DPL to the accumulator (AC).	ZF	
	IPM	Input port to M	0 0 0 1	1 0 0 1	1	1	M(HL) ← (P(DPL))	Inputs the contents of port accessed by DPL to the M(HL).		
	IPDR i4	Input port to AC direct	1 1 0 0 0 1 1 0	1 1 1 1 i <sub>3</sub> i <sub>2</sub> i <sub>1</sub> i <sub>0</sub>	2	2	AC ← (P(i4))	Inputs the contents of port accessed by i4 to the accumulator (AC).	ZF	
	IP45	Input port 4,5 to E, AC respectively	1 1 0 0 1 1 0 1	1 1 1 1 0 1 0 0	2	2	E ← (P(4)) AC ← (P(5))	Inputs the contents of ports 4 and 5 to the E register and accumulator (AC) respectively.		
	OP	Output AC to port	0 0 1 0	0 1 0 1	1	1	P(DPL) ← (AC)	Outputs the contents of the accumulator (AC) to a port accessed by DPL.		
	OPM	Output M to port	0 0 0 1	1 0 1 0	1	1	P(DPL) ← (M(HL))	Outputs the contents of the M(HL) to a port accessed by DPL.		
	OPDR i4	Output AC to port direct	1 1 0 0 0 1 1 1	1 1 1 1 i <sub>3</sub> i <sub>2</sub> i <sub>1</sub> i <sub>0</sub>	2	2	P(i4) ← (AC)	Outputs the contents of the accumulator (AC) to a port accessed by i4.		
	OP45	Output E, AC to port 4,5 respectively	1 1 0 0 1 1 0 1	1 1 1 1 0 1 0 1	2	2	P(4) ← (E) P(5) ← (AC)	Outputs the contents of the E register and accumulator (AC) to ports 4 and 5 respectively.		
	SPB i2	Set port bit	0 0 0 0	1 0 t <sub>1</sub> t <sub>0</sub>	1	1	(P(DPL), i2) ← 1	Sets a bit specified by immediate data t1t0 of a port accessed by DPL.		
	RPB i2	Reset port bit	0 0 1 0	1 0 t <sub>1</sub> t <sub>0</sub>	1	1	(P(DPL), i2) ← 0	Resets a bit specified by immediate data t1t0 of a port accessed by DPL.	ZF	
	ANDPDR i4, p4	AND port with immediate data then output	1 1 0 0 i <sub>3</sub> i <sub>2</sub> i <sub>1</sub> i <sub>0</sub>	0 1 0 1 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	P(P <sub>3</sub> -P <sub>0</sub> ) ← (P(P <sub>3</sub> -P <sub>0</sub> ) ∨ i <sub>3</sub> -i <sub>0</sub> )	Performs a logical AND operation between the contents of a port specified by P3 to P0 and immediate data i3i2i1i0 and outputs the resulted product to the port.	ZF	
ORPDR i4, p4	OR port with immediate data then output	1 1 0 0 i <sub>3</sub> i <sub>2</sub> i <sub>1</sub> i <sub>0</sub>	0 1 0 0 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	P(P <sub>3</sub> -P <sub>0</sub> ) ← (P(P <sub>3</sub> -P <sub>0</sub> ) ∨ i <sub>3</sub> -i <sub>0</sub> )	Performs a logical OR operation between the contents of a port specified by P3 to P0 and immediate data i3i2i1i0 and outputs the resulted sum to the port.	ZF		
Timer control instructions	WTTM0	Write timer 0	1 1 0 0	1 0 1 0	1	2	TIMER0 ← (M2(HL)), (AC)	Writes the contents of the M(HL) and the accumulator (AC) to the timer 0 reload register.		
	WTTM1	Write timer 1	1 1 0 0 1 1 1 1	1 1 1 1 0 1 0 0	2	2	TIMER1 ← (E), (AC)	Writes the contents of the E register and the accumulator (AC) to the timer 1 reload register.		
	RTIMO	Read timer 0	1 1 0 0	1 0 1 1	1	2	M2(HL), AC ← (TIMER0)	Reads the contents of the timer 0 counter into the M2(HL) and the accumulator (AC).		
	RTIM1	Read timer 1	1 1 0 0 1 1 1 1	1 1 1 1 0 1 0 1	2	2	E, AC ← (TIMER1)	Reads the contents of the timer 1 counter into the E register and the accumulator (AC).		
	START0	Start timer 0	1 1 0 0 1 1 1 0	1 1 1 1 0 1 1 0	2	2	Start timer 0 counter	Starts the timer 0 counter operation.		
	START1	Start timer 1	1 1 0 0 1 1 1 0	1 1 1 1 0 1 1 1	2	2	Start timer 1 counter	Starts the timer 1 counter operation.		
	STOP0	Stop timer 0	1 1 0 0 1 1 1 1	1 1 1 1 0 1 1 0	2	2	Stop timer 0 counter	Stops the timer 0 counter operation.		
	STOP1	Stop timer 1	1 1 0 0 1 1 1 1	1 1 1 1 0 1 1 1	2	2	Stop timer 1 counter	Stops the timer 1 counter operation.		

Instruction type	Mnemonics	Instruction code		Bytes	Cycles	Function	Description	Status flags affected	Remarks
		D <sub>7</sub> D <sub>6</sub> D <sub>5</sub> D <sub>4</sub>	D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>						
Interrupt control instructions	MSET	Set Interrupt Master Enable Flag	1 1 0 0 0 1 0 1	1 1 0 1 0 0 0 0	2	2	MSE←1	Sets the interrupt master enable flag.	
	MRESET	Reset Interrupt Master Enable Flag	1 1 0 0 1 0 0 1	1 1 0 1 0 0 0 0	2	2	MSE←0	Resets the interrupt master enable flag.	
	EIH i4	Enable interrupt high	1 1 0 0 0 1 0 1	1 1 0 1 i <sub>3</sub> i <sub>2</sub> i <sub>1</sub> i <sub>0</sub>	2	2	EDIH←(EDIH)∨i4	Sets the interrupt enable flag.	
	EIL i4	Enable interrupt low	1 1 0 0 0 1 0 0	1 1 0 1 i <sub>3</sub> i <sub>2</sub> i <sub>1</sub> i <sub>0</sub>	2	2	EDIL←(EDIL)∨i4	Sets the interrupt enable flag.	
	DIH i4	Disable interrupt high	1 1 0 0 1 0 0 1	1 1 0 1 i <sub>3</sub> i <sub>2</sub> i <sub>1</sub> i <sub>0</sub>	2	2	EDIH←(EDIH)∧i4	Resets the interrupt enable flag.	ZF
	DIL i4	Disable interrupt low	1 1 0 0 1 0 0 0	1 1 0 1 i <sub>3</sub> i <sub>2</sub> i <sub>1</sub> i <sub>0</sub>	2	2	EDIL←(EDIL)∧i4	Resets the interrupt enable flag.	ZF
	WTSP	Write SP	1 1 0 0 1 1 0 1	1 1 1 1 1 0 1 0	2	2	SP←(E), (AC)	Transfers the contents of the E register and accumulator (AC) to the stack area.	
	RSP	Read SP	1 1 0 0 1 1 0 1	1 1 1 1 1 0 1 1	2	2	E, AC←(SP)	Transfers the contents of the stack area to the E register and accumulator (AC).	
Standby control instructions	HALT	HALT	1 1 0 0 1 1 0 1	1 1 1 1 1 1 1 0	2	2	HALT	Selects the HALT mode.	
	HOLD	HOLD	1 1 0 0 1 1 0 1	1 1 1 1 1 1 1 1	2	2	HOLD	Selects the HOLD mode.	
Serial I/O control instructions	STARTS	Start serial I/O	1 1 0 0 1 1 1 0	1 1 1 1 1 1 1 0	2	2	START SIO	Starts the SIO operation mode.	
	WTSIO	Write serial I/O	1 1 0 0 1 1 1 0	1 1 1 1 1 1 1 1	2	2	SIO←(E), (AC)	Writes the contents of the E register and accumulator (AC) to the SIO register.	
	RSIO	Read serial I/O	1 1 0 0 1 1 1 1	1 1 1 1 1 1 1 1	2	2	E, AC←(SIO)	Reads the contents of the SIO register into the E register and the accumulator (AC).	
Other instructions	NOP	No operation	0 0 0 0	0 0 0 0	1	1	No operation	A dummy instruction that is coded 00H and has no effect when executed. Just one machine cycle signal reaches the CPU.	
	SB i2	Select bank	1 1 0 0 1 1 0 0	1 1 1 1 0 0 1 1	2	2	PC12←i <sub>1</sub> i <sub>0</sub>	Selects memory banks.	

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