

**SANYO**

No. 2156B

**LC6554D,6554H****4K-Byte ROM-Contained Single-Chip 4-Bit Microcomputers  
with FLT, LED Drivers**

The LC6554D/H are single-chip 4-bit microcomputers that contain a 4K-byte ROM, 1K-bit RAM, and have 64 pins. The LC6554D/H have 57 pins for ports – 28 pins for 7 input/output common ports, 21 pins for 6 output ports, and 8 pins for 2 input ports. The LC6554D/H have specific ports that are used to provide the interrupt function, 4-bit/8-bit serial input/output function and burst pulse output function. Each of the 28 pins for input/output common ports contains a driver with a withstand voltage of 15V max. and a drive current of 15mA max. and each of the 21 pins for output ports contains a high-voltage output driver of the P-channel open drain type. Since the high-voltage output driver can be used as general-purpose high-current driver as well as fluorescent tube driver, the LC6554D/H can be also widely used in applications where no fluorescent display is provided. The LC6554D/H are the same as our LC6500 series in the basic architecture of the CPU and the instruction set, but are made more powerful in the stack level and also made easier-to-use in the standby function.

**Features**

- Instruction set with 80 instructions (Common to the LC6500 series)
- On-chip 4096-byte ROM, 1024-bit RAM
- Instruction cycle time: 2.85  $\mu$ s (D version,  $V_{DD} = 4$  to 5.5V)  
0.92  $\mu$ s (H version,  $V_{DD} = 4.5$  to 5.5V)
- Serial input/output interface x 1 (4 bit/8 bit program-selectable)
- I/O ports: 57 pins in all
 

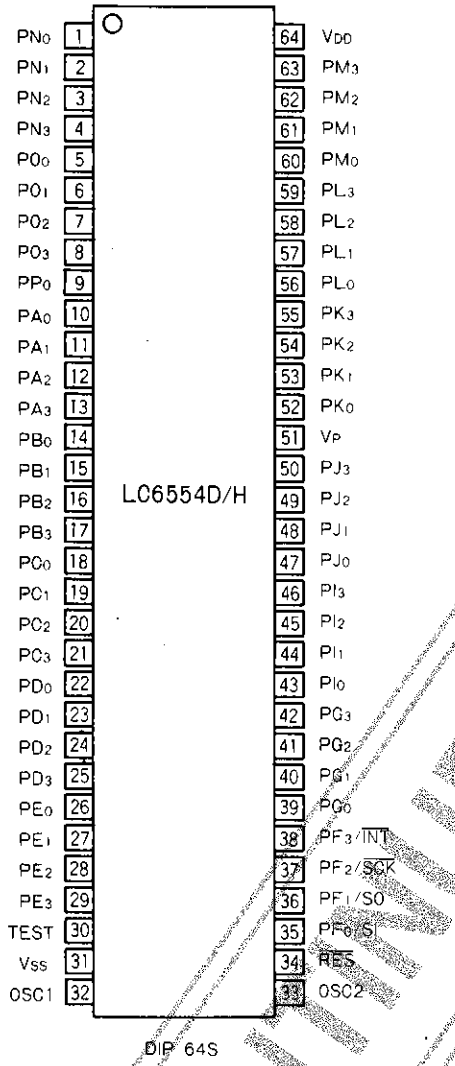
Input ports	8 pins
Input/output common ports	28 pins: 15V max., 15 mA max., LED drivable, pull-up resistance option available
Output ports	21 pins: $V_{DD} - 45$ V withstand voltage, FLT drivable, common with general-purpose output, pull-down resistance option available
- Output level during reset: For ports C, D, output (H or L) during reset may be specified portwise by option.
- Interrupt function
 

Timer interrupt: 1
INT pin or serial I/O interrupt: 1
- Stack level: 8 levels (Common with interrupt)
- Timer: 4-bit prescaler + 8-bit programmable timer
- Burst pulse (64 x cycle time output function)
- Oscillator option
 

Circuit mode: Ceramic resonator mode, RC mode, external clock mode (384 kHz to 4.33 MHz)
Predivider option: 1/1, 1/3, 1/4
- Standby function: Standby function provided by the HALT instruction. Provides the function to absorb the OSC stabilizing time in the ceramic resonator mode.
- Supply Voltage: 4 to 5.5 V (D version)  
4.5 to 5.5 V (H version)
- Package: DIP64 shrink type, QIP64

LC6554D, 6554H

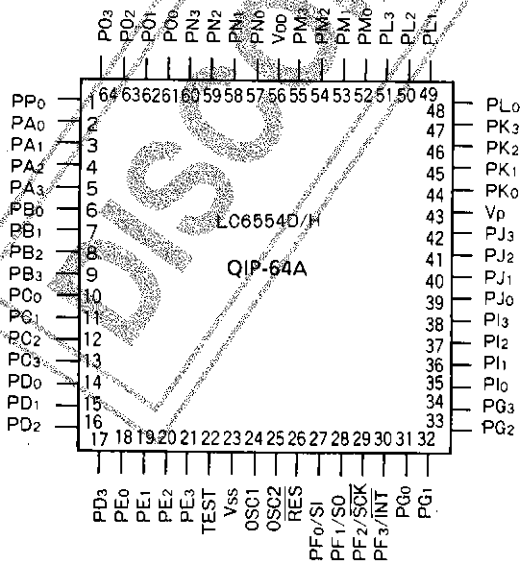
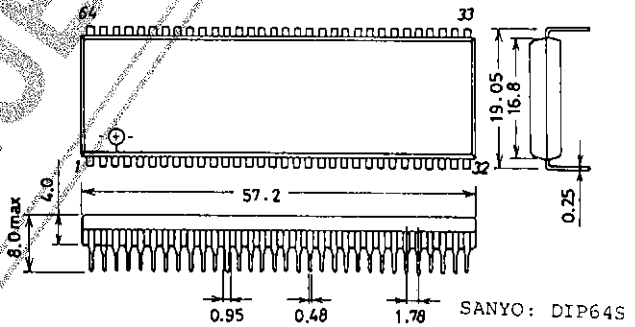
Pin Assignment



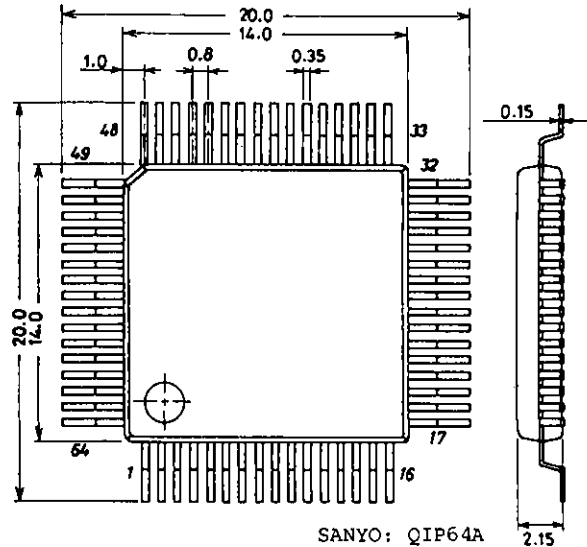
- OSC1, OSC2 : C, R, or ceramic resonator oscillator for OSC
- PA0-3 : Port for input only A0-3
- PB0-3 : Port for input only B0-3
- PC0-3 : Input/output common port C0-3
- PD0-3 : Input/output common port D0-3
- PE0-3 : Input/output common port E0-3
- PF0-3 : Input/output common port F0-3
- PG0-3 : Input/output common port G0-3
- PI0-3 : Input/output common port I0-3
- PJ0-3 : Input/output common port J0-3
- PK0-3 : Port for output only K0-3
- PL0-3 : Port for output only L0-3
- PM0-3 : Port for output only M0-3
- PN0-3 : Port for output only N0-3
- PO0-3 : Port for output only O0-3
- PP0 : Port for output only P0
- SI : 4-bit/8-bit serial input port
- SO : 4-bit/8-bit serial output port
- SCK : Input/output for serial clock
- INT : Interrupt request input
- Vp : Vp pin
- RES : Reset
- TEST : Test

With high-voltage output driver

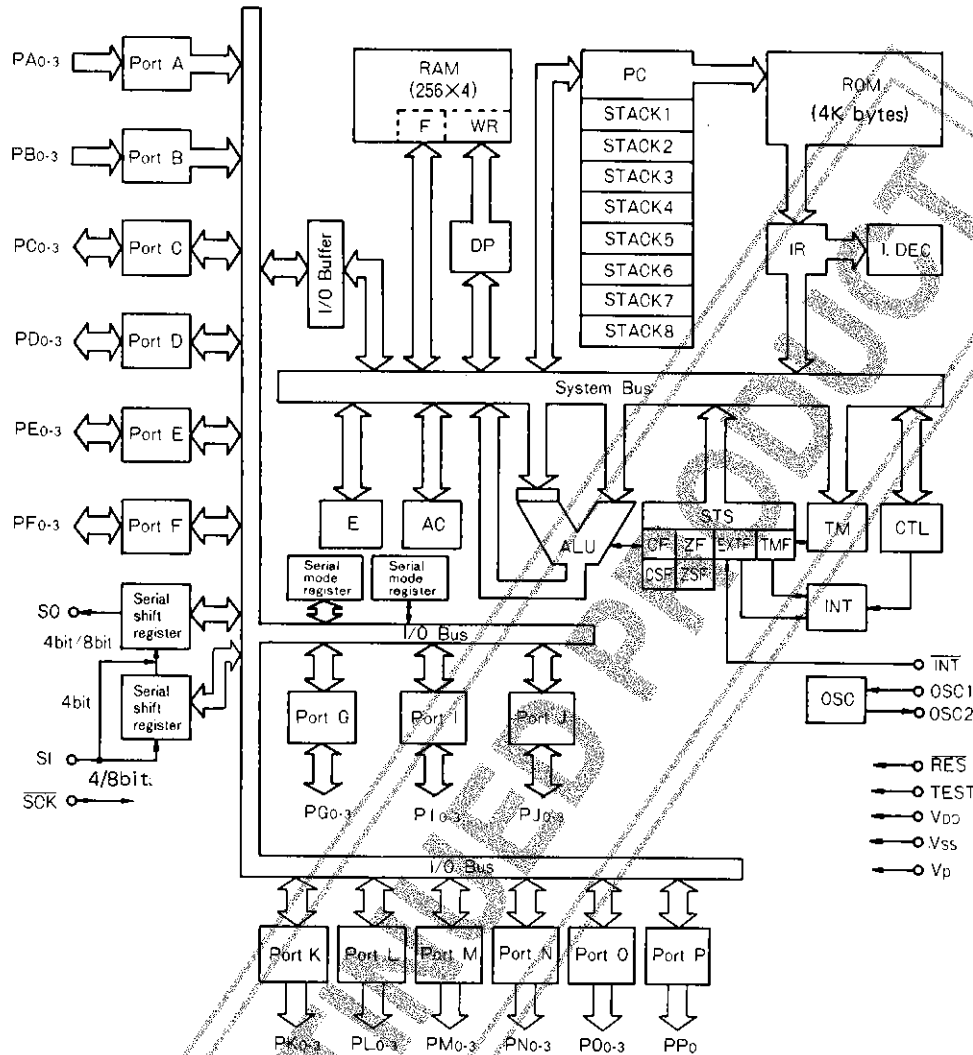
Package Dimensions 3071-D64IC (unit: mm)



Package Dimensions 3057-Q64AIC (unit: mm)



System Block Diagram



- |     |                             |         |                               |
|-----|-----------------------------|---------|-------------------------------|
| RAM | : Data memory               | STS     | : Status register             |
| F   | : Flag                      | ROM     | : Program memory              |
| WR  | : Working register          | PC      | : Program counter             |
| AC  | : Accumulator               | INT     | : Interrupt control           |
| ALU | : Arithmetic and logic unit | IR      | : Instruction register        |
| DP  | : Data pointer              | I.DEC   | : Instruction decoder         |
| E   | : E register                | CF, CSF | : Carry flag, carry save flag |
| CTL | : Control register          | ZF, ZSF | : Zero flag, zero save flag   |
| OSC | : Oscillator                | EXTF    | : External interrupt request  |
| TM  | : Timer                     | TMF     | : Internal interrupt request  |

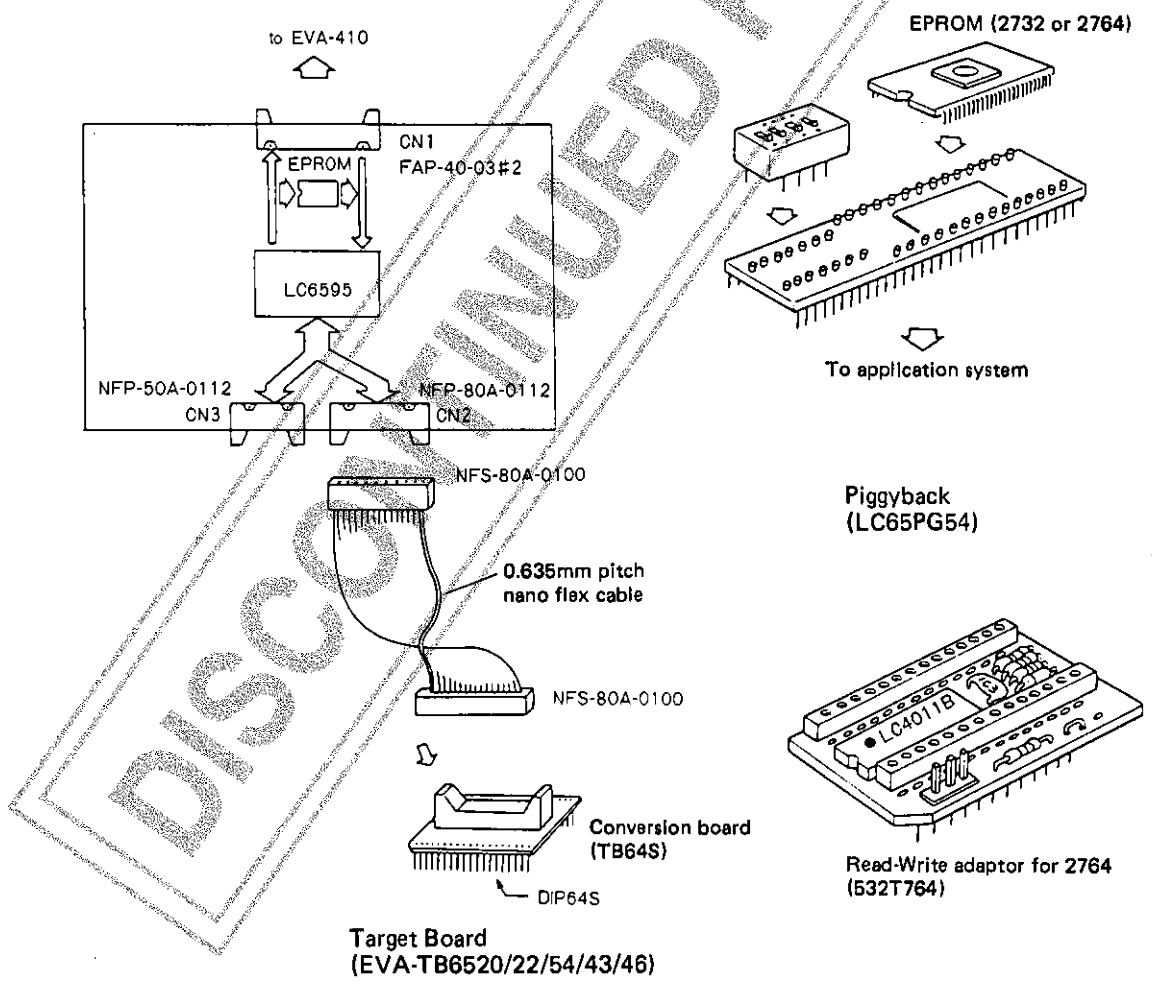
(Note) SI, SO, SCK, INT: Common to PF<sub>0</sub> to PF<sub>3</sub>

**Development Support Tools**

The following are available to support the program development for the LC6554.

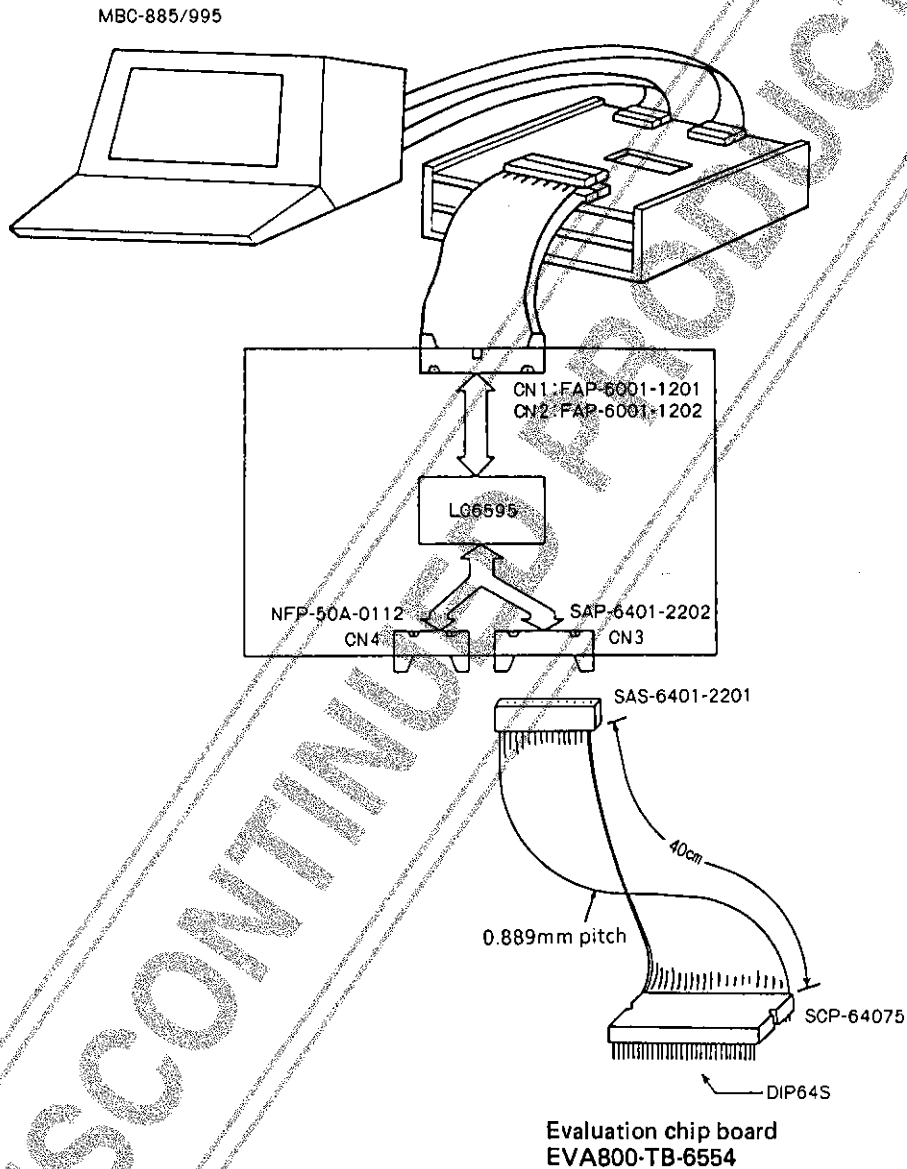
- (1) User's Manual  
"LC6554 Series User's Manual" No. E21B (Issued in December, 1987)
- (2) Development Tool Manual  
For the EVA-410 system, refer to the description of Development support tool in "LC6554 Series User's Manual".  
For the EVA-800 system, refer to "EVA-800 · LC6554 Series Development Tool Manual".
- (3) Development Tools
  - 1) For program development (EVA-410 system)
    - i. (SDS-410) system
    - ii. CP/M80 base cross assembler: (LC6554, COM)
    - iii. Evaluation kit (EVA-410C)
    - iv. Target board (EVA-TB6520/22/54/43/46), evaluation dhip (LC6595)
  - 2) For program evaluation
    - i. Piggyback (LC65PG54)

**Note.** For notes for program evaluation, do not fail to refer to "5-3-4. Notes when evaluating programs for the LC6554" in "LC6554 Series User's Manual".



- (3) For program development (EVA-800 system)
- i. MBC-885/995 (IBM PC/XT, IBM PC-AT compatible) system and cross assembler
  - ii. Cross assembler ..... MS-DOS base cross assembler: (LC6554D.COM, LC6554H.COM)
  - iii. Evaluation chip: LC6595
  - iv. Emulator : EVA-800 control board and evaluation chip board

**Appearance of Development Support System**



(Note 1) IBM PC/XT, IBM PC-AT: Products of IBM Corporation  
 MS-DOS: Trademark of Microsoft Corporation

(Note 2) The EVA-800 is a general term for emulator. A suffix (A, B, ...) is added at the end of EVA-800 as the EVA-800 is improved to be a newer version. Do not use the EVA-800 with no suffix added.

Pin Description

Pin Name	Pins	I/O	Functions	Options	During Reset
VDD VSS	1 1	—	Power supply	—	—
OSC1	1	Input	<ul style="list-style-type: none"> <li>Pin for externally connecting R,C or a ceramic resonator for system clock generation</li> <li>For the external clock mode, the OSC2 pin is open.</li> </ul>	<ol style="list-style-type: none"> <li>External clock input</li> <li>2-pin RC OSC</li> <li>2-pin ceramic resonator OSC</li> <li>Predivider option                             <ol style="list-style-type: none"> <li>No predivider</li> <li>1/3 predivider</li> <li>1/4 predivider</li> </ol> </li> </ol>	—
OSC2	1	Output			—
PA0 PA1 PA2 PA3	4	Input	<ul style="list-style-type: none"> <li>Input port A0 to 3 (Low-threshold input)</li> <li>4-bit input (IP instruction)</li> <li>Single-bit decision (BP, BNP instructions)</li> </ul>	—	—
PB0 PB1 PB2 PB3	4	Input	<ul style="list-style-type: none"> <li>Input port B0 to 3 (Low-threshold input)</li> <li>4-bit input (IP instruction)</li> <li>Single-bit decision (BP, BNP instructions)</li> <li>Standby is controlled by the PB3</li> <li>The PB3 pin must be free from chattering during the HALT instruction execution cycle.</li> </ul>	—	—
PC0 PC1 PC2 PC3	4	Input/output	<ul style="list-style-type: none"> <li>Input/output common port C0 to 3.</li> <li>4-bit input (IP instruction)</li> <li>4-bit output (OP instruction)</li> <li>Single-bit decision (BP, BNP instructions)</li> <li>Single-bit set/reset (SPB, RPB instructions)</li> <li>Output ("H" or "L") during reset may be specified by option.</li> </ul>	<ol style="list-style-type: none"> <li>Open drain type output</li> <li>With pull-up resistance</li> <li>Output during reset: "H"</li> <li>Output during reset: "L"</li> </ol> <ul style="list-style-type: none"> <li>(1), (2): Specified bit by bit.</li> <li>(3), (4): Specified in a group of 4 bits.</li> </ul>	<ul style="list-style-type: none"> <li>"H" output</li> <li>"L" output (Option-selectable)</li> </ul>
PD0 PD1 PD2 PD3	4	Input/output	<ul style="list-style-type: none"> <li>Input/output common port D0 to 3.</li> <li>The functions, options are the same as for the PC0 to 3.</li> </ul>	Same as for the PC0 to 3.	Same as for the PC0 to 3.
PE0 PE1 PE2 PE3	4	Input/output	<ul style="list-style-type: none"> <li>Input/output common port E0 to 3</li> <li>4-bit input (IP instruction)</li> <li>4-bit output (OP instruction)</li> <li>Single-bit decision (BP, BNP instructions)</li> <li>Single-bit set/reset (SPB, RPB instructions)</li> <li>PE0: With burst pulse (64T<sub>cyc</sub>) output function</li> </ul>	<ol style="list-style-type: none"> <li>Open drain type output</li> <li>With pull-up resistance</li> </ol> <p>(1), (2): Specified bit by bit.</p>	<ul style="list-style-type: none"> <li>"H" output (Output Nch transistor OFF)</li> </ul>

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Pin Name	Pins	I/O	Functions	Options	During Reset
PF0/SI PF1/SO PF2/SCK PF3/INT	4	Input/output	<ul style="list-style-type: none"> <li>Input/output port F0 to 3 The functions, options are the same as for the PE0 to 3. However, no burst pulse output function is provided.</li> <li>PF0 to 3: Also used for serial interface, INT input. Program-selectable.</li> <li>4-bits/8 bits of serial input/output: Program-selectable SI: Serial input port SO: Serial output port SCK: Serial clock input/output INT: Interrupt request input</li> </ul>	Same as for the PE0 to 3.	Same as for the PE0 to 3. Serial port: Disable Interrupt source: INT
PG0 PG1 PG2 PG3	4	Input/output	<ul style="list-style-type: none"> <li>Input/output common port G0 to 3. The functions, options are the same as for the PE0 to 3. However, no burst pulse output function is provided.</li> </ul>	Same as for the PE0 to 3.	Same as for the PE0 to 3.
PI0 PI1 PI2 PI3	4	Input/output	<ul style="list-style-type: none"> <li>Input/output common port I0 to 3 The functions, options are the same as for the PG0 to 3.</li> </ul>	Same as for the PG0 to 3.	Same as for the PG0 to 3.
PJ0 PJ1 PJ2 PJ3	4	Input/output	<ul style="list-style-type: none"> <li>Input/output common port J0 to 3 The functions, options are the same as for the PG0 to 3.</li> </ul>	Same as for the PG0 to 3.	Same as for the PG0 to 3.
PK0 PK1 PK2 PK3	4	Output	<ul style="list-style-type: none"> <li>Output port K0 to 3 (Segment driver output) 4-bit output (OP instruction) Single-bit decision (BP, BNP instructions) Single-bit set/reset (SPB, RPB instructions)</li> </ul>	(1) Open drain type output (2) With pull-down resistance <ul style="list-style-type: none"> <li>(1), (2): Specified bit by bit.</li> </ul>	"L" output (Output Pch transistor OFF)
PL0 PL1 PL2 PL3	4	Output	<ul style="list-style-type: none"> <li>Output port L0 to 3 (Segment driver output) The functions, options are the same as for the PK0 to 3.</li> </ul>	Same as for the PK0 to 3.	Same as for the PK0 to 3.
PM0 PM1 PM2 PM3	4	Output	<ul style="list-style-type: none"> <li>Output port M0 to 3 (Digit driver output) The functions, options are the same as for the PK0 to 3.</li> </ul>	Same as for the PK0 to 3.	Same as for the PK0 to 3.
PN0 PN1 PN2 PN3	4	Output	<ul style="list-style-type: none"> <li>Output port N0 to 3 (Digit driver output) The functions, options are the same as for the PK0 to 3.</li> </ul>	Same as for the PK0 to 3.	Same as for the PK0 to 3.

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Pin Name	Pins	I/O	Functions	Options	During Reset
PO <sub>0</sub> PO <sub>1</sub> PO <sub>2</sub> PO <sub>3</sub>	4	Output	<ul style="list-style-type: none"> <li>Output port O<sub>0</sub> to 3 (Digit driver output)</li> <li>The functions, options are the same as for the PK<sub>0</sub> to 3.</li> </ul>	Same as for the PK <sub>0</sub> to 3.	Same as for the PK <sub>0</sub> to 3.
PP <sub>0</sub>	1	Output	<ul style="list-style-type: none"> <li>Output port P<sub>0</sub> (Digit driver output)</li> <li>The functions, options are the same as for the PK<sub>0</sub> to 3.</li> <li>This port consists of a single bit.</li> </ul>	Same as for the PK <sub>0</sub> to 3.	Same as for the PK <sub>0</sub> to 3.
$\overline{\text{RES}}$	1	Input	<ul style="list-style-type: none"> <li>System reset input</li> <li>For power-up reset, C is connected externally.</li> <li>For reset restart, "L" level is applied for 4 clock cycles or more.</li> </ul>	—	—
TEST	1	Input	<ul style="list-style-type: none"> <li>LSI test pin</li> <li>Normally connected to V<sub>SS</sub></li> </ul>	—	—
V <sub>p</sub>	1	—	<ul style="list-style-type: none"> <li>Power supply pin for pull-down resistance</li> </ul>	—	—

Oscillator Circuit Option

Option Name	Circuit	Conditions, etc.
1. External Clock		<ul style="list-style-type: none"> <li>Input: Schmitt type.</li> </ul>
2. 2-pin RC OSC		<ul style="list-style-type: none"> <li>Input: Schmitt type.</li> </ul>
3. Ceramic Resonator OSC		



Predivider Option

Option Name	Circuit	Conditions, etc.
1. No predivider		<ul style="list-style-type: none"> <li>• Applicable to all of 3 OSC options.</li> <li>• The OSC frequency, external clock do not exceed 1444 kHz. (LC6554D)</li> <li>• The OSC frequency, external clock do not exceed 4330 kHz. (LC6554H)</li> <li>• Refer to Table of OSC, Predivider Option (Table 2).</li> </ul>
2. 1/3 predivider		<ul style="list-style-type: none"> <li>• Applicable to only 2 options of external clock, ceramic resonator OSC.</li> <li>• The OSC frequency, external clock do not exceed 4330 kHz.</li> <li>• Refer to Table of OSC, Predivider Option (Table 2).</li> </ul>
3. 1/4 predivider		<ul style="list-style-type: none"> <li>• Applicable to only 2 options of external clock, ceramic resonator OSC.</li> <li>• The OSC frequency, external clock do not exceed 4330 kHz.</li> <li>• Refer to Table of OSC, Predivider Option (Table 2).</li> </ul>

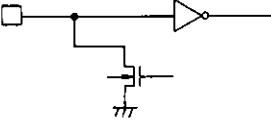
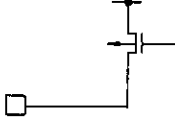
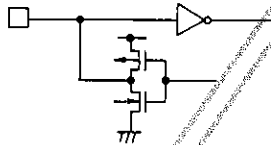
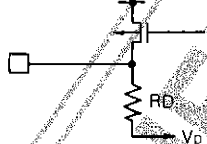
Options of Ports C, D Output Level during Reset

For input/output common ports C, D, either of the following two output levels may be selected in a group of 4 bits during reset by option.

Option Name	Conditions, etc.
1. Output during reset: "H" level	All of 4 bits of ports C, D
2. Output during reset: "L" level	All of 4 bits of ports C, D

Options of Port Output Configuration

For each input/output common port, either of the following two output configurations may be selected by option (bitwise).

Option Name	Circuit	Applicable Ports
1. Open drain type output		Ports C, D, E, F, G, I, J
		Ports K, L, M, N, O, P
2. Output with pull-up resistance		Ports C, D, E, F, G, I, J
3. Output with pull-down resistance		Ports K, L, M, N, O, P

DISCONTINUED PRODUCT

## LC6554D

1. Absolute Maximum Ratings/ $T_a=25^\circ\text{C}$ ,  $V_{SS}=0\text{V}$ 

				unit
Maximum Supply Voltage	$V_{DD\text{ max}}$	$V_{DD}$	-0.3 to +7.0	V
Output Voltage	$V_{O(1)}$	OSC2	Allowable up to voltage generated	V
Input Voltage	$V_{O(2)}$	Port K to P	$V_{DD}-45$ to $V_{DD}+0.3$	V
	$V_{I(1)}$	OSC1 (Note 1)	-0.3 to $V_{DD}+0.3$	V
	$V_{I(2)}$	TEST, RES	-0.3 to $V_{DD}+0.3$	V
	$V_{I(3)}$	Port A, B	-0.3 to +15	V
Input/Output Voltage	$V_{I(4)}$	$V_p$	$V_{DD}-45$ to $V_{DD}+0.3$	V
	$V_{IO(1)}$	Port of OD type (Port C to J)	-0.3 to +15	V
	$V_{IO(2)}$	Port of PU type (Port C to J)	-0.3 to $V_{DD}+0.3$	V
Peak Output Current	$I_{OP(1)}$	Port C to J	-2 to +15	mA
	$I_{OP(2)}$	Port K, L	-10 to 0	mA
	$I_{OP(3)}$	Port M to P	-15 to 0	mA
Average Output Current	$I_{OA(1)}$	Per pin over the period of 100 ms Port C to J	-2 to +15	mA
	$I_{OA(2)}$	Per pin over the period of 100 ms Port K, L	-10 to 0	mA
	$I_{OA(3)}$	Per pin over the period of 100 ms Port M to P	-15 to 0	mA
	$\Sigma I_{OA(1)}$	Total current of all pins (Note 2) Port C, D, E	-30 to +50	mA
	$\Sigma I_{OA(2)}$	Total current of all pins (Note 2) Port F to J	-30 to +50	mA
	$\Sigma I_{OA(3)}$	Total current of all pins (Note 2) Port K, L, M	-50 to 0	mA
	$\Sigma I_{OA(4)}$	Total current of all pins (Note 2) Port N, O, P	-50 to 0	mA
	Allowable Power Dissipation	$P_{d\text{ max}(1)}$	$T_a=-30$ to $+70^\circ\text{C}$ (QIP)	430
$P_{d\text{ max}(2)}$		$T_a=-30$ to $+70^\circ\text{C}$ (DIP)	600	mW
Operating Temperature	$T_{opr}$		-30 to +70	$^\circ\text{C}$
Storage Temperature	$T_{stg}$		-55 to +125	$^\circ\text{C}$

2. Allowable Operating Conditions/ $T_a=-30$  to  $+70^\circ\text{C}$ ,  $V_{SS}=0\text{V}$ ,  $V_{DD}=4.0$  to  $5.5\text{V}$ 

			min	typ	max	unit
Operating Supply Voltage	$V_{DD}$	$V_{DD}$	4.0		5.5	V
Standby Supply Voltage	$V_{st}$	RAM, register hold(Note 3)	1.8		5.5	V
"H"-Level Input Voltage	$V_{IH(1)}$	Port A, B0 to 2	1.9		+13.5	V
	$V_{IH(2)}$	Output Nch Tr OFF Port of OD type (Port C to J)	$0.7V_{DD}$		+13.5	V
$V_{IH(3)}$	Output Nch Tr OFF Port of PU type (Port C to J)	$0.7V_{DD}$		$V_{DD}$	V	
$V_{IH(4)}$	Output Nch Tr OFF INT, SCK, SI of OD type	$0.8V_{DD}$		+13.5	V	
$V_{IH(5)}$	Output Nch Tr OFF INT, SCK, SI of PU type	$0.8V_{DD}$		$V_{DD}$	V	
$V_{IH(6)}$		RES	$0.8V_{DD}$		$V_{DD}$	V
$V_{IH(7)}$	External clock mode	OSC1	$0.8V_{DD}$		$V_{DD}$	V
$V_{IH(8)}$	Fig. 8	High $V_t$ input circuit of Port B3	$V_{DD}-0.5$		+13.5	V
$V_{IH(9)}$	Fig. 8	Low $V_t$ input circuit of Port B3	$0.5V_{DD}$		+13.5	V

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			min	typ	max	unit
"L"-Level Input Voltage	V <sub>IL</sub> (1)	Port A, B <sub>0</sub> to 2	V <sub>SS</sub>		+0.5	V
	V <sub>IL</sub> (2)	Port C to J	V <sub>SS</sub>	0.3V <sub>DD</sub>		V
	V <sub>IL</sub> (3)	INT, SCK, SI	V <sub>SS</sub>	0.25V <sub>DD</sub>		V
	V <sub>IL</sub> (4)	TEST	V <sub>SS</sub>	0.3V <sub>DD</sub>		V
	V <sub>IL</sub> (5)	RES	V <sub>SS</sub>	0.25V <sub>DD</sub>		V
	V <sub>IL</sub> (6)	External clock mode OSC1	V <sub>SS</sub>	0.25V <sub>DD</sub>		V
	V <sub>IL</sub> (7)	Fig. 8 Low V <sub>t</sub> input circuit of Port B <sub>3</sub>	V <sub>SS</sub>		+0.9	V
Operating Frequency (Cycle Time)	f <sub>op</sub>		384		1444	kHz
	(TCYC)		(10.4)		(2.77)	(μs)
External Clock Conditions (When the external clock or 2-pin RC OSC option is selected)						
Frequency	f <sub>ext</sub>					
Pulse Width	textH, textL	Fig. 1	OSC1			
Rise/Fall Time	textR, textF		OSC1	90		
Oscillation Guaranteed Constants						
2-Pin RC Oscillation	C <sub>ext</sub>	Fig. 2	OSC1, OSC2	220±5%		pF
	R <sub>ext</sub>	Fig. 2	OSC1, OSC2	6.8±1%		kΩ
Ceramic Resonator Oscillation		Fig. 3				See Table 1.
<b>3. Electrical Characteristics/T<sub>a</sub>=-30 to +70°C, V<sub>SS</sub>=0V, V<sub>DD</sub>=4.0 to 5.5V</b>						
"H"-Level Input Current	I <sub>IH</sub> (1)	Output Nch Tr OFF (Including OFF leakage current of Nch Tr) V <sub>IN</sub> =+13.5V	Port of OD type (Port C to J) Port A, B		+5.0	μA
	I <sub>IH</sub> (2)	External clock mode, V <sub>IN</sub> =V <sub>DD</sub>	OSC1		+1.0	μA
"L"-Level Input Current	I <sub>IL</sub> (1)	Output Nch Tr OFF V <sub>IN</sub> =V <sub>SS</sub>	Port of OD type (Port C to J) Port A, B	-1.0		μA
	I <sub>IL</sub> (2)	Output Nch Tr OFF V <sub>IN</sub> =V <sub>SS</sub>	Port of PU type (Port C to J)	-1.3	-0.35	mA
	I <sub>IL</sub> (3)	V <sub>IN</sub> =V <sub>SS</sub>	RES	-45	-10	μA
	I <sub>IL</sub> (4)	External clock mode, V <sub>IN</sub> =V <sub>SS</sub>	OSC1	-1.0		μA
"H"-Level Output Voltage	V <sub>OH</sub> (1)	I <sub>OH</sub> =-50μA	Port of PU type (Port C to J)	V <sub>DD</sub> -1.2		V
	V <sub>OH</sub> (2)	I <sub>OH</sub> =-3mA	Port K, L	V <sub>DD</sub> -1.8		V
	V <sub>OH</sub> (3)	I <sub>OH</sub> =-10mA	Port M to P	V <sub>DD</sub> -1.8		V
"L"-Level Output Voltage	V <sub>OL</sub> (1)	I <sub>OL</sub> =10mA	Port C to J		1.5	V
	V <sub>OL</sub> (2)	I <sub>OL</sub> =2mA, When I <sub>OL</sub> of each port is 2mA or less	Port C to J		0.5	V
	V <sub>OL</sub> (3)	Output Pch Tr OFF V <sub>p</sub> =-35V Output open	Port of PD type (Port K to P)		-33	V
Output OFF Leakage Current	I <sub>OFF</sub> (1)	Output Pch Tr OFF V <sub>OUT</sub> =V <sub>DD</sub>	Port of OD type (Port K to P)		+30	μA
	I <sub>OFF</sub> (2)	Output Pch Tr OFF V <sub>OUT</sub> =V <sub>DD</sub> -40V	Port of OD type (Port K to P)	-30		μA
Hysteresis Voltage	V <sub>HYS</sub>		RES, INT, SCK, SI, OSC1 of Schmitt type (Note 5)	0.1V <sub>DD</sub>		V

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LC6554D

				min	typ	max	unt
Current Dissipation	Operation mode, Output Nch Tr, Pch Tr OFF, Port=VDD						
2-Pin RC Oscillation Mode	I <sub>DDOP(1)</sub>	Fig. 2 f <sub>OSC</sub> =700kHz(TYP)	V <sub>DD</sub>		1.5	5	mA
Ceramic Resonator Oscillation Mode	I <sub>DDOP(2)</sub>	Fig. 3 4MHz, 1/3 predivider	V <sub>DD</sub>		5	10	mA
	I <sub>DDOP(3)</sub>	Fig. 3 4MHz, 1/4 predivider	V <sub>DD</sub>		5	10	mA
	I <sub>DDOP(4)</sub>	Fig. 3 3MHz, 1/3 predivider	V <sub>DD</sub>		4	9	mA
	I <sub>DDOP(5)</sub>	Fig. 3 3MHz, 1/4 predivider	V <sub>DD</sub>		4	9	mA
	I <sub>DDOP(6)</sub>	Fig. 3 400kHz	V <sub>DD</sub>		0.6	3	mA
	I <sub>DDOP(7)</sub>	Fig. 3 800kHz*	V <sub>DD</sub>		1.2	4	mA
External Clock Mode	I <sub>DDOP(8)</sub>	384kHz to 1444kHz, 1/1 predivider	V <sub>DD</sub>		2	6	mA
		1152kHz to 4330kHz, 1/3 predivider	V <sub>DD</sub>		5	10	mA
		1536kHz to 4330kHz, 1/4 predivider					
Standby Mode	I <sub>DDSt</sub>	V <sub>DD</sub> =5.5V	V <sub>DD</sub>		0.05	10	μA
		Output Nch Tr OFF					
		Output Pch Tr OFF					
		Port=V <sub>DD</sub>					
Oscillation Characteristics							
Ceramic Resonator Oscillation							
Oscillation Frequency	f <sub>CFOSC</sub> (Note 4)	Fig. 3 fo=400kHz	OSC1, OSC2	392	400	408	kHz
		Fig. 3 fo=800kHz	OSC1, OSC2	784	800	816	kHz
		Fig. 3 fo=3MHz, 1/3 predivider	OSC1, OSC2	2940	3000	3060	kHz
		1/4 predivider					
		Fig. 3 fo=4MHz, 1/3 predivider	OSC1, OSC2	3920	4000	4080	kHz
		1/4 predivider					
Oscillation Stabilizing Period	t <sub>CFS</sub>	Fig. 4 fo=400kHz, 800kHz, 3MHz, 4MHz				10	ms
2-Pin RC Oscillation							
Oscillation Frequency	f <sub>MOSC</sub>	Fig. 2 C <sub>ext</sub> =220pF ±5% R <sub>ext</sub> =6.8kΩ ±1%	OSC1, OSC2	486	700	1056	kHz
Pull-up Resistance							
I/O Port Pull-up Resistance	R <sub>pp</sub>	V <sub>DD</sub> =5V	Port of PU type (Port C to J)		14		kΩ
Pull-down Resistance							
Output Port Pull-down Resistance	R <sub>pd</sub>	V <sub>DD</sub> =5V	Port of PD type (Port K to P)	50		200	kΩ
External Reset Characteristics							
Reset Time	T <sub>RST</sub>						See Fig. 5.

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**LC6554D**

				min	typ	max	unit
Pin Capacitance	CP	f=1MHz Other than pins to be tested, V <sub>IN</sub> =V <sub>SS</sub>			10		pF
<b>Serial Clock</b>							
Input Clock Cycle Time	t <sub>CKCY</sub> (1)	Fig. 6	$\overline{\text{SCK}}$	3.0			μs
Output Clock Cycle Time	t <sub>CKCY</sub> (2)	Fig. 6	$\overline{\text{SCK}}$		64 × T <sub>CYC</sub>		μs
					(T <sub>CYC</sub> =4 × System clock period)		
Input Clock "L"-Level Pulse Width	t <sub>CKL</sub> (1)	Fig. 6	$\overline{\text{SCK}}$	1.0			μs
Output Clock "L"-Level Pulse Width	t <sub>CKL</sub> (2)	Fig. 6	$\overline{\text{SCK}}$		32 × T <sub>CYC</sub>		μs
Input Clock "H"-Level Pulse Width	t <sub>CKH</sub> (1)	Fig. 6	$\overline{\text{SCK}}$	1.0			μs
Output Clock "H"-Level Pulse Width	t <sub>CKH</sub> (2)	Fig. 6	$\overline{\text{SCK}}$		32 × T <sub>CYC</sub>		μs
<b>Serial Input</b>							
Data Setup Time	t <sub>ICK</sub>	Specified for ↑ of $\overline{\text{SCK}}$ , Fig. 6	SI	0.5			μs
Data Hold Time	t <sub>CKI</sub>		SI	0.5			μs
<b>Serial Output</b>							
Output Delay Time	t <sub>CKO</sub>	Specified for ↓ of $\overline{\text{SCK}}$ , Nch OD only: External 1kohm, external 50pF Fig. 6	SO			0.5	μs
<b>Pulse Output</b>							
Period	t <sub>PCY</sub>	Fig. 7	PE <sub>0</sub>		64 × T <sub>CYC</sub>		μs
"H"-Level Pulse Width	t <sub>PH</sub>	T <sub>CYC</sub> =4 × System clock period, Nch OD only:	PE <sub>0</sub>		32 × T <sub>CYC</sub> ±10%		μs
"L"-Level Pulse Width	t <sub>PL</sub>	External 1kohm, external 50pF	PE <sub>0</sub>		32 × T <sub>CYC</sub> ±10%		μs

- Note 1: When oscillated internally under the oscillating conditions in Fig. 3, up to the oscillation amplitude generated is allowable.
- Note 2: Average over the period of 100msec.
- Note 3: Operating supply voltage V<sub>DD</sub> must be held until the standby mode is entered after the execution of the HALT instruction.  
The PB<sub>3</sub> pin must be free from chattering during the HALT instruction execution cycle.
- Note 4: f<sub>COSC</sub> represents an oscillatable frequency. There is a tolerance of approximately 1% between the center frequency at the ceramic mode and the nominal value presented by the ceramic resonator supplier. For details, refer to the specification for the ceramic resonator.
- Note 5: The OSC1 becomes the Schmitt type when the OSC option is the 2-pin RC OSC or external clock OSC.
- Note 6: When mounting the QIP version on the board, do not dip it in solder.

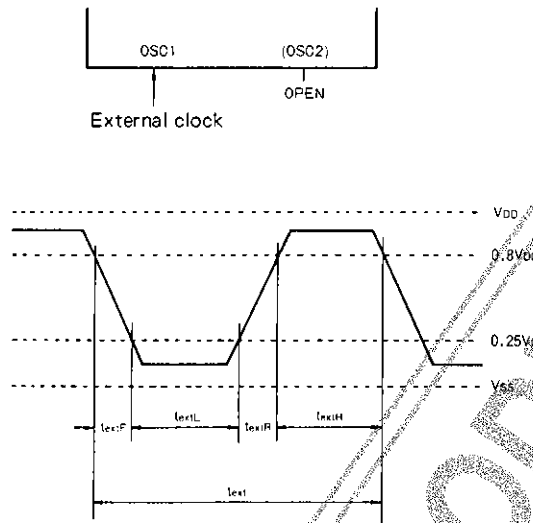


Fig. 1 External Clock Input Waveform

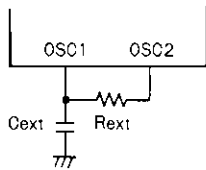


Fig. 2 2-Pin RC Oscillation Circuit

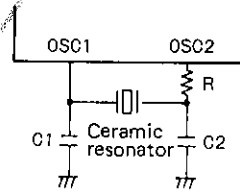


Fig. 3 Ceramic Resonator Oscillation Circuit

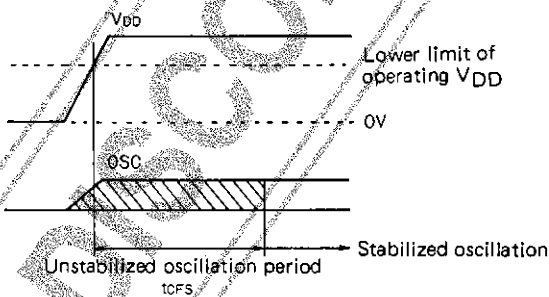


Fig. 4 Oscillation Stabilizing Period

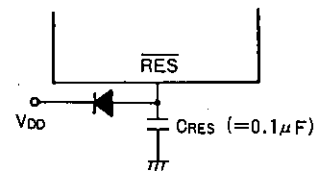


Fig. 5 Reset Circuit

Note 7: When the rise time of the power supply is 0, the reset time becomes 10 ms to 100 ms at  $C_{RES}=0.1 \mu F$ . If the rise time of the power supply is long, the value of  $C_{RES}$  must be increased so that the reset time becomes 10 ms or greater.

4MHz CSA4.00MG (Murata)	C 1	33pF ± 10%	800KHz CSB800D CSB800K (Murata)	C 1	220pF ± 10%
	C 2	33pF ± 10%		C 2	220pF ± 10%
	R	0 Ω		R	0 Ω
4MHz KBR4.0MS (Kyocera)	C 1	33pF ± 10%	800KHz KBR800H (Kyocera)	C 1	220pF ± 10%
	C 2	33pF ± 10%		C 2	220pF ± 10%
	R	0 Ω		R	0 Ω
3MHz CSA3.00MG (Murata)	C 1	33pF ± 10%	400KHz CSB400P (Murata)	C 1	330pF ± 10%
	C 2	33pF ± 10%		C 2	330pF ± 10%
	R	0 Ω		R	0 Ω
3MHz KBR3.0MS (Kyocera)	C 1	47pF ± 10%	400KHz KBR400B (Kyocera)	C 1	330pF ± 10%
	C 2	47pF ± 10%		C 2	330pF ± 10%
	R	0 Ω		R	0 Ω

Table 1 Constants Guaranteed for Ceramic Resonator Oscillation

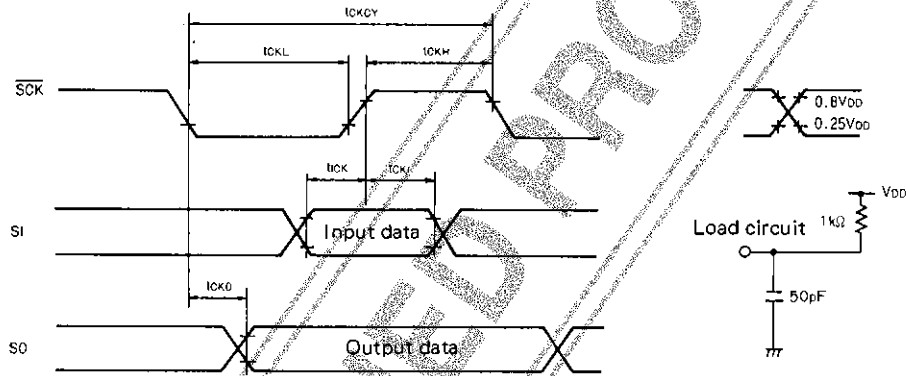


Fig. 6 Serial Input/Output Timing

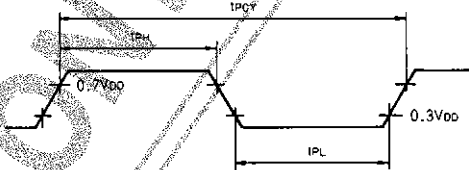


Fig. 7 Pulse Output Timing at Port PEg

The load conditions are the same as in Fig. 6.

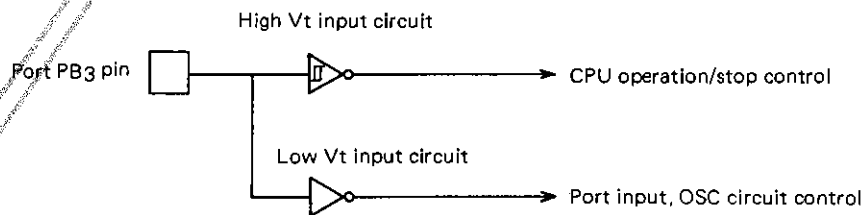


Fig. 8 Port PB3 High Vt/Low Vt Input Circuit



Table 2 LC6554D

Table of Oscillation, Predivider Option (All selectable combinations are shown. Do not use any other combinations than shown below.)  $V_{DD}=4$  to  $5.5V$

Circuit Configuration	Frequency	Predivider Option (Cycle Time)	Remarks
Ceramic Resonator Option	400 kHz	1/1 (10 $\mu$ s)	Unusable with 1/3, 1/4 predivider
	800 kHz	1/1 (5 $\mu$ s)	Unusable with 1/3, 1/4 predivider
	3 MHz	1/3 (4 $\mu$ s)	Unusable with 1/1 predivider
		1/4 (5.33 $\mu$ s)	
4 MHz	1/3 (3 $\mu$ s)	Unusable with 1/1 predivider	
	1/4 (4 $\mu$ s)		
External Clock Option or External Clock Drive by RC OSC Option	384 to 1444 kHz	1/1 (10.4 to 2.77 $\mu$ s)	
	1152 to 4330 kHz	1/3 (10.4 to 2.77 $\mu$ s)	
	1536 to 4330 kHz	1/4 (10.4 to 3.70 $\mu$ s)	
External Clock Drive by Ceramic Resonator OSC Option	The external clock drive is impossible. When using the external clock drive, specify the external clock option or RC OSC option.		
RC OSC Option	Used with 1/1 predivider, recommended constants. If used with other than recommended constants, the predivider option, frequency, $V_{DD}$ range must be the same as for the external clock option.		

RC Oscillation Characteristic of the LC6554D

Fig. 8 shows the RC oscillation characteristic of the LC6554D. For the variation range of RC OSC frequency of the LC6554D, the following are guaranteed at the external constants only shown below.

External constants  $C_{ext}=220$  pF,  $R_{ext}=6.8$  kohms

$$486 \text{ kHz} \leq f_{MOSC} \leq 1056 \text{ kHz} \quad (T_a = -30^\circ\text{C} \text{ to } +70^\circ\text{C}, V_{DD}=4.0 \text{ to } 5.5 \text{ V})$$

If any other constants than specified above are used, the range of  $R_{ext} = 4$  kohms to  $20$  kohms,  $C_{ext} = 150$  pF to  $390$  pF must be observed. (See Fig. 8.)

Note 8: The oscillation frequency at  $V_{DD}=5.0$  V,  $T_a=25^\circ\text{C}$  must not exceed  $700$  kHz.

Note 9: The oscillation frequency at  $V_{DD}=4$  to  $5.5$  V,  $T_a=-30$  to  $+70^\circ\text{C}$  must be within the operation clock frequency range ( $384$  kHz to  $1444$  kHz).

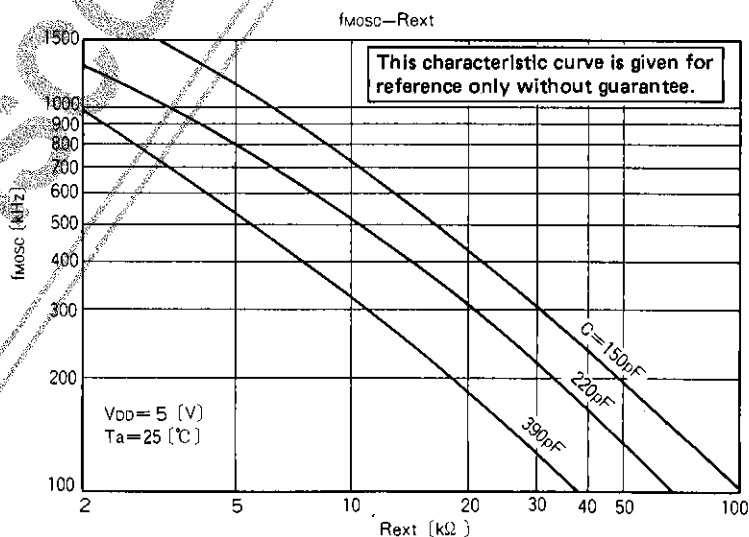


Fig. 8 RC Oscillation Frequency Data (Typ.)

**LC6554H**

**1. Absolute Maximum Ratings/Ta=25°C, VSS=0V**

				unit
Maximum Supply Voltage	VDD max	VDD	-0.3 to +7.0	V
Output Voltage	VO(1)	OSC2	Allowable up to voltage generated	V
Input Voltage	VO(2)	Port K to P	VDD-45 to VDD+0.3	V
	VI(1)	OSC1 (Note 1)	-0.3 to VDD+0.3	V
	VI(2)	TEST, RES	-0.3 to VDD+0.3	V
	VI(3)	Port A, B	-0.3 to +15	V
Input/Output Voltage	VI(4)	Vp	VDD-45 to VDD+0.3	V
	VI(1)	Port of OD type (Port C to J)	-0.3 to +15	V
	VI(2)	Port of PU type (Port C to J)	-0.3 to VDD+0.3	V
Peak Output Current	IOP(1)	Port C to J	-2 to +15	mA
	IOP(2)	Port K, L	-10 to 0	mA
	IOP(3)	Port M to P	-15 to 0	mA
Average Output Current	IOA(1)	Per pin over the period of 100 msec. Port C to J	-2 to +15	mA
	IOA(2)	Per pin over the period of 100 msec. Port K, L	-10 to 0	mA
	IOA(3)	Per pin over the period of 100 msec. Port M to P	-15 to 0	mA
	ΣIOA(1)	Total current of all pins (Note 2) Port C, D, E	-30 to +50	mA
	ΣIOA(2)	Total current of all pins (Note 2) Port F to J	-30 to +50	mA
	ΣIOA(3)	Total current of all pins (Note 2) Port K, L, M	-50 to 0	mA
	ΣIOA(4)	Total current of all pins (Note 2) Port N, O, P	-50 to 0	mA
	Allowable Power Dissipation	Pd max(1)	Ta=-30 to +70°C(QIP)	430
Pd max(2)		Ta=-30 to +70°C(DIP)	600	mW
Operating Temperature	Topr		-30 to +70	°C
Storage Temperature	Tstg		-55 to +125	°C

**2. Allowable Operating Conditions/Ta=-30 to +70°C, VSS=0V, VDD=4.5 to 5.5V**

			min	typ	max	unit
Operating Supply Voltage	VDD	VDD	4.5		5.5	V
Standby Supply Voltage	Vst	RAM, register hold(Note 3)	1.8		5.5	V
"H"-Level Input Voltage	VIH(1)	Port A, B0 to 2	1.9		+13.5	V
	VIH(2)	Output Nch Tr OFF Port of OD type (Port C to J)	0.7VDD		+13.5	V
VIH(3)	Output Nch Tr OFF Port of PU type (Port C to J)	0.7VDD		VDD	V	
VIH(4)	Output Nch Tr OFF INT, SCK, SI of OD type	0.8VDD		+13.5	V	
VIH(5)	Output Nch Tr OFF INT, SCK, SI of PU type	0.8VDD		VDD	V	
VIH(6)	External clock mode RES	0.8VDD		VDD	V	
VIH(7)	External clock mode OSC1	0.8VDD		VDD	V	
VIH(8)	Fig. 7 High Vt input circuit of Port B3	VDD-0.5		+13.5	V	
VIH(9)	Fig. 7 Low Vt input circuit of Port B3	0.5VDD		+13.5	V	

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**LC6554H**

			min	typ	max	unit	
"L"-Level Input Voltage	V <sub>IL</sub> (1)	Port A, B <sub>0</sub> to 2	V <sub>SS</sub>		+0.5	V	
	V <sub>IL</sub> (2)	Port C to J	V <sub>SS</sub>		0.3V <sub>DD</sub>	V	
	V <sub>IL</sub> (3)	$\overline{INT}$ , $\overline{SCK}$ , SI	V <sub>SS</sub>		0.25V <sub>DD</sub>	V	
	V <sub>IL</sub> (4)	TEST	V <sub>SS</sub>		0.3V <sub>DD</sub>	V	
	V <sub>IL</sub> (5)	$\overline{RES}$	V <sub>SS</sub>		0.25V <sub>DD</sub>	V	
	V <sub>IL</sub> (6)	External clock mode OSC1	V <sub>SS</sub>		0.25V <sub>DD</sub>	V	
	V <sub>IL</sub> (7)	Fig. 7 Low V <sub>t</sub> input circuit of Port B <sub>3</sub>	V <sub>SS</sub>		+0.9	V	
Operating Frequency (Cycle Time)	f <sub>op</sub> (T <sub>CYC</sub> )		384 (10.4)		4330 (0.92)	kHz ( $\mu$ s)	
External Clock Conditions (When the external clock option is selected)							
Frequency	f <sub>ext</sub>	OSC1			See Table 2.		
Pulse Width	textH, textL	OSC1	90			ns	
Rise/Fall Time	textR, textF	OSC1			30	ns	
Oscillation Guaranteed Constants							
Ceramic Resonator Oscillation		Fig. 2			See Table 1.		
<b>3. Electrical Characteristics/T<sub>a</sub>=-30 to +70°C, V<sub>SS</sub>=0V, V<sub>DD</sub>=4.5 to 5.5V</b>							
"H"-Level Input Current	I <sub>IH</sub> (1)	Output Nch Tr OFF (Including OFF leakage current of Nch Tr)	Port of OD type (Port C to J)		+5.0	$\mu$ A	
		V <sub>IN</sub> =+13.5V	Port A, B				
	I <sub>IH</sub> (2)	External clock mode, V <sub>IN</sub> =V <sub>DD</sub>	OSC1		+1.0	$\mu$ A	
"L"-Level Input Current	I <sub>IL</sub> (1)	Output Nch Tr OFF V <sub>IN</sub> =V <sub>SS</sub>	Port of OD type (Port C to J)	-1.0		$\mu$ A	
			Port A, B				
		Output Nch Tr OFF V <sub>IN</sub> =V <sub>SS</sub>	Port of PU type (Port C to J)	-1.3	-0.35		mA
		V <sub>IN</sub> =V <sub>SS</sub>	$\overline{RES}$	-45	-10		$\mu$ A
	I <sub>IL</sub> (4)	External clock mode, V <sub>IN</sub> =V <sub>SS</sub>	OSC1	-1.0		$\mu$ A	
"H"-Level Output Voltage	V <sub>OH</sub> (1)	I <sub>OH</sub> =-50 $\mu$ A	Port of PU type (Port C to J)	V <sub>DD</sub> -1.2		V	
		I <sub>OH</sub> =-3mA	Port K, L	V <sub>DD</sub> -1.8		V	
		I <sub>OH</sub> =-10mA	Port M to P	V <sub>DD</sub> -1.8		V	
"L"-Level Output Voltage	V <sub>OL</sub> (1)	I <sub>OL</sub> =10mA	Port C to J		1.5	V	
		I <sub>OL</sub> =2mA, When I <sub>OL</sub> of each port is 2mA or less	Port C to J		0.5	V	
		Output Pch Tr OFF V <sub>p</sub> =-35V Output open	Port of PD type (Port K to P)		-33	V	
Output OFF-Leakage Current	I <sub>OFF</sub> (1)	Output Pch Tr OFF V <sub>OUT</sub> =V <sub>DD</sub>	Port of OD type (Port K to P)		+30	$\mu$ A	
		Output Pch Tr OFF V <sub>OUT</sub> =V <sub>DD</sub> -40V	Port of OD type (Port K to P)	-30		$\mu$ A	
Hysteresis Voltage	V <sub>HYS</sub>	$\overline{RES}$ , $\overline{INT}$ , $\overline{SCK}$ , SI, OSC1 of Schmitt type (Note 5)		0.1V <sub>DD</sub>		V	

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**LC6554H**

				min	typ	max	unit
<b>Current Dissipation</b>							
Ceramic Resonator Oscillator Mode	$I_{DDOP(1)}$	Fig. 2 4MHz	VDD Operating mode, Output Nch Tr, Pch Tr OFF, Port = VDD		5	10	mA
External Clock Mode Standby Mode	$I_{DDOP(2)}$ $I_{DDST}$	384 kHz to 4330 kHz Output Nch Tr OFF Output Pch Tr OFF Port VDD, VDD=5.5 V		VDD VDD	5 0.05	10 10	mA $\mu$ A
<b>Oscillation Characteristics</b>							
<b>Ceramic Resonator Oscillation</b>							
Oscillation Frequency	$f_{CFOSC}$ (Note 4)	Fig. 2 $f_0=4$ MHz	OSC1, OSC2	3920	4000	4080	kHz
Oscillation Stabilizing Period	$t_{CFS}$	Fig. 3 $f_0=4$ MHz				10	ms
<b>Pull-up Resistance</b>							
I/O Port Pull-up Resistance	$R_{pp}$	VDD=5V	Port of PU type (Port C to J)		14		k $\Omega$
<b>Pull-down Resistance</b>							
Output Port Pull-down Resistance	$R_{pd}$	VDD=5V	Port of PD type (Port K to P)	50		200	k $\Omega$
<b>External Reset Characteristics</b>							
Reset Time	$T_{RST}$					See Fig. 4.	

DISCONTINUED PRODUCT

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**LC6554H**

				min	typ	max	unit
Pin Capacitance	CP	f=1MHz Other than pins to be tested, VIN=VSS			10		pF
<b>Serial Clock</b>							
Input Clock Cycle Time	tCKCY(1)	Fig. 5	$\overline{\text{SCK}}$	3.0			μs
Output Clock Cycle Time	tCKCY(2)	Fig. 5	$\overline{\text{SCK}}$		64 × TCYC		μs
(TCYC=4 × System clock period)							
Input Clock "L"-Level Pulse Width	tCKL(1)	Fig. 5	$\overline{\text{SCK}}$	1.0			μs
Output Clock "L"-Level Pulse Width	tCKL(2)	Fig. 5	$\overline{\text{SCK}}$		32 × TCYC		μs
Input Clock "H"-Level Pulse Width	tCKH(1)	Fig. 5	$\overline{\text{SCK}}$	1.0			μs
Output Clock "H"-Level Pulse Width	tCKH(2)	Fig. 5	$\overline{\text{SCK}}$		32 × TCYC		μs
<b>Serial Input</b>							
Data Setup Time	tJCK	Specified for ↑ of $\overline{\text{SCK}}$ , Fig. 5	SI	0.5			μs
Data Hold Time	tCKI		SI	0.5			μs
<b>Serial Output</b>							
Output Delay Time	tCKO	Specified for ↓ of $\overline{\text{SCK}}$ , Nch OD only: External 1kohm, external 50pF Fig. 5	SO			0.5	μs
<b>Pulse Output</b>							
Period	TPCY	Fig. 6	PE0		64 × TCYC		μs
"H"-Level Pulse Width	TPH	TCYC=4 × System clock period, Nch OD only:	PE0		32 × TCYC ±10%		μs
"L"-Level Pulse Width	TPL	External 1kohm, external 50pF	PE0		32 × TCYC ±10%		μs

- Note 1: When oscillated internally under the oscillating conditions in Fig. 2, up to the oscillation amplitude generated is allowable.
- Note 2: Average over the period of 100ms
- Note 3: Operating supply voltage VDD must be held until the standby mode is entered after the execution of the HALT instruction.  
The PB3 pin must be free from chattering during the HALT instruction execution cycle.
- Note 4: fCOSC represents an oscillatable frequency. There is a tolerance of approximately 1% between the center frequency at the ceramic mode and the nominal value presented by the ceramic resonator supplier. For details, refer to the specification for the ceramic resonator.
- Note 5: The OSC1 becomes the Schmitt type when the OSC option is the external clock OSC.
- Note 6: When mounting the QIP version on the board, do not dip it in solder.

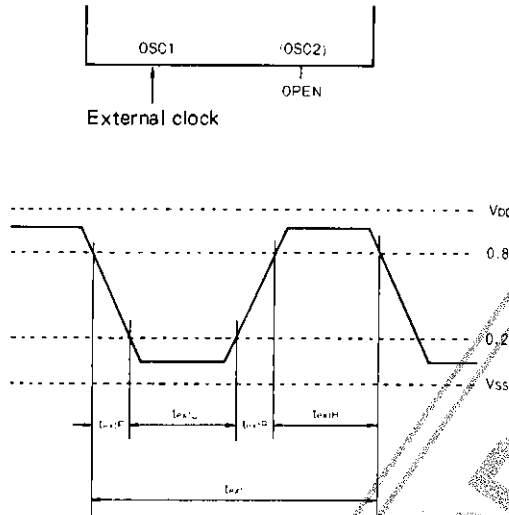


Fig. 1 External Clock Input Waveform

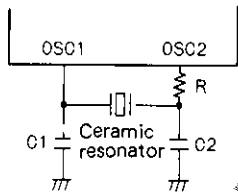


Fig. 2 Ceramic Resonator Oscillation Circuit

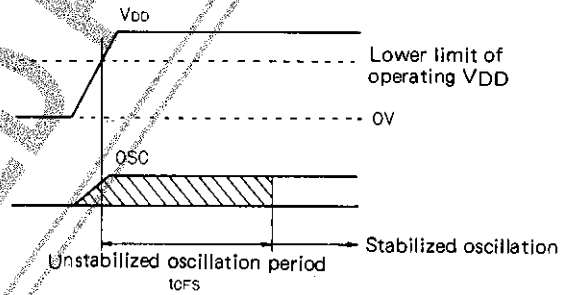


Fig. 3 Oscillation Stabilizing Period

4MHz CSA4.00MG (Murata)	C 1	33pF ± 10%
	C 2	33pF ± 10%
	R	0 Ω
4MHz KBR4.0MS (Kyocera)	C 1	33pF ± 10%
	C 2	33pF ± 10%
	R	0 Ω

Table 1 Constants Guaranteed for Ceramic Resonator Oscillation

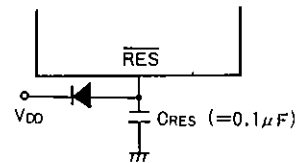


Fig. 4 Reset Circuit

Note 7: When the rise time of the power supply is 0, the reset time becomes 10 ms to 100ms at  $C_{RES}=0.1\mu F$ . If the rise time of the power supply is long, the value of  $C_{RES}$  must be increased so that the reset time becomes 10ms or greater.

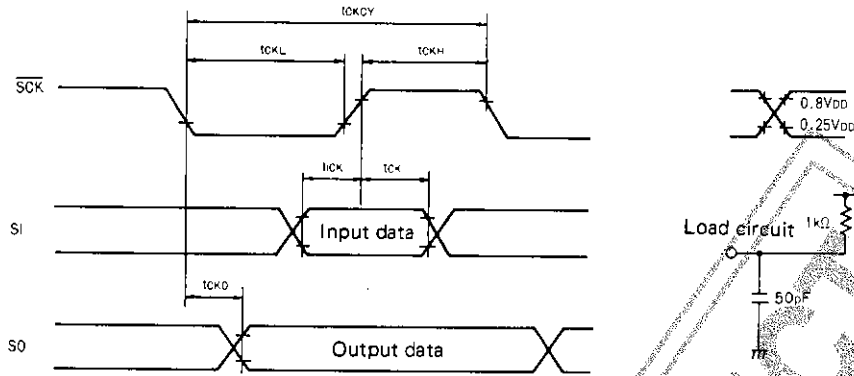
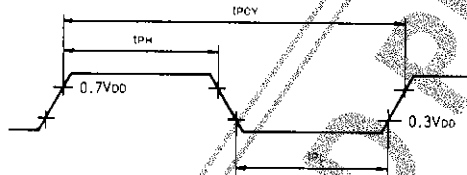


Fig. 5 Serial Input/Output Timing



The load conditions are the same as in Fig. 5.

Fig. 6 Pulse Output Timing at Port PE0

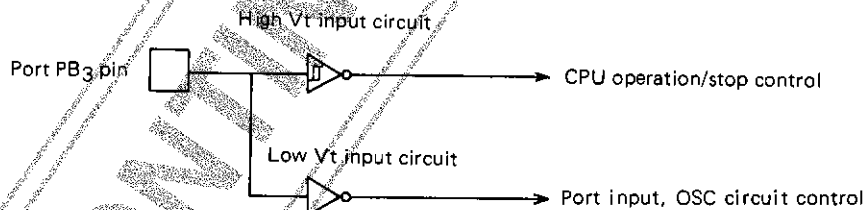


Fig. 7 Port PB3 High Vt/Low Vt Input Circuit

Table 2 LC6554H

Table of Oscillation, Predivider Option (All selectable combinations are shown. Do not use any other combinations than shown below.)  $V_{DD}=4.5$  to  $5.5V$

Circuit Configuration	Frequency	Predivider Option (Cycle Time)	Remarks
Ceramic Resonator OSC Option	4 MHz	1/1 (1 $\mu$ s)	
External Clock Option	384 to 4330 kHz	1/1 (10.4 to 0.92 $\mu$ s)	
External Clock Drive by Ceramic Resonator OSC Option	The external clock drive is impossible. When using the external clock drive, specify the external clock option.		

LC6554D/H INSTRUCTION SET

<b>Symbol</b>	<b>Description</b>			
AC	: Accumulator	M(DP)	: Memory addressed by DP	( ), [ ] : Contents
ACt	: Accumulator bit t	P(DP <sub>L</sub> )	: Input/output port addressed by DP <sub>L</sub>	- : Transfer and direction
CF	: Carry flag	PC	: Program counter	+ : Addition
CTL	: Control register	STACK	: Stack register	- : Subtraction
DP	: Data pointer	TM	: Timer	∧ : AND
E	: E register	TMF	: Timer (internal) interrupt request flag	∨ : OR
EXTF	: External interrupt request flag	At, Ha, La	: Working register	⊙ : Exclusive OR
Fn	: Flag bit n	ZF	: Zero flag	
M	: Memory			

Instruction group	Mnemonic	Instruction code		Bytes	Cycles	Function	Description	Status flag affected	Remarks													
		D <sub>7</sub> -D <sub>6</sub> D <sub>5</sub> D <sub>4</sub>	D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>																			
Accumulator manipulation instructions	CLA	Clear AC	1 1 0 0	0 0 0 0	1	1	AC ← 0	The AC contents are cleared.	ZF	* 1												
	CLC	Clear CF	1 1 1 0	0 0 0 1	1	1	CF ← 0	The CF contents are cleared.	CF													
	STC	Set CF	1 1 1 1	0 0 0 1	1	1	CF ← 1	The CF is set.	CF													
	CMA	Complement AC	1 1 1 0	1 0 1 1	1	1	AC ← $\overline{AC}$	The AC contents are complemented.	ZF													
	INC	Increment AC	0 0 0 0	1 1 1 0	1	1	AC ← (AC) + 1	The AC contents are incremented +1.	ZF CF													
	DEC	Decrement AC	0 0 0 0	1 1 1 1	1	1	AC ← (AC) - 1	The AC contents are decremented -1.	ZF CF													
	RAL	Rotate AC left through CF	0 0 0 0	0 0 0 1	1	1	AC <sub>0</sub> ← (CF), AC <sub>n-1</sub> ← (AC) <sub>n</sub> , CF ← (AC) <sub>0</sub>	The AC contents are shifted left through the CF.	ZF CF													
	TAE	Transfer AC to E	0 0 0 0	0 0 1 1	1	1	E ← (AC)	The AC contents are transferred to the E.														
XAE	Exchange AC with E	0 0 0 0	1 1 0 1	1	1	(AC) ↔ (E)	The AC contents and the E contents are exchanged.															
Memory manipulation instructions	INM	Increment M	0 0 1 0	1 1 1 0	1	1	M(DP) ← M(DP) + 1	The M(DP) contents are incremented +1.	ZF CF													
	DEM	Decrement M	0 0 1 0	1 1 1 1	1	1	M(DP) ← M(DP) - 1	The M(DP) contents are decremented -1.	ZF CF													
	SMB bit	Set M data bit	0 0 0 0	1 0 B <sub>1</sub> B <sub>0</sub>	1	1	M(DP, B <sub>1</sub> B <sub>0</sub> ) ← 1	A single bit of the M(DP) specified with B <sub>1</sub> B <sub>0</sub> is set.														
RMB bit	Reset M data bit	0 0 1 0	1 0 B <sub>1</sub> B <sub>0</sub>	1	1	M(DP, B <sub>1</sub> B <sub>0</sub> ) ← 0	A single bit of the M(DP) specified with B <sub>1</sub> B <sub>0</sub> is reset.	ZF														
Arithmetic operation/comparison instructions	AD	Add M to AC	0 1 1 0	0 0 0 0	1	1	AC ← (AC) + (M(DP))	Binary addition of the AC contents and the M(DP) contents is performed and the result is stored in the AC.	ZF CF													
	ADC	Add M to AC with CF	0 0 1 0	0 0 0 0	1	1	AC ← (AC) + (M(DP)) + (CF)	Binary addition of the AC, CF contents and the M(DP) contents is performed and the result is stored in the AC.	ZF CF													
	DAA	Decimal adjust AC in addition	1 1 1 0	0 1 1 0	1	1	AC ← (AC) + 6	6 is added to the AC contents.	ZF													
	DAS	Decimal adjust AC in subtraction	1 1 1 0	1 0 1 0	1	1	AC ← (AC) + 10	10 is added to the AC contents.	ZF													
	EXL	Exclusive or M to AC	1 1 1 0	0 1 0 1	1	1	AC ← (AC) ∨ (M(DP))	The AC contents and the M(DP) contents are exclusive-ORed and the result is stored in the AC.	ZF													
	AND	And M to AC	1 1 1 0	0 1 1 1	1	1	AC ← (AC) ∧ (M(DP))	The AC contents and the M(DP) contents are ANDed and the result is stored in the AC.	ZF													
	OR	Or M to AC	1 1 1 0	0 1 0 1	1	1	AC ← (AC) ∨ (M(DP))	The AC contents and the M(DP) contents are ORed and the result is stored in the AC.	ZF													
	CM	Compare AC with M	1 1 1 1	1 0 1 1	1	1	(M(DP)) + (AC) + 1	The AC contents and the M(DP) contents are compared and the CF and ZF are set/reset. <table border="1" style="margin-left: 20px;"> <tr><td>Comparison result</td><td>CF</td><td>ZF</td></tr> <tr><td>(M(DP)) &gt; (AC)</td><td>0</td><td>0</td></tr> <tr><td>(M(DP)) = (AC)</td><td>1</td><td>1</td></tr> <tr><td>(M(DP)) &lt; (AC)</td><td>1</td><td>0</td></tr> </table>	Comparison result	CF	ZF	(M(DP)) > (AC)	0	0	(M(DP)) = (AC)	1	1	(M(DP)) < (AC)	1	0	ZF CF	
	Comparison result	CF	ZF																			
	(M(DP)) > (AC)	0	0																			
(M(DP)) = (AC)	1	1																				
(M(DP)) < (AC)	1	0																				
CI data	Compare AC with immediate data	0 0 1 0 0 1 0 0	1 1 0 0 1 3 2 1 1 0	2	2	( $\overline{I_3 I_2 I_1 I_0}$ ) + (AC) + 1	The AC contents and the immediate data $I_3 I_2 I_1 I_0$ are compared and the ZF and CF are set/reset. <table border="1" style="margin-left: 20px;"> <tr><td>Comparison result</td><td>CF</td><td>ZF</td></tr> <tr><td><math>\overline{I_3 I_2 I_1 I_0} &gt; (AC)</math></td><td>0</td><td>0</td></tr> <tr><td><math>\overline{I_3 I_2 I_1 I_0} = (AC)</math></td><td>1</td><td>1</td></tr> <tr><td><math>\overline{I_3 I_2 I_1 I_0} &lt; (AC)</math></td><td>1</td><td>0</td></tr> </table>	Comparison result	CF	ZF	$\overline{I_3 I_2 I_1 I_0} > (AC)$	0	0	$\overline{I_3 I_2 I_1 I_0} = (AC)$	1	1	$\overline{I_3 I_2 I_1 I_0} < (AC)$	1	0	ZF CF		
Comparison result	CF	ZF																				
$\overline{I_3 I_2 I_1 I_0} > (AC)$	0	0																				
$\overline{I_3 I_2 I_1 I_0} = (AC)$	1	1																				
$\overline{I_3 I_2 I_1 I_0} < (AC)$	1	0																				
CLI data	Compare DP <sub>L</sub> with immediate data	0 0 1 0 0 1 0 1	1 1 0 0 1 3 2 1 1 0	2	2	(DP <sub>L</sub> ) ∨ ( $\overline{I_3 I_2 I_1 I_0}$ )	The DP <sub>L</sub> contents and the immediate data $I_3 I_2 I_1 I_0$ are compared.	ZF														
Load/store instructions	LI data	Load AC with immediate data	1 1 0 0	$I_3 I_2 I_1 I_0$	1	1	AC ← $\overline{I_3 I_2 I_1 I_0}$	The immediate data $I_3 I_2 I_1 I_0$ is loaded in the AC.	ZF	* 1												
	S	Store AC to M	0 0 0 0	0 0 1 0	1	1	M(DP) ← (AC)	The AC contents are stored in the M(DP).														
	L	Load AC from M	0 0 1 0	0 0 0 1	1	1	AC ← (M(DP))	The M(DP) contents are loaded in the AC.	ZF													
	XM data	Exchange AC with M, then modify DP <sub>H</sub> with immediate data	1 0 1 0	0 M <sub>2</sub> M <sub>1</sub> M <sub>0</sub>	1	2	AC ↔ (M(DP)) DP <sub>H</sub> ← (DP <sub>H</sub> ) ∨ (M <sub>2</sub> M <sub>1</sub> M <sub>0</sub> )	The AC contents and the M(DP) contents are exchanged and then the DP <sub>H</sub> contents are modified with the contents of (DP <sub>H</sub> ) ∨ OM <sub>2</sub> M <sub>1</sub> M <sub>0</sub> .	ZF	The ZF is set/reset according to the result of (DP <sub>H</sub> ) ∨ OM <sub>2</sub> M <sub>1</sub> M <sub>0</sub> .												
	X	Exchange AC with M	1 0 1 0	0 0 0 0	1	2	(AC) ↔ (M(DP))	The AC contents and the M(DP) contents are exchanged.	ZF	The ZF is set/reset according to the DP <sub>H</sub> contents at the time of instruction execution.												
	XI	Exchange AC with M, then increment DP <sub>L</sub>	1 1 1 1	1 1 1 0	1	2	(AC) ↔ (M(DP)) DP <sub>L</sub> ← (DP <sub>L</sub> ) + 1	The AC contents and the M(DP) contents are exchanged and then the DP <sub>L</sub> contents are incremented +1.	ZF	The ZF is set/reset according to the result of (DP <sub>L</sub> + 1).												
XD	Exchange AC with M, then decrement DP <sub>L</sub>	1 1 1 1	1 1 1 1	1	2	(AC) ↔ (M(DP)) DP <sub>L</sub> ← (DP <sub>L</sub> ) - 1	The AC contents and the M(DP) contents are exchanged and then the DP <sub>L</sub> contents are decremented -1.	ZF	The ZF is set/reset according to the result of (DP <sub>L</sub> - 1).													
RTBL	Read table data from program ROM	0 1 1 0	0 0 1 1	1	2	AC, E ← ROM (PCn, E, AC)	The contents of ROM addressed by the PC whose low-order 8 bits are replaced with the E and AC contents are loaded in the AC and E.															



LC6554D, 6554H

Instruction group	Mnemonic	Instruction code		Bytes	Cycles	Function	Description	Status flag affected	Remarks	
		D <sub>7</sub> D <sub>6</sub> D <sub>5</sub> D <sub>4</sub>	D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>							
Data pointer manipulation instructions	LZ data	Load DP <sub>H</sub> with Zero and DP <sub>L</sub> with immediate data respectively	1 0 0 0	I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub>	1	1	DP <sub>H</sub> ← 0 DP <sub>L</sub> ← I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub>	The DP <sub>H</sub> and DP <sub>L</sub> are loaded with 0 and the immediate data I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub> respectively.		
	LHI data	Load DP <sub>H</sub> with immediate data	0 1 0 0	I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub>	1	1	DP <sub>H</sub> ← I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub>	The DP <sub>H</sub> is loaded with the immediate data I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub> .		
	IND	Increment DP <sub>L</sub>	1 1 1 0	1 1 1 0	1	1	DP <sub>L</sub> ← (DP <sub>L</sub> ) + 1	The DP <sub>L</sub> contents are incremented +1.	ZF	
	DED	Decrement DP <sub>L</sub>	1 1 1 0	1 1 1 1	1	1	DP <sub>L</sub> ← (DP <sub>L</sub> ) - 1	The DP <sub>L</sub> contents are decremented -1.	ZF	
	TAL	Transfer AC to DP <sub>L</sub>	1 1 1 1	0 1 1 1	1	1	DP <sub>L</sub> ← (AC)	The AC contents are transferred to the DP <sub>L</sub> .		
	TAL	Transfer DP <sub>L</sub> to AC	1 1 1 0	1 0 0 1	1	1	AC ← (DP <sub>L</sub> )	The DP <sub>L</sub> contents are transferred to the AC.	ZF	
	XAH	Exchange AC with DP <sub>L</sub>	0 0 1 0	0 0 1 1	1	1	(AC) ↔ (DP <sub>L</sub> )	The AC contents and the DP <sub>L</sub> contents are exchanged.		
Working register manipulation instructions	XAI	Exchange AC with working register A <sub>i</sub>	1 1 1 0	t <sub>1</sub> t <sub>0</sub> 0 0 0 0	1	1	(AC) ↔ (A <sub>0</sub> )	The AC contents and the contents of working register A <sub>i</sub> are exchanged. A <sub>i</sub> is assigned one of A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> , A <sub>3</sub> according to t <sub>1</sub> t <sub>0</sub> .		
	XAI		1 1 1 0	0 1 0 0	1	1	(AC) ↔ (A <sub>1</sub> )			
	XAI		1 1 1 0	1 0 0 0	1	1	(AC) ↔ (A <sub>2</sub> )			
	XAI		1 1 1 0	1 1 0 0	1	1	(AC) ↔ (A <sub>3</sub> )			
	XHa	Exchange DP <sub>H</sub> with working register Ha	1 1 1 1	a 0 0 0 0	1	1	(DP <sub>H</sub> ) ↔ (H <sub>0</sub> )	The DP <sub>H</sub> contents and the contents of working register H <sub>a</sub> are exchanged. H <sub>a</sub> is assigned either of H <sub>0</sub> or H <sub>1</sub> according to a.		
	XH1		1 1 1 1	1 0 0 0	1	1	(DP <sub>H</sub> ) ↔ (H <sub>1</sub> )			
XLa	Exchange DP <sub>L</sub> with working register La	1 1 1 1	a 0 0 0 0	1	1	(DP <sub>L</sub> ) ↔ (L <sub>0</sub> )	The DP <sub>L</sub> contents and the contents of working register L <sub>a</sub> are exchanged. L <sub>a</sub> is assigned either of L <sub>0</sub> or L <sub>1</sub> according to a.			
XL1		1 1 1 1	0 1 0 0	1	1	(DP <sub>L</sub> ) ↔ (L <sub>1</sub> )				
Flag manipulation instructions	SFB flag	Set flag bit	0 1 0 1	B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>	1	1	F <sub>n</sub> ← 1	The flag specified with B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub> is set.		
	RFB flag	Reset flag bit	0 0 0 1	B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>	1	1	F <sub>n</sub> ← 0	The flag specified with B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub> is reset.	ZF	The flags are divided into 4 groups of F <sub>0</sub> to F <sub>3</sub> , F <sub>4</sub> to F <sub>7</sub> , F <sub>8</sub> to F <sub>11</sub> , F <sub>12</sub> to F <sub>15</sub> . The ZF is set/reset according to the 4 bits including a single bit specified with the immediate data B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub> .
Jump/subroutine instructions	JMP addr	Jump in the current bank	0 1 1 0	1 P <sub>10</sub> P <sub>9</sub> P <sub>8</sub> P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	2	2	PC ← PC <sub>11</sub> (∨) (I <sub>3</sub> I <sub>2</sub> I <sub>1</sub> I <sub>0</sub> ) P <sub>0</sub> P <sub>9</sub> P <sub>8</sub> P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	A jump to the address specified with the PC <sub>11</sub> (or PC <sub>11</sub> ) and immediate data P <sub>10</sub> P <sub>9</sub> P <sub>8</sub> P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> occurs.		If the BANK and JMP instructions are executed consecutively, PC <sub>11</sub> → PC <sub>11</sub> .
	JPEA	Jump in the current page modified by E and AC	1 1 1 1	1 0 0 0	1	1	PC ← (E, AC)	A jump to the address specified with the contents of the PC whose low-order 8 bits are replaced by the E and AC contents occurs.		
	CZP addr	Call subroutine in the zero page	1 0 0 1	P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	1	1	STACK ← (PC) + 1 PC ← P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> PC <sub>5-2</sub> ← B <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	A subroutine in page 0 of bank 0 is called.		
	CAL addr	Call subroutine in the zero bank	1 0 0 0	1 P <sub>10</sub> P <sub>9</sub> P <sub>8</sub> P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	2	2	STACK ← (PC) + 2 PC ← P <sub>10</sub> P <sub>9</sub> P <sub>8</sub> P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	A subroutine in bank 0 is called.		
	RT	Return from subroutine	0 1 1 0	0 0 0 1	1	1	PC ← (STACK)	A return from a subroutine occurs.		
	RTI	Return from interrupt routine	0 0 1 0	0 0 0 0	1	1	PC ← (STACK) CF ZF ← CSF, ZSF	A return from an interrupt service routine occurs.	ZF CF	
	BANK	Change bank	1 1 1 1	1 0 0 1	1	1	PC ← (PC <sub>11</sub> )	The bank is changed.		Effective only when used immediately before the JMP instruction.
Branch instructions	BAI addr	Branch on AC bit	0 1 1 1	0 0 t <sub>1</sub> t <sub>0</sub> P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	2	2	PC <sub>7-0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	If a single bit of the AC specified with the immediate data t <sub>1</sub> t <sub>0</sub> is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.		Mnemonic is BA0 to BA3 according to the value of t.
	BNAI addr	Branch on no AC bit	0 0 1 1	0 0 t <sub>1</sub> t <sub>0</sub> P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	2	2	PC <sub>7-0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	If a single bit of the AC specified with the immediate data t <sub>1</sub> t <sub>0</sub> is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.		Mnemonic is BNA0 to BNA3 according to the value of t.
	BMI addr	Branch on M bit	0 1 1 1	0 1 t <sub>1</sub> t <sub>0</sub> P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	2	2	PC <sub>7-0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	If a single bit of the M(DP) specified with the immediate data t <sub>1</sub> t <sub>0</sub> is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.		Mnemonic is BM0 to BM3 according to the value of t.
	BNMI addr	Branch on no M bit	0 0 1 1	0 1 t <sub>1</sub> t <sub>0</sub> P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	2	2	PC <sub>7-0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	If a single bit of the M(DP) specified with the immediate data t <sub>1</sub> t <sub>0</sub> is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.		Mnemonic is BNM0 to BNM3 according to the value of t.
	BPi addr	Branch on Port bit	0 1 1 1	1 0 t <sub>1</sub> t <sub>0</sub> P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	2	2	PC <sub>7-0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	If a single bit of port P(DP <sub>L</sub> ) specified with the immediate data t <sub>1</sub> t <sub>0</sub> is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.		Mnemonic is BP0 to BP3 according to the value of t.
	BNPi addr	Branch on no Port bit	0 0 1 1	1 0 t <sub>1</sub> t <sub>0</sub> P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	2	2	PC <sub>7-0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	If a single bit of port P(DP <sub>L</sub> ) specified with the immediate data t <sub>1</sub> t <sub>0</sub> is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.		Mnemonic is BNP0 to BNP3 according to the value of t.

LC6554D, 6554H

Instruction group	Mnemonic	Instruction code		Bytes	Cycles	Function	Description	Status flag affected	Remarks	
		D <sub>7</sub> D <sub>6</sub> D <sub>5</sub> D <sub>4</sub>	D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>							
Branch instructions	BTM addr	Branch on timer	0 1 1 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	1 1 0 0 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC <sub>7-0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if TMF = 1 then TMF ← 0	If the TMF is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs. The TMF is reset.	TMF	
	BNTM addr	Branch on no timer	0 0 1 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	1 1 0 0 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC <sub>7-0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if TMF = 0 then TMF ← 0	If the TMF is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs. The TMF is reset.	TMF	
	BI addr	Branch on interrupt	0 1 1 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	1 1 0 1 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC <sub>7-0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if EXTF = 1 then EXTF ← 0	If the EXTF is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs. The EXTF is reset.	EXTF	
	BNI addr	Branch on no interrupt	0 0 1 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	1 1 0 1 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC <sub>7-0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if EXTF = 0 then EXTF ← 0	If the EXTF is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs. The EXTF is reset.	EXTF	
	BC addr	Branch on CF	0 1 1 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	1 1 1 1 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC <sub>7-0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if CF = 1	If the CF is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.		
	BNC addr	Branch on no CF	0 0 1 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	1 1 1 1 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC <sub>7-0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if CF = 0	If the CF is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.		
	BZ addr	Branch on ZF	0 1 1 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	1 1 1 0 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC <sub>7-0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if ZF = 1	If the ZF is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.		
	BNZ addr	Branch on no ZF	0 0 1 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	1 1 1 0 P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC <sub>7-0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if ZF = 0	If the ZF is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.		
	BFn addr	Branch on flag bit	1 1 0 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	n <sub>3</sub> n <sub>2</sub> n <sub>1</sub> n <sub>0</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC <sub>7-0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if F <sub>n</sub> = 1	If the flag bit of the 16 flags specified with the immediate data n <sub>3</sub> n <sub>2</sub> n <sub>1</sub> n <sub>0</sub> is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.		Mnemonic is BFD to BFI5 according to the value of n.
	BNFn addr	Branch on no flag bit	1 0 0 1 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	n <sub>3</sub> n <sub>2</sub> n <sub>1</sub> n <sub>0</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC <sub>7-0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> if F <sub>n</sub> = 0	If the flag bit of the 16 flags specified with the immediate data n <sub>3</sub> n <sub>2</sub> n <sub>1</sub> n <sub>0</sub> is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.		Mnemonic is BNF0 to BNF15 according to the value of n.
Input/Output instructions	IP	Input port to AC	0 0 0 0	1 1 0 0	1	1	AC ← (P <sub>1</sub> DP <sub>L</sub> )	Port P(DP <sub>L</sub> ) contents are loaded in the AC.	ZF	
	OP	Output AC to port	0 1 1 0	0 0 0 1	1	1	P(DP <sub>L</sub> ) ← (AC)	The AC contents are outputted to port P(DP <sub>L</sub> ).		
	SPB bit	Set port bit	0 0 0 0	0 1 B <sub>1</sub> B <sub>0</sub>	2	2	P(DP <sub>L</sub> ) B <sub>1</sub> B <sub>0</sub> ← 1	A single bit in port P(DP <sub>L</sub> ) specified with the immediate data B <sub>1</sub> B <sub>0</sub> is set.		When this instruction is executed, the E contents are destroyed.
	RPB bit	Reset port bit	0 0 0 0	0 1 B <sub>1</sub> B <sub>0</sub>	2	2	P(DP <sub>L</sub> ) B <sub>1</sub> B <sub>0</sub> ← 0	A single bit in port P(DP <sub>L</sub> ) specified with the immediate data B <sub>1</sub> B <sub>0</sub> is reset.	ZF	When this instruction is executed, the E contents are destroyed.
Other instructions	SCTL bit	Set control register bit(S)	0 0 1 0 1 0 0 0	1 1 0 0 B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>	2	2	CTL ← (CTL) V B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>	The bits of the control register specified with the immediate data B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub> are set.		
	RCTL bit	Reset control register bit(S)	0 0 1 0 1 0 0 1	1 1 0 0 B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>	2	2	CTL ← (CTL) A B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>	The bits of the control register specified with the immediate data B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub> are reset.	ZF	
	WTTM	Write timer	1 1 1 1	1 0 0 1	1	1	TM ← (E) (AC) TMF ← 0	The E and AC contents are loaded in the timer. The TMF is reset.	TMF	
	HALT	Halt	1 1 1 1	0 1 1 0	1	1	Halt	All operations stop.		
	NOP	No operation	0 0 0 0	0 0 0 0	1	1	No operation	No operation is performed, but 1 machine cycle is consumed.		

\*1 If the CLA instruction is used consecutively in such a manner as CLA, CLA, ---, the first CLA instruction only is effective and the following CLA instructions are changed

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