CMOS LSI

No. 3341C

SANYO

LC5851N

Small-Scale Control, Medium-Speed Type,
On-Chip LCD Driver
4-Bit Single Chip Microcomputer

The LC5851N is a 4-bit/single-chip, high-performance microcomputer equipped with LCD drivers. They are produced by CMOS process technology. Their numerous features include low-voltage operation and low current dissipation.

A 4-bit parallel-processing ALU, program memory (ROM), data memory (RAM), input and output ports, timer, clock generator, and LCD drivers are integrated on one chip. A total of 79 instructions, including the operation and processing instructions executable in 4-bit units, and various conditional branch instructions and LCD driver data transfer instructions, form an easy-to-use and effective instruction system.

Because there is a halt function (HALT) which stops, thus reduces current to circuits other than the oscillation, divider, LCD driving circuitries, the time-keeping function having very low power dissipation can be easily performed.

These microcomputers are very useful for controlling electronic tuners, cameras, and other portable devices at low voltage, thereby cutting power dissipation.

Features
Hardware Features
· A wide range of allowable operations

Supply Option	Cycle Time	Supply Voltage Range	Remarks
EXT-V	20μs	V_{ss2}=-4.0 to -5.5V	400kHz Ceramic oscillator
EXT-V	40μs	V_{ss2}=-4.0 to -5.5V	200kHz Ceramic oscillator
EXT-V	61μs	V_{ss2}=-2.3 to -5.5V	65kHz Crystal oscillator
EXT-V	122μs, 244μs	V_{ss2}=-2.0 to -5.5V	32kHz Crystal oscillator
Li	122μs, 244μs	V_{ss2}=-2.6 to -3.6V (Note)	32kHz Crystal oscillator
Ag	122μs, 244μs	V_{ss1}=-1.3 to -1.65V	32kHz Crystal oscillator

(Note) If the backup flag is set, pin BAK is connected to V_{ss2}.
   (For further details, refer to the User's Manual.)

Notes for developing an LC5800 series microcomputer-used system

The low current dissipation is a distinctive feature of the LC5800 series microcomputers. However, it is not easy to determine the total current to be dissipated in an LC5800 series microcomputer-used system by actual measurement when you develop a software, because much current flows in the peripherals of the evaluation tools.

For a system which require low current dissipation, check the current dissipation using an evaluation sample before mass-producing the system.

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- Micro-current operation
  Only micro level current is needed to operate the LC5851N if the HALT function is used efficiently.
- The actual current reguired, however, depends on the program structure.
  The following values are typical for normal clock programs.
        3.0μA (typ) ..... Ag specifications (1.5V supply)
        1.5μA (typ) ..... Li specifications (3.0V supply)
- The terminals are capable of driving various types of LCD panel. (25 terminals)

LCD panel	Number of LCD segments
1/3 bias - 1/3 duty	75 segments
1/2 bias - 1/3 duty	75 segments
1/2 bias - 1/2 duty	50 segments
Static	25 segments

- The built-in segment PLA circuit is capable of joining the LCD driver outputs to any patterns on the LCD panel without software.
- A number of input and output terminals are provided.
        Input port: 2 ports/8 pins (With a chatter removal circuit)
        Input/output port: 2 ports/8 pins
        Output port: 1 port/4 pins (Also used as the pseudo-serial output port)
        Control output terminal: 2 pins
- The LCD panel drive output terminal can be switched to the output-only port (mask option).
- An initial reset terminal is provided.
- ROM: 1024 x 15 bits
- RAM: 64 x 4 bits
- Built-in oscillation circuit for crystal oscillation or ceramic resonator oscillation.
- Built-in voltage doubler/halver circuits for the LCD power source.
- Form of shipment: QFP64 (QIP64) or chip

Software Features
- As many as 79 instructions.
- Binary addition/subtractions and logical operation.
- Input and output instructions in 4-bit units.
- Conditional branch instructions.
- 8 working registers and operation instructions.
- LCD driver data transfer instructions.
- 4-level subroutine nesting (common with interrupts)
- Interrupt function ... External source: 2 (INT terminal, input ports S and M)
                        Internal source: 2 (Timer, frequency divider circuit)
- HALT/HOLD release functions ... The HALT release is caused by the same elements as in interrupt.
- Built-in 6-bit programmable timer.
- Built-in 15-bit clock frequency divider circuit.
- All instructions are executable in one machine cycle.

Application Development Tools
· Relations between power specifications for cycle time and evaluation chip

Cycle Time	Oscillation Frequency	Power Specification								Evaluation Chip & Evaluation Chip Board
		Ag Specification		Li Specification		EXTV Specification				
		Use	IDD(typ) /1.5V	Use	IDD(typ) /2.9V	Use	IDD(typ) /3.0V	Use	IDD(typ) /5.0V	
10μsec	800kHz	×	—	×	—	×	—	○		Evaluation Chip: LC5895HII Evaluation Chip Board: TB5851
20μsec	400kHz	×	—	×	—	×	—	○		
61μsec	65.536kHz	×	—	×	—	○	10~40μA	○	20~80μA	
122μsec	32.768kHz	○	4~20μA	○	2~20μA	○	8~35μA	○	15~50μA	
244μsec	32.768kHz	○	2~6μA	○	1~4μA	○		○		

Table 1. Relations between power specifications for cycle time and evaluation chip.

Note) The I_{DD} (typ) value is determined by the contents of the software.

· Software support tool
  Cross assembler and mask option selection program for MS-DOS based system
  (1) Cross assembler   :LC5851. EXE
  (2) Mask option selection program   :SU5851N. EXE

· Hardware support tool
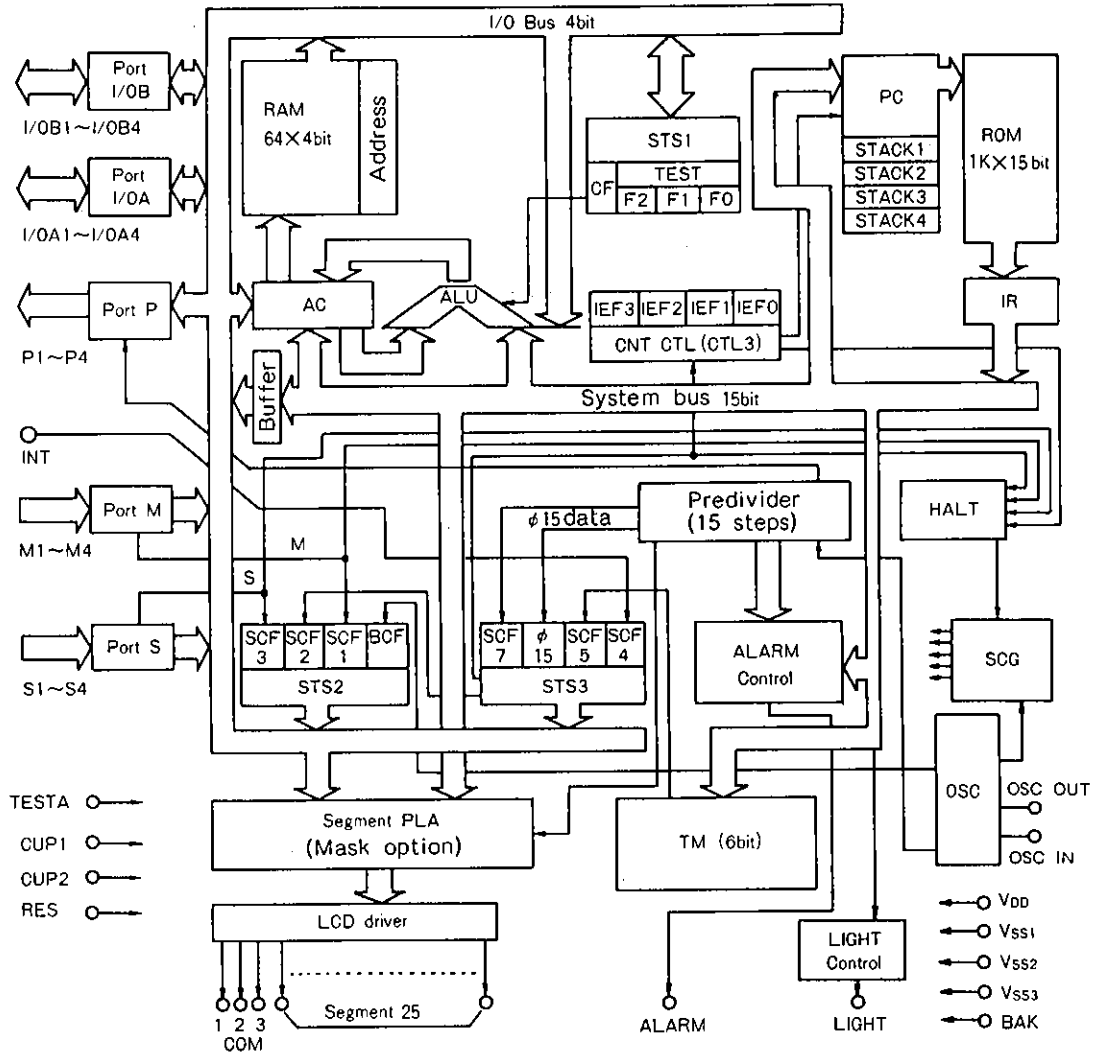 (1) Evaluation chip   :LC5895HII
  (2) Mask option controller   :DCB-1A
  (3) Evaluation chip board   :TB5851
  (4) Evaluation board   :EVA-520 (EVA-510)
  (5) Control ROM   :SCR5851

· Development support tool system
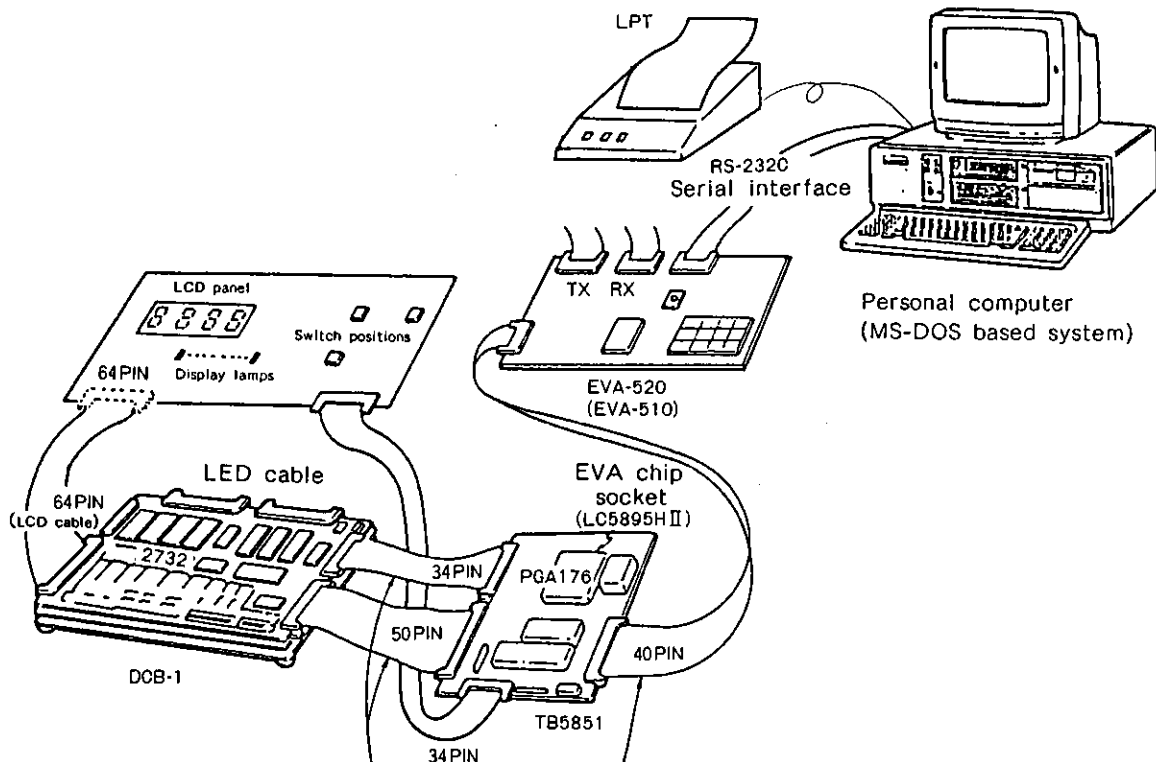
Note: These cables must not be connected
on the cross or reversely.

Equivalent Circuit Block Diagram

| AC	: Accumulator	CF	: Carry flag
ALU	: Arithmetic and logic unit	BCF	: Backup flag
INT CTL	: Interrupt control circuit	SCF1	: M port flag
PC	: Program counter	SCF2	: STS3 flag
TM	: Preset timer (8 bits)	SCF3	: S port flag
IR	: Instruction register	SCF4	: INT signal change flag
HALT	: Intermittent control circuit	SCF5	: Timer overflow flag
SCG	: System clock generator	$\phi 15$	: Content of 15th step of divider
STS1	: Status register 1	SCF7	: Overflow flag of divider
STS2	: Status register 2		
STS3	: Status register 3		

Application Examples

- Portable equipment (timer, watch, clock, hand-held calculator, and thermometer)
- Audio equipment (electronic controller, electronic tuning controller, and clock)
- Home appliances (remote control, and timer control)
- Telephone (dial/clock display)

Application Circuit Examples

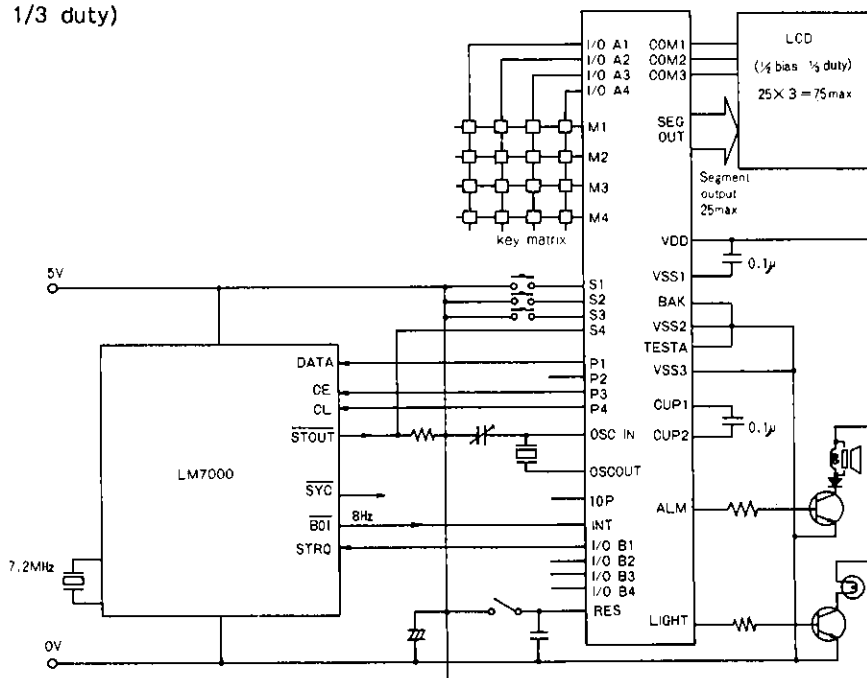**(1) Typical application circuit for the Ag specifications (1/3 bias - 1/3 duty)**
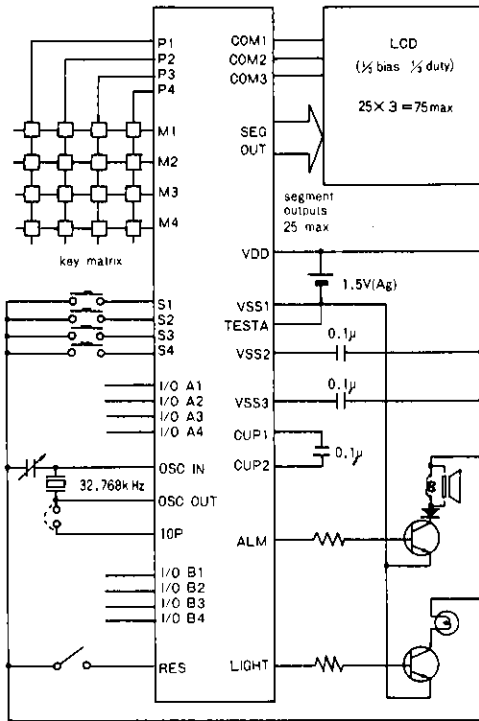
(2) Typical application circuit for the Li specifications (1/2 bias - 1/3 duty)
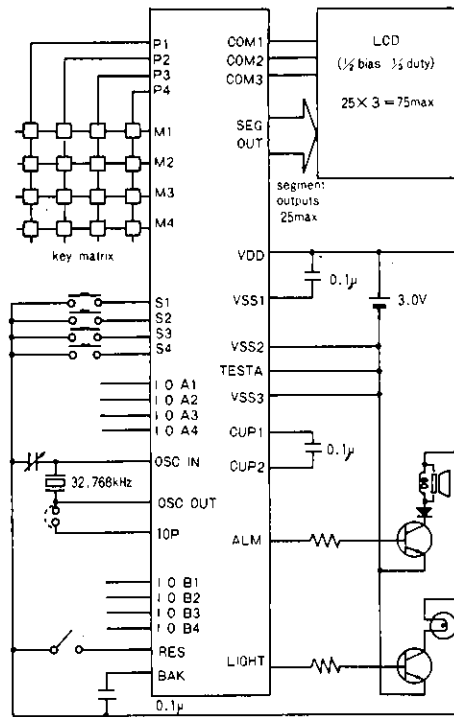
INPUT OUTPUT PORT	I O A1~4, I O B1~4
INPUT PORT	S1~4, M1~4
OUTPUT PORT	P1~4

Unit (capacitance: F)
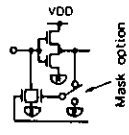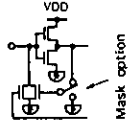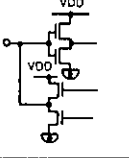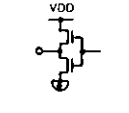
(3) Typical application circuit for the EXT-V specifications (1/2 bias - 1/3 duty)

Unit (capacitance: F)

Terminal Description

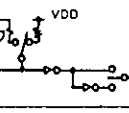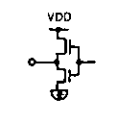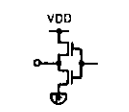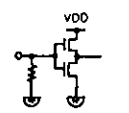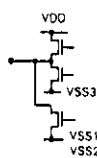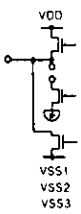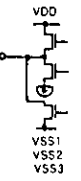| Terminal Name	Input/Output	Circuit Configuration	Function	Option	Status after Reset
OSC IN	Input		Used as the reference clock and system clock.	① Terminals for crystal oscillator (XT option) ② Terminals for ceramic resonator oscillator (CF option) The CF option is available only for the EXT-V specification.	
OSC OUT	Output				
IOP			Used as an oscillation phase compensating capacitor by connecting it to OSCOUT or OSCIN. Used for chip only.		
S1 S2 S3 S4	Input		Input-only port. Contains a Ø10(32ms), Ø8 (8ms) or Ø6 (2ms) chatter-removal circuit. (PLA mask option) *The values are for 32.768kHz crystal oscillation.	Selection of "L" level Hold Tr. Chatter-removal time is either Ø10, Ø8 or Ø6. ØN indicates the output at the Nth step of the frequency divider circuit.	Transistor for pull-down resistance is ON.
M1 M2 M3 M4	Input		Input terminals for writing data in RAM.	Selection of "L" level Hold Tr.	Transistor for pull-down resistance is ON.
I/O A1 I/O A2 I/O A3 I/O A4	Input/Output		Input/output port with mode switched by instructions to perform the following operations: ① Input port: Writes data in RAM. ② Output port: Outputs data from RAM.		Input mode
P1 P2 P3 P4	Output		Output-only port		"H" or "L" output (not fixed).
INT	Input		Control Input port for external interrupt request.	① Pull-up resistor ② Pull-down resistor ③ Fall trigger ④ Rise trigger	
BAK			(−) supply voltage terminal for the logic section of LSI circuit. In the LI specifications a capacitor is provided between BAK and VDD to prevent malfunction at the logic section.		Backup flag is set/reset depending on the power source option.
LIGHT	Output		Output-only port. Suitable for delivering signal to drive high-current driving.		"L" output
ALM	Output		Output-only port. Able to output 4kHz-2kHz or 4kHz-1kHz modulating signals according to instructions as well as nonmodulating signals. *The value is for 32.768kHz crystal oscillation.	① Modulating signal (4kHz, 2kHz, Nonmodulation) ② Modulating signal (4kHz, 1kHz, Nonmodulation)	"L" output
RES	Input		System reset terminal. Sets the program counter to address 00. "H" level signal should be input more than 200μs in the stable oscillation state.		

Terminal Name	Input/ Output	Circuit Configuration	Function	Option	Status after Reset
V_DD			(+) supply voltage terminal.		
VSS3 VSS2 VSS1			(-) supply voltage terminal. • Connection of external device varies according to the mask option: The (-) terminal is connected to VSS1 for the Ag specifications. The (-) terminal is connected to VSS2 for other specifications. • Terminals other than the (-) terminal are used as the source supply for the LCD drive.	① Ag specifications ② Li specifications ③ EXT-V specifications	
CUP1 CUP2			Connection terminals for voltage doubler (halver) capacitor.		
COM1 COM2 COM3	Output	(circuit diagram with VDD, VSS3, VSS1, VSS2)	Output terminals for common plate of LCD panel. Use of terminals varies. |	Static	½duty	⅓duty
COM1	O	O	O
COM2	—	O	O
COM3	—	—	O
Alternating frequency	32Hz*	32Hz*	43Hz* | * The values are for 32.768kHz crystal oscillation. * 1/2 or double of the frequency can be used depending on the PLA.	① LCD driving specification • Static • 1/2bias-1/2duty • 1/2bias-1/3duty • 1/3bias-1/3duty ② Alternating frequency specification (The following values are for the 32.768kHz system clock.) • 16Hz • 32Hz • 64Hz	
Segment driver (Only for 3 terminals)	Output	(circuit diagram with VDD, VSS1, VSS2, VSS3)	LCD panel segment output terminal. • The terminal can be switched to the output-only port by mask option (See the Option Instruction Sheet for the terminals to be used.) • During the LSI system reset, the static lighting signal is fed to COM1 to COM3 and to each of the LCD segment outputs, and all LCD panel segments go on. • The segment PLA system is used to provide any layout of the LCD panel. * The values are for 32.768kHz crystal oscillation.	① Output for LCD ② CMOS output port ③ Pch open drain output port Options ①, ②, and ③ can be selected in bit units.	Full lighting (for LCD) "H" level (except for LCD)=ACTIVE state
Segment driver (For other terminals)	Output	(circuit diagram with VDD, VSS1, VSS2, VSS3)	LCD panel segment output terminal. • The terminal can be switched to the output port by mask option. • If the LSI system is reset, the static lighting signal is fed to COM1 to COM3 and to each of the LCD segment outputs, and all LCD panel segments go on. • The segment PLA system is used to provide any layout of the LCD panel. * The values are for 32.768kHz crystal oscillation.	① Output for LCD ② CMOS output port Options ① and ② can be selected in bit units.	Full lighting (for LCD) "H" level (except for LCD)=ACTIVE state
TEST TEST TEST			Terminals for test (not used by the users)		
TESTA			Terminal for test apply (-) voltage.		
(V_DD)			Auxiliary supply voltage terminal. Do not use the terminal.		

Remarks: ⚓ Ag specifications: VSS1   Li specifications, EXT-V specifications: VSS2

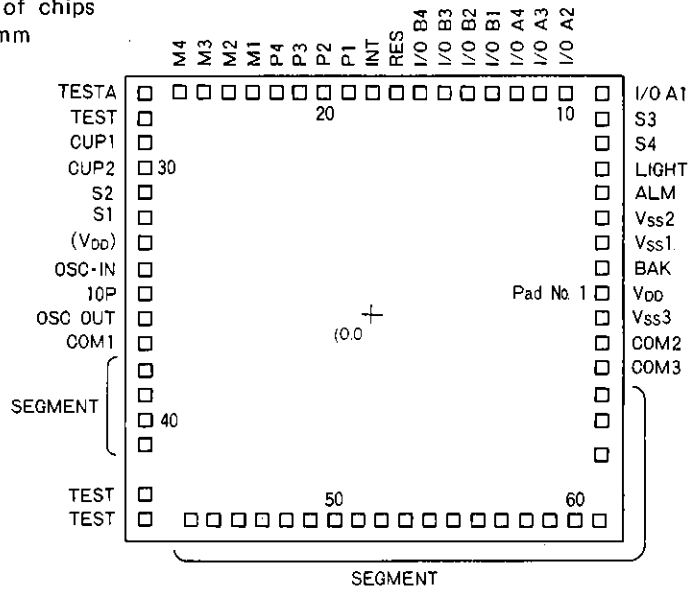## Pad Assignment on LSI Chip

Reference data for the shipment of chips
Chips size: 3.85mm X 3.48mm
Chip thickness: 480μm
Pad size: 120μm X 120μm

Package Dimensions 3057
(unit:mm)

SANYO : QIP64A
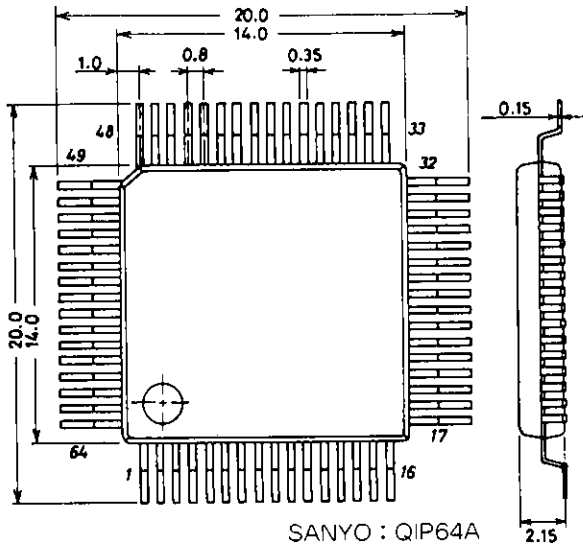
Package Dimensions 3026B
(unit:mm)

SANYO : QIP64B
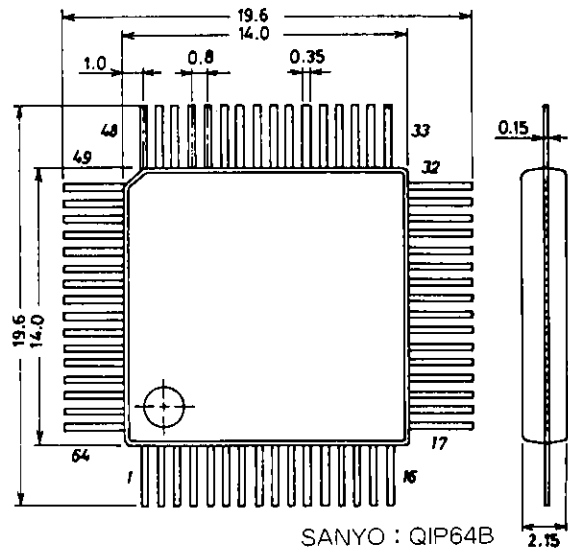
Please contact your local Sales Representative if you plan to use the QIP64B.
(Special packages need to be specially ordered.)

Pin Assignment
Pad Name and Coordinates

QFP(QIP) 64 Pin No.	Pad No	Terminal Name	Coordinate x(μm)	y(μm)	QFP(QIP) 64 Pin No.	Pad No	Terminal Name	Coordinate x(μm)	y(μm)
40	1	VDD	1728	105	—	35	10P	−1728	105
41	2	BAK	1728	285	9	36	OSC-OUT	−1728	−75
42	3	Vss1	1728	465	10	37	COM1	−1728	−255
43	4	Vss2	1728	645	11	38	SEG01	−1728	−461
44	5	ALM	1728	825	12	39	SEG02	−1728	−641
45	6	LIGHT	1728	1005	13	40	SEG03	−1728	−821
46	7	S4	1728	1185	14	41	SEG04	−1728	−1001
47	8	S3	1728	1365	—	42	TEST	−1728	−1365
48	9	I/O A1	1728	1545	—	43	TEST	−1728	−1545
49	10	I/O A2	1428	1545	15	44	SEG05	−1399	−1545
50	11	I/O A3	1248	1545	16	45	SEG06	−1218	−1545
51	12	I/O A4	1068	1545	17	46	SEG07	−1038	−1545
52	13	I/O B1	888	1545	18	47	SEG08	−858	−1545
53	14	I/O B2	708	1545	19	48	SEG09	−678	−1545
54	15	I/O B3	528	1545	20	49	SEG10	−498	−1545
55	16	I/O B4	348	1545	21	50	SEG11	−318	−1545
56	17	RES	166	1545	22	51	SEG12	−138	−1545
57	18	INT	14	1545	23	52	SEG13	42	−1545
58	19	P1	−196	1545	25	53	SEG14	222	−1545
59	20	P2	−376	1545	26	54	SEG15	402	−1545
60	21	P3	−556	1545	27	55	SEG16	582	−1545
61	22	P4	−736	1545	28	56	SEG17	762	−1545
62	23	M1	−916	1545	29	57	SEG18	942	−1545
63	24	M2	−1096	1545	30	58	SEG19	1122	−1545
64	25	M3	−1276	1545	31	59	SEG20	1302	−1545
1	26	M4	−1456	1545	32	60	SEG21	1482	−1545
2	27	TESTA	−1728	1545	33	61	SEG22	1662	−1545
3	28	TEST	−1728	1365	34	62	SEG23	1728	−1075
4	29	CUP1	−1728	1185	35	63	SEG24	1728	−821
5	30	CUP2	−1728	1005	36	64	SEG25	1728	−641
6	31	S2	−1728	825	37	65	COM3	1728	−435
7	32	S1	−1728	645	38	66	COM2	1728	−255
—	33	(VDD)	−1728	465	39	67	Vss3	1728	−75
8	34	OSC-IN	−1728	285					

- Pin 24 on the QFP64 (QIP64) package is NC. (Use the NC pin in the open position.)
- The pad coordinates are determined with the center of these chip as origin. The values for (X, Y) are the coordinates for the center of each pad.
- Use the terminals for test in the open position.
- When selecting the chip, connect the substrate to VDD.
- When mounting the QFP64 (QIP64) package on the board, do not dip it in solder.

Oscillation Circuit Options

Unit (capacitance: F)

Option	Circuit	Remarks
XT oscillation (32.768kHz)		• The 10P terminal can be used only for chip selection.
XT oscillation (65kHz)		• The 10P terminal can be used only for chip selection. • Used for the cycle time 61μ version.
CF oscillation		

Input Port Options

Option	Circuit	Remarks
Hold Tr		• The Hold Tr option is used to reduce the current required, for example, for a pushbutton switch for S1, and a slide switch for S2. • For example, the "L" level signal can be held after the pull-down resistor is set to ON for a short period of time by software in case of open type of input port.
Open		• Pull-down Tr can be used as a pull-down resistor. • Pull-down Tr can be set to ON/OFF by software.

"L" level Hold Tr can be selected for ports S1 to S4 and M1 to M4.

• Port S has an independent chatter-removal circuit (in bit units) that operates at Ø10 period, Ø8 period or Ø6 period.
• Port M has a chatter-removal circuit that operates upon of the HALT release request signal. With this circuit, chatter at Ø10 period, Ø8 period or Ø6 period is removed when three terminales of M port are in the "L" level and any signal to the other terminal changes.
Note that ØN indicates the output at the Nth step of the oscillator frequency divider circuit. If a 32.768kHz oscillator is used,

    Ø6...About 2msec.
    Ø8...About 8msec.
    Ø10...About 32msec.

LCD Output Options

LCD output options for the LCD driver, the CMOS output port and the Pch open drain output port can be selected (the Pch open drain option can be specified only for the predetermined 3 bits).

Option	Output Form
LCD drive	• Terminal for LCD segment drive. • The drive is selected according to the LCD driving system specified separately. The LCD driving system is common to all terminals, and can be selected from among the static, 1/2bias-1/2duty, 1/2bias-1/3duty, and 1/3bias-1/3duty methods.
CMOS output port	• General-purpose CMOS type output port
Pch open drain output port	• General-purpose Pch open drain type output port It's usable according to the PLA option for the predetermined three ports. Usable ports...Pad No. 62 to 64 (Pin No. 34 to 36)

Alternating waveform for the LCD driver for LCD output is generated by hardware logic.

Segment PLA Circuit

A schema of the structure of the segment PLA circuit is shown below.
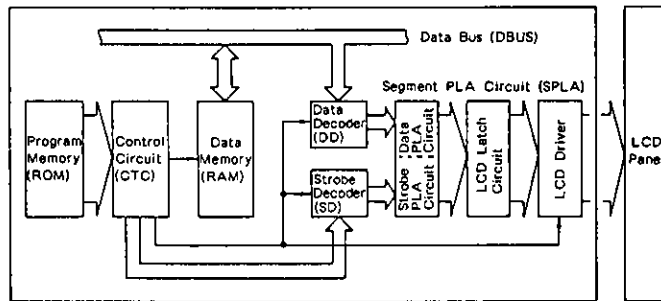
The contents of the Data Memory are sent through to the LCD Latch Circuit for display as is or after being decoded by the Data Decoder. The PLA Circuit is used to rearrange the input data to output it to the LCD latches. With this circuit, data memory can be edited to suit to the LCD panel specifications without software processing. The PLA circuit can be specified by the ROM for PLA. The user must release the ROM for PLA with the program ROM.

Output Port P

The following two modes can be selected by software:
1) General-purpose output port
2) Pseudo-serial output port
The time chart in the Pseudo-Serial mode is shown below:
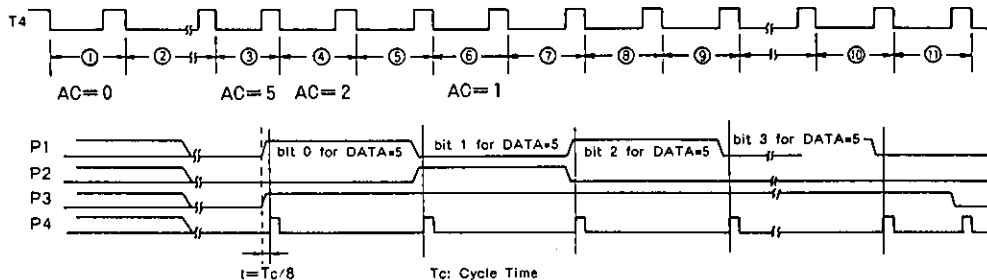
① , ② .... Initial processing for serial data transfer.
③ , ⑤ , ⑦ , ⑨ ... The first and the second bits of the RAM data are output to ports P1 and P2, respectively.
④ , ⑥ , ⑧ .... RAM data is shifted to the right.

As shown above, the RAM data can be transferred in 1-bit serial data form every two machine cycles. (For this, however, it is necessary to process (e.g., replace) the RAM data every 4-bit transfer.)

Alarm Output

The following frequency divider output can be used directly as alarm output:
1) Output signal either at $\emptyset 3$, $\emptyset 4$ (or $\emptyset 5$)
2) Any combination output signal at $\emptyset 10$, $\emptyset 11$, $\emptyset 12$, $\emptyset 13$, $\emptyset 14$ and $\emptyset 15$.
3) Modulating output signal of 1) or 2).
These signals can be output by software.
$\emptyset_N$ indicates the output at the Nth step of the oscillator frequency divider.

Operation Mode of Internal Logic

• The following diagram shows the supply voltages and the operation levels of internal logic.

Ag specifications (1.5V supply)
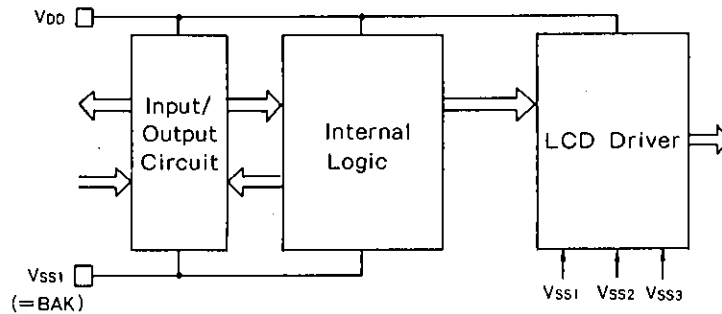
Li specifications (3V supply)
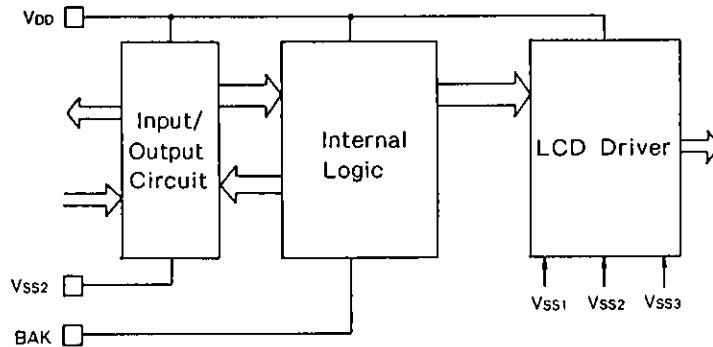
The BAK terminal is connected to V_{SS1} or V_{SS2} by software.
It is, however, connected to V_{SS2} after the initial clear is issued.

EXT-V specifications (3 to 5V supply)
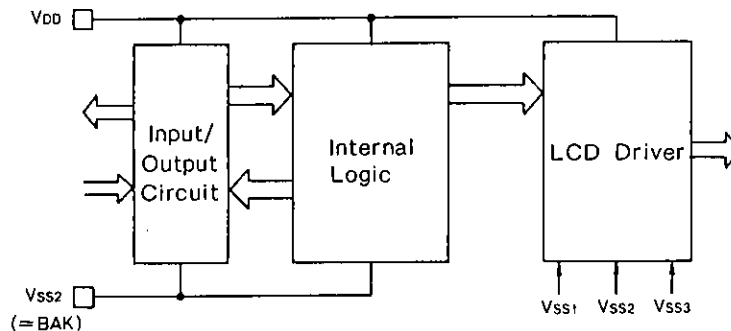
• The level of voltage applied to BAK is shown below.

| Power source option | BAK terminal level | | Input/output* port | Relations between V_{SS1}, V_{SS2}, and V_{SS3} |
	Normal mode	Backup mode		
Ag	V_{SS1}	V_{SS1}	$V_{DD}-V_{SS1}$	$V_{SS2} \approx V_{SS1} \times 2$
Li	V_{SS1}	V_{SS2}	$V_{DD}-V_{SS2}$	$V_{SS3} = V_{SS2}$ (other than 1/3 bias)
EXT-V	V_{SS2}	V_{SS2}	$V_{DD}-V_{SS2}$	$V_{SS3} \approx V_{SS1} \times 3$ (⅓ bias)

* The LCD output used as general-purpose port is included.

• The backup mode is called by setting the backup flag by software, and the normal mode is reinstated by resetting the flag.

Backup Mode

1) The backup mode is useful with Li specifications to prevent malfunctions of LSI circuits under heavy load.
An example of a time chart is shown below.
Power source option ... Li specifications

Heavy Load Operation Timing
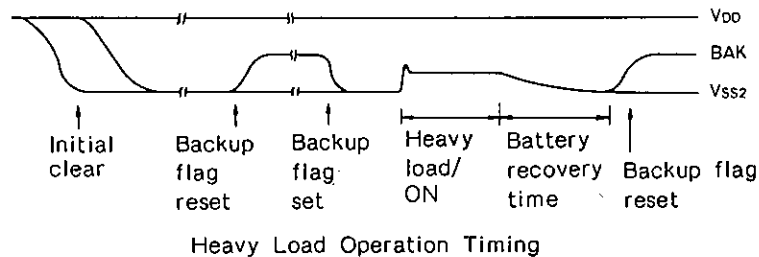
• To prevent a sudden change at BAK, a smoothing capacitor must be inserted between BAK and V_{DD}.

2) In the Ag and Li specifications, the backup mode is called with an initial clear. The reason is:
Ag specifications ... To shorten the oscillation start time of the crystal oscillator circuit.
Li specifications ... To start oscillation by applying supply voltage to the oscillator.
Be sure to reset the backup flag to return to normal mode, after the initial clear is released.
The backup-mode-related elements enter the following.

Power Source Specifications	BACK UP FLAG	Oscillator Inverter Size	BAK Terminal	Current Required
Ag	Set	Large	Connected to V_{SS1} (Fixed).	Becomes large.
Li	Set	Large	Brought to V_{SS2} level.	Becomes large.
EXT-V	Reset	Small	Connected to V_{SS2} (Fixed).	As usual.

Operation of Backup Flag at Initial Clear Mode

3) The current required in backup mode is 20 to 40 times that for normal mode.
Therefore, be sure to reset the backup flag except when necessary. For the EXT-V specifications, it is unnecessary to set the backup flag.

Resetting Internal Logic

There are three functions for resetting internal logic:
1. On-chip power-ON clear function ... Use of this option can be determined by the mask option.
2. Reset terminal RES ⎫
3. Simultaneous operation of S1 to S4 ⎬ Either option 2. or 3. can be specified (mask option).

These reset functions are explained below.
1) Built-in power-ON clear circuit
   The initial clear circuit provided in the microcomputer automatically operates and resets internal logic when power is turned on. This function is very useful in that it can be activated without external devices, but it has the two disadvantages listed below. It is, therefore, recommended that this function be used with other reset functions or that other methods be used according to applications.

   a) The circuit may not operate under certain power-rise conditions during the power-ON sequence or due to chatter.
   b) Malfunctions may take place due to pulse noise in V_{DD} port or a sudden change in status.
   One of the following two reset options can be selected:
       INHIBIT: The built-in power-ON clear circuit is not used.
                       Malfunction due to pulse noise in V_{DD} port can be prevented.
       NORMAL ACTION: The built-in power-ON clear circuit is used.
                       This option should be selected only when pulse noise in the power does not affect.
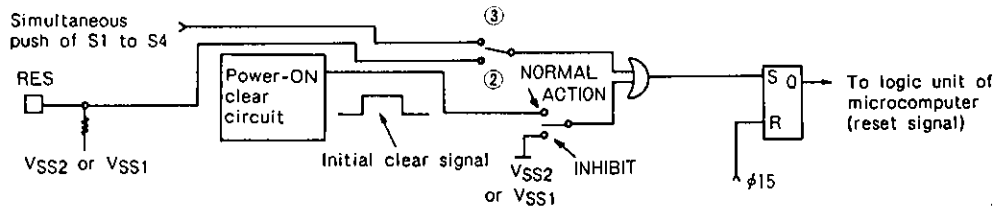
   The built-in power-ON clear function in LSI circuits may not work under certain power-rise conditions. Use an external reset switch (the reset terminal or simultaneous operation of S1 to S4).

2) To activate the initial clear function completely with the reset terminal, the following conditions must be satisfied:
1 Oscillation must be normal.
2 The "H" level signal must be applied for more than 200μs.

   An example of the reset circuit is shown below.
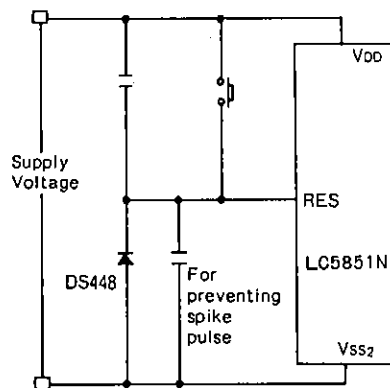
Reset release
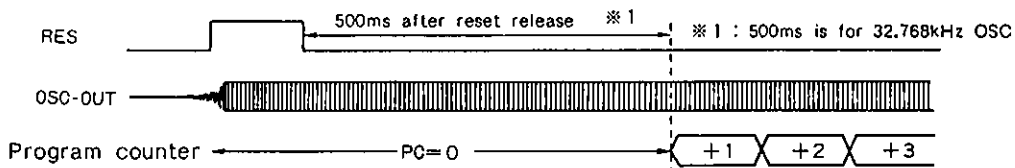
Even with this circuit, the above two requisites may not be satisfied due to the power-rise conditions or oscillation start time, and therefore the power-ON clear function may not work. To prevent this, an external reset switch should be used.

3) The same requisites as in 2) must be satisfied for the simultaneous operation of S1 to S4. If the timing for applying signals to S1 to S4 (i.e., the timing for signals changing from "H" to "L" levels) is not even, the microcomputer starts operating according to the built-in program.

Option List

Parameter		Option Selection	Remarks
Power Select		• Ag specifications • Li specificaitons • EXT-V specifications	
LCD lighting		• Static • 1/2 Bias -1/2 Duty • 1/2 Bias - 1/3 Duty • 1/3 Bias - 1/3 Duty • NON USE	Select "non use" if all LCD outputs are to be used as general-purpose ports.
LCD frequency		• SLOW (OSC/2048) • TYP (OSC/1024) • FAST (OSC/512)	
"L" level HOLD Tr	S PORT (S1−4)	• Use "L"-level hold Tr • Non Use "L"-level hold Tr	
	M PORT (M1−4)	• Use "L"-level hold Tr • Non Use "L"-level hold Tr	
S,M port chatter-removal frequency		• SLOW (OSC/1024) • TYP (OSC/256) • FAST (OSC/64)	
INT terminal	Input resistance	• Pull-up • Pull-down • Open	
	Signal change	• Rise • Fall	
External reset		• RES terminal • Simultaneous operation of S1 to S4	
Internal timer clock		• SLOW (OSC/512) • FAST (OSC/8)	
ALARM signal modulating reference frequency		• TYP (OSC/8, OSC/16) • SLOW (OSC/8, OSC/32)	
Built-in power-ON clear function		• Use • Non Use	
Oscillator configuration		• 32.768kHz crystal use • 65.536kHz crystal use • Ceramic oscillator use	
Cycle Time		• SLOW (OSC/8) • FAST (OSC/4)	Select SLOW at 200kHz ceramic resonator mode.

EXT-V Specifications

Absolute Maximum Ratings at Ta=25°C, V$_{DD}$=0V

Item	Symbol	Condition/Terminal	Rating	unit
Maximum Supply Voltage	V$_{SS}$1		−7.0 to +0.3	V
	V$_{SS}$2		−7.0 to +0.3	V
	V$_{SS}$3		−8.5 to +0.3	V
Maximum Input Voltage	V$_{IN}$1		$\binom{V_{SS}2}{-0.3}$ to +0.3	V
Maximum Output Voltage	V$_{OUT}$1	ALM, LIGHT, P1to4, CUP2, OSCOUT, TEST, I/O A1-4, I/O B1-4,(I/O A, I/O B: output mode.)	$\binom{V_{SS}2}{-0.3}$ to +0.3	V
	V$_{OUT}$2	SEGOUT, COM1-3, CUP1	$\binom{V_{SS}3}{-0.3}$ to +0.3	V
Operating Temperature	Topr		−20 to +70	°C
Storage Temperature	Tstg		−30 to +125	°C

Allowable Operating Conditions at Ta=-20 to +70°C, V$_{DD}$=0V

Item	Symbol	Condition/Terminal	min	typ	max	unit
Supply Voltage	V$_{SS}$1		−5.5		−1.3	V
	V$_{SS}$2	32kHz crystal mode	−5.5		−2.0	V
	V$_{SS}$3		−8.25		−2.0	V
Supply Voltage	V$_{SS}$1		−5.5		−1.3	V
	V$_{SS}$2	65kHz crystal mode	−5.5		−2.3	V
	V$_{SS}$3		−8.25		−2.3	V
Supply Voltage	V$_{SS}$1		−5.5		−1.7	V
	V$_{SS}$2	External input mode	−5.5		−3.5	V
	V$_{SS}$3		−8.25		−3.5	V
Supply Voltage	V$_{SS}$1		−5.5		−2.0	V
	V$_{SS}$2	CF mode (200kHz,400kHz,800kHz)	−5.5		−4.0	V
	V$_{SS}$3		−8.25		−4.0	V
Input "H"-Level Voltage	V$_{IH}$1	All input terminal except OSCIN	$\binom{0.3\times}{V_{SS}2}$		0	V
Input "L"-Level Voltage	V$_{IL}$1		V$_{SS}$2		$\binom{0.7\times}{V_{SS}2}$	V
Input "H"-Level Voltage	V$_{IH}$2	OSCIN terminal, external input mode	$\binom{0.2\times}{V_{SS}2}$		0	V
Input "L"-Level Voltage	V$_{IL}$2		V$_{SS}$2		$\binom{0.8\times}{V_{SS}2}$	V
Operating Frequency	fopg1	V$_{SS}$2=−2.0to −5.5V OSCIN/OSCOUT 32kHz crystal, Fig.2	32		66	kHz
Operating Frequency	fopg2	V$_{SS}$2=−2.3to −5.5V OSCIN/OSCOUT 65kHz crystal, Fig.2	60		66	kHz
Operating Frequency	fopg3	V$_{SS}$2=−3.5to −5.5V OSCIN, external input, Fig.8	32		220	kHz
Operating Frequency	fopg4	V$_{SS}$2=−4.0to −5.5V OSCIN/OSCOUT CF 200kHz, Fig.1	180	200	220	kHz
Operating Frequency	fopg5	V$_{SS}$2=−4.0to −5.5V OSCIN/OSCOUT CF 400kHz, Fig.1	360	400	440	kHz
Operating Frequency	fopg6	V$_{SS}$2=−4.0to −5.5V OSCIN/OSCOUT CF800kHz Fig.1	720	800	810	kHz

LC5851N

Electrical Characteristics at Ta=-20 to +70°C, V_{DD}=0V

Item	Symbol	Condition/Terminal		min	typ	max	unit
Input Resistance	$R_{IN}1A$	Vss2=−2.9V V_{IN}=0.8·Vss2	"L" level hold Tr *1, Fig.3	10		200	kΩ
	$R_{IN}1B$	Vss2=−2.9V V_{IN}=VDD	"L" level pull-in Tr *1, Fig.3	200	700	2000	kΩ
	$R_{IN}2A$	Vss2=−2.9V V_{IN}=Vss2	Resistance for INT pull-up	200	700	2000	kΩ
Input Resistance	$R_{IN}2B$	Vss2=−2.9V V_{IN}=VDD	Resistance for INT pull-down	200	700	2000	kΩ
	$R_{IN}3$	Vss2=−2.9V V_{IN}=VDD or Vss2	RES	5		50	kΩ
Output "H"-Level Voltage	$V_{OH}(1)$	Vss2=−2.4V I_{OH}=−1mA	ALM	−1	−0.3		V
Output "L"-Level Voltage	$V_{OL}(1)$	Vss2=−2.4V I_{OL}=1mA	ALM		(Vss2 +0.3	(Vss2 +1	V
Output "H"-Level Voltage	$V_{OH}(2)$	Vss2=−2.4V I_{OH}=−0.3mA	LIGHT, port P	−1	−0.3		V
Output "L"-Level Voltage	$V_{OL}(2)$	Vss2=−2.4V I_{OL}=0.5mA	LIGHT, port P		(Vss2 +0.3	(Vss2 +1	V
Output "H"-Level Voltage	$V_{OH}(3)$	Vss2=−2.4V I_{OH}=−0.1mA	I/O port	−1	−0.3		V
Output "H"-Level Voltage	$V_{OH}(4)$	Vss2=−2.4V I_{OH}=−50μA	I/O port	−0.6	−0.2		V
Output "L"-Level Voltage	$V_{OL}(4)$	Vss2=−2.4V I_{OL}=0.1mA	I/O port		(Vss2 +0.3	(Vss2 +1	V

Segment Driver Output Impedance

● CMOS Output Port Mode

Item	Symbol	Condition/Terminal		min	typ	max	unit
Output "H"-Level Voltage	$V_{OH}(5)$	Vss2=−2.4V I_{OH}=−10μA	Segment PAD No.62to64 QIP64 pin No. 34to36	−1	−0.3		V
Output "L"-Level Voltage	$V_{OL}(5)$	Vss2=−2.4V I_{OL}=100μA			(Vss2 +0.3	(Vss2 +1	V
Output "H"-Level Voltage	$V_{OH}(6)$	Vss2=−2.4V I_{OH}=−5μA	Segment PAD No 38to41,44to61 QIP64 pin No. 11to23,25to33	−1	−0.3		V
Output "L"-Level Voltage	$V_{OL}(6)$	Vss2=−2.4V I_{OL}=20μA			(Vss2 +0.3	(Vss2 +1	V

● PCH Open Drain Output Port Mode

Item	Symbol	Condition/Terminal		min	typ	max	unit
Output "H"-Level Voltage	$V_{OH}(5)$	Vss2=−2.4V I_{OH}=−10μA	Segment PAD No.62to64 QIP64 pin No. 34to36	−1	−0.3		V
Output OFF-State Leakage Current	I_{OFF}	Vss2=−2.9V V_{OL}=Vss2				1	μA

● Static Display

Item	Symbol	Condition/Terminal		min	typ	max	unit
Output "H"-Level Voltage	$V_{OH}(5)$	Vss2=−2.4V I_{OH}=−0.4μA	All segments	−0.2			V
Output "L"-Level Voltage	$V_{OL}(5)$	Vss2=−2.4V I_{OL}=0.4μA				(Vss2 +0.2	V
Output "H"-Level Voltage	$V_{OH}(7)$	Vss2=−2.4V I_{OH}=−4μA	COM1	−0.2			V
Output "L"-Level Voltage	$V_{OL}(7)$	Vss2=−2.4V I_{OL}=4μA				(Vss2 +0.2	V

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Electrical Characteristics at Ta=-20 to +70°C, V$_{DD}$=0V

Item	Symbol	Condition/Terminal		min	typ	max	unit
● **Duplex Display (1/2Bias, 1/2Duty)**							
Output "H"-Level Voltage	V$_{OH}$(5)	V$_{SS2}$=−2.4V I$_{OH}$=−0.4μA	All segments	−0.2			V
Output "L"-Level Voltage	V$_{OL}$(5)	V$_{SS2}$=−2.4V I$_{OL}$=0.4μA				$\left(\begin{array}{c} Vss2 \\ +0.2 \end{array}\right.$	V
Output "H"-Level Voltage	V$_{OH}$(7)	V$_{SS2}$=−2.4V I$_{OH}$=−4 μA	COM1-2	−0.2			V
Output "M"-Level Voltage	V$_{OM}$	V$_{SS2}$=−2.4V I$_{OH}$=−4 μA I$_{OL}$=4 μA		$\left(\begin{array}{c} Vss2/2 \\ −0.2 \end{array}\right.$		$\left(\begin{array}{c} Vss2/2 \\ +0.2 \end{array}\right.$	V
Output "L"-Level Voltage	V$_{OL}$(7)	V$_{SS2}$=−2.4V I$_{OL}$=4 μA				$\left(\begin{array}{c} Vss2 \\ +0.2 \end{array}\right.$	V
● **1/2Bias, 1/3Duty Display**							
Output "H"-Level Voltage	V$_{OH}$(5)	V$_{SS2}$=−2.4V I$_{OH}$=−0.4μA	All segments	−0.2			V
Output "L"-Level Voltage	V$_{OL}$(5)	V$_{SS2}$=−2.4V I$_{OL}$=0.4μA				$\left(\begin{array}{c} Vss2 \\ +0.2 \end{array}\right.$	V
Output "H"-Level Voltage	V$_{OH}$(7)	V$_{SS2}$=−2.4V I$_{OH}$=−4 μA	COM1-3	−0.2			V
Output "M"-Level Voltage	V$_{OM}$	V$_{SS2}$=−2.4V I$_{OH}$=−4 μA I$_{OL}$=4 μA		$\left(\begin{array}{c} Vss2/2 \\ −0.2 \end{array}\right.$		$\left(\begin{array}{c} Vss2/2 \\ +0.2 \end{array}\right.$	V
Output "L"-Level Voltage	V$_{OL}$(7)	V$_{SS2}$=−2.4V I$_{OL}$=4 μA				$\left(\begin{array}{c} Vss2 \\ +0.2 \end{array}\right.$	V
● **1/3Bias, 1/3Duty Display**							
Output "H"-Level Voltage	V$_{OH}$(5)	V$_{SS2}$=−2.4V I$_{OH}$=−0.4μA	All segments	−0.2			V
Output "M"-Level Voltage	V$_{OM}$1-1	V$_{SS2}$=−2.4V I$_{OH}$=−0.4μA		$\left(\begin{array}{c} Vss2/2 \\ −0.2 \end{array}\right.$		$\left(\begin{array}{c} Vss2/2 \\ +0.2 \end{array}\right.$	V
	V$_{OM}$1-2	I$_{OL}$=0.4μA		$\left(\begin{array}{c} Vss2 \\ −0.2 \end{array}\right.$		$\left(\begin{array}{c} Vss2 \\ +0.2 \end{array}\right.$	V
Output "L"-Level Voltage	V$_{OL}$(5)	V$_{SS2}$=−2.4V I$_{OL}$=0.4μA				$\left(\begin{array}{c} Vss3 \\ +0.2 \end{array}\right.$	V
Output "H"-Level Voltage	V$_{OH}$(7)	V$_{SS2}$=−2.4V I$_{OH}$=−4 μA	COM1-3	−0.2			V
Output "M"-Level Voltage	V$_{OM}$2-1	V$_{SS2}$=−2.4V I$_{OH}$=−4 μA		$\left(\begin{array}{c} Vss2/2 \\ −0.2 \end{array}\right.$		$\left(\begin{array}{c} Vss2/2 \\ +0.2 \end{array}\right.$	V
	V$_{OM}$2-2	I$_{OL}$=4 μA		$\left(\begin{array}{c} Vss2 \\ −0.2 \end{array}\right.$		$\left(\begin{array}{c} Vss2 \\ +0.2 \end{array}\right.$	V
Output "L"-Level Voltage	V$_{OL}$(7)	V$_{SS2}$=−2.4V I$_{OL}$=4 μA				$\left(\begin{array}{c} Vss3 \\ +0.2 \end{array}\right.$	V

Continued from preceding page.

Electrical Characteristics at Ta=-20 to +70°C, V_DD=0V

Item	Symbol	Condition/Terminal		min	typ	max	unit
Input Resistance	R_IN1A	V_SS2=−5.0V V_IN=0.8·V_SS2	"L" level hold Tr, *1, Fig.3	10	45	150	kΩ
	R_IN1B	V_SS2=−5.0V V_IN=V_DD	Pull-in "L" level Tr, *1, Fig.3	100	350	1000	kΩ
	R_IN2A	V_SS2=−5.0V V_IN=V_SS2	Resistance for INT pull-up	100	350	1000	kΩ
	R_IN2B	V_SS2=−5.0V V_IN=V_DD	Resistance for INT pull-down	100	350	1000	kΩ
	R_IN3	V_SS2=−5.0V V_IN=V_DD or V_SS2	RES	10	20	50	kΩ
Output "H"-Level Voltage	V_OH(1)	V_SS2=−3.5V to −5.5V I_OH=−1.5mA	ALM	−1	−0.3		V
Output "L"-Level Voltage	V_OL(1)	V_SS2=−3.5V to −5.5V I_OL=1.5mA	ALM		$\left(\begin{array}{c}V_{SS2}\\+0.3\end{array}\right.$	$\left(\begin{array}{c}V_{SS2}\\+1\end{array}\right.$	V
Output "H"-Level Voltage	V_OH(2)	V_SS2=−3.5V to −5.5V I_OH=0.5mA	LIGHT, port P	−1	−0.3		V
Output "L"-Level Voltage	V_OL(2)	V_SS2=−3.5V to −5.5V I_OL=0.7mA	LIGHT, port P		$\left(\begin{array}{c}V_{SS2}\\+0.3\end{array}\right.$	$\left(\begin{array}{c}V_{SS2}\\+1\end{array}\right.$	V
Output "H"-Level Voltage	V_OH(3)	V_SS2=−3.5V to −5.5V I_OH=−0.13mA	I/O port	−1	−0.3		V
Output "H"-Level Voltage	V_OH(4)	V_SS2=−3.5V to −5.5V I_OH=−50μA	I/O port	−0.6	−0.2		V
Output "L"-Level Voltage	V_OL(4)	V_SS2=−3.5V to −5.5V I_OL=0.13mA	I/O port		$\left(\begin{array}{c}V_{SS2}\\+0.3\end{array}\right.$	$\left(\begin{array}{c}V_{SS2}\\+1\end{array}\right.$	V

Segment Driver Output Impedance

● CMOS Output Port Mode

Item	Symbol	Condition/Terminal		min	typ	max	unit
Output "H"-Level Voltage	V_OH(5)	V_SS2=−3.5V to −5.5V I_OH=−15μA	Segment ⌐ PAD No.62to64 ¬ ⌊ QIP64 pin No. 34to36 ⌋	−1	−0.3		V
Output "L"-Level Voltage	V_OL(5)	V_SS2=−3.5V to −5.5V I_OL=150μA			$\left(\begin{array}{c}V_{SS2}\\+0.3\end{array}\right.$	$\left(\begin{array}{c}V_{SS2}\\+1\end{array}\right.$	V
Output "H"-Level Voltage	V_OH(6)	V_SS2=−3.5V to −5.5V I_OH=−10μA	Segment ⌐ PAD No. 38to41,44to61 QIP64 pin No. ⌊ 11to23,25to33 ⌋	−1	−0.3		V
Output "L"-Level Voltage	V_OL(6)	V_SS2=−3.5V to −5.5V I_OL=60μA			$\left(\begin{array}{c}V_{SS2}\\+0.3\end{array}\right.$	$\left(\begin{array}{c}V_{SS2}\\+1\end{array}\right.$	V

Continued from preceding page.

Electrical Characteristics at Ta=-20 to +70°C, V_{DD}=0V

Item	Symbol	Condition/Terminal		min	typ	max	unit
●PCH Open Drain Output Port Mode							
Output "H"-Level Voltage	$V_{OH}(5)$	V_{SS2}=−3.5V to −5.25V I_{OH}=−15μA	Segment ⌈ PAD No62to64 QIP64 pin No. ⌊ 34to36 ⌋	−1	−0.3		V
Output OFF-State Leakage Current	I_{OFF}	V_{SS2}=−3.5V to −5.25V V_{OL}=Vss2				1	μA
● Static Display							
Output "H"-Level Voltage	$V_{OH}(5)$	V_{SS2}=−3.5V to −5.25V I_{OH}=−0.4μA	All segments	−0.2			V
Output "L"-Level Voltage	$V_{OL}(5)$	V_{SS2}=−3.5V to −5.25V I_{OL}=0.4μA				(Vss2 +0.2	V
Output "H"-Level Voltage	$V_{OH}(7)$	V_{SS2}=−3.5V to −5.25V I_{OH}=−4μA	COM1	−0.2			V
Output "L"-Level Voltage	$V_{OL}(7)$	V_{SS2}=−3.5V to −5.25V I_{OL}=4μA				(Vss2 +0.2	V
●Duplex Display (1/2Bias, 1/2Duty)							
Output "H"-Level Voltage	$V_{OH}(5)$	V_{SS2}=−3.5V to −5.25V I_{OH}=−0.4μA	All segments	−0.2			V
Output "L"-Level Voltage	$V_{OL}(5)$	V_{SS2}=−3.5V to −5.25V I_{OL}=0.4μA				(Vss2 +0.2	V
Output "H"-Level Voltage	$V_{OH}(7)$	V_{SS2}=−3.5V to −5.25V I_{OH}=−4μA		−0.2			V
Output "M"-Level Voltage	V_{OM2-1}	V_{SS2}=−3.5V to −5.25V I_{OH}=−4μA I_{OL}=4μA	COM1-2	(Vss2/2 −0.2		(Vss2/2 +0.2	V
Output "L"-Level Voltage	$V_{OL}(7)$	V_{SS2}=−3.5V to −5.25V I_{OL}=4μA				(Vss2 +0.2	V
●1/2Bias, 1/3Duty Display							
Output "H"-Level Voltage	$V_{OH}(5)$	V_{SS2}=−3.5V to −5.25V I_{OH}=−0.4μA	All segments	−0.2			V
Output "L"-Level Voltage	$V_{OL}(5)$	V_{SS2}=−3.5V to −5.25V I_{OL}=0.4μA				(Vss2 +0.2	V
Output "H"-Level Voltage	$V_{OH}(7)$	V_{SS2}=−3.5V to −5.25V I_{OH}=−4μA		−0.2			V
Output "M"-Level Voltage	V_{OM2-1}	V_{SS2}=−3.5V to −5.25V I_{OH}=−4μA I_{OL}=4μA	COM1-3	(Vss2/2 −0.2		(Vss2/2 +0.2	V
Output "L"-Level Voltage	$V_{OL}(7)$	V_{SS2}=−3.5V to −5.25V I_{OL}=4μA				(Vss2 +0.2	V

Continued from preceding page.

Electrical Characteristics at Ta=-20 to +70℃, VDD=0V

Item	Symbol	Condition/Terminal		min	typ	max	unit
● 1/3Bias, 1/3Duty Display							
Output "H"-Level Voltage	VOH(5)	Vss2=−3.5V to −5.25V IOH=−0.4μA		−0.2			V
Output "M"-Level Voltage	VOM1-1	Vss2=−3.5V to −5.25V IOH=−0.4μA	All segments	(Vss2/2 −0.2		(Vss2/2 +0.2	V
	VOM1-2	IOL=0.4μA		(Vss2 −0.2		(Vss2 +0.2	V
Output "L"-Level Voltage	VOL(5)	Vss2=−3.5V to −5.25V IOL=0.4μA				(Vss3 +0.2	V
Output "H"-Level Voltage	VOH(7)	Vss2=−3.5V to −5.25V IOH=−4 μA		−0.2			V
Output "M"-Level Voltage	VOM2-1	Vss2=−3.5V to −5.25V IOH=−4 μA	COM1-3	(Vss2/2 −0.2		(Vss2/2 +0.2	V
	VOM2-2	IOL=4 μA		(Vss2 −0.2		(Vss2 +0.2	V
Output "L"-Level Voltage	VOL(7)	Vss2=−3.5V to −5.25V IOL=4 μA				(Vss3 +0.2	V
Power Supply Leakage Current	ILEK	Vss2=Vss3=−4.5V Ta=25℃				10	μA
Input Leakage Current	IIN	Vss2=−2.0to −4.5V VIN=Vss2toVDD		−1		1	μA
Output Voltage	Vss1	Vss2=−2.9V	C1=C2=C3= 0.1μF fopg=32.768kHz Ta=25℃ Fig.7		−1.45	−1.35	V
	Vss3	Vss2=−2.9V			−4.35	−4.1	V
Output Voltage	Vss1	Vss2=−4.5V	C1=C2=C3= 0.1μF fopg=32.768kHz Ta=25℃ Fig.7		−2.25	−2.2	V
	Vss3	Vss2=−4.5V			−6.70	−6.6	V
Supply Current	ΙDD 1 Ι	Vss2=−2.9V Ta=25℃,HALT mode	C1=C2=0.1μF Cl=25kΩ fopg=32.768kHz Cg=20pF		3.0	5	μA
	ΙDD 2 Ι	Vss2=−4.5V Ta=25℃,HALT mode			10	20	μA
		Static:Fig.9, 1/3B. 1/3D:Fig.7, others:Fig.4					
Supply Current	ΙDD 3Ι	Vss2=−4.5V Ta=25℃ HALT mode	C1=C2=0.1μF Cl=25kΩ fopg=65.536kHz Cg=10pF		20	50	μA
		Static:Fig.9, 1/3B. 1/3D:Fig.7, others:Fig.4					
Supply Current	ΙDD 4 Ι	Vss2=−4.5V Ta=25℃ HALT mode	C1=C2=0.1μF fopg=200kHz Cg=Cd=330pF or 180pF Rf=1MΩ Fig.6		100	300	μA
Supply Current	ΙDD5 Ι	Vss2=−4.5V Ta=25℃ HALT mode	C1=C2=0.1μF fopg=400kHz Cg=Cd=100pF or 330pF Rf=1MΩ Fig.6		150	400	μA

Continued from preceding page.

Electrical Characteristics at Ta=-20 to +70°C, V$_{DD}$=0V

Item	Symbol	Condition/Terminal		min	typ	max	unit
Supply Current	I$_{DD}$6I	Vss2=−4.5V Ta=25°C HALT mode	⌐C1=C2=0.1μF │fopg=800kHz │Cg=Cd=100pF └Rf=1MΩ Fig.6		200	500	μA
Oscillation Hold Voltage	IV$_{HOLD}$1I	Ta=25°C Static:Fig.9, 1/3B. 1/3D:Fig.7, others:Fig.4	⌐C1=C2=0.1μF │CI=25kΩ │fopg=32.768kHz └Cg=20pF	2.0		5.5	V
Oscillation Hold Voltage	IV$_{HOLD}$2I	Ta=25°C Static:Fig.10, 1/3B. 1/3D:Fig.7, others:Fig.4	⌐C1=C2=0.1μF │CI=25kΩ │fopg=65.536kHz └Cg=10pF	2.3		5.5	V
Oscillation Start Voltage	IVstt1I	Ta=25°C	⌐C1=C2=0.1μF │CI=25kΩ Fig.5 │fopg=32.768kHz └Cg=20pF			2.2	V
Oscillation Start Voltage	IVstt2I	Ta=25°C	⌐C1=C2=0.1μF │CI=25kΩ Fig.5 │fopg=65.536kHz └Cg=10pF			2.6	V
Oscillation Start Time	Tstt1	Vss2=−2.9V Ta=25°C Vss2=−4.5V Ta=25°C	⌐C1=C2=0.1μF │CI=25kΩ Fig.5 │fopg=32.768kHz └Cg=20pF			10 10	s s
Oscillation Start Time	Tstt2	Vss2=−2.9V Ta=25°C Vss2=−4.5V Ta=25°C	⌐C1=C2=0.1μF │CI=25kΩ Fig.5 │fopg=65.536kHz └Cg=10pF			10 10	s s
Oscillation Start Voltage	IVstt4I	Ta=25°C	⌐fopg=200kHz Fig.6 │Cg=Cd=330pF or │ 180pF └Rf=1MΩ			4.0	V
Oscillation Hold Voltage	IV$_{HOLD}$4I	Ta=25°C	⌐fopg=200kHz Fig.6 │Cg=Cd=330pF or │ 180pF └Rf=1MΩ	3.5		5.25	V
Oscillation Start Time	Tstt4	Vss2=−4.5V Ta=25°C	⌐fopg=200kHz Fig.6 │Cg=Cd=330pF or │ 180pF └Rf=1MΩ		50	500	ms
Oscillation Start Voltage	IVstt5I	Ta=25°C	⌐fopg=400kHz Fig.6 │Cg=Cd=100pF or │ 330pF └Rf=1MΩ			4.0	V
Oscillation Hold Voltage	IV$_{HOLD}$5I	Ta=25°C	⌐fopg=400kHz Fig.6 │Cg=Cd=100pF or │ 330pF └Rf=1MΩ	3.5		5.5	V
Oscillation Start Time	Tstt5	Vss2=−4.5V Ta=25°C	⌐fopg=400kHz Fig.6 │Cg=Cd=100pF or │ 330pF └Rf=1MΩ			30	ms

Continued from preceding page.

Electrical Characteristics at Ta=-20 to +70℃, V_DD=0V

Item	Symbol	Condition/Terminal		min	typ	max	unit
Oscillation Start Voltage	IVstt6I	Ta=25℃	fopg=800kHz Fig.6 Cg=Cd=100pF Rf= 1 MΩ			4.0	V
Oscillation Hold Voltage	IVHOLD6I	Ta=25℃	fopg=800kHz Fig.6 Cg=Cd=100pF Rf= 1 MΩ	3.5		5.5	V
Oscillation Start Time	Tstt6	Vss2=−4.5V Ta=25℃	fopg=800kHz Fig.6 Cg=Cd=100pF Rf= 1 MΩ			30	ms
Oscillation Compensation Capacitance	10P	Vss2=−2.9V	10p terminal (for chip only)		10		pF
	10P	Vss2=−4.5V	10p terminal (for chip only)		10		pF
	20P	Vss2=−2.9V	OSCOUT terminal		20		pF
	20P	Vss2=−4.5V	OSCOUT terminal		20		pF

※1 S1, S2, S3, S4, M1, M2, M3, M4

Fig. 1 Ceramic Resonator Oscillation

Recommended Ceramic Resonator

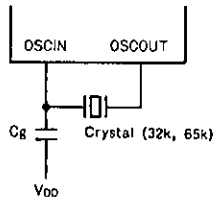| Maker	Murata				Kyocera			
Frequency　Item	Type Number	Cg	Cd	Rf	Type Number	Cg	Cd	Rf
200kHz	CSB200D	330pF	330pF	1 MΩ	KBR-200B	180pF	180pF	1 MΩ
400kHz	CSB400P	100pF	100pF	1 MΩ	KBR-400B	330pF	330pF	1 MΩ
800kHz	CSB800J	100pF	100pF	1 MΩ	KBR-800H	100pF	100pF	1 MΩ

Fig. 2 Crystal Oscillation (32kHz, 65kHz)
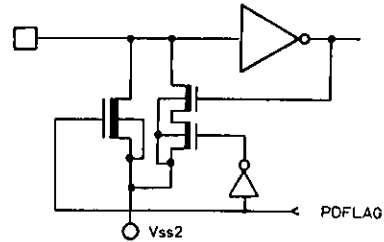
Fig. 3 Input Configuration of S1 to S4, M1 to M4
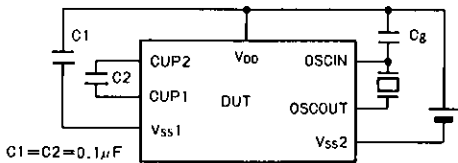
Fig. 4 Supply Current, Oscillation Hold Voltage Test Circuit
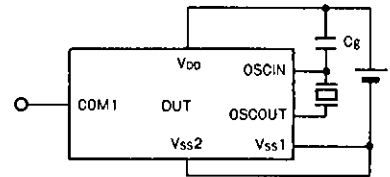
Fig. 5 Oscillation Start Voltage, Oscillation Start Time, Frequency Stability Test Circuit

Fig. 6 Oscillation Start Voltage, Oscillation Start Time, Supply Current, Oscillation Hold Voltage Test Circuit

Fig. 7 Supply Current, Oscillation Hold Voltage, Test Circuit

Fig. 8 External Input Mode

Fig. 9 Supply Current, Oscillation Hold Voltage Test Circuit

Ag Specifications

Absolute Maximum Ratings at Ta=25℃, V$_{DD}$=0V

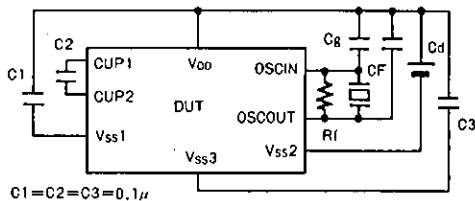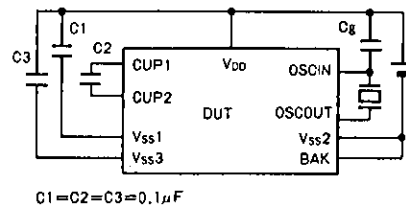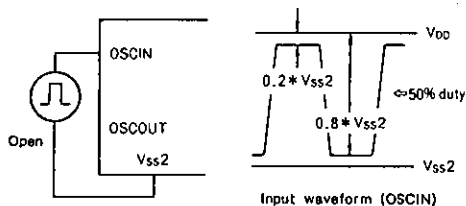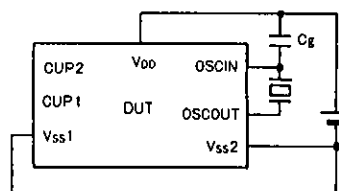| Item	Symbol	Condition/Terminal	Rating	unit
Maximum Supply Voltage	V$_{SS}$1		−4.0 to +0.3	V
	V$_{SS}$2		−4.0 to +0.3	V
	V$_{SS}$3	(LCD lighting:1/3bias display)	−5.5 to +0.3	V
	V$_{SS}$3	(LCD lighting:Other than 1/3bias display)	−4.0 to +0.3	V
Maximum Input Voltage	V$_{IN}$1	S1-4, M1-4, I/OA1-4, I/OB1-4, INT, TESTA(I/OA1-4, I/OB1-4 are in the input mode.)1OP, OSCIN, RES, BAK	$\left(\begin{array}{c}V_{SS}1 \\ -0.3\end{array}\right.$ to +0.3	V
Maximum Output Voltage	Vout1	ALM, LIGHT, P1-4, I/OA1-4, I/OB1-4, CUP2(I/OA1-4, I/OB1-4 are in the output mode.)TEST, OSCOUT	$\left(\begin{array}{c}V_{SS}1 \\ -0.3\end{array}\right.$ to +0.3	V
	Vout3	SEGOUT, COM1toCOM3, cup1	$\left(\begin{array}{c}V_{SS}3 \\ -0.3\end{array}\right.$ to +0.3	V
Operating Temperature	Topr		−20 to +65	℃
Storage Temperature	Tstg		−30 to +125	℃

Allowable Operating Conditions at Ta=25±2℃, V$_{DD}$=0V

Item	Symbol	Condition/Terminal	min	typ	max	unit
Supply Voltage	V$_{SS}$1	VBAK=VSS1	−1.65		−1.3	V
	V$_{SS}$2		−3.3		−2.4	V
	V$_{SS}$3	(LCD lighting:1/3bias display)	−4.95		−3.7	V
	V$_{SS}$3	(LCD lighting:Other than 1/3bias display)		V$_{SS}$3=V$_{SS}$2		
Input "H"-Level Voltage	V$_{IH}$	S1-4, M1-4, I/OA1-4, I/OB1-4, INT, (I/OA1-4, I/OB1-4 are in the input mode.)	−0.2		0	V
Input "L"-Level Voltage	V$_{IL}$	S1-4, M1-4, I/OA1-4, I/OB1-4, INT, (I/OA1-4, I/OB1-4 are in the input mode.)	Vss1		$\left(\begin{array}{c}V_{SS}1 \\ +0.2\end{array}\right.$	V
Operating Frequency	fopg	Ta=−20to+65℃	32		33	kHz

Electrical Characteristics at Ta=25±2℃, V$_{DD}$=0V

Item	Symbol	Condition/Terminal	min	typ	max	unit
Input Resistance	R$_{IN}$1A	Vss1=−1.55V, "L" level hold Tr V$_{IL}$=Vss1+0.2V *1, Fig.1	10		200	kΩ
	R$_{IN}$1B	Vss1=−1.55V, pull-down resistor *1, Fig.1	200		2000	kΩ
	R$_{IN}$2A	Vss1=−1.55V, pull-up resistor for V$_{IL}$=Vss1 INT	200		2000	kΩ
	R$_{IN}$2B	Vss1=−1.55V, pull-up resistor for V$_{IH}$=VDD INT	5		50	kΩ
	R$_{IN}$3	Vss=−1.55V, pull-down resistor V$_{IH}$=VDD for RES	5		50	kΩ
Output "H"-Level Voltage	V$_{OH}$(1)	Vss1=−1.35V, ALM, LIGHT IOH=−250μA	−0.65			V
Output "L"-Level Voltage	V$_{OL}$(1)	Vss1=−1.35V, ALM, LIGHT IOL=250μA			$\left(\begin{array}{c}Vss1 \\ +0.65\end{array}\right.$	V
Output "H"-Level Voltage	V$_{OH}$(2)	Vss1=−1.55V, I/OA1-4, I/OB1-4, IOH=−20μA, P1-4 (I/OA1-4, I/OB1-4 are in the output mode.)	−0.2			V
Output "L"-Level Voltage	V$_{OL}$(2)	Vss1=−1.55V, I/OA1-4, I/OB1-4, IOH=20μA, P1-4, (I/OA1-4, I/OB1-4 are in the output mode.)			$\left(\begin{array}{c}Vss1 \\ +0.2\end{array}\right.$	V

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Continued from preceding page.
Electrical Characteristics at Ta=25±2°C, V$_{DD}$=0V

Item	Symbol	Condition/Terminal	min	typ	max	unit
Segment Driver Output Impedance						
●Static Display						
Output "H"-Level Voltage	V$_{OH}$(3)	Vss1=−1.55V, SEGOUT I$_{OH}$=−0.4μA	−0.2			V
Output "L"-Level Voltage	V$_{OL}$(3)	Vss1=−1.55V, SEGOUT I$_{OL}$=0.4μA			(Vss2 +0.2	V
Output "H"-Level Voltage	V$_{OH}$(4)	Vss1=−1.55V, COM1 I$_{OH}$=−4μA	−0.2			V
Output "L"-Level Voltage	V$_{OL}$(4)	Vss1=−1.55V, COM1 I$_{OL}$=4μA			(Vss2 +0.2	V
●Duplex Display (1/2Bias, 1/2Duty)						
Output "H"-Level Voltage	V$_{OH}$(3)	Vss1=−1.55V, all SEGOUTs I$_{OH}$=−0.4μA	−0.2			V
Output "L"-Level Voltage	V$_{OL}$(3)	Vss1=−1.55V, all SEGOUTs I$_{OL}$=0.4μA			(Vss2 +0.2	V
Output "H"-level Voltage	V$_{OH}$(4)	Vss1=−1.55V, COM1·COM2 I$_{OH}$=−4μA	−0.2			V
Output "M"-Level Voltage	V$_{OM}$	Vss1=−1.55V, COM1·COM2 I$_{OH}$=−4μA, I$_{OL}$=4μA	(Vss1 −0.2		(Vss1 +0.2	V
Output "L"-Level Voltage	V$_{OL}$(4)	Vss1=−1.55V, COM1·COM2 I$_{OL}$=4μA			(Vss2 +0.2	V
●1/2Bias, 1/3Duty Display						
Output "H"-Level Voltage	V$_{OH}$(3)	Vss1=−1.55V, all SEGOUTs I$_{OH}$=−0.4μA	−0.2			V
Output "L"-Level Voltage	V$_{OL}$(3)	Vss1=−1.55V, all SEGOUTs I$_{OL}$=0.4μA			(Vss2 +0.2	V
Output "H"-Level Voltage	V$_{OH}$(4)	Vss1=−1.55V, COM1·COM2· I$_{OH}$=−4μA　COM3	−0.2			V
Output "M"-Level Voltage	V$_{OM}$	Vss1=−1.55V, COM1·COM2· I$_{OH}$=−4μA, I$_{OL}$=4μA, COM3	(Vss1 −0.2		(Vss1 +0.2	V
Output "L"-Level Voltage	V$_{OL}$(4)	Vss1=−1.55V, COM1·COM2· I$_{OL}$=4μA　COM3			(Vss2 +0.2	V
●1/3Bias, 1/3Duty Display						
Output "H"-Level Voltage	V$_{OH}$(3)	Vss1=−1.55V, all SEGOUTs I$_{OH}$=−0.4μA	−0.2			V
Output "M1"-Level Voltage	V$_{OM}$1-3	Vss1=−1.55V, all SEGOUTs I$_{OH}$=−0.4μA, I$_{OL}$=0.4μA	(Vss1 −0.2		(Vss1 +0.2	V
Output "M2"-Level Voltage	V$_{OM}$2-3	Vss1=−1.55V, all SEGOUTs I$_{OH}$=−0.4μA, I$_{OL}$=0.4μA	(Vss2 −0.2		(Vss2 +0.2	V
Output "L"-Level Voltage	V$_{OL}$(3)	Vss1=−1.55V, all SEGOUTs I$_{OL}$=0.4μA			(Vss3 +0.2	V
Output "H"-Level Voltage	V$_{OH}$(4)	Vss1=−1.55V, COM1·COM2· I$_{OH}$=−4μA　COM3	−0.2			V
Output "M1"-Level Voltage	V$_{OM}$1-4	Vss1=−1.55V, COM1·COM2· I$_{OH}$=−4μA, I$_{OL}$=4μA　COM3	(Vss1 −0.2		(Vss1 +0.2	V
Output "M2"-Level Voltage	V$_{OM}$2-4	Vss1=−1.55V, COM1·COM2· I$_{OH}$=−4μA, I$_{OL}$=4μA　COM3	(Vss2 −0.2		(Vss2 +0.2	V
Output "L"-Level Voltage	V$_{OL}$(4)	Vss1=−1.55V, COM1·COM2· I$_{OL}$=4μA　COM3			(Vss3 +0.2	V
●CMOS Output Port Mode						
Output "H"-Level Voltage	V$_{OH}$(3)	Vss1=−1.55V　Segment I$_{OH}$=−3μA　┌PAD No		−0.3		V
Output "L"-Level Voltage	V$_{OL}$(3)	Vss1=−1.55V　38to41, 44to61 I$_{OL}$=3μA　QIP64 pin No. └11to23, 25to33┘		(Vss2 +0.3		V

Continued from preceding page.

Electrical Characteristics at Ta=25±2°C, V$_{DD}$=0V

Item	Symbol	Condition/Terminal	min	typ	max	unit
● Output Voltage LCD Lighting: 1/3Bias Method						
(doubler)	Vss2	Vss1=−1.35V, fopg=32.768kHz C1toC4=0.1μF　　　　Fig.7			−2.5	V
(tripler)	Vss3	Vss1=−1.35V, fopg=32.768kHz C1toC4=0.1μF　　　　Fig.7			−3.75	V
LCD Lighting: 1/2Bias Method						
(doubler)	Vss2	Vss1=−1.35V, fopg=32.768kHz C1=C2=0.1μF　　　　Fig.2			−2.5	V
● Supply Current (Backup flag is reset.)						
LCD Lighting: 1/3Bias Display	| I$_{DD}$ |	Vss1=−1.55V, HALT mode C1toC4=0.1μF, Cl=25kΩ　Fig.7 Cd=Cg=20pF, 32.768kHz X'tal		3.5		μA
LCD Lighting: Other than 1/3Bias Display	| I$_{DD}$ |	Vss1=−1.55V, HALT mode C1=C2=0.1μF, Cl=25kΩ　Fig.2 Cd=Cg=20pF, 32.768kHz X'tal		2.0		μA
Oscillation Start Voltage V$_{SS1}$	| Vstt |	Cd=Cg=20pF, Cl=25kΩ　Fig.3 32.768kHz X'tal			1.35	V
Oscillation Hold Voltage V$_{SS1}$	| V$_{HOLD}$ |	Cd=Cg=20pF, Cl=25kΩ　Fig.2 32.768kHz X'tal	1.3		1.6	V
Oscillation Start Time	Tstt	Vss1=−1.35V, Cl=25kΩ　Fig.3 Cd=Cg=20pF, 32.768kHz X'tal			10	sec
Oscillation Compensation Capacitance	10P 20P	External terminal OSCOUT	8 16	10 20	12 24	pF pF

※1　S1, S2, S3, S4, M1, M2, M3, M4

Li Specifications

Absolute Maximum Ratings at Ta=25±2℃, VDD=0V

Item	Symbol	Condition/Terminal	Rating	unit
Maximum Supply Voltage	Vss1	VBAK=Vss1 or Vss2	−4.0 to +0.3	V
	Vss2		−4.0 to +0.3	V
	Vss3	(LCD lighting:1/3bias display)	−5.5 to +0.3	V
	Vss3	(LCD lighting:Other than 1/3bias display)	−4.0 to +0.3	V
Maximum Input Voltage	VIN1	10p, OSCIN	$\left(\begin{array}{c} V_{BAK} \\ -0.3 \end{array}\right.$ to +0.3	V
	VIN2	S1-4, M1-4, I/OA1-4, I/OB1-4, INT, TESTA(I/OA1-4, I/OB1-4 are in the input mode.)	$\left(\begin{array}{c} V_{SS2} \\ -0.3 \end{array}\right.$ to +0.3	V
Maximum Output Voltage	Vout1	TEST, OSCOUT	$\left(\begin{array}{c} V_{BAK} \\ -0.3 \end{array}\right.$ to +0.3	V
	Vout2	ALM, LIGHT, P1-4, I/OA1-4, I/OB1-4, CUP2 (I/OA1-4, I/OB1-4 are in the output mode.)	$\left(\begin{array}{c} V_{SS2} \\ -0.3 \end{array}\right.$ to +0.3	V
	Vout3	SEGOUT, COM1toCOM3, CUP1	$\left(\begin{array}{c} V_{SS3} \\ -0.3 \end{array}\right.$ to +0.3	V
Operating Temperature	Topr		−20 to +65	℃
Storage Temperature	Tstg		−30 to +125	℃

Allowable Operating Conditions at Ta=25±2℃, VDD=0V

Item	Symbol	Condition/Terminal	min	typ	max	unit
Supply Voltage	VBAK		−3.6		−1.3	V
	Vss2	VBAK=Vss2/2 (Backup flag is reset.)	−3.6		−2.6	V
	Vss2	VBAK=Vss2 (Backup flag is set.)	−3.6		−1.3	V
	Vss3	(LCD lighting:1/3bias display)	−4.95		−3.7	V
	Vss3	(LCD lighting:Other than 1/3bias display)		Vss3=Vss2		
Input "H"-Level Voltage	VIH	S1-4, M1-4, I/OA1-4, I/OB1-4, INT, (I/OA1-4, I/OB1-4 are in the input mode.)	−0.4		0	V
Input "L"-Level Voltage	VIL	S1-4, M1-4, I/OA1-4, I/OB1-4, INT, (I/OA1-4, I/OB1-4 are in the input mode.)	Vss2		$\left(\begin{array}{c} V_{SS2} \\ +0.4 \end{array}\right.$	V
Operating Frequency	fopg	Ta=−20to+65℃	32		33	kHz

Electrical Characteristics at Ta=25±2℃, VDD=0V

Item	Symbol	Condition/Terminal	min	typ	max	unit
Input Resistance	RIN1A	Vss2=−2.9V, VIL=Vss2+0.4V, "L" level hold Tr *1, Fig.4	10		200	kΩ
	RIN1B	Vss2=−2.9V, pull-down resistor *1, Fig.4	200		2000	kΩ
	RIN2A	Vss2=−2.9V, VIL=Vss2, pull-up resistor for INT	200		2000	kΩ
	RIN2B	Vss2=−2.9V, VIH=VDD, pull-down resistor for INT	200		2000	kΩ
	RIN3	Vss2=−2.9V, VIH=VDD, pull-down resistor for RES	5		50	kΩ

Continued from preceding page.

Electrical Characteristics at Ta=25±2℃, V$_{DD}$=0V

Item	Symbol	Condition/Terminal	min	typ	max	unit
Output "H"-Level Voltage	V$_{OH}$(1)	Vss2=−2.4V, ALM I$_{OH}$=−250μA	−0.65			V
Output "L"-Level Voltage	V$_{OL}$(1)	Vss2=−2.4V, ALM I$_{OL}$=250μA			(Vss2 +0.65	V
Output "H"-Level Voltage	V$_{OH}$(2)	Vss2=−2.9V, I/OA1-4, I/OB1-4, I$_{OH}$=−40μA, P1-4 (I/OA1-4, I/OB1-4 are in the output mode.)	−0.4			V
Output "L"-Level Voltage	V$_{OL}$(2)	Vss2=−2.9V, I/OA1-4, I/OB1-4, I$_{OL}$=40μA, P1-4 (I/OA1-4, I/OB1-4 are in the output mode.)			(Vss2 +0.4	V
Output "H"-Level Voltage	V$_{OH}$(3)	Vss2=−2.9V, LIGHT I$_{OH}$=−150μA	−1.5			V
Output "L"-Level Voltage	V$_{OL}$(3)	Vss2=−2.9V, LIGHT I$_{OL}$=150μA			(Vss2 +1.5	V

Segment Driver Output Impedance
● Static Display

Item	Symbol	Condition/Terminal	min	typ	max	unit
Output "H"-Level Voltage	V$_{OH}$(4)	Vss2=−2.9V, all SEGOUTs I$_{OH}$=−0.4μA	−0.2			V
Output "L"-Level Voltage	V$_{OL}$(4)	Vss2=−2.9V, all SEGOUTs I$_{OL}$=0.4μA			(Vss2 +0.2	V
Output "H"-Level Voltage	V$_{OH}$(5)	Vss2=−2.9V, COM1 I$_{OH}$=−4μA	−0.2			V
Output "L"-Level Voltage	V$_{OL}$(5)	Vss2=−2.9V, COM1 I$_{OL}$=4μA			(Vss2 +0.2	V

● Duplex Display (1/2Bias, 1/2Duty)

Item	Symbol	Condition/Terminal	min	typ	max	unit
Output "H"-Level Voltage	V$_{OH}$(4)	Vss2=−2.9V, all SEGOUTs I$_{OH}$=−0.4μA	−0.2			V
Output "L"-Level Voltage	V$_{OL}$(4)	Vss2=−2.9V, all SEGOUTs I$_{OL}$=0.4μA			(Vss2 +0.2	V
Output "H"-Level Voltage	V$_{OH}$(5)	Vss2=−2.9V, COM1 · COM2 I$_{OH}$=−4μA	−0.2			V
Output "M"-Level Voltage	V$_{OM}$	Vss2=−2.9V, COM1 · COM2 I$_{OH}$=−4μA, I$_{OL}$=4μA	(Vss2/2 −0.2		(Vss2/2 +0.2	V
Output "L"-Level Voltage	V$_{OL}$(5)	Vss2=−2.9V, COM1 · COM2 I$_{OL}$=4μA			(Vss2 +0.2	V

● 1/2Bias, 1/3Duty Display

Item	Symbol	Condition/Terminal	min	typ	max	unit
Output "H"-Level Voltage	V$_{OH}$(4)	Vss2=−2.9V, all SEGOUTs I$_{OH}$=−0.4μA	−0.2			V
Output "L"-Level Voltage	V$_{OL}$(4)	Vss2=−2.9V, all SEGOUTs I$_{OL}$=0.4μA			(Vss2 +0.2	V
Output "H"-Level Voltage	V$_{OH}$(5)	Vss2=−2.9V, COM1 · COM2 · I$_{OH}$=−4μA COM3	−0.2			V
Output "M"-Level Voltage	V$_{OM}$	Vss2=−2.9V, COM1 · COM2 · I$_{OH}$=−4μA, I$_{OL}$=4μA COM3	(Vss2/2 −0.2		(Vss2/2 +0.2	V
Output "L"-Level Voltage	V$_{OL}$(5)	Vss2=−2.9V, COM1 · COM2 · I$_{OL}$=4μA COM3			(Vss2 +0.2	V

● CMOS Output Port Mode

Item	Symbol	Condition/Terminal	min	typ	max	unit
Output "H"-Level Voltage	V$_{OH}$(4)	Vss2=−2.9V Segment I$_{OH}$=−5μA ┌PAD No.		−0.3		V
Output "L"-Level Voltage	V$_{OL}$(4)	Vss2=−2.9V ⎰38to41, 44to61 I$_{OL}$=5μA ⎱FLP64 pin No. └11to23, 25to33┘		(Vss2 +0.3		V

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Electrical Characteristics at Ta=25±2°C, V_DD=0V

Item	Symbol	Condition/Terminal	min	typ	max	unit
● 1/3Bias, 1/3Duty Display						
Output "H"-Level Voltage	V_OH(4)	Vss2=−2.9V, all SEGOUTs IOH=−0.4μA	−0.2			V
Output "M1"-Level Voltage	V_OM1-4	Vss2=−2.9V, all SEGOUTs IOH=−0.4μA, IOL=0.4μA	(Vss2/2 −0.2		(Vss2/2 +0.2	V
Output "M2"-Level Voltage	V_OM2-4	Vss2=−2.9V, all SEGOUTs IOH=−0.4μA, IOL=0.4μA	(Vss2 −0.2		(Vss2 +0.2	V
Output "L"-Level Voltage	V_OL(4)	Vss2=−2.9V, all SEGOUTs IOL=0.4μA			(Vss3 +0.2	V
Output "H"-Level Voltage	V_OH(5)	Vss2=−2.9V, COM1·COM2· IOH=−4μA COM3	−0.2			V
Output "M1"-Level Voltage	V_OM1-5	Vss2=−2.9V, COM1·COM2· IOH=−4μA, IOL=4μA COM3	(Vss2/2 −0.2		(Vss2/2 +0.2	V
Output "M2"-Level Voltage	V_OM2-5	Vss2=−2.9V, COM1·COM2· IOH=−4μA, IOL=4μA COM3	(Vss2 −0.2		(Vss2 +0.2	V
Output "L"-Level Voltage	V_OL(5)	Vss2=−2.9V, COM1·COM2· IOL=4μA COM3			(Vss3 +0.2	V
Output Voltage **LCD Lighting: 1/3Bias Display**						
(halver)	Vss1	Vss2=−2.9V, fopg=32.768kHz C1toC4=0.1μF Fig.8			−1.35	V
(tripler)	Vss3	Vss2=−2.9V, fopg=32.768kHz C1toC4=0.1μF Fig.8			−4.1	V
LCD Lighting: Other than 1/3Bias Display						
(halver)	Vss1	Vss2=−2.9V, fopg=32.768kHz C1=C2=0.1μF Fig.5			−1.35	V
Supply Current (Backup flag is reset.)						
LCD Lighting: 1/3Bias Display	|IDD|	Vss2=−2.9V, HALT mode C1toC4=0.1μF, Cl=25kΩ Fig.8 Cd=Cg=20pF, 32.768kHz X'tal		5.0		μA
LCD Lighting: Other than 1/3Bias Display	|IDD|	Vss2=−2.9V, HALT mode C1=C2=0.1μF, Cl=25kΩ Fig.5 Cd=Cg=20pF, 32.768kHz X'tal		1.0		μA
Oscillation Start Voltage Vss2	|Vstt|	VBAK=Vss2, Cl=25kΩ Fig.6 Cd=Cg=20pF, 32.768kHz X'tal			1.35	V
Oscillation Hold Voltage Vss2 (Backup flag is reset.)	|VHOLD(1)|	VBAK=Vss2/2, Cl=25kΩ Fig.5 Cd=Cg=20pF, 32.768kHz X'tal	2.6		3.6	V
(Backup flag is set.)	|VHOLD(2)|	VBAK=Vss2, Cl=25kΩ Fig.6 Cd=Cg=20pF, 32.768kHz X'tal	1.3		3.6	V
Oscillation Start Time	Tstt	VBAK=Vss2=−2.9V, Cl=25kΩ, Fig.6 Cd=Cg=20pF, 32.768kHz X'tal			10	sec
Oscillation Compensation Capacitance	10P	External terminal	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

※1   S1, S2, S3, S4, M1, M2, M3, M4

Fig. 1 S1-4, M1-4 Input Configuration

Fig. 2 Supply Current, Oscillation
Hold Voltage Test Circuit

Fig. 3 Oscillation Start Voltage,
Oscillation Start Time,
Frequency Stability Test Circuit

Fig. 4 S1-4, M1-4 Input Configuration

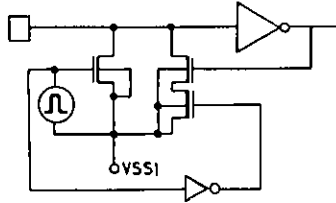Fig. 5 Supply Current, Oscillation Hold
Voltage Test Circuit

Fig. 6 Oscillation Start Voltage
Oscillation Start Time,
Frequency Stability Test circuit

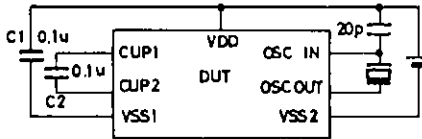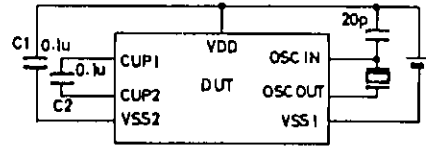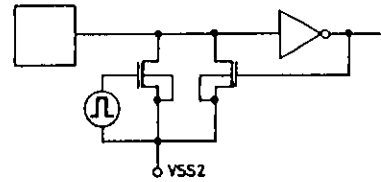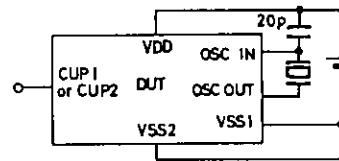Fig. 7 Supply Current, Oscillation Hold
Voltage Test Circuit

Fig. 8 Supply Current, Oscillation Hold
Voltage Test Circuit

Fig. 9 Supply Current, Oscillation Hold
Voltage Test Circuit