LC5851H,5851

CMOS LSI

LCD DRIVER-CONTAINED 4-BIT MICROCOMPUTERS

The LC5851H and LC5851 are 4-bit/single-chip, high-performance microcomputers equipped with LCD drivers. They are produced by CMOS process technology. Their numerous features include low-voltage operation and low current consumption.
A 4-bit parallel-processing ALU, program memory (ROM), data memory (RAM), input and output ports, timer, clock generator, and LCD drivers are integrated on one chip. A total of 79 instructions, including the operation and processing instructions executable in 4-bit units, and various conditional branch instructions and LCD driver data transfer instructions, form an easy-to-use and effective instruction system.
Because there is a halt function (HALT) which stops, thus reduces current to circuits other than the oscillation, divider, LCD driving circuitries, the time-keeping function having very low power dissipation can be easily performed.
These microcomputers are very useful for controlling electronic tuners, cameras, and other portable devices at low voltage, thereby cutting power consumption.

Features

Hardware Features

A wide range of allowable operations

Type No.	Supply option	Cycle time	Range of supply voltage	Remarks
LC5851H	-	122us	V_{SS2}=-2.0 to -5.25V	32k crystal
	-	61us	V_{SS2}=-2.3 to -5.25V	65k crystal
	-	40us	V_{SS2}=-4.0 to -5.25V	200k ceramic
LC5851	Ag	244us	V_{SS1}=-1.30 to -1.65V	32k crystal
	Li	244us	V_{SS2}=-2.6 to -3.6V(Note)	32k crystal
	EXT-V	122us	V_{SS2}=-2.0 to -3.6V	32k crystal

(Note) If the backup flag (refer to the User's Manual) is set,
$V_{SS2}=V_{BAK}$=-1.3 to -3.6V

Notes for developing an LC5800 series microcomputer-used system

The low current dissipation is a distinctive feature of the LC5800 series microcomputers. However, it is not easy to determine the total current to be dissipated in an LC5800 series microcomputer-used system by actual measurement when you develop a software, because much current flows in the peripherals of the evaluation tools.
For a system which require low current dissipation, check the current dissipation using an evaluation sample before mass-producing the system.

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.Micro-current operation
Only micro level current is needed to operate the LC5851/5851H if the HALT function is used efficiently. For example, a typical current requirement may be 1.6 to 7uA(typ) for the Ag specifications, 0.6 to 3uA(typ) for the Li specifications, and 2.8 to 4.0uA(typ) for the EXT-V specifications.
. The actual current required, however, depends on the program structure. The following values are typical for normal clock programs.
3.0uA (typ) ..... Ag specifications(1.5V supply)
1.5uA (typ) ..... Li specifications(3.0V supply)

.The terminals are capable of driving various types of LCD panel.

(25 terminals)

LCD panel	Number of LCD segments
1/3 bias - 1/3 duty	75 segments
1/2 bias - 1/3 duty	75 segments
1/2 bias - 1/2 duty	50 segments
Static	25 segments

.The built-in segment PLA circuit is capable of joining the LCD driver outputs to any patterns on the LCD panel without software.
.A number of input and output terminals are provided.
Input port: 2 ports/8 pins (With a chatter removal circuit)
Input/output port: 2 ports/8 pins
Output port: 1 port/4 pins (Also used as the pseudo-serial output port)
Control output terminal: 2 pins
.The LCD panel drive output terminal can be switched to the output-only port (mask option).
.An initial reset terminal is provided.
.ROM: 1024 x 15 bits
.RAM: 64 x 4 bits
.Built-in oscillation circuit for crystal oscillation or ceramic resonator oscillation (Oscillation circuit for ceramic resonator is provided only in the LC5851H.)
.Built-in voltage doubler/halver circuits for the LCD power source.
.Form of shipment: QIP64 (or chip)

Software Features

.As many as 79 instructions.
.Binary addition/subtraction and logical operation.
.Input and output instructions in 4-bit units.
.Conditional branch instructions.
.8 working registers and operation instructions.
.LCD driver data transfer instructions.
.4-level subroutine nesting (common with interrupts)
.Interrupt function ... External source: 2 (INT terminal, input ports S and M)
Internal source: 2 (Timer, frequency divider circuit)
.HALT/HOLD release functions ... The HALT release is caused by the same elements as in interrupt.
.Built-in 6-bit programmable timer.
.Built-in 15-bit clock frequency divider circuit.
.All instructions are executable in one machine cycle.

Application Development Tools

.Relations between power specifications for cycle time and evaluation chip

Cycle Time	Evaluation Chip	LC5851				LC5851H		Oscillation Frequency	Machine Cycle (option)	Version	Target Board
		Ag/Li		EXTV							
		Use	IDD(typ)	Use	IDD(typ)	Use	IDD(typ)				
40μ	LC5895H	×	—	×	—	○	50to100uA	200kHz	OSC/8	—	TB5851
81μ	LC5895H	×	—	×	—	○	20to50uA	65.536kHz	OSC/4	—	
122μ	LC5895H	×	—	×	—	○	10to20uA	32.768kHz	OSC/4	—	
122μ	LC5895G	×	—	○	3to20uA	×	—	32.768kHz	—	G	TB51
244μ	LC5895F	○	2to6uA(Ag) 0.6to3uA(Li)	○	3to20uA	×	—	32.768kHz	—	F	

Table 1. Relations between power specifications for cycle time and evaluation chip

Note) The I_{DD} (typ) value is determined by the contents of the software.

Note) LC5895F ... Evaluation chip for the LC5851F
LC5895G ... Evaluation chip for the LC5851G
LC5895H ... Evaluation chip for the LC5851H

An evaluation chip (LC5895) for application development and dedicated boards for the application development tools will be provided.

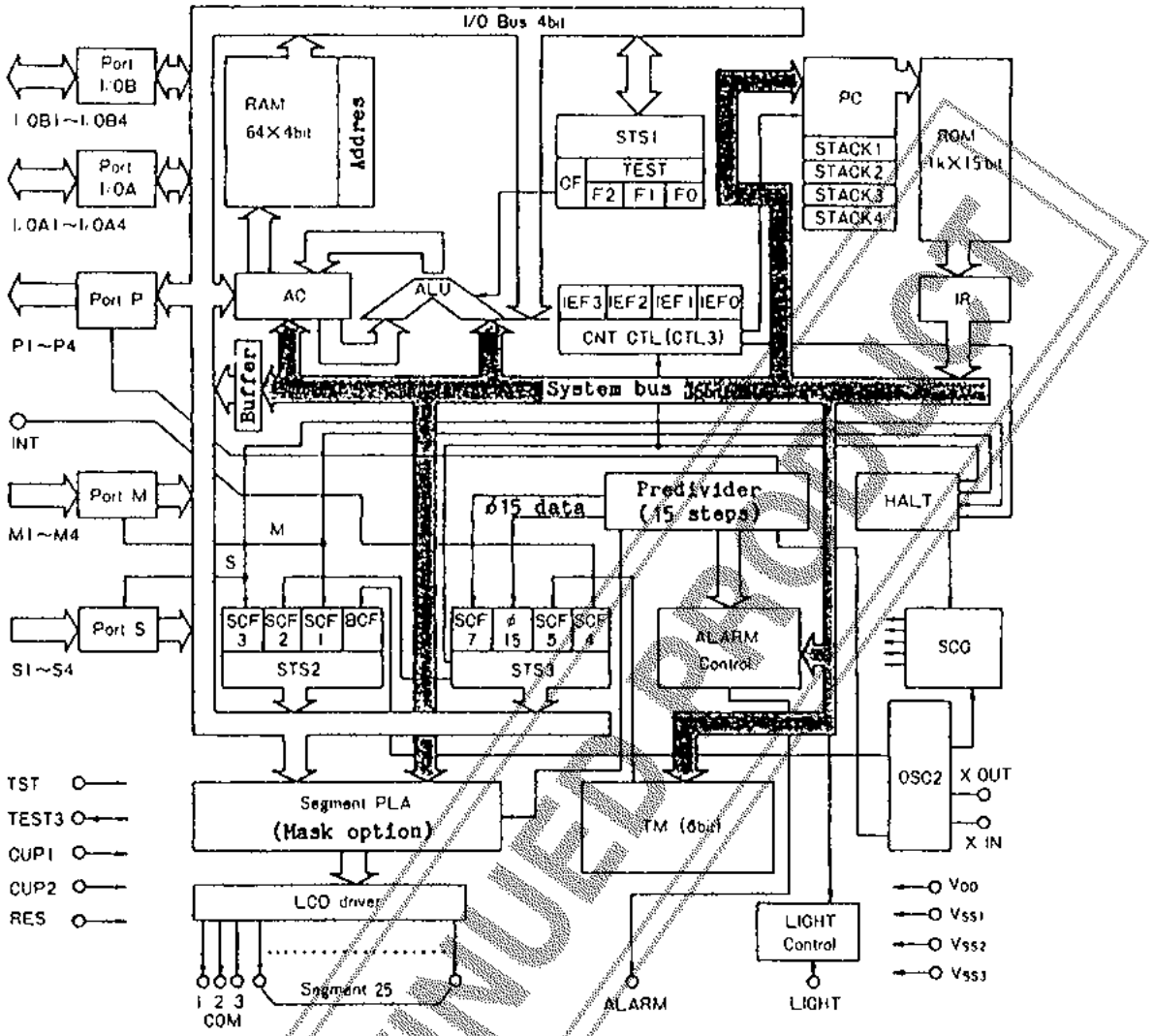
.SDS410 system (CP/M-80)
Enables the user to create an application development program for microcomputer in assembler language (edit, assemble).
(A microcomputer equivalent to the IBM-PC can be used to develop a software.)

.For the LC5851 (LED drive use)
.EVA-510 + EVA-TB51C + Application Evaluation Board + LC5895F/G
Modification and debugging of the application development program are possible by connecting to the SDS410.
.EVA-TB51 + Application Evaluation Board + LC5895F/G
Installation evaluation (evaluation by LED) is possible using the EPROM (2732) in which the data for the application development program is contained.

.For the LC5851H (LED or LCD drive use)
.EVA-510 + TB-5851 + DCB-1 + Application Evaluation Board + LC5895H
Modification and debugging of the application development program are possible by connecting to the SDS410.
.TB-5851 + DCB-1 + Application Evaluation Board + LC5895H
Installation evaluation is possible using the EPROM (2732) in which the data for the application development program is contained.

Note) The application evaluation board is created by the user.
The EVA-510 is a control ROM-replaced version of the EVA-410.

Equivalent Circuit Block Diagram



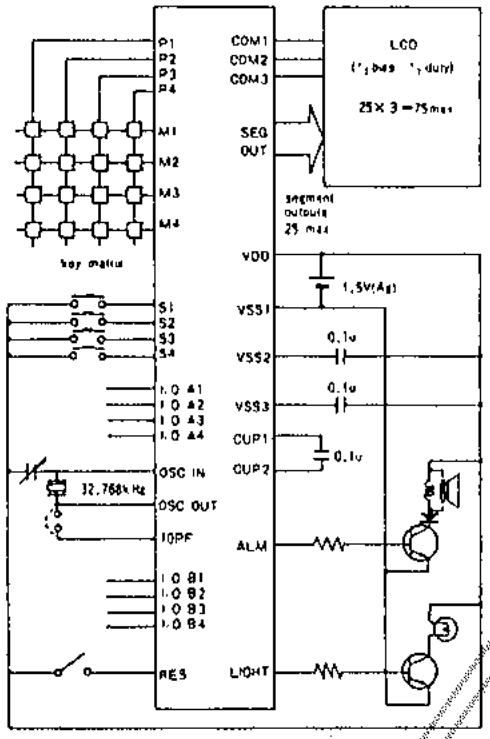
AC	: Accumulator	CF	: Carry flag
ALU	: Arithmetic and logic unit	BCF	: Backup flag
INT CTL	: Interrupt control circuit	SCF1	: M port flag
PC	: Program counter	SCF2	: STS3 flag
TM	: Preset timer (6 bits)	SCF3	: S port flag
IR	: Instruction register	SCF4	: INT signal change flag
HALT	: Intermittent control circuit	SCF5	: Timer overflow flag
SCG	: System clock generator	ϕ15	: Content of 15th step of divider
STS1	: Status register 1	SCF7	: Overflow flag of divider
STS2	: Status register 2		
STS3	: Status register 3		

Application Examples

- Portable equipment (timer, watch, clock, hand-held calculator, and thermometer)
- Audio equipment (electronic controller, electronic tuning controller, and clock)
- Home appliances (remote control, and timer control)
- Telephone (dial/clock display)

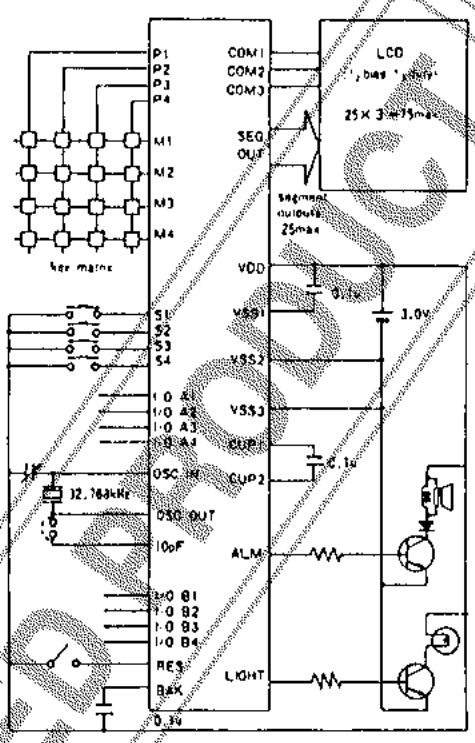
Application Circuit Examples

(1) Typical application circuit for the Ag specifications (1/3 bias - 1/3 duty)

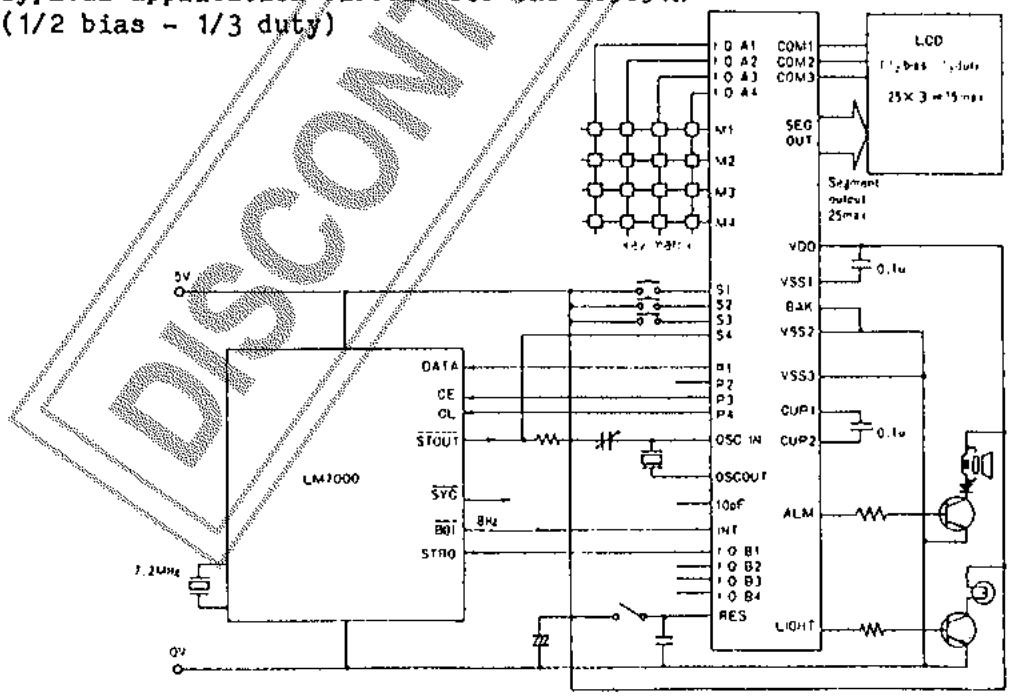


INPUT OUTPUT PORT	I/O A1~4 I/O B1~4
INPUT PORT	S1~4, M1~4
OUTPUT PORT	P1~4

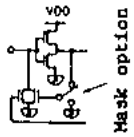
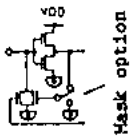
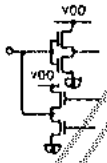
(2) Typical application circuit for the Li specifications (1/2 bias - 1/3 duty)



(3) Typical application circuit for the LC5851H (1/2 bias - 1/3 duty)



Terminal Description

Terminal Name	Input/ Output	Circuit Configuration	Function	Option	Status after Reset
OSC IN OSC OUT	Input Output		Used as the reference clock and system clock.	① Terminals for crystal oscillator (XT option) ② Terminals for ceramic resonator oscillator (CF option) The CF option is available only for the LC5851H.	
IOP			Used as an oscillation phase compensating capacitor by connecting it to OSCOUT or OSCIN. Used for chip only.		
S1 S2 S3 S4	Input		Input-only port. Contains a ø8 (8 ms) or ø6 (2 ms) chatter-removal circuit. (PLA mask option) (ø6 can be used only for the LC5851H.) *The values are for 32.768 kHz crystal oscillation.	Selection of "L" level Hold Tr. Chatter-removal time is either ø8 or ø6. (ø6 can be used only for the LC5851H.) $ø_N$ indicates the output at the Nth step of the frequency divider circuit.	Transistor for pull-down resistance is ON.
M1 M2 M3 M4	Input		Input terminals for writing data in RAM.	Selection of "L" level Hold Tr.	Transistor for pull-down resistance is ON.
I/O A1 I/O A2 I/O A3 I/O A4	Input/ Output		Input/output port with mode switched by instructions to perform the following operations: ① Input port: Writes data in RAM. ② Output port: Outputs data from RAM.		Input mode
P1 P2 P3 P4	Output		Output-only port		"H" or "L" output (not fixed).
INT	Input		Control input port for external interrupt request.	① Pull-up resistor ② Pull-down resistor ③ Fall trigger ④ Rise trigger	

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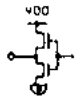
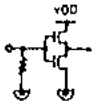
Terminal Name	Input/ Output	Circuit Configuration	Function	Option	Status during Reset
BAK			(-) supply voltage terminal for the logic section of LSI circuit. In the Li specifications a capacitor is provided between BAK and V_{DD} to prevent malfunction at the logic section.		Backup flag is set/ reset depending on the power source option.
LIGHT	Output		Output-only port. Suitable for delivering signal to drive high-current driving transistor.		"L" output
ALM	Output		Output-only port. Able to output 4kHz-2kHz or 4kHz-1kHz modulating signals according to instructions as well as nonmodulating signals. *The value is for 32.768kHz crystal oscillation.	① Modulating signal (4kHz, 2kHz, Nonmodulaing) ② Modulating signal (4kHz, 1kHz, Nonmodulaing) Optin ② is a special specification.	"L" output
RES	Input		System reset terminal. Sets the program counter to address 00. "H" level signal should be input for one or more machine cycles in the stable oscillation state.		
V_{DD}			(+) supply voltage terminal.		
V_{SS3} V_{SS2} V_{SS1}			(-) supply voltage terminal. . Connection of external device varies according to the mask option: The(-) terminal is connected to V_{SS1} for the Ag specifications. The (-) terminal is connected to V_{SS2} for other specifications. . Terminals other than the (-) terminal are used as the source supply for the LCD drive.	LC5851 ① Ag specifications/ ② Li specifications/ ③ EXT-V specifications LC5851H No options are available.	
CUP1 CUP2			Connection terminals for voltage doubler (halver) capacitor.		

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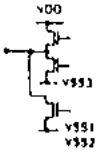
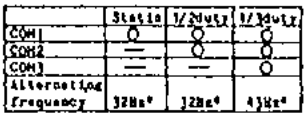
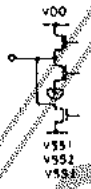
Terminal Name	Input/ Output	Circuit Configuration	Function	Option	Status during Reset
COM1 COM2 COM3	Output		Output terminals for common plate of LCD panel. Use of terminals varies.  *The values are for 32.768kHz crystal oscillation. *1/2 or double of the frequency can be used depending on the PLA.	① LCD driving specification .Static, duplex, .1/2bias-1/3duty .1/3bias-1/3duty ② Alternating frequency specification (The following values are for the 32.768kHz system clock.) .16Hz, 32Hz, 64Hz	
Segment driver (Only for 3 terminals)	Output		LCD panel segment output terminal. .The terminal can be switched to the output-only port by mask option (See the Option Instruction Sheet for the terminals to be used.) .During the LSI system reset, the static lighting signal is fed to COM1 to COM3 and to each of the LCD segment outputs, and all LCD panel segments go on. .The segment PLA system is used to provide any layout of the LCD panel. *The values are for 32.768kHz crystal oscillation.	① Output for LCD ② CMOS output port ③ Nch open drain output port Options ①, ②, and ③ can be selected in bit units.	Full lighting (for LCD) "H" level (except for LCD)=Nonaction state
Segment driver (For other terminals)	Output		LCD panel segment output terminal. .The terminal can be switched to the output port by mask option. .If the LSI system is reset, the static lighting signal is fed to COM1 to COM3 and to each of the LCD segment outputs, and all LCD panel segments go on. .The segment PLA system is used to provide any layout of the LCD panel. *The values are for 32.768kHz crystal oscillation.	① Output for LCD / ② CMOS output port / Options ① and ② can be selected in bit units.	Full lighting (for LCD) "H" level (except for LCD) = Nonaction state

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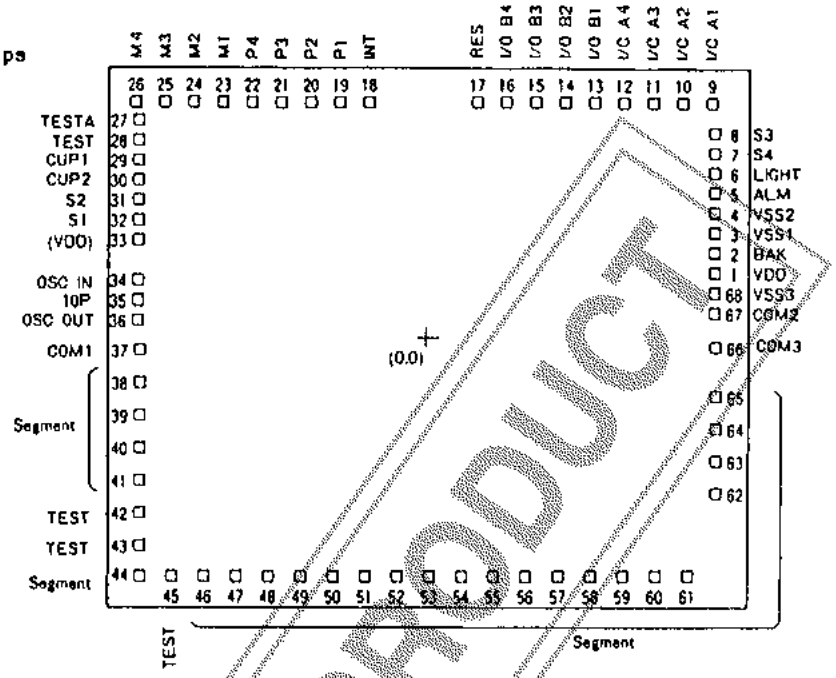
Terminal Name	Input/ Output	Circuit Configuration	Function	Option	Status during Reset
TEST TEST TESTA TEST TEST TEST			Terminals for test (not used by the users)		
(V_{DD})			Auxiliary supply voltage terminal. Do not use the terminal.		

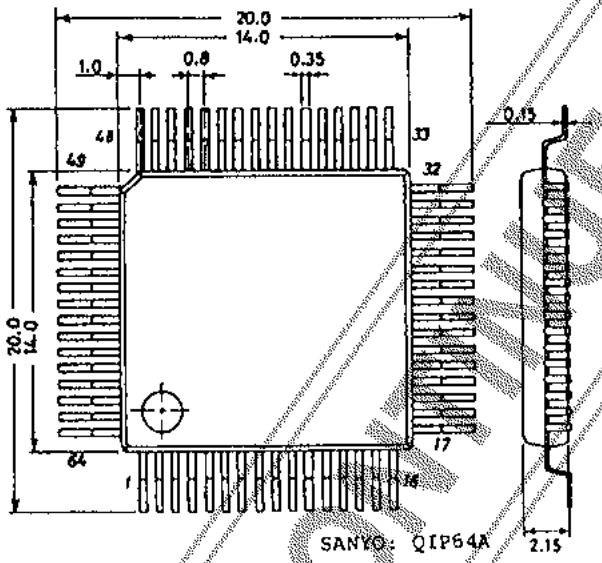
Remarks: ⏚ Ag specifications: V_{SS1} Li specifications, EXT-V specifications: V_{SS2}

Pad Assignment on LSI Chip

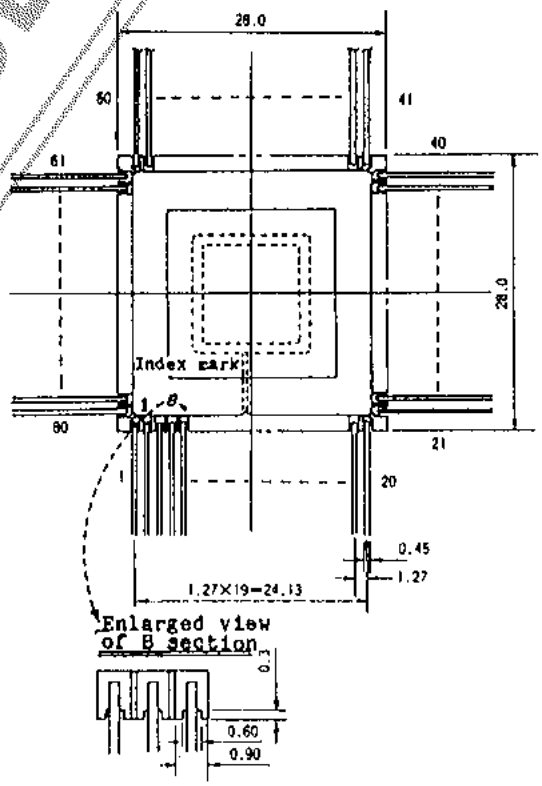
Reference data for the shipment of chips
Chip size: 5.72mm x 4.76mm
Chip thickness: 480um
Pad size: 120um x 120um



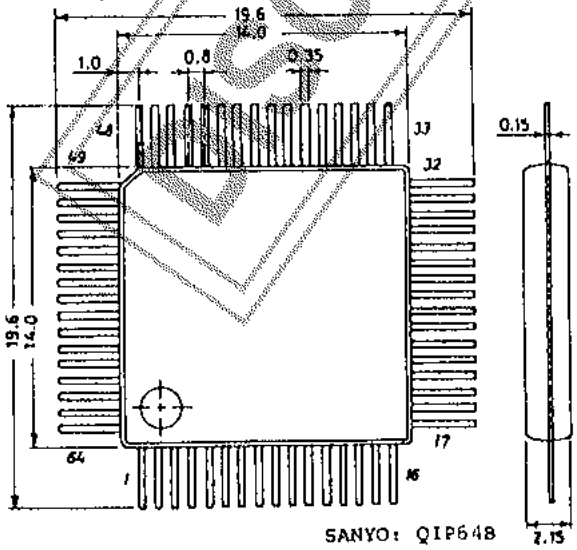
Case Outline 3057-Q64AIC
(unit:mm)



Case Outline QIC-80(for ES sample)
(unit:mm)



Case Outline 3026B-Q64BIC
(unit:mm)



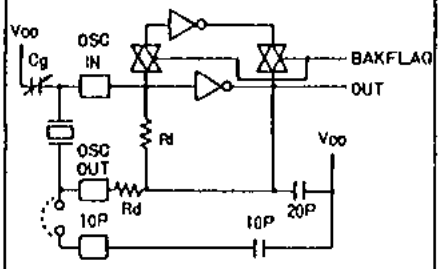
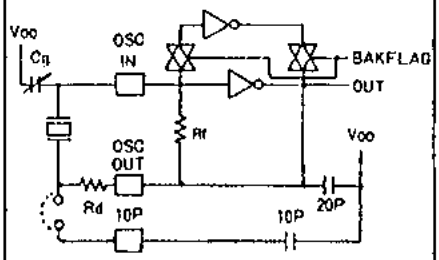
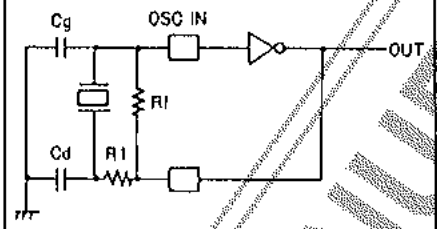
Pin Assignment

Pad Name and Coordinates

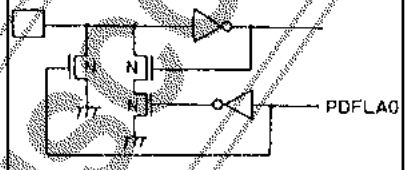
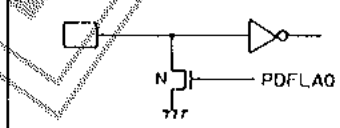
QIC80/ Pin Assignment	QIP64/Pin Assignment	Pad No	Terminal Symbol	X (μm)	Y (μm)	QIC80/ Pin Assignment	QIP64/Pin Assignment	Pad No	Terminal Symbol	X (μm)	Y (μm)
10	40	1	VDD	2707	869	50	8	34	OSC IN	−2707	608
11	41	2	BAK	2707	878	51	—	35	10PF	−2707	428
12	42	3	VSS1	2707	1058	52	9	36	OSC OUT	−2707	248
13	43	4	VSS2	2707	1238	53	10	37	COM1	−2707	−36
14	44	5	ALM	2707	1418	54	11	38	Segment	−2707	−324
15	45	6	LIGHT	2707	1589	55	12	39	Segment	−2707	−630
16	46	7	S4	2707	1778	56	13	40	Segment	−2707	−936
17	47	8	S3	2707	1958	57	14	41	Segment	−2707	−1242
18	48	9	I/O A1	2707	2228	—	—	42	TEST	−2707	−1611
22	49	10	I/O A2	2385	2228	—	—	43	TEST	−2707	−1899
23	50	11	I/O A3	2070	2228	62	15	44	Segment	−2707	−2228
24	51	12	I/O A4	1800	2228	—	—	45	TEST	−2446	−2238
25	52	13	I/O B1	1530	2228	63	16	46	Segment	−2140	−2228
26	53	14	I/O B2	1260	2228	64	17	47	Segment	−1834	−2228
27	54	15	I/O B3	990	2228	65	18	48	Ssgment	−1528	−2228
28	55	16	I/O B4	720	2228	66	19	49	Segment	−1222	−2228
29	56	17	RES	450	2228	67	20	50	Segment	−916	−2228
31	57	18	INT	−362	2228	68	21	51	Segment	−610	−2228
32	58	19	P1	−681	2228	69	22	52	Segment	−304	−2228
33	59	20	P2	−1007	2228	70	23	53	Segment	2	−2228
34	60	21	P3	−1331	2228	71	25	54	Segment	308	−2228
35	61	22	P4	−1656	2228	72	26	55	Segment	614	−2228
36	62	23	M1	−1926	2228	73	27	56	Segment	920	−2228
37	63	24	M2	−2176	2228	74	28	57	Segment	1226	−2228
38	64	25	M3	−2430	2228	75	29	58	Segment	1532	−2228
41	1	26	M4	−2707	2228	76	30	59	Segment	1838	−2228
42	2	27	TESTA	−2707	2048	77	31	60	Segment	2144	−2228
43	3	28	TEST	−2707	1868	78	32	61	Segment	2450	−2228
44	4	29	CUP1	−2707	1688	3	33	62	Segment	2707	−1382
45	5	30	CUP2	−2707	1508	4	34	63	Segment	2707	−1087
46	6	31	S2	−2707	1149	5	35	64	Segment	2707	−792
47	7	32	S1	−2707	968	6	36	65	Segment	2707	−496
—	—	33	TEST(VDD)	−2707	788	7	37	66	COM3	2707	−15
						8	38	67	COM2	2707	309
						9	39	68	VSS3	2707	489

- Pin 24 on the QIP package is NC. (Use the NC pin in the open position.)
- The pad coordinates are determined with the center of thes chip as origin. The values for (X,Y) are the coordinates for the center of each pad.
- QIC80 is available only for ES.
- Use the terminals for test in the open position.
- When selecting the chip, connect the substrate to V_{DD}

Oscillation Circuit Options

Option	Circuit	Remarks:
XT oscillation (32.768kHz)		.The 10P terminal can be used only for chip selection.
XT oscillation (65kHz)		.The 10P terminal can be used only for chip selection. .Used for the cycle time 61u version of the LC5851H.
CF oscillation		.This option is available only for the LC5851H.

Input Port Options

Option	Circuit	Remarks:
Hold Tr		.The Hold Tr option is used to reduce the current required, for example, for a pushbutton switch for S1, or a slide switch for S2. .For example, the "L" level signal can be held after the pull-down resistor is set to ON for a short period of time by software in case of open type of input port.
Open		.Pull-down Tr can be used as a pull-down resistor. .Pull-down Tr can be set to ON/OFF by software.

"L" level Hold Tr can be selected for ports S1 to S4 and M1 to M4.

- Port S has an indepedent chatter-removal circuit (in bit units) that operates at ø8 period. (The option for the ø6 period is provided for the LC5851H.)
- Port M has a chatter-removal circuit that operates upon receipt of the HALT release request signal. With this circuit, chatter at ø8 period is removed when three ports are in the "L" level and any signal to other port changes. (The option for the ø6 period is provided for the LC5851H, but it is interlocked to the S port.)
  Note that $ø_N$ indicates the output at the Nth step of the oscillation frequency divider circuit. If a 32.768kHz oscillator is used,
  ø6 ... About 2msec.
  ø8 ... About 8msec.

LCD Output Options

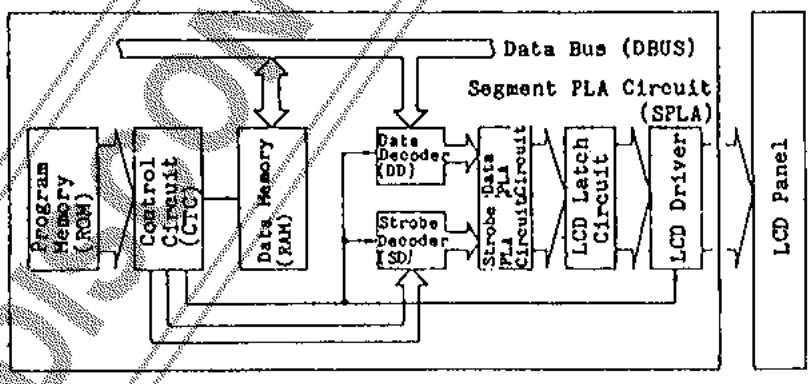
LCD output options for the LCD driver, the CMOS output port and the Pch open drain output port can be selected (the Pch open drain option can be specified only for the predetermined 3 bits).

Option	Output Form
LCD drive	. Terminal for LCD segment drive. . The drive is selected according to the LCD driving system specified separately. . The LCD driving system is common to all terminals, and can be selected from among the static, duplex, 1/2 bias - 1/3 duty, and 1/3 bias - 1/3 duty methods.
CMOS output port	. General-purpose CMOS type output port
Pch open drain output port	. General-purpose Pch open drain type output port It's usable according to the PLA option for the predetermined three ports. Usable ports ... Pad No. 63 to 65 (Pin No 34 to 36)

Alternating waveform for the LCD driver for LCD output is generated by hardware logic.

Segment PLA Circuit

A schema of the structure of the segment PLA circuit is shown below.



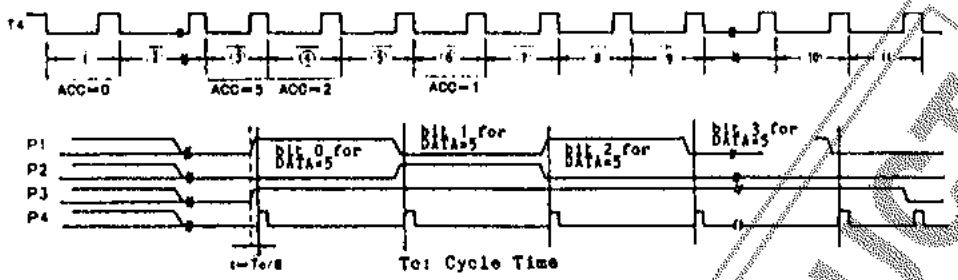
The contents of the Data Memory are sent through to the LCD Latch Circuit for display as is or after being decoded by the Data Decoder. The PLA Circuit is used to rearrange the input data to output it to the LCD latches. With this circuit, data memory can be edited to suit to the LCD panel specifications without software processing. The PLA circuit can be specified by the ROM for PLA. The user must release the ROM for PLA with the program ROM.

Output Port P

The following two modes can be selected by software:

1) General-purpose output port
2) Pseudo-serial output port

The time chart in the Pseudo-Serial mode is shown below:



①, ② ..... Initial processing for serial data transfer.
③, ⑤, ⑦, ⑨, ... The first and the second bits of the RAM data are output to ports P1 and P2, respectively.
④, ⑥, ⑧ ..... RAM data is shifted to the right.

As shown above, the RAM data can be transferred in 1-bit serial data form every two machine cycles. (For this, however, it is necessary to process (e.g., replace) the RAM data every 4-bit transfer.)

Alarm Output

The following frequency divider output can be used directly as alarm output:

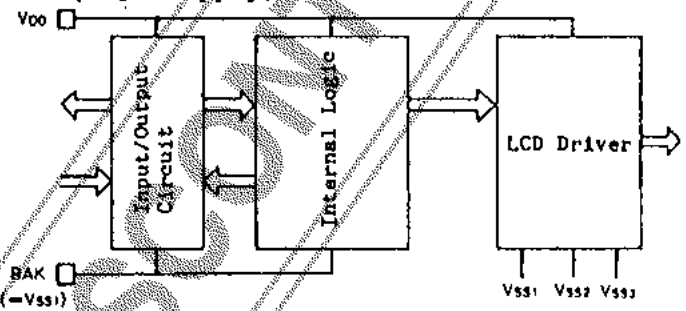
1) Output signal either at ϕ3, ϕ4 (or ϕ5)
2) Any combination output signal at ϕ10, ϕ11, ϕ12, ϕ13, ϕ14 and ϕ15.
3) Modulating output signal of 1) or 2).

These signals can be output by software.
ϕ_N indicates the output at the Nth step of the oscillator frequency divider.

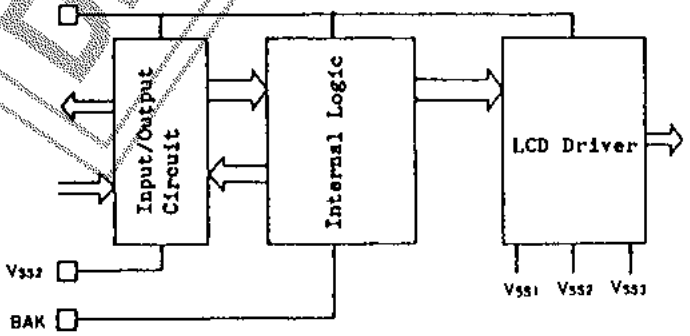
Operation Mode of Internal Logic

.The following diagram shows the supply voltages and the operation levels of internal logic.

Ag specifications(1.5V supply)

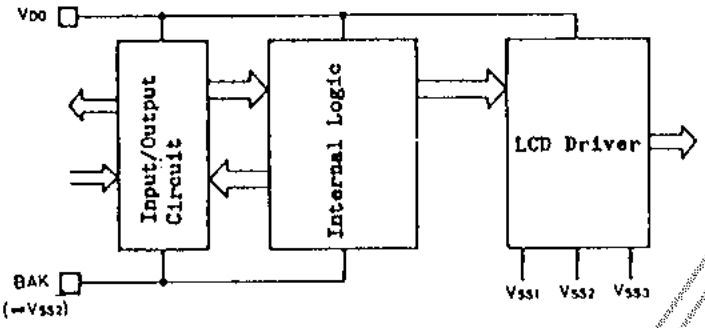


Li specifications(3V supply)



The BAK terminal is connected to V_{SS1} or V_{SS2} by software.
It is, however, connected to V_{SS2} after the initial clear is issued.

・EXT-V specifications (3V supply)



.LC5851H(3 to 5V supply)
Same as EXT-V of the LC5851.

・The level of voltage applied to BAK is shown below.

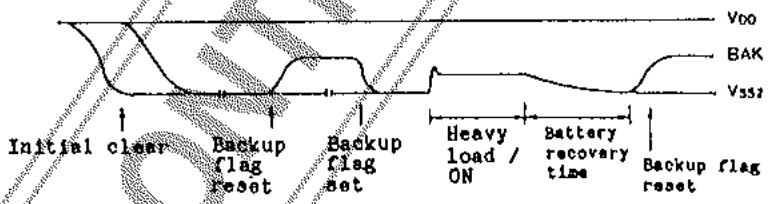
	Power source option	BAK terminal level		Input /output port	Relations between V_{SS1}, V_{SS2}, and V_{SS3}
		Normal mode	Backup mode		
LC5851	Ag	VSS1	VSS1	VDD-VSS1	VSS2≈VSS1×2 VSS3=VSS2 (other than 1/3bias) VSS3≈VSS1×3 (1/3bias)
	Li	VSS1	VSS2	VDD-VSS2	
	EXT-V	VSS2	VSS2	VDD-VSS2	
LC5851H	—	VSS2	VSS2	VDD-VSS2	

*The LCD output used as general-purpose port is included.

・The backup mode is called by setting the backup flag by software, and the normal mode is reinstated by resetting the flag.

Backup Mode

1) The backup mode is useful with Li specificaitons to prevent malfunctions of LSI circuits under heavy load.
An example of a time chart is shown below.
Power source option ... Li specificaions



Heavy Load Operation Timing

.To prevent a sudden change at BAK, a smoothing capacitor must be inserted between BAK and V_{DD}.

2) In the Ag and Li specificaons, the backup mode is called with an initial clear. The reason is:
Ag specifications ... To shorten the oscillation start time of the crystal oscillator circuit.
Li specifications ... To start oscillation by applying supply voltage to the oscillator.
Be sure to reset the backup flag to return to normal mode, after the initial clear is released.
The backup-mode-related elements enter the following.

Power Source Specifications	Backup Flag	Oscillator Inverter Size	BAK Terminal	Current Required
Ag	Set	Large	Connected to V_{SS1} (Fixed)	Becomes large.
Li	Set	Large	Brought to V_{SS2} level	"
EXTV	Reset	Small	Connected to V_{SS2} (Fixed)	As usual
LC5851H	Reset	Small	"	"

Operation of Backup Flag at Initial Clear Mode

3) The current required in backup mode is 20 to 40 times that for normal mode. Therefore, be sure to reset the backup flag except when necessary. For the LC5851 EXTV and the LC5851H, it is unnecessary to set the backup flag.

Resetting Internal Logic

There are three functions for resetting internal logic:

1. On-chip power-ON clear function ... Use of this option can be determined by the mask option.
2. Reset terminal RES
3. Simultaneous operation of S1 to S4
   Either option 2 or 3 can be specified (mask option).

These reset functions are explained below.

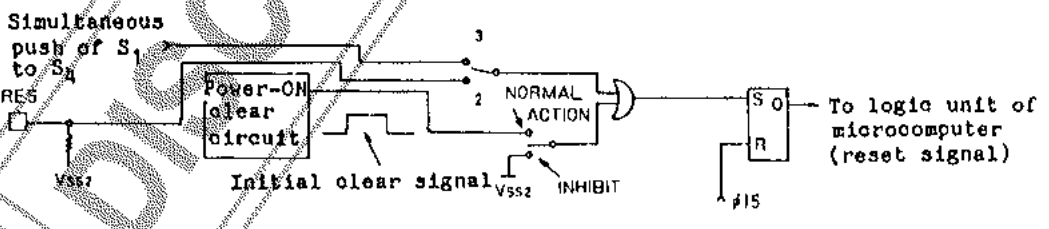
1) Built-in power-ON clear circuit
   The initial clear circuit provided in the microcomputer automatically operates and resets internal logic when power is turned on. This function is very useful in that it can be activated without external devices, but it has the two disadvantages listed below. It is, therefore, recommended that this function be used with other reset functions or that other methods be used according to applications.

   a) The circuit may not operate under certain power-rise conditions during the power-ON sequence or due to chatter.
   b) Malfunctions may take place due to pulse noise in V_{DD} port or a sudden change in status.

   One of the following two reset options can be selected:

   INHIBIT: The built-in power-ON clear circuit is not used.
   ... Malfunction due to pulse noise in V_{DD} port can be prevented.

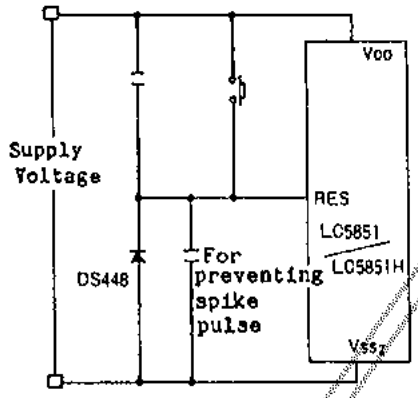
   NORMAL ACTION: The built-in power-ON clear circuit is used.
   ... This option should be selected only when pulse noise in the power does not affect.



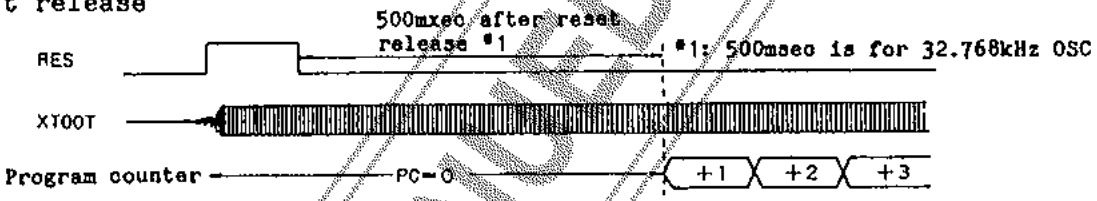
The built-in power-ON clear function in LSI circuits may not work under certain power-rise conditions. Use an external reset switch (the reset terminal or simulataneous operation of S1 to S4).

2) To activate the initial clear function completely with the reset terminal, the following conditions must be satisfied:
   ① Oscillation must be normal.
   ② The "H" level signal must be applied for at least one machine cycle.

A example of the reset circuit is shown below.



Reset release



Even with this circuit, the above two requisites may not be satisfied due to the power-rise conditions or oscillation start time, and therefore the power-ON clear function may not work. To prevent this, an external reset switch should be used.

3) The same requisites as in 2) must be satisfied for the simultaneous operation of S1 to S4. If the timing for applying signals to S1 to S4 (i.e., the timing for signals changing from "H" to "L" levels) is not even, the microcomputer starts operating according to the built-in program.

Option List

		LC5851	LC5851H	Remarks:
Power Select		Ag specifications Li specifications EXT-V specifications		
LCD lighting		Static Duplex 1/2 bias – 1/3 duty 1/3 bias – 1/3 duty Non use	Static Duplex 1/2 bias – 1/3 duty 1/3 bias – 1/3 duty Non use	Select "non use" if all LCD outputs are to be used as general-purpose ports.
LCD Frequency		SLOW (16Hz) TYP (32Hz) FAST (64Hz)	SLOW (OSC/2048Hz) TYP (OSC/1024Hz) FAST (OSC/512Hz)	
"L" level HOLD Tr	S PORT (S1~S4)	Use "L"-level hold Tr Not use "L"-level hold Tr	Use "L"-level hold Tr Non use "L"-level hold Tr	
	M PORT (M1~M4)	Use "L"-level hold Tr Non use "L"-level hold Tr	Use "L"-level hold Tr Non use "L"-level hold Tr	
S,M port chatter-removal frequency		TYP (256Hz)	TYP (OSC/256Hz) FAST (OSC/64Hz)	
ALARM signal modulating reference frequency		• TYP (4kHz, 2kHz) • SLOW (4kHz, 1kHz)	TYP (OSC/8, OSC/16Hz) SLOW (OSC/8, OSC/32Hz)	
External reset		• RES terminal • Simultaneous operation of S1 to S4	• RES terminal • Simultaneous operation of S1 to S4	
Built-in power-ON clear function		• Used • Not used	• Used • Not used	
Cycle Time		F version (244μs) G version (122μs)	SLOW (OSC/8) FAST (OSC/4)	Select SLOW at 200kHz ceramic resonator mode
INT terminal	Input resistance	• Pull-up • Pull-down • Open		
	Signal change	• Rise • Fall		
Internal timer clock		• 244μsec	• SLOW (OSC/512) • FAST (OSC/8)	
Oscillator configuration		• 32.768kHz use	• 32.768kHz use } Crystal • 65.536kHz use } • 200kHz use Ceramic	

LC5851H

Absolute Maximum Ratings at Ta=25°C, V_{DD}=0V

				unit
Maximum Supply Voltage	V_{SS1}		-5.5 to +0.3	V
	V_{SS2}		-5.5 to +0.3	V
	V_{SS3}		-8.25 to +0.3	V
Maximum Input Voltage	V_{IN1}		V_{SS2} -0.3 to +0.3	V
Maximum Output Voltage	V_{OUT1}	ALM,LIGHT,P1to4,CUP2,OSCOUT, TEST,I/O A1-4,I/O B1-4,(I/OA, I/OB: output mode.)	V_{SS2} -0.3 to +0.3	V
	V_{OUT2}	SEGOUT,COM1-COM3,CUP1	V_{SS3} -0.3 to +0.3	V
Operating Temperature	Topg		-20 to +70	°C
Storage Temperature	Tstg		-30 to +125	°C

Allowable Operating Conditions at Ta=-20to+70°C, V_{DD}=0V

			min	typ	max	unit
Supply Voltage	V_{SS1}	32kHz crystal mode	-5.25		-1.3	V
	V_{SS2}		-5.25		-2.0	V
	V_{SS3}		-8.0		-2.0	V
Supply Voltage	V_{SS1}	65kHz crystal mode	-5.25		-1.3	V
	V_{SS2}		-5.25		-2.3	V
	V_{SS3}		-8.0		-2.3	V
Supply Voltage	V_{SS1}	External input mode	-5.25		-1.7	V
	V_{SS2}		-5.25		-3.5	V
	V_{SS3}		-8.0		-3.5	V
Supply Voltage	V_{SS1}	200kHz CF mode	-5.25		-2.0	V
	V_{SS2}		-5.25		-4.0	V
	V_{SS3}		-8.0		-4.0	V
Input "H"-Level Voltage	V_{IH1}	All input terminals except OSCIN	0.3x V_{SS2}		0	V
Input "L"-level Voltage	V_{IL1}		V_{SS2}		0.7x V_{SS2}	V
Input "H"-level Voltage	V_{IH2}	OSCIN terminal, external input mode	0.2x V_{SS2}		0	V
Input "L"-level Voltage	V_{IL2}		V_{SS2}		0.8x V_{SS2}	V
Operating Frequency	fopg1	V_{SS2}=-2.0to-5.25V, OSCIN/OSCOUT, 32kHz crystal, Fig.2	32		66	kHz
Operating Frequency	fopg2	V_{SS2}=-2.3to-5.25V, OSCIN/OSCOUT, 65kHz crystal, Fig.2	60		66	kHz
Operating Frequency	fopg3	V_{SS2}=-3.5to-5.25V, OSCIN, external input, Fig.8	32		220	kHz
Operating Frequency	fopg4	V_{SS2}=-4.0to-5.25V, OSCIN/OSCOUT, CF OSC mode, Fig.1	180	200	220	kHz

Electrical Characteristics (LC5851H) at Ta=-20to+70°C, V_{DD}=0V				min	typ	max	unit
Input Resistance	R_{IN}1A	V_{SS2}=-2.9V V_{IN}=0.8V_{SS2}	"L" level hold Tr *1, Fig.3	10		200	kohm
	R_{IN}1B	V_{SS2}=-2.9V V_{IN}=V_{DD}	"L" level pull-in Tr *1, Fig.3	200	700	2000	kohm
	R_{IN}2A	V_{SS2}=-2.9V V_{IN}=V_{SS2}	Resistance for INT pull-up	200	700	2000	kohm
Input Resistance	R_{IN}2B	V_{SS2}=-2.9V V_{IN}=V_{DD}	Resistance for INT pull-down	200	700	2000	kohm
	R_{IN}3	V_{SS2}=-2.9V V_{IN}=V_{DD} or V_{SS2}	RES	5		50	kohm
Output "H"-Level Voltage	V_{OH}(1)	V_{SS2}=-2.4V I_{OH}=-1mA	ALM	-1	-0.3		V
Output "L"-Level Voltage	V_{OL}(1)	V_{SS2}=-2.4V I_{OL}=1mA	ALM		V_{SS2} +0.3	V_{SS2} +1	V
Output "H"-Level Voltage	V_{OH}(2)	V_{SS2}=-2.4V I_{OH}=-0.3mA	LIGHT,port P	-1	-0.3		V
Output "L"-Level Voltage	V_{OL}(2)	V_{SS2}=-2.4V I_{OL}=0.5mA	LIGHT,port P		V_{SS2} +0.3	V_{SS2} +1	V
Output "H"-Level Voltage	V_{OH}(3)	V_{SS2}=-2.4V I_{OH}=-0.1mA	I/O port	-1	-0.3		V
Output "H"-Level Voltage	V_{OH}(4)	V_{SS2}=-2.4V I_{OH}=-50uA	I/O port	-0.6	-0.2		V
Output "L"-Level Voltage	V_{OL}(4)	V_{SS2}=-2.4V I_{OL}=0.1mA	I/O port		V_{SS2} +0.3	V_{SS2} +1	V
Segment Driver Output Impedance							
• **CHOS Output Port Mode**							
Output "H"-Level Voltage	V_{OH}(5)	V_{SS2}=-2.4V I_{OH}=-10uA	Segment PAD No.63to65 QIP64 pin No. 34to46	-1	-0.3		V
Output "L"-Level Voltage	V_{OL}(5)	V_{SS2}=-2.4V I_{OL}=100uA			V_{SS2} +0.3	V_{SS2} +1	V
Output "H"-Level Voltage	V_{OH}(6)	V_{SS2}=-2.4V I_{OH}=-5uA	Segment PAD No. 38to41,46to62 QIP64 pin No. 11to14,16to33	-1	-0.3		V
Output "L"-Level Voltage	V_{OL}(6)	V_{SS2}=-2.4V I_{OL}=20uA			V_{SS2} +0.3	V_{SS2} +1	V
• **PCH Open Drain Output Port Mode**							
Output "H"-Level Voltage	V_{OH}(5)	V_{SS2}=-2.4V I_{OH}=-10uA	Segment PAD No.63to65 QIP64 pin No. 34to36	-1	-0.3		V
Output OFF-State Leakage Current	I_{OFF}	V_{SS2}=-2.4V I_{OL}=V_{SS2}				1	uA
• **Static Display**							
Output "H"-Level Voltage	V_{OH}(5)	V_{SS2}=-2.4V I_{OH}=-0.4uA	All segments	-0.2			V
Output "L"-Level Voltage	V_{OL}(5)	V_{SS2}=-2.4V I_{OL}=0.4uA				V_{SS2} +0.2	V
Output "H"-Level Voltage	V_{OH}(7)	V_{SS2}=-2.4V I_{OH}=-4uA	COM1	-0.2			V
Output "L"-Level Voltage	V_{OL}(7)	V_{SS2}=-2.4V I_{OL}=4uA				V_{SS2} +0.2	V

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			min	typ	max	unit
• Duplex Display (1/2Bias, 1/2Duty)						
Output "H"-Level Voltage	$V_{OH}(5)$	V_{SS2}=-2.4V, I_{OH}=-0.4uA	-0.2			V
Output "L"-Level Voltage	$V_{OL}(5)$	V_{SS2}=-2.4V, I_{OL}=0.4uA	All segments		V_{SS2} +0.2	V
Output "H"-Level Voltage	$V_{OH}(7)$	V_{SS2}=-2.4V, I_{OH}=-4uA	-0.2			V
Output "M"-Level Voltage	V_{OM}	V_{SS2}=-2.4V, I_{OH}=-4uA, I_{OL}=4uA	$V_{SS2}/2$ -0.2		$V_{SS2}/2$ +0.2	V
Output "L"-Level Voltage	$V_{OL}(7)$	V_{SS2}=-2.4V, I_{OL}=4uA	COM1-2		V_{SS2} +0.2	V
• 1/2Bias, 1/3Duty Display						
Output "H"-Level Voltage	$V_{OH}(5)$	V_{SS2}=-2.4V, I_{OH}=-0.4uA	-0.2			V
Output "L"-Level Voltage	$V_{OL}(5)$	V_{SS2}=-2.4V, I_{OL}=0.4uA	All segments		V_{SS2} +0.2	V
Output "H"-Level Voltage	$V_{OH}(7)$	V_{SS2}=-2.4V, I_{OH}=-4uA, I_{OL}=4uA	-0.2			V
Output "M"-Level Voltage	V_{OM}	V_{SS2}=-2.4V, I_{OH}=-4uA, I_{OL}=4uA	COM1-3 $V_{SS2}/2$ -0.2		$V_{SS2}/2$ +0.2	V
Output "L"-Level Voltage	$V_{OL}(7)$	V_{SS2}=-2.4V, I_{OL}=4uA			V_{SS2} +0.2	V
• 1/3Bias, 1/3Duty Display						
Output "H"-Level Voltage	$V_{OH}(5)$	V_{SS2}=-2.4V, I_{OH}=-0.4uA	-0.2			V
Output "M"-Level Voltage	$V_{OM}1$-1	V_{SS2}=-2.4V, I_{OH}=-0.4uA	$V_{SS2}/2$ -0.2		$V_{SS2}/2$ +0.2	V
	$V_{OM}1$-2	I_{OL}=0.4uA	All segments V_{SS2} -0.2		V_{SS2} +0.2	V
Output "L"-Level Voltage	$V_{OL}(5)$	V_{SS2}=-2.4V, I_{OL}=0.4uA			V_{SS3} +0.2	V
Output "H"-Level Voltage	$V_{OH}(7)$	V_{SS2}=-2.4V, I_{OH}=-4uA	-0.2			V
Output "M"-Level Voltage	$V_{OM}2$-1	V_{SS2}=-2.4V, I_{OH}=-4uA	COM1-3 $V_{SS2}/2$ -0.2		$V_{SS2}/2$ +0.2	V
	$V_{OM}2$-2	I_{OL}=4uA	V_{SS2} -0.2		V_{SS2} +0.2	V
Output "L"-Level Voltage	$V_{OL}(7)$	V_{SS2}=-2.4V, I_{OL}=4uA			V_{SS3} +0.2	V

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			min	typ	max	unit
Input Resistance	$R_{IN}1A$	V_{SS2}=-5.0V "L" level hold V_{IN}=0.8V_{SS2} Tr, *1, Fig.3	10	45	150	kohm
	$R_{IN}1B$	V_{SS2}=-5.0V Pull-in "L" level V_{IN}=V_{DD} Tr, *1, Fig.3	100	350	1000	kohm
	$R_{IN}2A$	V_{SS2}=-5.0V Resistance for V_{IN}=V_{SS2} INT pull-up	100	350	1000	kohm
	$R_{IN}2B$	V_{SS2}=-5.0V Resistance for V_{IH}=V_{DD} INT pull-down	100	350	1000	kohm
	$R_{IN}3$	V_{SS2}=-5.0V RES V_{IH}=V_{DD}orV_{SS2}	10	20	50	kohm
Output "H"-Level Voltage	$V_{OH}(1)$	V_{SS2}=-3.5Vto -5.25V ALM I_{OH}=-1.5mA	-1	-0.3		V
Output "L"-Level Voltage	$V_{OL}(1)$	V_{SS2}=-3.5Vto -5.25V ALM I_{OL}=1.5mA		V_{SS2} +0.3	V_{SS2} +1	V
Output "H"-Level Voltage	$V_{OH}(2)$	V_{SS2}=-3.5Vto -5.25V LIGHT,port P I_{OH}=0.5mA	-1	-0.3		V
Output "L"-Level Voltage	$V_{OL}(2)$	V_{SS2}=-3.5Vto -5.25V LIGHT,port P I_{OL}=0.7mA		V_{SS2} +0.3	V_{SS2} +1	V
Output "H"-Level Voltage	$V_{OH}(3)$	V_{SS2}=-3.5Vto -5.25V I/O port I_{OH}=-0.13mA	-1	-0.3		V
Output "H"-Level Voltage	$V_{OH}(4)$	V_{SS2}=-3.5Vto -5.25V I/O port I_{OH}=-50uA	-0.6	-0.2		V
Output "L"-Level Voltage	$V_{OL}(4)$	V_{SS2}=-3.5Vto -5.25V I/O port I_{OL}=0.13mA		V_{SS2} +0.3	V_{SS2} +1	V
Segment Driver Output Impedance						
• CMOS Output Port Mode						
Output "H"-Level Voltage	$V_{OH}(5)$	V_{SS2}=-3.5Vto -5.25V Segment [PAD No.63to65 QIP64 pin No. 34to36] I_{OH}=-15uA	-1	-0.3		V
Output "L"-Level Voltage	$V_{OL}(5)$	V_{SS2}=-3.5Vto -5.25V I_{OL}=150uA		V_{SS2} +0.3	V_{SS2} +1	V
Output "H"-Level Voltage	$V_{OH}(6)$	V_{SS2}=-3.5Vto -5.25V Segment [PAD No. 38to41,46to62 QIP64 pin No. 11to14,16to33] I_{OH}=-10uA	-1	-0.3		V
Output "L"-Level Voltage	$V_{OL}(6)$	V_{SS2}=-3.5Vto -5.25V I_{OL}=60uA		V_{SS2} +0.3	V_{SS2} +1	V
• PCH Open Drain Output Port						
Output "H"-Level Voltage	$V_{OH}(5)$	V_{SS2}=-3.5Vto -5.25V Segment [PAD No.63to65 QIP64 pin No. 34to46] I_{OH}=-15uA	-1	-0.3		V
Output OFF-State Leakage Current	I_{OFF}	V_{SS2}=-3.5Vto -5.25V V_{OL}=V_{SS2}			1	uA

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				min	typ	max	unit
• Static Display							
Output "H"-Level Voltage	$V_{OH}(5)$	V_{SS2}=-3.5Vto -5.25V, I_{OH}=-0.4uA	All segments	-0.2			V
Output "L"-Level Voltage	$V_{OL}(5)$	V_{SS2}=-3.5Vto -5.25V, I_{OL}=0.4uA	All segments			V_{SS2} +0.2	V
Output "H"-Level Voltage	$V_{OH}(7)$	V_{SS2}=-3.5Vto -5.25V, I_{OH}=-4uA	COM1	-0.2			V
Output "L"-Level Voltage	$V_{OL}(7)$	V_{SS2}=-3.5Vto -5.25V, I_{OL}=4uA	COM1			V_{SS2} +0.2	V
• Duplex Display (1/2Bias, 1/2Duty)							
Output "H"-Level Voltage	$V_{OH}(5)$	V_{SS2}=-3.5Vto -5.25V, I_{OH}=-0.4uA	All segments	-0.2			V
Output "L"-Level Voltage	$V_{OL}(5)$	V_{SS2}=-3.5Vto -5.25V, I_{OL}=0.4uA	All segments			V_{SS2} +0.2	V
Output "H"-Level Voltage	$V_{OH}(7)$	V_{SS2}=-3.5Vto -5.25V, I_{OH}=-4uA	COM1-2	-0.2			V
Output "M"-Level Voltage	$V_{OM}2\text{-}1$	V_{SS2}=-3.5Vto -5.25V, I_{OH}=-4uA, I_{OL}=4uA	COM1-2	$V_{SS}2/2$ -0.2		$V_{SS}2/2$ +0.2	V
Output "L"-Level Voltage	$V_{OL}(7)$	V_{SS2}=-3.5Vto -5.25V, I_{OL}=4uA	COM1-2			V_{SS2} +0.2	V
• 1/2Bias, 1/3Duty Display							
Output "H"-Level Voltage	$V_{OH}(5)$	V_{SS2}=-3.5Vto -5.25V, I_{OH}=-0.4uA	All segments	-0.2			V
Output "L"-Level Voltage	$V_{OL}(5)$	V_{SS2}=-3.5Vto -5.25V, I_{OL}=0.4uA	All segments			V_{SS2} +0.2	V
Output "H"-Level Voltage	$V_{OH}(7)$	V_{SS2}=-3.5Vto -5.25V, I_{OH}=-4uA	COM1-3	-0.2			V
Output "M"-Level Voltage	$V_{OM}2\text{-}1$	V_{SS2}=-3.5Vto -5.25V, I_{OH}=-4uA, I_{OL}=4uA	COM1-3	$V_{SS}2/2$ -0.2		$V_{SS}2/2$ +0.2	V
Output "L"-Level Voltage	$V_{OL}(7)$	V_{SS2}=-3.5Vto -5.25V, I_{OL}=4uA	COM1-3			V_{SS2} +0.2	V

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• 1/3Bias, 1/3Duty Display				min	typ	max	unit
Output "H"-Level Voltage	$V_{OH}(5)$	V_{SS2}=-3.5Vto-5.25V I_{OH}=-0.4uA		-0.2			V
Output "M"-Level Voltage	$V_{OM}1-1$	V_{SS2}=-3.5Vto-5.25V I_{OH}=-0.4uA		$V_{SS}2/2$ -0.2		$V_{SS}2/2$ +0.2	V
	$V_{OM}1-2$	I_{OL}=0.4uA	All segments	V_{SS2} -0.2		V_{SS2} +0.2	V
Output "L"-Level Voltage	$V_{OL}(5)$	V_{SS2}=-3.5Vto-5.25V I_{OL}=0.4uA				V_{SS3} +0.2	V
Output "H"-Level Voltage	$V_{OH}(7)$	V_{SS2}=-3.5Vto-5.25V I_{OH}=-4uA		-0.2			V
Output "M"-Level Voltage	$V_{OM}2-1$	V_{SS2}=-3.5Vto-5.25V I_{OH}=-4uA	COM1-3	$V_{SS}2/2$ -0.2		$V_{SS}2/2$ +0.2	V
	$V_{OM}2-2$	I_{OL}=4uA		V_{SS2} -0.2		V_{SS2} +0.2	V
Output "L"-Level Voltage	$V_{OL}(7)$	V_{SS2}=-3.5Vto-5.25V I_{OL}=4uA				V_{SS3} +0.2	V
Power Supply Leakage Current	I_{LEK}	V_{SS2}=V_{SS3}=-4.5V Ta=25°C				10	uA
Input Leakage Current	I_{IN}	V_{SS2}=-2.0to4.5V V_{IN}=V_{SS2}toV_{DD}		-1		1	uA
Output Voltage	V_{SS1}	V_{SS2}=-2.9V	C1=C2=C3=0.1uF fopg=32.768kHz Ta=25°C Fig.7		-1.45	-1.35	V
	V_{SS3}	V_{SS2}=-2.9V			-4.35	-4.1	V
Output Voltage	V_{SS1}	V_{SS2}=-4.5V	C1=C2=C3=0.1uF fopg=32.768kHz Ta=25°C, Fig.7		-2.25	-2.2	V
	V_{SS3}	V_{SS2}=-4.5V			-6.70	-6.6	V
Supply Current	$\lvert I_{DD}1\rvert$	V_{SS2}=-2.9V Ta=25°C HALT mode	C1=C2=0.1uF CI=25kohms fopg=32.768kHz Cg=20pF		3.0	5	uA
	$\lvert I_{DD}2\rvert$	V_{SS2}=-4.5V Ta=25°C,HALT mode			10	20	uA
		Static: Fig.9, 1/3B.1/3D: Fig.7, others: Fig.4					
Supply Current	$\lvert I_{DD}3\rvert$	V_{SS2}=-4.5V Ta=25°C HALT mode	C1=C2=0.1uF CI=25kohms fopg=65.536kHz Cg=10pF		20	50	uA
		Static: Fig.9, 1/3B.1/3D: Fig.7, others: Fig.4					
Supply Current	$\lvert I_{DD}4\rvert$	V_{SS2}=-4.5V Ta=25°C HALT mode	C1=C2=0.1uF CI=25kohms,Fig.6 fopg=200kHz Cg=180pF,330pF		100	300	uA

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			min	typ	max	unit
Oscillation Hold Voltage	$V_{HOLD}1$	Ta=25°C C1=C2=0.1uF,CI=25kohms, fopg=32.768kHz,Cg=20pF Static: Fig.9, 1/3B.1/3D: Fig.7, others: Fig.4	2.0		5.25	V
Oscillation Hold Voltage	$V_{HOLD}2$	Ta=25°C C1=C2=0.1uF,CI=25kohms fopg=65.536kHz,Cg=10pF Static: Fig.10, 1/3B.1/3D: Fig.7, others: Fig.4	2.3		5.25	V
Oscillation Start Voltage	$V_{stt}1$	Ta=25°C C1=C2=0.1uF,CI=25kohms,Fig.5, fopg=32.768kHz,Cg=20pF			2.2	V
Oscillation Start Voltage	$V_{stt}2$	Ta=25°C C1=C2=0.1uF,CI=25kohms,Fig.5, fopg=65.536kHz,Cg=10pF			2.6	V
Oscillation Start Time	Tstt1	V_{SS2}=-2.9V,C1=C2=0.1uF Ta=25°C CI=25kohms,Fig.5 V_{SS2}=-4.5V,fopg=32.768kHz Ta=25°C Cg=20pF			10 10	s s
Oscillation Start Time	Tstt2	V_{SS2}=-2.9V C1=C2=0.1uF Ta=25°C CI=25kohms,Fig.5, V_{SS2}=-4.5V fopg=65.536kHz Ta=25°C Cg=10pF			10 10	s s
Oscillation Start Voltage	Vstt4	Ta=25°C fopg=200kHz Fig.6, Cg=Cd=180pF,330pF			4.0	V
Oscillation Hold Time	$V_{HOLD}4$	Ta=25°C fopg=200kHz,Fig.6, 3.5 Cg=Cd=180pF,330pF			5.25	V
Oscillation Start Time	$T_{stt}4$	V_{SS2}=-4.5V fopg=200kHz,Fig.6 Ta=25°C Cg=Cd=180pF,330pF		50	500	ms
Oscillation Compsensation Capacitance	10p	V_{SS2}=-2.9V 10p terminal (for chip only)		10		pF
	10p	V_{SS2}=-4.5V 10p terminal (for chip only)		10		pF
	20p	V_{SS2}=-2.9V OSCOUT terminal		20		pF
	20p	V_{SS2}=-4.5V OSCOUT terminal		20		pF

*1 S1,S2,S3,S4 M1,M2,M3,M4

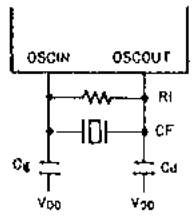


Fig.1 Ceramic Resonator Oscillation (200kHz)

CF: Ceramic resonator

Item	Rf	Cg	Cd
CSB200 (Murata)	1 MΩ	330pF	330pF
KBR-200H (Kyocera)	1 MΩ	180pF	180pF

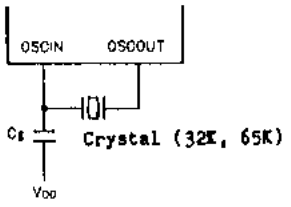


Fig.2 Crystal Oscillation (32kHz,65kHz)

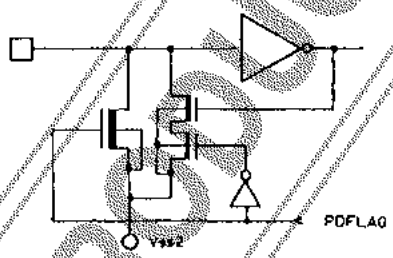


Fig.3 Input Configuration of S1 to S4, M1 to M4

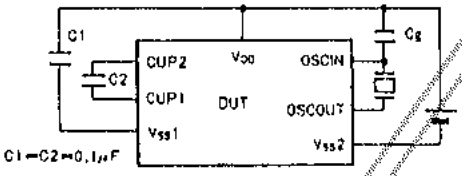


Fig.4 Supply Current, Oscillation Hold Voltage Test Circuit

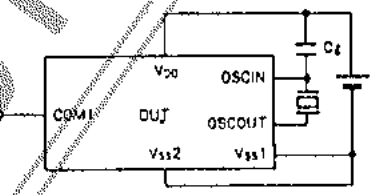
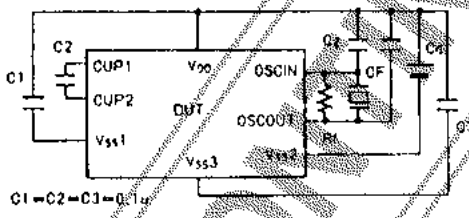


Fig.5 Oscillation Start Voltage, Oscillation Start Time, Frequency Stability Test Circuit



Note: Connect C3 at 1/3bias mode.

Fig.6 Oscillation Start Voltage, Oscillation Start Time, Supply Current, Oscillation Hold Voltage Test Circuit

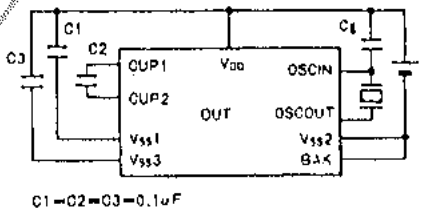


Fig.7 Supply Current, Oscillation Hold Voltage, Test Circuit

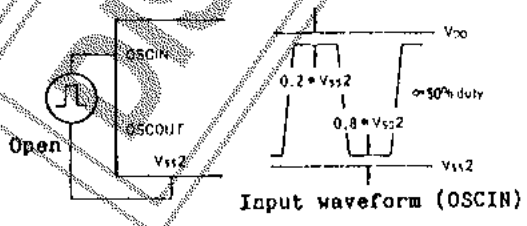


Fig.8 External Input Mode

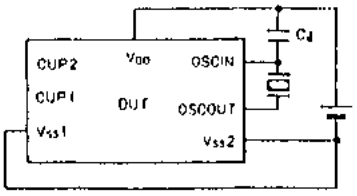


Fig.9 Supply Current, Oscillation Hold Voltage Test Circuit

LC5851

Ag Specifications

Absolute Maximum Ratings at Ta=25°C, V_{DD}=0V

				unit
Maximum Supply Voltage	V_{SS1}		-4.0to+0.3	V
	V_{SS2}		-4.0to+0.3	V
	V_{SS3}	(LCD lighting: 1/3bias display)	-5.5to+0.3	V
	V_{SS3}	(LCD lighting: Other than 1/3 bias display)	-4.0to+0.3	V
Maximum Input Voltage	V_{IN1}	S1-4,M1-4,I/OA1-4,I/OB1-4,INT, TESTA(I/OA1-4 and I/OB1-4 are in the input mode. 10P,OSCIN,RES, BAK	V_{SS1} to+0.3 -0.3	V
Maximum Output Voltage	Vout1	ALM,LIGHT,P1-4,I/OA1-4, I/OB1-4,CUP2(I/OA1-4,I/OB1-4 are in the output mode.) TEST,OSCOUT	V_{SS1} to+0.3 -0.3	V
	Vout3	SEGOUT,COM1toCOM3,CUP1	V_{SS3} to+0.3 -0.3	V
Operating Temperature			-20to+65	°C
Storage Temperature			-30to+125	°C

Allowable Operating Conditions at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Supply Voltage	V_{SS1}	$V_{BAK}=V_{SS1}$	-1.65		-1.3	V
	V_{SS2}		-3.3		-2.4	V
	V_{SS3}	(LCD lighting: 1/3bias display)	-4.95		-3.7	V
	V_{SS3}	(LCD lighting: Other than 1/3bias display)		$V_{SS3}=V_{SS2}$		
Input "H"-Level Voltage	V_{IH}	S1-4,M1-4,I/OA1-4,I/OB1-4, INT,(I/OA1-4,I/OB1-4 are in the input mode.)	-0.2		0	V
Input "L"-Level Voltage	V_{IL}	S1-4,M1-4,I/OA1-4,I/OB1-4, INT,(I/OA1-4,I/OB1-4 are in the input mode.)	V_{SS1}		V_{SS1} +0.2	V
Operating frequency	fopg	Ta=-20to+65°C	32		33	kHz

Electrical Characteristics [LC5851] at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Input Resistance	$R_{IN}1A$	V_{SS1}=-1.55V,"L"level hold Tr $V_{IL}=V_{SS2}$+0.2V *1, Fig.1	10		200	kohm
	$R_{IN}1B$	V_{SS1}=-1.55V,pull-down resistor *1, Fig.1	200		2000	kohm
	$R_{IN}2A$	V_{SS1}=-1.55V,pull-up resistor for INT $V_{IL}=V_{SS2}$	200		2000	kohm
	$R_{IN}2B$	V_{SS1}=-1.55V,pull-up resistor for INT $V_{IH}=V_{DD}$	5		50	kohm
	$R_{IN}3$	V_{SS1}=-1.55V,pull-down resistor for RES $V_{IH}=V_{DD}$	5		50	kohm
Input "H"-Level Voltage	$V_{OH}(1)$	V_{SS1}=-1.35V,ALM,LIGHT I_{OH}=-250uA	-0.65			V
Input "L"-Level Voltage	$V_{OL}(1)$	V_{SS1}=-1.35V,ALM,LIGHT I_{OL}=250uA			V_{SS1} +0.65	V
Input "H"-Level Voltage	$V_{OH}(2)$	V_{SS1}=-1.55V,I/OA1-4, I/OB1-4,I_{OH}=-20uA,P1-4 (I/OA1-4,I/OB1-4 are in the output mode.)	-0.2			V

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			min	typ	max	unit
Input "L"-Level Voltage	$V_{OL}(2)$	V_{SS1}=-1.55V,I/OA1-4,I/OB1-4, I_{OH}=20uA,P1-4(I/OA1-4,I/OB1-4 are in the output mode.)			V_{SS1} +0.2	V

Segment Driver Output Impedance

			min	typ	max	unit
• Static Display						
Output "H"-Level Voltage	$V_{OH}(3)$	V_{SS1}=-1.55V,SEGOUT I_{OH}=-0.4uA	-0.2			V
Output "L"-Level Voltage	$V_{OL}(3)$	V_{SS1}=-1.55V,SEGOUT I_{OL}=0.4uA			V_{SS2} +0.2	V
Output "H"-Level Voltage	$V_{OH}(4)$	V_{SS1}=-1.55V,COM1 I_{OH}=-4uA	-0.2			V
Output "L"-Level Voltage	$V_{OL}(4)$	V_{SS1}=-1.55V,COM1 I_{OL}=4uA			V_{SS2} +0.2	V
• Duplex Display(1/2Bias,1/2Duty)						
Output "H"-Level Voltage	$V_{OH}(3)$	V_{SS1}=-1.55V,all SEGOUTs I_{OH}=-0.4uA	-0.2			V
Output "L"-Level Voltage	$V_{OL}(3)$	V_{SS1}=-1.55V,all SEGOUTs I_{OL}=0.4uA			V_{SS2} +0.2	V
Output "H"-Level Voltage	$V_{OH}(4)$	V_{SS1}=-1.55V,COM1.COM2 I_{OH}=-4uA	-0.2			V
Output "M"-Level Voltage	V_{OM}	V_{SS1}=-1.55V,COM1.COM2 I_{OH}=-4uA,I_{OL}=4uA	V_{SS1} -0.2		V_{SS1} +0.2	V
Output "L"-Level Voltage	$V_{OL}(4)$	V_{SS1}=-1.55V,COM1.COM2 I_{OL}=4uA			V_{SS2} +0.2	V
• 1/2Bias, 1/3Duty Display						
Output "H"-Level Voltage	$V_{OH}(3)$	V_{SS1}=-2.9V,all SEGOUTs I_{OH}=-0.4uA	-0.2			V
Output "L"-Level Voltage	$V_{OL}(3)$	V_{SS1}=-2.9V,all SEGOUTs I_{OL}=0.4uA			V_{SS2} +0.2	V
Output "H"-Level Voltage	$V_{OH}(4)$	V_{SS1}=-2.9V,COM1.COM2.COM3 I_{OH}=-4uA	-0.2			V
Output "M"-Level Voltage	V_{OM}	V_{SS1}=-2.9V,COM1.COM2.COM3 I_{OH}=-4uA I_{OL}=4uA	V_{SS1} -0.2		V_{SS1} +0.2	V
Output "L"-Level Voltage	$V_{OL}(4)$	V_{SS1}=-2.9V,COM1.COM2.COM3 I_{OL}=4uA			V_{SS2} +0.2	V
• 1/3Bias, 1/3Duty Display						
Output "H"-Level Voltage	$V_{OH}(3)$	V_{SS1}=-1.55V,all SEGOUTs I_{OH}=-0.4uA	-0.2			V
Output "M1"-Level Voltage	$V_{OM}1-3$	V_{SS1}=-1.55V,all SEGOUTs I_{OH}=-0.4uA,I_{OL}=0.4uA	V_{SS1} -0.2		V_{SS1} +0.2	V
Output "M2"-Level Voltage	$V_{OM}2-3$	V_{SS1}=-1.55V,all SEGOUTs I_{OH}=-0.4uA,I_{OL}=0.4uA	V_{SS2} -0.2		V_{SS2} +0.2	V
Output "L"-Level Voltage	$V_{OL}(3)$	V_{SS1}=-1.55V,all SEGOUTs I_{OL}=0.4uA			V_{SS3} +0.2	V
Output "H"-Level Voltage	$V_{OH}(4)$	V_{SS1}=-1.55V,COM1.COM2.COM3 I_{OH}=-4uA	-0.2			V
Output "M1"-Level Voltage	$V_{OM}1-4$	V_{SS1}=-1.55V,COM1.COM2.COM3 I_{OH}=-4uA,I_{OL}=4uA	V_{SS1} -0.2		V_{SS1} +0.2	V
Output "M2"-Level Voltage	$V_{OM}2-4$	V_{SS1}=-1.55V,COM1.COM2.COM3 I_{OH}=-4uA,I_{OL}=4uA	V_{SS2} -0.2		V_{SS2} +0.2	V
Output "L"-Level Voltage	$V_{OL}(4)$	V_{SS1}=-1.55V,COM1.COM2.COM3 I_{OL}=4uA			V_{SS3} +0.2	V

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- **Output Voltage**

			min	typ	max	unit
LCD Lighting:						
1/3Bias Method (Doubler)	V_{SS2}	V_{SS1}=-1.35V,fopg=32.768kHz C1toC4=0.1uF Fig.7			-2.5	V
(Tripler)	V_{SS3}	V_{SS1}=-1.35V,fopg=32.768kHz C1toC4=0.1uF Fig.7			-3.75	V
1/2Bias Method (Doubler)	V_{SS2}	V_{SS1}=-1.35V,fopg=32.768kHz C1=C2=0.1uF Fig.2			-2.5	V

- **Supply Current (Backup Flag Reset)**

LCD Lighting: 1/3Bias Display	I_{DD}	V_{SS1}=-1.55V,during HALT, C1toC4=0.1uF,CI=256kohms Fig.7 Cd=Cg=20pF,32.768kHz X'tal		3.5		uA
LCD Lighting: Other than 1/3Bias Display	I_{DD}	V_{SS1}=-1.55V,during HALT, C1=C2=0.1uF,CI=25kohms,Fig.2 Cd=Cg=20pF,32.768kHz X'tal		2.0		uA
Oscillation Start Voltage V_{SS1}	V_{stt}	Cd=Cg=20pF,CI=25kohms, 32.768kHz X'tal,Fig.3	-1.35			V
Oscillation Hold Voltage V_{SS1}	V_{HOLD}	Cd=Cg=20pF,CI=25kohms, 32.768kHz X'tal,Fig.2	-1.6		-1.3	V
Oscillation Start Time	t_{stt}	V_{SS1}=-1.35V,CI=25kohms, Fig.3 Cd=Cg=20pF,32.768kHz X'tal			10	sec
Oscillation Compensation Capacitance	10P	External terminal	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

Li specifications

Absolute Maximum Ratings at Ta=25±2°C,V_{DD}=0V				unit
Maximum Supply Voltage	V_{SS1}	V_{BAK}=V_{SS1}orV_{SS2}	-4.0to+0.3	V
	V_{SS2}		-4.0to+0.3	V
	V_{SS3}	(LCD lighting: 1/3bias display)	-5.5to+0.3	V
	V_{SS3}	(LCD lighting: Other than 1/3 bias display)	-4.0to+0.3	V
Maximum Input Voltage	$V_{IN}1$	10p,OSCIN	V_{BAK}-0.3to+0.3	V
	$V_{IN}2$	S1-4,M1-4,I/OA1-4,I/OB1-4,INT TESTA(I/OA1-4,I/OB1-4 are in the input mode.)	V_{SS2}-0.3to+0.3	V
Maximum Output Voltage	$V_{out}1$	TEST,OSCOUT	V_{BAK}-0.3to+0.3	V
	$V_{out}2$	ALM,LIGHT,P1-4,I/OA1-4, I/OB1-4,CUP2(I/OA1-4,I/OB are in the output mode.)	V_{SS2}-0.3to+0.3	V
	$V_{out}3$	SEGOUT,COM1toCOM3,CUP1	V_{SS3}-0.3to+0.3	V
Operating Temperature	Topg		-20to+65	°C
Storage Temperature	Tstg		-30to+125	°C

Allowable Operating Conditions at Ta=25±2°C, V_{DD}=0V			min	typ	max	unit
Supply Voltage	V_{BAK}		-3.6		-1.3	V
	V_{SS2}	$V_{BAK}=V_{SS2}/2$ (Backup flag is reset.)	-3.6		-2.6	V
	V_{SS2}	$V_{BAK}=V_{SS2}$ (Backup flag is reset.)	-3.6		-1.3	V
	V_{SS3}	(LCD lighting: 1/3bias display)	-4.95		-3.7	V
	V_{SS3}	(LCD lighting: Oter than 1/3 bias display)		$V_{SS3}=V_{SS2}$		V
Output "H"-Level Voltage	V_{IH}	S1-4,M1-4,I/OA1-4,I/OB1-4, INT,(I/OA1-4,I/OB1-4 are in the input mode.)	-0.4		0	V
Output "L"-Level Voltage	V_{IL}	S1-4,M1-4,I/OA1-4,I/OB1-4, INT,(I/OA1-4,I/OB1-4 are in the input mode.)	V_{SS2}		V_{SS2} +0.4	V
Operating Frequency	fopg	Ta=-20to+65	32		33	kHz

Electrical Characteristics [LC5851] at Ta=25±2°C, V_{DD}=0V			min	typ	max	unit
Input Resistance	R_{IN}1A	V_{SS2}=-2.9V,"L" level hold Tr $V_{IL}=V_{SS2}$+0.4V *1,Fig.4	10		200	kohm
	R_{IN}1B	V_{SS2}=-2.9V,pull-down resistor *1,Fig.4	200		2000	kohm
	R_{IN}2A	V_{SS2}=-2.9V,pull-up resistor $V_{IL}=V_{SS2}$ for INT	200		2000	kohm
	R_{IN}2B	V_{SS2}=-2.9V,pull-down resistor $V_{IH}=V_{DD}$ for INT	200		2000	kohm
	R_{IN}3	V_{SS2}=-2.9V,pull-down resistor $V_{IH}=V_{DD}$ for RES	5		50	kohm
Output "H"-Level Voltage	V_{OH}(1)	V_{SS2}=-2.4V,ALM I_{OH}=-250uA	-0.65			V
Output "L"-Level Voltage	V_{OL}(1)	V_{SS2}=-2.4V,ALM I_{OL}=250uA			V_{SS2} +0.65	V
Output "H"-Level Voltage	V_{OH}(2)	V_{SS2}=-2.9V,I/OA1-4,I/OB1-4 I_{OH}=-40uA,P1-4 (I/OA1-4,I/OB1-4 are in the output mode.)	-0.4			V
Output "L"-Level Voltage	V_{OL}(2)	V_{SS2}=-2.9V,I/OA1-4,I/OB1-4 I_{OH}=40uA,P1-4 (I/OA1-4,I/OB1-4 are in the output mode.)			V_{SS2} +0.4	V
Output "H"-Level Voltage	V_{OH}(3)	V_{SS2}=-2.9V,LIGHT I_{OH}=-150uA	-1.5			V
Output "L"-Level Voltage	V_{OL}(3)	V_{SS2}=-2.9V,LIGHT I_{OL}=150uA			V_{SS2} +1.5	V

Segment Driver Output Impedance

			min	typ	max	unit
• Static Display						
Output "H"-Level Voltage	$V_{OH}(4)$	V_{SS2}=-2.9V,all SEGOUTs I_{OH}=-0.4uA	-0.2			V
Output "L"-Level Voltage	$V_{OL}(4)$	V_{SS2}=-2.9V,all SEGOUTs I_{OL}=0.4uA			V_{SS2} +0.2	V
Output "H"-Level Voltage	$V_{OH}(5)$	V_{SS2}=-2.9V,COM1 I_{OH}=-4uA	-0.2			V
Output "L"-Level Voltage	$V_{OL}(5)$	V_{SS2}=-2.9V,COM1 I_{OL}=4uA			V_{SS2} +0.2	V
• Duplex Display (1/2Bias,1/2Duty)						
Output "H"-Level Voltage	$V_{OH}(4)$	V_{SS2}=-2.9V,all SEGOUTs I_{OH}=-0.4uA	-0.2			V
Output "L"-Level Voltage	$V_{OL}(4)$	V_{SS2}=-2.9V,all SEGOUTs I_{OL}=0.4uA			V_{SS2} +0.2	V
Output "H"-Level Voltage	$V_{OH}(5)$	V_{SS2}=-2.9V,COM1.COM2 I_{OH}=-4uA	-0.2			V
Output "M"-Level Voltage	V_{OM}	V_{SS2}=-2.9V,COM1.COM2 I_{OH}=-4uA,I_{OL}=4uA	$V_{SS2}/2$ -0.2		$V_{SS2}/2$ +0.2	V
Output "L"-Level Voltage	$V_{OL}(5)$	V_{SS2}=-2.9V,COM1.COM2 I_{OL}=4uA			V_{SS2} +0.2	V
• 1/2Bias, 1/3Duty Display						
Output "H"-Level Voltage	$V_{OH}(4)$	V_{SS2}=-2.9V,all SEGOUTs I_{OH}=-0.4uA	-0.2			V
Output "L"-Level Voltage	$V_{OL}(4)$	V_{SS2}=-2.9V,all SEGOUTs I_{OL}=0.4uA			V_{SS2} +0.2	V
Output "H"-Level Voltage	$V_{OH}(5)$	V_{SS2}=-2.9V,COM1.COM2. I_{OH}=-4uA COM3	-0.2			V
Output "M"-Level Voltage	V_{OM}	V_{SS2}=-2.9V,COM1.COM2. I_{OH}=-4uA,I_{OL}=4uA,COM3	$V_{SS2}/2$ -0.2		$V_{SS2}/2$ +0.2	V
Output "L"-Level Voltage	$V_{OL}(5)$	V_{SS2}=-2.9V,COM1.COM2. I_{OL}=4uA COM3			V_{SS2} +0.2	V
• 1/3Bias, 1/3Duty Display						
Output "H"-Level Voltage	$V_{OH}(4)$	V_{SS2}=-2.9V,all SEGOUTs I_{OH}=-0.4uA	-0.2			V
Output "M1"-Level Voltage	$V_{OM}1\text{-}4$	V_{SS2}=-2.9V,all SEGOUTs I_{OH}=-0.4uA,I_{OL}=0.4uA	$V_{SS2}/2$ -0.2		$V_{SS2}/2$ +0.2	V
Output "M2"-Level Voltage	$V_{OM}2\text{-}4$	V_{SS2}=-2.9V,all SEGOUTs I_{OH}=-0.4uA,I_{OL}=0.4uA	V_{SS2} -0.2		V_{SS2} +0.2	V
Output "L"-Level Voltage	$V_{OL}(4)$	V_{SS2}=-2.9V,all SEGOUTs I_{OL}=0.4uA			V_{SS3} +0.2	V
Output "H"-Level Voltage	$V_{OH}(5)$	V_{SS2}=-2.9V,COM1.COM2. I_{OH}=-4uA COM3	-0.2			V
Output "M1"-Level Voltage	$V_{OM}1\text{-}5$	V_{SS2}=-2.9V,COM1.COM2. I_{OH}=-4uA,I_{OL}=4uA,COM3	$V_{SS2}/2$ -0.2		$V_{SS2}/2$ +0.2	V
Output "M2"-Level Voltage	$V_{OM}2\text{-}5$	V_{SS2}=-2.9V,COM1.COM2. I_{OH}=-4uA,I_{OL}=4uA,COM3	V_{SS2} -0.2		V_{SS2} +0.2	V
Output "L"-Level Voltage	$V_{OL}(5)$	V_{SS2}=-2.9V,COM1.COM2. I_{OL}=4uA COM3			V_{SS3} +0.2	V

Output Voltage

			min	typ	max	unit
LCD Lighting:						
1/3Bias Display (Halver)	V_{SS1}	V_{SS2}=-2.9V,fopg=32.768kHz, C1toC4=0.1uF Fig.8			-1.35	V
(Tripler)	V_{SS3}	V_{SS2}=-2.9V,fopg=32.768kHz, C1toC4=0.1uF Fig.8			-4.1	V
LCD Lighting: Other than 1/3Bias Display						
(Halver)	V_{SS1}	V_{SS2}=-2.9V,fopg=32.768kHz, C1=C2=0.1uF Fig.5			-1.35	V

Supply Current (Backup flag is reset.)

LCD Lighting: 1/3Bias Display	I_{DD}	V_{SS2}=-2.9V,during HALT, C1toC4=0.1uF,C1=25kohms, Fig.8 Cd=Cg=20pF,32.768kHz X'tal		5.0		uA
LCD Lighting: Other than 1/3Bias Display	I_{DD}	V_{SS2}=-2.9V,during HALT, C1=C2=0.1uF,C1=25kohms, Fig.5 Cd=Cg=20pF,32.768kHz X'tal		1.0		uA
Oscillation Start Voltage V_{SS2}	V_{stt}	$V_{BAK}=V_{SS2/2}$,CI=25kohms,Fig.6 Cd=Cg=20pF,32.768kHz X'tal	-1.35			V
Oscillation Hold Voltage V_{SS2} (Backup flag is reset.)	V_{HOLD}(1)	$V_{BAK}=V_{SS2/2}$,CI=25kohms,Fig.5 Cd=Cg=20pF,32.768kHz X'tal	-3.6		-2.6	V
(Backup flag is set.)	V_{HOLD}(2)	$V_{BAK}=V_{SS2}$,CI=25kohms,Fig.6 Cd=Cg=20pF,32.768kHz X'tal	-3.6		-1.3	V
Oscillation Start Time	t_{stt}	$V_{BAK}=V_{SS2}$=-2.9V,CI=25kohms,Fig.6 Cd=Cg=20pF,32.768kHz X'tal			10	sec
Oscillation Compensation Capacitance	10p	External terminal	8	10	12	pF
	20p	OSCOUT	16	20	24	pF

EXT-V specificaitions

Absolute Maximum Ratings at Ta=25±2°C, V_{DD}=0V

				unit
Maximum Supply Voltage	V_{SS1}		-4.0to+0.3	V
	V_{SS2}		-4.0to+0.3	V
	V_{SS3}	(LCD lighting: 1/3bias display)	-5.5to+0.3	V
	V_{SS3}	(LCD lighting: Other than 1/3 bias display)	-4.0to+0.3	V
Maximum Input Voltage	$V_{IN}1$	10p,OSCIN	V_{SS2}-0.3to+0.3	V
	$V_{IN}2$	S1-4,M1-4,I/OA1-4.I/OB1-4,INT, TESTA(I/OA1-4,I/OB1-4,I/OB1-4 are in the input mode.)	V_{SS2}-0.3to+0.3	V
Maximum Output Voltage	$V_{out}1$	TEST,OSCOUT	V_{SS2}-0.3to+0.3	V
	$V_{out}2$	ALM,LIGHT,P1-4,I/OA1-4,I/OB1-4 CUP2(I/OA1-4,I/OB1-4 are in the output mode.)	V_{SS2}-0.3to+0.3	V
	$V_{out}3$	SEGOUT,COM1toCOM3,CUP1	V_{SS3}-0.3to+0.3	V
Operating Ambient Temperature	Topg		-20to+65	°C
Storage Temperature	Tstg		-30to+125	°C

Allowable Operating Conditions at Ta=25±2°C, V_{DD}=0V			min	typ	max	unit
Supply Voltage	V_{SS1}		-3.6		-1.3	V
	V_{SS2}	$V_{BAK}=V_{SS2}$	-3.6		-2.0	V
	V_{SS3}	(LCD lighting: 1/3bias display)	-5.0		-3.3	V
	V_{SS3}	(LCD lighting: Other than 1/3 bias display)		$V_{SS3}=V_{SS2}$		V
Output "H"-Level Voltage	V_{IH}	S1-4,M1-4,I/OA1-4,I/OB1-4,INT, (I/OA1-4 and I/OB1-4 are in the input mode.)	0.3 V_{SS2}		0	V
Output "L"-Level Voltage	V_{IL}	S1-4,M1-4,I/OA1-4,I/OB1-4,INT, (I/OA1-4 and I/OB1-4 are in the input mode.)	V_{SS2}		0.7 V_{SS2}	V
Operating Frequency	fopg	Ta=-20to+65°C	32		33	kHz

Electrical Characteristics [LC5851] at Ta=25±2°C, V_{DD}=0V			min	typ	max	unit
Input Resistance	$R_{IN}1A$	V_{SS2}=-2.9V,"L" level hold Tr $V_{IL}=V_{SS2}$+0.4V *1, Fig.4	10		200	kohm
	$R_{IN}1B$	V_{SS2}=-2.9V,pull-down resistor *1, Fig.4	200		2000	kohm
	$R_{IN}2A$	V_{SS2}=-2.9V,pull-up resistor for INT $V_{IL}=V_{SS2}$	200		2000	kohm
	$R_{IN}2B$	V_{SS2}=-2.9V,pull-down resistor for INT $V_{IL}=V_{DD}$	200		2000	kohm
	$R_{IN}3$	V_{SS2}=-2.9V,pull-down resistor for RES $V_{IH}=V_{DD}$	5		50	kohm
Output "H"-Level Voltage	$V_{OH}(1)$	V_{SS2}=-2.4V,ALM,LIGHT I_{OH}=-0.4mA	-1.0	-0.3		V
Output "L"-Level Voltage	$V_{OL}(1)$	V_{SS2}=-2.4V,ALM,LIGHT I_{OL}=0.4mA		V_{SS2} +0.3	V_{SS2} +1.0	V
Output "H"-Level Voltage	$V_{OH}(2)$	V_{SS2}=-2.4V,I/OA1-4,I/OB1-4 I_{OH}=-0.1mA,P1-4 (I/OA1-4 and I/OB1-4 are in the output mode.)	-1.0	-0.3		V
Output "H"-Level Voltage	$V_{OH}(3)$	V_{SS2}=-2.4V,I/OA1-4,I/OB1-4 I_{OH}=-50uA,P1-4 (I/OA1-4 and I/OB1-4 are in the output mode.)	-0.6	-0.2		V
Output "L"-Level Voltage	$V_{OL}(3)$	V_{SS2}=-2.4V,I/OA1-4,I/OB1-4 I_{OL}=0.1mA,P1-4 (I/OA1-4 and I/OB1-4 are in the output mode.)		V_{SS2} +0.3	V_{SS2} +1.0	V

Segment Driver Output Impedance **CMOS Output Port**			min	typ	max	unit
Output "H"-Level Voltage	$V_{OH}(4)$	V_{SS2}=-2.4V, I_{OH}=-10uA (for output port)	-1	-0.3		V
Output "L"-Level Voltage	$V_{OL}(4)$	V_{SS2}=-2.4V, I_{OL}=50uA (PAD No.63to65 / QIP64 pin No. 34to36)		V_{SS2} +0.3	V_{SS2} +1	V
Output "H"-Level Voltage	$V_{OH}(5)$	V_{SS2}=-2.4V, I_{OH}=-5uA (for output port)	-1	-0.3		V
Output "L"-Level Voltage	$V_{OL}(5)$	V_{SS2}=-2.4V, I_{OL}=20uA (PAD No.38to41 / 44,46to62 / QIP64 pin No. 11to33)		V_{SS2} +0.3	V_{SS2} +1	V

			min	typ	max	unit
Pch Open Drain Output Port						
Output "H"-Level Voltage	V_{OH}(4)	V_{SS2}=-2.4V, segment I_{OH}=-10uA (for output port)	-1	-0.3		V
Output OFF-State Leakage Current	I_{OFF}	V_{SS2}=-2.6V, V_{OUT}=V_{SS2} (PAD No.63to65 QIP64 pin No. 34to36)			1	uA
Static Display						
Output "H"-Level Voltage	V_{OH}(4)	V_{SS2}=-2.9V,all SEGOUTs I_{OH}=-0.4uA	-0.2			V
Output "L"-Level Voltage	V_{OL}(4)	V_{SS2}=-2.9V,all SEGOUTs I_{OL}=0.4uA			V_{SS2} +0.2	V
Output "H"-Level Voltage	V_{OH}(5)	V_{SS2}=-2.9V,COM1 I_{OH}=-4uA	-0.2			V
Output "L"-Level Voltage	V_{OL}(5)	V_{SS2}=-2.9V,COM1 I_{OL}=4uA			V_{SS2} +0.2	V
Duplex Display (1/2Bias, 1/2Duty)			min	typ	max	unit
Output "H"-Level Voltage	V_{OH}(4)	V_{SS2}=-2.9V,all SEGOUTs I_{OH}=-0.4uA	-0.2			V
Output "L"-Level Voltage	V_{OL}(4)	V_{SS2}=-2.9V,all SEGOUTs I_{OL}=0.4uA			V_{SS2} +0.2	V
Output "H"-Level Voltage	V_{OH}(5)	V_{SS2}=-2.9V,COM1.COM2. I_{OH}=-4uA	-0.2			
Output "M"-Level Voltage	V_{OM}	V_{SS2}=-2.9V,COM1.COM2. I_{OH}=-4uA,I_{OL}=4uA	$V_{SS2}/2$ -0.2		$V_{SS2}/2$ +0.2	V
Output "L"-Level Voltage	V_{OL}(5)	V_{SS2}=-2.9V,COM1.COM2. I_{OL}=4uA			V_{SS2} +0.2	V
1/2Bias, 1/3Duty Display						
Output "H"-Level Voltage	V_{OH}(4)	V_{SS2}=-2.9V,all SEGOUTs I_{OH}=-0.4uA	-0.2			V
Output "L"-Level Voltage	V_{OL}(4)	V_{SS2}=-2.9V,all SEGOUTs I_{OL}=0.4uA			V_{SS2} +0.2	V
Output "H"-Level Voltage	V_{OH}(5)	V_{SS2}=-2.9V,COM1.COM2.COM3 I_{OH}=-4uA	-0.2			V
Output "M"-Level Voltage	V_{OM}	V_{SS2}=-2.9V,COM1.COM2.COM3 I_{OH}=-4uA,I_{OL}=4uA	$V_{SS2}/2$ -0.2		$V_{SS2}/2$ +0.2	V
Output "L"-Level Voltage	V_{OL}(5)	V_{SS2}=-2.9V,COM1.COM2.COM3 I_{OL}=4uA			V_{SS2} +0.2	V
1/3Bias, 1/3Duty Display						
Output "H"-Level Voltage	V_{OH}(4)	V_{SS2}=-2.9V,SEGOUT I_{OH}=-0.4uA	-0.2			V
Output "M1"-Level Voltage	V_{OM}1-4	V_{SS2}=-2.9V,SEGOUT I_{OH}=-0.4uA,I_{OL}=4uA	$V_{SS2}/2$ -0.2		$V_{SS2}/2$ +0.2	V
Output "M2"-Level Voltage	V_{OM}2-4	V_{SS2}=-2.9V,SEGOUT I_{OH}=-0.4uA,I_{OL}=0.4uA	V_{SS2} -0.2		V_{SS2} +0.2	V
Output "L"-Level Voltage	V_{OL}(4)	V_{SS2}=-2.9V,SEGOUT I_{OL}=0.4uA			V_{SS3} +0.2	V
Output "H"-Level Voltage	V_{OH}(5)	V_{SS2}=-2.9V,COM1.COM2.COM3 I_{OH}=-4uA	-0.2			V
Output "M1"-Level Voltage	V_{OM}1-5	V_{SS2}=-2.9V,COM1.COM2.COM3 I_{OH}=-4uA,I_{OL}=0.4uA	$V_{SS2}/2$ -0.2		$V_{SS2}/2$ +0.2	V
Output "M2"-Level Voltage	V_{OM}2-5	V_{SS2}=-2.9V,COM1.COM2.COM3 I_{OH}=-4uA,I_{OL}=4uA	V_{SS2} -0.2		V_{SS2} +0.2	V
Output "L"-Level Voltage	V_{OL}(5)	V_{SS2}=-2.9V,COM1.COM2.COM3 I_{OL}=4uA			V_{SS3} +0.2	V

				min	typ	max	unit
Output Voltage							
LCD Lighting: 1/3Bias Display							
(Halver)		V_{SS1}	V_{SS2}=-2.9V,fopg=32.768kHz C1toC3=0.1uF Fig.9			-1.35	V
(Tripler)		V_{SS3}	V_{SS2}=-2.9V,fopg=32.768kHz C1toC3=0.1uF Fig.9			-4.1	V
LCD Lighting: Other than 1/3Bias Display							
(Halver)		V_{SS1}	V_{SS2}=-2.9V,fopg=32.768kHz C1=C2=0.1uF Fig.5			-1.35	V
Supply Current (Backup flag is reset.)							
LCD Lighting:	1/3Bias Display	$\|I_{DD}\|$	V_{SS2}=-2.9V,During HALT C1toC3=0.1uF,CI=25kohms,Fig.9 Co=Cg=20pF,32.768kHz X'tal		5.0		uA
LCD Lighting:	Other than 1/3Bias Display	I_{DD}	V_{SS2}=-2.9V,during HALT, C1=C2=0.1uF,CI=25kohms,Fig.5 Co=Cg=20pF,32.768kHz X'tal		5.0		uA
Oscillation Start Voltage V_{SS2}		Vstt	Co=Cg=20pF,CI=25kohms,Fig.6 32.768kHz X'tal	-2.2			V
Oscillation Hold Voltage V_{SS2}		V_{HOLD}	Co=Cg=20pF,CI=25kohms,Fig.5 32.768kHz X'tal	-3.6		-2.0	V
Oscillation Start Time		t_{stt}	V_{SS2}=-2.9V,CI=25kohms,Fig.6 Co=Cg=20pF,32.768kHz X'tal			10	sec
Oscillation Compensation Capacitance		10p	External terminal	8	10	21	pF
		20p	OSCOUT	16	20	24	pF

*1 S1・S2・S3・S4・M1・M2・M3・M4

Fig.1 S1-4, M1-4 Input Configuration

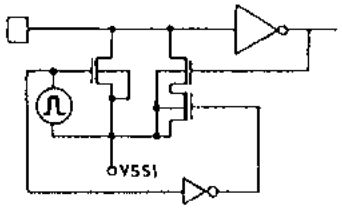

Fig.2 Supply Current, Oscillation Hold Voltage Test Circuit

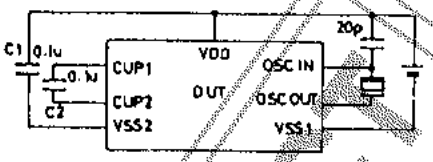

Fig.3 Oscillation Start Voltage, Oscillation Start Time, Frequency Stability Test Circuit

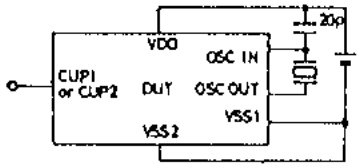

Fig.4 S1-4, M1-4 Input Configuration

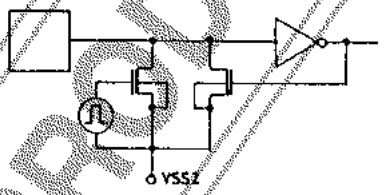

Fig.5 Supply Current, Oscillation Hold Voltage Test Circuit

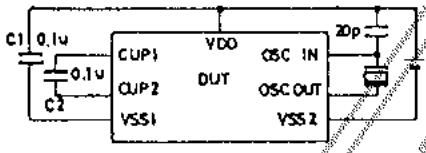

Fig.6 Oscillation Start Voltage, Oscillation Start Time, Frequency Stability Test Circuit

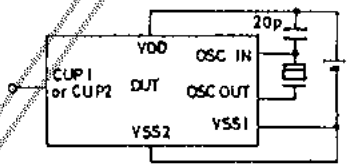

Fig.7 Supply Current, Oscillation Hold Voltage Test Circuit

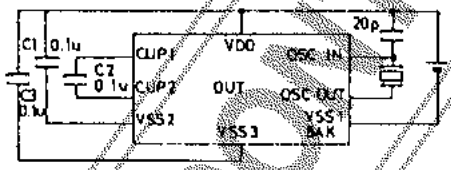

Fig.8 Supply Current, Oscillation Hold Voltage Test Circuit

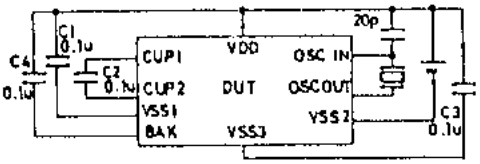

Fig.9 Supply Current, Oscillation Hold Voltage Test Circuit