SANYO No1271G

LC5800

CMOS LSI

Single-Chip 4-Bit Microcomputer with LCD Driver

The LC5800 is a C-MOS 4-bit microcomputer that operates on low voltage, very low current and contains LCD drivers. It contains a 4-bit parallel processing ALU, many LCD segment outputs, many I/O ports, a 32.768kHz crystal oscillator, and a divider. It is ideally suited for use in desk-top calculator, camera, speech synthesis LSI controller, equipment controller applications as well as high-grade game watch/clock applications.

(1) Hardware features

- Supply voltage: 1.5V or 3.0V (typ.) (mask option)
- Very low current dissipation:
  3.0μA type. (1.5V supply voltage, at watch/clock operating mode)
  1.5μA type. (3.0V supply voltage, at watch/clock operating mode)
- Built-in crystal oscillator for watch/clock (32.768kHz crystal connected externally)
- Many output pins for LCD panel drive (42 pins)

Drivable LCD panel	Number of drivable LCD segments
1/3 bias 1/3 duty	126 segments
1/2 bias 1/3 duty	126 segments
1/2 bias 1/2 duty	84 segments
Static	42 segments

- Many input/output pins
  Ports for input only: 2 ports/8 pins
  Input/output common ports: 2 ports/8 pins
  Control output pins: 4 pins
- Possible to use LCD panel drive output pins as ports for output only (mask option)
  Note: For the Ag version (1.5V), the segment output pins cannot be used as ports for output only.
- With initial reset pin
- ROM: 2048 x 16 bits
- RAM: 152 x 4 bits
- Cycle time: 244μsec. (or 122μsec./mask option)
- Built-in step-up circuit, step-down circuit
- Shipping style: Chip (or QIP80)

(2) Software features

- Powerful instruction sets: 121 instructions
- 8-level subroutine nesting (common with interrupt)
- External interrupt function
- 15-bit divider for watch/clock
- Built-in counter for 1/100-second chronograph
- Built-in 10-bit programmable timer
- HALT function
- Automatic select of all addresses (direct addressing type)
- Single stepping of all instructions
- Built-in data pointer

Specifications and information herein are subject to change without notice.

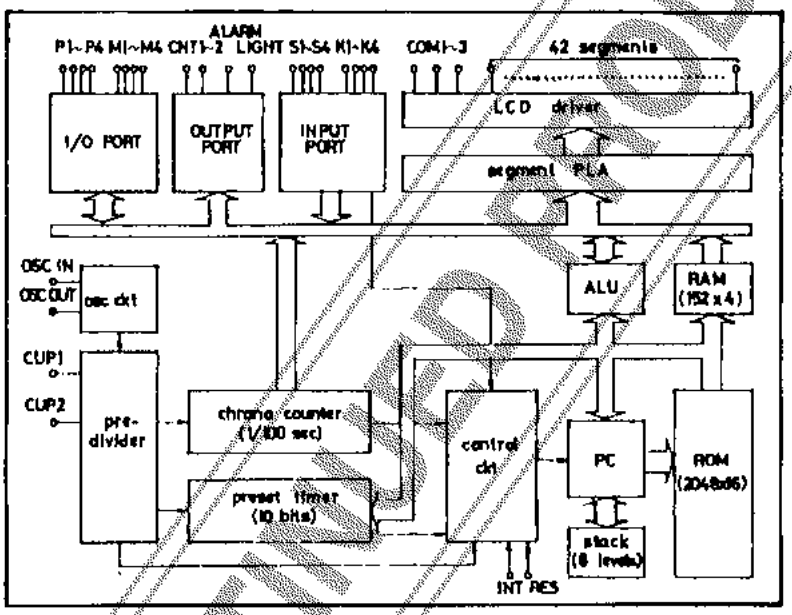
SANYO Electric Co.,Ltd. Semiconductor Overseas Marketing Div.
Natsume Bldg., 18-6, 2-chome, Yushima, Bunkyo-ku, TOKYO 113 JAPAN

(3) Application development tools

For performing application development, the evaluation chip (LC5899) and the dedicated application development tools are prepared.

- SDS410 system
  Application development program of microcomputer can be made in assembly language (edit, assemble).
- EVA510 + TB51 + display board + LC5899
  By connecting to the SDS410, application development program can be corrected and debugged. The EVE510 is a control ROM-replaced version of the EVA410.
- TB51 + display board + LC5899
  By using the EPROM (2732) with application development program data written in, mounting evaluation can be performed.

Equivalent Circuit Block Diagram

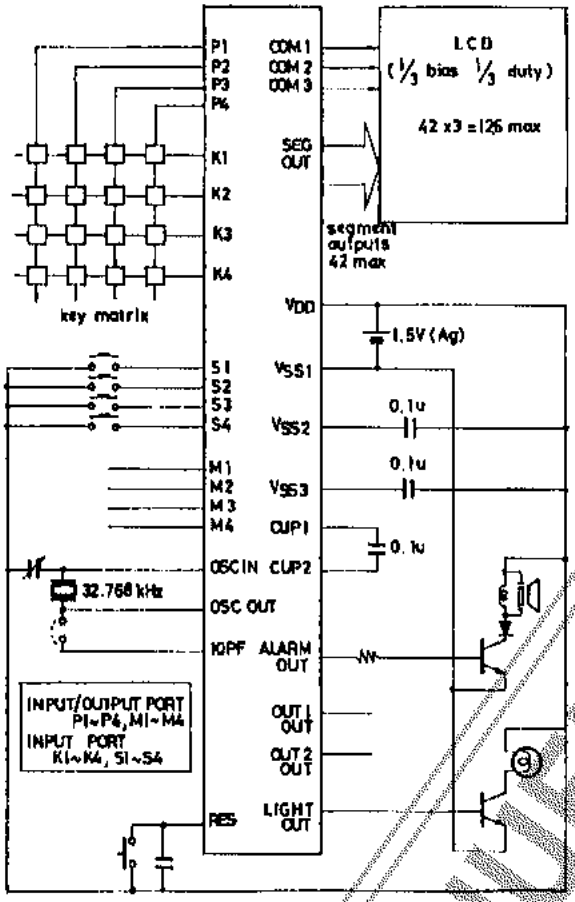


Application Areas

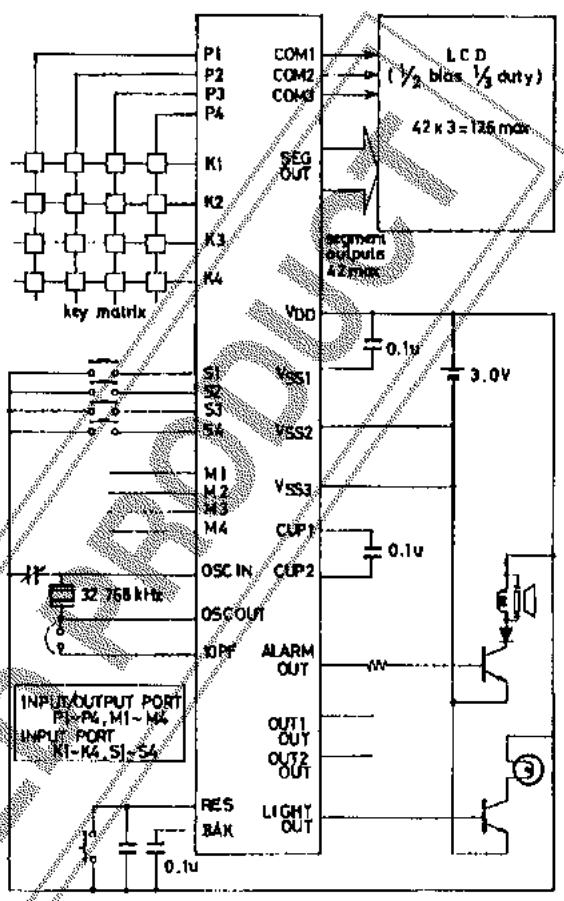
1) Multifunction watch/clock with calculator
2) Controller of speech synthesis LSI
3) Watch/clock with memory (external memory)
4) Controller of camera
5) Mechanical controller of VTR, radio-cassette recorder, tape deck, etc.
6) Controller of telephone dialer, etc.

Sample Application Circuits

(1) Typical application circuit using Ag battery (1/3 bias 1/3 duty)



(2) Typical application circuit using LI battery (1/2 bias 1/3 duty)

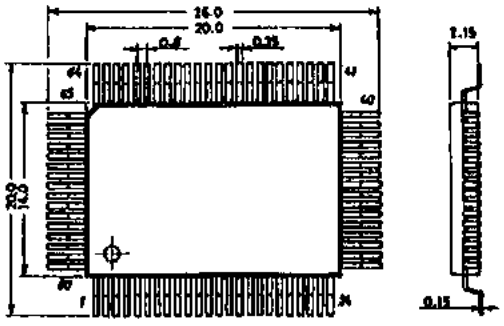


Pad Assignment of LSI Chip

CHIP SIZE	7.44 mm x 5.68 mm
CHIP THICKNESS	480 um
PAD SIZE	120 um x 120 um

Case Outline 3044B-Q80AIC

(unit: mm)



Note : When mounting the QIP version on the board, do not dip it in solder.

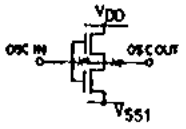
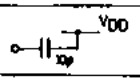
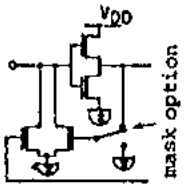
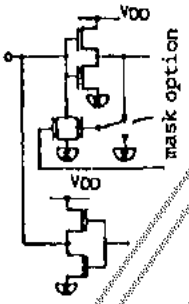
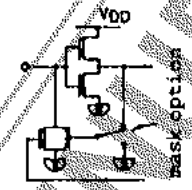
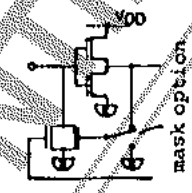
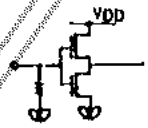
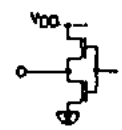
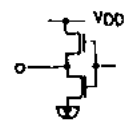
Pad Name and Coordinates

Pin assignment of QIP80				
	Pad No.	Pin name	X (μm)	Y (μm)
73	1	V_{DD}	−3560	+ 193
74	2	OSCIN	"	+ 12
75	3	OSCOUT	"	− 168
—	4	10P	"	− 348
76	5	TEST3	"	− 527
77	6	T4	"	− 708
78	7	S3	"	− 888
—	8	P1	"	−1068
—	9	P2	"	−1247
79	10	P3	"	−1428
80	11	P4	"	−1608
1	12	COM2	"	−2146
2	13	COM3	"	−2684
3	14	Seg	−3042	"
4	15	↑	−2810	"
5	16		−2516	"
6	17		−2221	"
7	18		−1925	"
8	19		−1630	"
9	20		−1334	"
10	21		−1040	"
11	22		− 744	"
12	23		− 438	"
13	24		− 133	"
14	25		+ 174	"
15	26		+ 480	"
16	27		+ 786	"
17	28		+1093	"
18	29		+1398	"
19	30		+1703	"
20	31		+2010	"
21	32		+2315	"
22	33		+2621	"
23	34	Seg	+2928	"
—	35	TEST	+3560	"
—	36	TEST	"	−2473
25	37	BAK	"	−2253
—	38	(V_{SS})	"	−2031
—	39	(V_{DD})	"	−1851
26	40	K4	"	−1545
27	41	K3	"	−1110
28	42	K2	"	− 928
29	43	K1	"	− 494

Pin assignment of QIP80				
	Pad No.	Pin name	X (μm)	Y (μm)
30	44	RES	+3560	− 314
32	45	INT	"	+ 676
33	46	TEST2	"	+ 856
34	47	TEST1	"	+1083
35	48	M4	"	+1264
36	49	M3	"	+1444
37	50	M2	"	+1623
38	51	M1	"	+1804
39	52	S2	"	+1983
40	53	S1	"	+2294
—	54	TEST	"	+2475
41	55	CUP2	"	+2684
42	56	CUP1	+3256	"
43	57	Seg	+3065	"
44	58	↓	+2770	"
45	59		+2475	"
46	60		+2179	"
47	61		+1884	"
48	62		+1588	"
49	63		+1294	"
50	64		+ 998	"
51	65		+ 693	"
52	66		+ 386	"
53	67		+ 81	"
54	68		− 226	"
55	69		− 532	"
56	70		− 837	"
57	71		−1143	"
58	72		−1450	"
59	73		−1756	"
60	74		−2061	"
61	75		−2367	"
62	76	↓	−2674	"
63	77	Seg	−2980	"
64	78	COM1	−3560	"
65	79	S4	"	+2079
66	80	CNT1	"	+1832
67	81	CNT2	"	+1272
68	82	LIGHT	"	+1092
69	83	ALARM	"	+ 913
70	84	V_{SS3}	"	+ 733
71	85	V_{SS2}	"	+ 552
72	86	V_{SS1}	"	+ 372

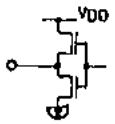
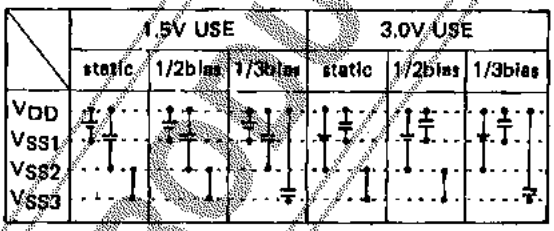
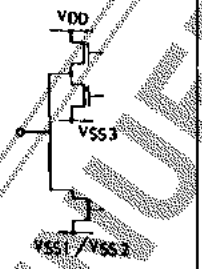
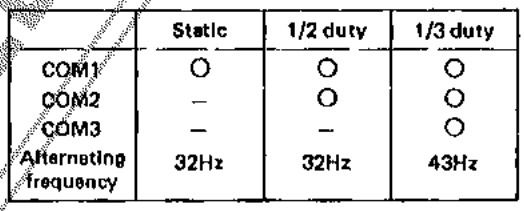
The above pad coordinates are such that the chip center is taken as the origin and the values of (X, Y) represent the coordinates of the center of each pad.
Pin 24 of QIP80: NC
Pin 31 of QIP80: SUB
(NC, SUB: Open)

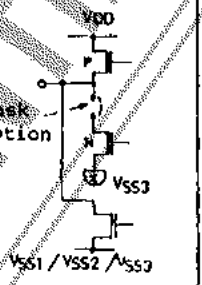
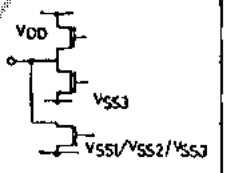
Pin Description

Pad No.	Pin Name	Input/Output	Circuit Configuration	Function
2 3	OSCIN OSCOUT	Input Output		32.768kHz crystal is connected across OSCIN and OSCOUT for oscillation. Used as reference clock for watch/clock and system clock. 20pF capacitor is connected across OSCOUT and V_{DD}.
4	10P	—		Connected to OSCOUT and used as oscillation phase compensation capacitor.
53 52 7 79	S1 S2 S3 S4	Input		Port for input only. With 7ms or 32ms chattering eliminator. By applying V_{DD} to S1 to S4 simultaneously, LSI inside is reset. (mask option)
8 9 10 11 51 50 49 48	P1 P2 P3 P4 M1 M2 M3 M4	Input/Output		Input/output pins for selecting between the following 2 operations with instruction. (1) Input pin for fetching data into RAM. (2) Output pin for outputting data from RAM.
43 42 41 40	K1 K2 K3 K4	Input		(1) Input pin for fetching data into RAM through 7ms or 32ms chattering eliminator. (2) K4 signal is used to operate decimal counter (for 1/100-second count) inside LSI with instruction.
45	INT	Input		External interrupt request control input pin.
44	RES	Input		Input pin for resetting LSI inside.
37	BAK			(—) power supply pin for logic unit inside LSI. When using 3.0V supply, a capacitor must be connected across BAK and V_{DD} to prevent logic unit from malfunctioning.
80 81	CNT1 CNT2	Output		Pins for output only.
82	LIGHT	Output		Pin for output only. Suited for outputting signal to drive transistor for light.

Continued on next page.

Continued from preceding page.

<table>
<tr><th>Pad No.</th><th>Pin Name</th><th>Input/Output</th><th>Circuit Configuration</th><th>Function</th></tr>
<tr><td>83</td><td>ALARM</td><td>Output</td><td>  </td><td>Pin for output only.
Used to output 4kHz, 2kHz, 1kHz modulation signal with instruction.
Also used to output non-modulation signal.</td></tr>
<tr><td>1</td><td>VDD</td><td></td><td></td><td>(+) Power supply pin.</td></tr>
<tr><td>84
85
86</td><td>VSS3
VSS2
VSS1</td><td></td><td></td><td>(–) Power supply pin.
• 1.5V/3.0V selectable with mask option.
For 1.5V use, apply (–) side to VSS1.
For 3.0V use, apply (–) side to VSS2.
• Also used as power supply for LCD drive.
 
The above Table shows how to connect external parts in each case.</td></tr>
<tr><td>55
56</td><td>CUP1
CUP2</td><td></td><td></td><td>Pins for connecting voltage step-up (step-down) capacitor.</td></tr>
<tr><td>78
12
13</td><td>COM1
COM2
COM3</td><td>Output</td><td>  </td><td>Output pins for LCD panel common electrode.
The following pin is used in each case.
  </td></tr>
<tr><td>14
to
22

57
to
64</td><td>Segment driver</td><td>Output</td><td>  </td><td>Output pins for LCD panel segments.
• Also used as output ports with mask option.
• When LSI inside is in reset mode, 32Hz, 64Hz or 128Hz static light-up signal is outputted at COM1 to COM3 and each LCD segment output and all LCD panel segments light up.
• Segment PLA system is adopted to support any type of LCD layout.</td></tr>
<tr><td>23
34
66</td><td>Segment driver</td><td>Output</td><td>  </td><td>Output pins for LCD panel segments.
• Also used as output ports with mask option.</td></tr>
<tr><td>5
6
35
36
46
47
54</td><td>TEST3
T4
TEST
TEST
TEST2
TEST1
TEST</td><td></td><td></td><td>Test pins (not used by user).</td></tr>
<tr><td>38
39</td><td>(VSS)
(VDD)</td><td></td><td></td><td>Backup power supply pin.
Normally, not used.</td></tr>
</table>

Note) Ag Battery: ⊕=VSS1, Li Battery: ⊖=VSS2

Operation from Ag Battery [Static]

Absolute Maximum Ratings at Ta=25±2°C, V_{DD}=0V

				unit
Maximum Supply Voltage	V_{SS1}		−4.0 to +0.3	V
	V_{SS2}	V_{SS2}=V_{SS3}	−4.0 to +0.3	V
Maximum Input Voltage	V_{IN1}	S1−4, M1−4, K1−4, P1−4, TEST−3, 10P, OSCIN, INT, RES (M1−4, P1−4: Input mode)	V_{SS1}−0.3 to 0.3	V
Maximum Output Voltage	V_{OUT1}	TEST3, CUP2, OSCOUT, ALARM, LIGHT, CNT1, CNT2, M1−4, P1−4 (M1−4, P1−4: Output mode)	V_{SS1}−0.3 to 0.3	V
	V_{OUT2}	SEGOUT, COM1, CUP1	V_{SS2}−0.3 to 0.3	V
Operating Temperature	Topg		−20 to +65	°C
Storage Temperature	Tstg		−30 to +125	°C

Allowable Operating Conditions at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Supply Voltage	V_{SS1}		−1.65		−1.30	V
	V_{SS2}	V_{SS2}=V_{SS3}	−3.3		−2.4	V
"H"-Level Input Voltage	V_{IH}	S1−4, M1−4, K1−4, P1−4, INT, RES, (M1−4, P1−4: Input mode)	−0.2		0	V
"L"-Level Input Voltage	V_{IL}	" "	V_{SS1}		V_{SS1}+0.2	V
Operating Frequency	fopg	Ta=−20 to +65°C "	32		33	kHz

Electrical Characteristics at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Input Resistance	R_{IN1A}	V_{SS1}=−1.55V, V_{IL}=V_{SS1}+0.2V, "L"-level hold tr., *1, Fig. 1	50		500	kohm
	R_{IN1B}	V_{SS1}=−1.55V, "L"-level pull-in tr., *1, Fig. 1	200		2000	kohm
	R_{IN2A}	V_{SS1}=−1.55V, V_{IL}=V_{SS1}+0.2V, input mode, "L"-level hold tr., *2, Fig. 1	50		500	kohm
	R_{IN2B}	V_{SS1}=−1.55V, input mode, "L"-level hold tr., *2, Fig. 1	200		2000	kohm
	R_{IN3}	V_{SS1}=−1.55V, TEST1, 2, RES	10		300	kohm
"H"-Level Output Voltage	V_{OH1}	V_{SS1}=−1.55V, I_{OH}=−0.4μA, SEGOUT	−0.2			V
"L"-Level Output Voltage	V_{OL1}	V_{SS1}=−1.55V, I_{OL}=0.4μA, SEGOUT			V_{SS2}+0.2	V
"H"-Level Output Voltage	V_{OH2}	V_{SS1}=−1.55V, I_{OH}=−4μA, COM1	−0.2			V
"L"-Level Output Voltage	V_{OL2}	V_{SS1}=−1.55V, I_{OL}=4μA, COM1			V_{SS2}+0.2	V
"H"-Level Output Voltage	V_{OH3}	V_{SS1}=−1.35V, I_{OH}=−250μA, ALM, LIGHT, CNT1, CNT2	−0.65			V
"L"-Level Output Voltage	V_{OL3}	V_{SS1}=−1.35V, I_{OL}=250μA, ALM, LIGHT, CNT1, CNT2			V_{SS1}+0.65	V
"H"-Level Output Voltage	V_{OH4}	V_{SS1}=−1.55V, I_{OH}=−20μA, M1−4, P1−4 (M1−4, P1−4: Output mode)	−0.2			V
"L"-Level Output Voltage	V_{OL4}	V_{SS1}=−1.55V, I_{OL}=20μA, M1−4, P1−4 (M1−4, P1−4: Output mode)			V_{SS1}+0.2	V
Output Voltage (doubler)	V_{SS2}	V_{SS1}=−1.35V, C1=C2=0.1μF, fopg=32.768kHz, Fig. 2			−2.5	V
Current Dissipation	$\|I_{DD}\|$	V_{SS1}=−1.55V, standard watch/clock operation, C1=C2=0.1μF, Co=Cg=20pF, Cl=25kohm, Fig.2		2.0		μA
Oscillation Start Voltage	V_{stt}	Co=Cg=20pF, Cl=25kohm, Fig. 3	−1.35			V
Oscillation Hold Voltage	V_{HOLD}	V_{BAK}=V_{SS1}, Co=Cg=20pF, Cl=25kohm, Fig. 2	−1.65		−1.30	V
Oscillation Start Time	t_{stt}	V_{SS}=−1.35V, Co=Cg=20pF, Cl=25kohm, Fig. 3			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

Operation form Li Battery [Static]

Absolute Maximum Ratings at Ta=25±2°C, V_{DD}=0V

				unit
Maximum Supply Voltage	V_{SS1}	V_{BAK}=V_{SS1} or V_{SS2}	−4.0 to +0.3	V
	V_{SS2}	V_{SS2}=V_{SS3}, V_{BAK}=V_{SS1} or V_{SS2}	−4.0 to +0.3	V
Maximum Input Voltage	V_{IN1}	10P, OSCIN, TEST3	V_{BAK}−0.3 to 0.3	V
	V_{IN2}	S1−4, M1−4, K1−4, P1−4, TEST1, TEST2, INT, RES (M1−4, P1−4: Input mode)	V_{SS2}−0.3 to 0.3	V
Maximum Output Voltage	V_{OUT1}	TEST3, CUP2, OSCOUT	V_{BAK}−0.3 to 0.3	V
	V_{OUT2}	SEGOUT, COM1, CUP1, ALARM, LIGHT, CNT1, CNT2, M1−4, P1−4 (M1−4, P1−4: Output mode)	V_{SS2}−0.3 to 0.3	V
Operating Temperature	Topg		−20 to +65	°C
Storage Temperature	Tstg		−30 to +125	°C

Allowable Operating Conditions at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Supply Voltage	V_{BAK}		−3.6		−1.3	V
	V_{SS2}	V_{SS2}=V_{SS3}	−3.6		−2.0	V
"H"-Level Input Voltage	V_{IH}	S1−4, K1−4, M1−4, P1−4, INT, RES (M1−4, P1−4: Input mode)	−0.4		0	V
"L"-Level Input Voltage	V_{IL}	" "	V_{SS2}		V_{SS2}+0.4	V
Operating Frequency	fopg	Ta=−20 to +65°C	32		33	kHz

Electrical Characteristics at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Input Resistance	R_{IN1A}	V_{SS2}=−2.9V, V_{IL}=V_{SS2}+0.4V, "L"-level hold tr., *1, Fig. 4	50		500	kohm
	R_{IN1B}	V_{SS2}=−2.9V, "L"-level pull-in tr., *1, Fig. 4	200		2000	kohm
	R_{IN2A}	V_{SS2}=−2.9V, V_{IL}=V_{SS2}+0.4V, input mode, "L"-level hold tr., *2, Fig. 4	50		500	kohm
	R_{IN2B}	V_{SS2}=−2.9V, input mode, "L"-level pull-in tr., *2, Fig. 4	200		2000	kohm
	R_{IN3}	V_{SS2}=−2.9V, TEST1, 2, RES	10		300	kohm
"H"-Level Output Voltage	V_{OH1}	V_{SS2}=−2.9V, I_{OH}=−0.4μA, SEGOUT	−0.2			V
"L"-Level Output Voltage	V_{OL1}	V_{SS2}=−2.9V, I_{OL}=0.4μA, SEGOUT			V_{SS2}+0.2	V
"H"-Level Output Voltage	V_{OH2}	V_{SS2}=−2.9V, I_{OH}=−4μA, COM1	−0.2			V
"L"-Level Output Voltage	V_{OL2}	V_{SS2}=−2.9V, I_{OL}=4μA, COM1			V_{SS2}+0.2	V
"H"-Level Output Voltage	V_{OH3}	V_{SS2}=−2.4V, I_{OH}=−250μA, ALM, CNT1, CNT2	−0.65			V
"L"-Level Output Voltage	V_{OL3}	V_{SS2}=−2.4V, I_{OL}=250μA, ALM, CNT1, CNT2			V_{SS2}+0.65	V
"H"-Level Output Voltage	V_{OH4}	V_{SS2}=−2.4V, I_{OH}=−150μA, LIGHT	−1.5			V
"L"-Level Output Voltage	V_{OL4}	V_{SS2}=−2.4V, I_{OL}=150μA, LIGHT			V_{SS2}+1.5	V
"H"-Level Output Voltage	V_{OH5}	V_{SS2}=−2.9V, I_{OH}=−40μA, M1−4, P1−4 (M1−4, P1−4: Output mode)	−0.4			V
"L"-Level Output Voltage	V_{OL5}	V_{SS2}=−2.9V, I_{OL}=40μA, M1−4, P1−4 (M1−4, P1−4: Output mode)			V_{SS2}+0.4	V
"H"-Level Output Voltage	V_{OH6}	V_{SS2}=−2.4V, I_{OH}=−10μA	−1	−0.3		V
"L"-Level Output Voltage	V_{OL6}	V_{SS2}=−2.4V, I_{OL}=40μA	V_{SS2}+0.3	V_{SS2}+1		V
"H"-Level Output Voltage	V_{OH7}	V_{SS2}=−2.4V, I_{OH}=−5μA	−1	−0.3		V
"L"-Level Output Voltage	V_{OL7}	V_{SS2}=−2.4V, I_{OL}=20μA	V_{SS2}+0.3	V_{SS2}+1		V
"H"-Level Output Voltage	V_{OH6}	V_{SS2}=−2.4V, I_{OH}=−10μA	−1	−0.3		V
Output OFF Leakage Current	I_{OFF}	V_{SS2}=−2.6V, V_{OUT}=V_{SS2}			1	μA

(Segment (output) port PAD No. 14 to 22, 57 to 64 QIP80pin No. 3 to 11, 43 to 50)

(Segment (output) port PAD No. 23 to 34, 65 to 77 QIP80 pin No. 12 to 23, 51 to 63)

(Segment (output) port PAD No. 14 to 22, 57 to 64 QIP80 pin No. 3 to 11, 43 to 50)

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			min	typ	max	unit
Output Voltage (halver)	V_{SS1}	V_{SS2}=−2.9V, C1=C2=0.1μF, fopg=32.768kHz			−1.35	V
Current Dissipation	I_{DD}	V_{SS2}=−2.9V, standard watch/clock operation, C1=C2=0.1μF, Co=Cg=20pF, Cl=25kohm, Fig. 5		1.0		V
Oscillation Start Voltage	V_{stt}	V_{SS1}=V_{SS2}, Co=Cg=20pF, Cl=25kohm, Fig. 6	−1.35			V
Oscillation Hold Voltage	V_{HOLD}	V_{BAK}=V_{SS1}≅V_{SS2}/2, Co=Cg=20pF, Cl=25kohm, Fig. 5			−2.6	V
Oscillation Start Time	t_{stt}	V_{SS1}=V_{SS2}=−2.9V, Co=Cg=20pF, Cl=25kohm, Fig. 6			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

Operation from EXTV [Static]

Absolute maximum Ratings at Ta=25±2°C, V_{DD}=0V

				unit
Maximum Supply Voltage	V_{SS2}	V_{SS2}=V_{SS3}	−4.0 to +0.3	V
Maximum Input Voltage	V_{IN1}	10P, OSCIN, TEST3	V_{SS1}−0.3 to 0.3	V
	V_{IN2}	S1−4, M1−4, K1−4, P1−4, TEST1, TEST2, INT, RES (M1−4, P1−4: Input mode)	V_{SS2}−0.3 to 0.3	V
Maximum Output Voltage	V_{OUT1}	TEST3, CUP2, OSCOUT	V_{SS1}−0.3 to 0.3	V
	V_{OUT2}	SEGOUT, COM1, CUP1, ALARM, LIGHT, CNT1, CNT2, M1−4, P1−4 (M1−4, P1−4: Output mode)	V_{SS2}−0.3 to 0.3	V
Operating Temperature	Topg		−20 to +65	°C
Storage Temperature	Tstg		−30 to +125	°C

Allowable Operating Conditions at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Supply Voltage	V_{SS2}	V_{SS2}=V_{SS3}	−3.6		−2.0	V
"H"-Level Input Voltage	V_{IH}	S1−4, M1−4, K1−4, P1−4, INT, RES, (M1−4, P1−4: Input mode)	−0.4		0	V
"L"-Level Input Voltage	V_{IL}	" "	V_{SS2}		V_{SS2}+0.4	V
Operating Frequency	fopg	Ta=−20 to +65°C	32		33	kHz

Electrical Characteristics at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Input Resistance	R_{IN1A}	V_{SS2}=−2.9V, V_{IL}=V_{SS2}+0.4, "L"-level hold tr., *1, Fig. 13	50		500	kohm
	R_{IN1B}	V_{SS2}=−2.9V, "L"-level pull-in tr., *1, Fig. 13	200		2000	kohm
	R_{IN2A}	V_{SS2}=−2.9V, V_{IL}=V_{SS2}+0.4V, input mode, "L"-level hold tr., *2, Fig. 13	50		500	kohm
	R_{IN2B}	V_{SS2}=−2.9V, input mode, "L"-level tr., *2, Fig. 13	200		2000	kohm
	R_{IN3}	V_{SS2}=−2.9V, TEST1, 2, RES	10		300	kohm
"H"-Level Output Voltage	V_{OH1}	V_{SS2}=−2.9V, I_{OH}=−0.4μA, SEGOUT	−0.2			V
"L"-Level Output Voltage	V_{OL1}	V_{SS2}=−2.9V, I_{OL}=0.4μA, SEGOUT			V_{SS2}+0.2	V
"H"-Level Output Voltage	V_{OH2}	V_{SS2}=−2.9V, I_{OH}=−4μA, COM1	−0.2			V
"L"-Level Output Voltage	V_{OL2}	V_{SS2}=−2.9V, I_{OL}=4μA, COM1			V_{SS2}+0.2	V
"H"-Level Output Voltage	V_{OH3}	V_{SS2}=−2.4V, I_{OH}=−250μA, ALM, LIGHT, CNT1, CNT2	−0.65			V
"L"-Level Output Voltage	V_{OL3}	V_{SS2}=−2.4V, I_{OL}=250μA, ALM, LIGHT, CNT1, CNT2			V_{SS2}+0.65	V
"H"-Level Output Voltage	V_{OH4}	V_{SS2}=−2.9V, I_{OH}=−40μA, M1−4, P1−4 (M1−4, P1−4: Output mode)	−0.4			V
"L"-Level Output Voltage	V_{OL4}	V_{SS2}=−2.9V, I_{OL}=40μA, M1−4, P1−4 (M1−4, P1−4: Output mode)			V_{SS2}+0.4	V
"H"-Level Output Voltage	V_{OH6}	V_{SS2}=−2.4V, I_{OH}=−10μA, Segment (output) port PAD No. 14 to 22, 57 to 64 QIP80 pin No. 3 to 11, 43 to 50	−1	−0.3		V
"L"-Level Output Voltage	V_{OL6}	V_{SS2}=−2.4V, I_{OL}=40μA, Segment (output) port PAD No. 14 to 22, 57 to 64 QIP80 pin No. 3 to 11, 43 to 50		V_{SS2}+0.3	V_{SS2}+1	V

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			min	typ	max	unit
"H"-Level Output Voltage	V_{OH7}	V_{SS2}=−2.4V, I_{OH}=−5μA, Segment (output port) PAD No. 23 to 34, 65 to 77 QIP80 pin No. 12 to 23, 51 to 63	−1	−0.3		V
"L"-Level Output Voltage	V_{OL7}	V_{SS2}=−2.4V, I_{OL}=20μA		V_{SS2}+0.3	V_{SS2}+1	V
"H"-Level Output Voltage	V_{OH6}	V_{SS2}=−2.4V, I_{OH}=−10μA, Segment PAD No. 14 to 22, 57 to 64 QIP80 pin No. 3 to 11, 43 to 50	−1	−0.3		V
Output OFF Leakage Current	I_{OFF}	V_{SS2}=−2.6V, V_{OUT}=V_{SS2}			1	μA
Current Dissipation	$\|I_{DD}\|$	V_{SS2}=−2.9V, standard watch/clock operation, Co=Cg=20pF, Cl=25kohm, Fig. 14		5.0		μA
Oscillation Start Voltage	V_{stt}	V_{SS1}=V_{SS2}, Co=Cg=20pF, Cl=25kohm, Fig. 15		−2.2		V
Oscillation Hold Voltage	V_{HOLD}	V_{BAK}=V_{SS2}, Co=Cg=20pF, Cl=25kohm, Fig. 14			−2.0	V
Oscillation Start Time	t_{stt}	V_{SS1}=V_{SS2}=−2.9V, Co=Cg=20pF, Cl=25kohm, Fig. 15			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

Operation from Ag Battery [1/2 bias, 1/2 duty]

Absolute Maximum Ratings at Ta=25±2°C, V_{DD}=0V

				unit
Maximum Supply Voltage	V_{SS1}		−4.0 to +0.3	V
	V_{SS2}	V_{SS}=V_{SS3}	−4.0 to +0.3	V
Maximum Input Voltage	V_{IN1}	S1–4, M1–4, K1–4, P1–4, TEST1–3, 10P OSCIN, INT, RES (M1–4, P1–4: Input mode)	V_{SS1}−0.3 to 0.3	V
Maximum Output Voltage	V_{OUT1}	TEST3, CUP2, OSCOUT, ALARM, LIGHT, CNT1, CNT2, M1–4, P1–4 (M1–4, P1–4: Output mode)	V_{SS1}−0.3 to 0.3	V
	V_{OUT2}	SEGOUT, COM1–2, CUP1	V_{SS2}−0.3 to 0.3	V
Operating Temperature	Topg		−20 to +65	°C
Storage Temperature	Tstg		−30 to +125	°C

Allowable Operating Conditions at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Supply Voltage	V_{SS1}		−1.65		−1.30	V
	V_{SS2}	V_{SS2}=V_{SS3}	−3.3		−2.4	V
"H"-Level Input Voltage	V_{IH}	S1–4, M1–4, P1–4, INT, RES (M1–4, P1–4: Input mode)	−0.2		0	V
"L"-Level Input Voltage	V_{IL}	" "	V_{SS1}		V_{SS1}+0.2	V
Operating Frequency	fopg	Ta=−20 to +65°C	32		33	kHz

Electrical Characteristics at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Input Resistance	R_{IN1A}	V_{SS1}=−1.55V, V_{IL}=V_{SS1}+0.2V, "L"-level hold tr., *1, Fig. 1	50		500	kohm
	R_{IN1B}	V_{SS1}=−1.55V, "L"-level pull-in tr., *1, Fig. 1	200		2000	kohm
	R_{IN2A}	V_{SS1}=−1.55V, V_{IL}=V_{SS1}+0.2V input mode, "L"-level hold tr., *2, Fig. 1	50		500	kohm
	R_{IN2B}	V_{SS1}=−1.55V, input mode, "L"-level hold tr., *2, Fig. 1	200		2000	kohm
	R_{IN3}	V_{SS1}=−1.55V, TEST1, 2, RES	10		300	kohm
"H"-Level Output Voltage	V_{OH1}	V_{SS1}=−1.55V, I_{OH}=−0.4μA, SEGOUT	−0.2			V
"L"-Level Output Voltage	V_{OL1}	V_{SS1}=−1.55V, I_{OL}=0.4μA, SEGOUT			V_{SS2}+0.2	V
"H"-Level Output Voltage	V_{OH2}	V_{SS1}=−1.55V, I_{OH}=−4μA, COM1–2	−0.2			V
"M"-Level Output Voltage	V_{OM}	V_{SS1}=−1.55V, I_{OH}=−4μA, I_{OL}=4μA, COM1–2	V_{SS1}−0.2		V_{SS1}+0.2	V
"L"-Level Output Voltage	V_{OL2}	V_{SS1}=−1.55V, I_{OL}=4μA, COM1–2			V_{SS2}+0.2	V

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			min	typ	max	unit
"H"-Level Output Voltage	V_{OH3}	V_{SS1}=−1.35V, I_{OH}=−250μA, ALM, LIGHT, CNT1, CNT2	−0.65			V
"L"-Level Output Voltage	V_{OL3}	V_{SS1}=−1.35V, I_{OL}=250μA, ALM, LIGHT, CNT1, CNT2			V_{SS1}+0.65	V
"H"-Level Output Voltage	V_{OH4}	V_{SS1}=−1.55V, I_{OH}=−20μA, M1−4, P1−4 (M1−4, P1−4: Output mode)	−0.2			V
"L"-Level Output Voltage	V_{OL4}	V_{SS1}=−1.55V, I_{OL}=20μA, M1−4, P1−4 (M1−4, P1−4: Output mode)			V_{SS1}+0.2	V
Output Voltage (doubler)	V_{SS2}	V_{SS1}=−1.35V, C1=C2=0.1μF, fopg=32.768kHz, Fig. 2			−2.5	V
Current Dissipation	I_{DD1}	V_{SS1}=−1.55V, standard watch/clock operation, C1=C2=0.1μF, Co=Cg=20pF, CI=25kohm, Fig. 2		2.0		μA
Oscillation Start Voltage	V_{stt}	Co=Cg=20pF, CI=25kohm, Fig. 3	−1.35			V
Oscillation Hold Voltage	V_{HOLD}	V_{BAK}=V_{SS1}, Co=Cg=20pF, CI=25kohm, Fig. 2	−1.65		−1.30	V
Oscillation Start Time	t_{stt}	V_{SS1}=−1.55V, Co=Cg=20pF, CI=25kohm, Fig. 3			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

Operation from LI Battery [1/2 bias, 1/2 duty]

Absolute Maximum Ratings at Ta=25±2°C, V_{DD}=0V

				unit
Maximum Supply Voltage	V_{SS1}	V_{BAK}=V_{SS1} or V_{SS2}	−4.0 to +0.3	V
	V_{SS2}	V_{SS2}=V_{SS3}, V_{BAK}=V_{SS1} or V_{SS2}	−4.0 to +0.3	V
Maximum Input Voltage	V_{IN1}	10P, OSCIN, TEST3	V_{BAK}−0.3 to 0.3	V
	V_{IN2}	S1−4, M1−4, K1−4, P1−4, TEST1, TEST2, INT, RES (M1−4, P1−4: Input mode)	V_{SS2}−0.3 to 0.3	V
Maximum Output Voltage	V_{OUT1}	TEST3, CUP2, OSCOUT	V_{BAK}−0.3 to 0.3	V
	V_{OUT2}	SEGOUT, COM1−2, CUP1, ALARM, LIGHT, CNT1, CNT2, M1−4, P1−4 (M1−4, P1−4: Output mode)	V_{SS2}−0.3 to 0.3	V
Operating Temperature	Topg		−20 to +65	°C
Storage Temperature	Tstg		−30 to +125	°C

Allowable Operating Conditions at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Supply Voltage	V_{BAK}		−3.6		−1.3	V
	V_{SS2}	V_{SS2}=V_{SS3}	−3.6		−2.0	V
"H"-Level Input Voltage	V_{IH}	S1−4, K1−4, M1−4, P1−4, INT, RES (M1−4, P1−4: Input mode)	−0.4		0	V
"L"-Level Input Voltage	V_{IL}	" "	V_{SS2}		V_{SS2}+0.4	V
Operating Frequency	fopg	Ta=−20 to +65°C	32		33	kHz

Electrical Characteristics at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Input Resistance	R_{IN1A}	V_{SS2}=−2.9V, V_{IL}=V_{SS2}+0.4, "L"-level hold tr., *1, Fig. 4	50		500	kohm
	R_{IN1B}	V_{SS2}=−2.9V, "L"-level pull-in tr., *1, Fig. 4	200		2000	kohm
	R_{IN2A}	V_{SS2}=−2.9V, V_{IL}=V_{SS2}+0.4V, input mode, "L"-level hold tr., *2, Fig. 4	50		500	kohm
	R_{IN2B}	V_{SS2}=−2.9V, input mode, "L"-level pull-in tr., *2, Fig. 4	200		2000	kohm
	R_{IN3}	V_{SS2}=−2.9V, TEST1, 2, RES	10		300	kohm
"H"-Level Output Voltage	V_{OH1}	V_{SS2}=−2.9V, I_{OH}=−0.4μA, SEGOUT	−0.2			V
"L"-Level Output Voltage	V_{OL1}	V_{SS2}=−2.9V, I_{OL}=0.4μA, SEGOUT			V_{SS2}+0.2	V
"H"-Level Output Voltage	V_{OH2}	V_{SS2}=−2.9V, I_{OH}=−4μA, COM1−2	−0.2			V
"M"-Level Output Voltage	V_{OM}	V_{SS2}=−2.9V, I_{OH}=−4μA, I_{OL}=4μA, COM1−2		V_{SS2}/2−0.2	V_{SS2}/2+0.2	V
"L"-Level Output Voltage	V_{OL2}	V_{SS2}=−2.9V, I_{OL}=4μA, COM1−2			V_{SS2}+0.2	V

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			min	typ	max	unit
"H"-Level Output Voltage	V_{OH3}	V_{SS2}=−2.4V, I_{OH}=−250μA, ALM, CNT1, CNT2	−0.65			V
"L"-Level Output Voltage	V_{OL3}	V_{SS2}=−2.4V, I_{OL}=250μA, ALM, CNT1, CNT2			V_{SS2}+0.65	V
"H"-Level Output Voltage	V_{OH4}	V_{SS2}=−2.4V, I_{OH}=−150μA, LIGHT	−1.5			V
"L"-Level Output Voltage	V_{OL4}	V_{SS2}=−2.4V, I_{OL}=150μA, LIGHT			V_{SS2}+1.5	V
"H"-Level Output Voltage	V_{OH5}	V_{SS2}=−2.9V, I_{OH}=−40μA, M1−4, P1−4 (M1−4, P1−4: Output mode)	−0.4			V
"L"-Level Output Voltage	V_{OL5}	V_{SS2}=−2.9V, I_{OL}=40μA, M1−4, P1−4 (M1−4, P1−4: Output mode)			V_{SS2}+0.4	V
"H"-Level Output Voltage	V_{OH6}	V_{SS2}=−2.4V, I_{OH}=−10μA, Segment ($^{output}_{port}$) PAD No. 14 to 22, 57 to 64 QIP80 pin No. 3 to 11, 43 to 50	−1	−0.3		V
"L"-Level Output Voltage	V_{OL6}	V_{SS2}=−2.4V, I_{OL}=40μA, Segment ($^{output}_{port}$) PAD No. 14 to 22, 57 to 64 QIP80 pin No. 3 to 11, 43 to 50		V_{SS2}+0.3	V_{SS2}+1	V
"H"-Level Output Voltage	V_{OH7}	V_{SS2}=−2.4V, I_{OH}=−5μA, Segment ($^{output}_{port}$) PAD No. 23 to 34, 65 to 77 QIP80 pin No. 12 to 23, 61 to 63	−1	−0.3		V
"L"-Level Output Voltage	V_{OL7}	V_{SS2}=−2.4V, I_{OL}=20μA, Segment ($^{output}_{port}$) PAD No. 23 to 34, 65 to 77 QIP80 pin No. 12 to 23, 61 to 63		V_{SS2}+0.3	V_{SS2}+1	V
"H"-Level Output Voltage	V_{OH6}	V_{SS2}=−2.4V, I_{OH}=−10μA, Segment PAD No. 14 to 22, 57 to 64 QIP80 pin No. 3 to 11, 43 to 50	−1	−0.3		V
Output OFF Leakage Current	I_{OFF}	V_{SS2}=−2.6V, V_{OUT}=V_{SS2}			1	μA
Output Voltage (halver)	V_{SS1}	V_{SS2}=−2.9V, C1=C2=0.1μF, fopg=32.768kHz, Fig. 5			−1.35	V
Current Dissipation	I_{DD1}	V_{SS2}=−2.9V, standard watch/clock operation, C1=C2=0.1μF, Co=Cg=20pF, Cl=25kohm, Fig. 5		1.0		μA
Oscillation Start Voltage	V_{stt}	V_{SS1}≅V_{SS2}, Co=Cg=20pF, Cl=25kohm, Fig. 6	−1.35			V
Oscillation Hold Voltage	V_{HOLD}	V_{BAK}=V_{SS1}=V_{SS2}/2, Co=Cg=20pF, Cl=25kohm, Fig. 5			−2.6	V
Oscillation Start Time	t_{stt}	V_{SS1}=V_{SS2}=−2.9V, Co=Cg=20pF, Cl=25kohm, Fig. 6			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

Operation from EXTV [1/2 bias, 1/2 duty]

Absolute Maximum Ratings at Ta=25±2°C, V_{DD}=0V

				unit
Maximum Supply Voltage	V_{SS1}		−4.0 to +0.3	V
	V_{SS2}	V_{SS2}=V_{SS3}	−4.0 to +0.3	V
Maximum Input Voltage	V_{IN1}	10P, OSCIN, TEST3	V_{SS1}−0.3 to 0.3	V
	V_{IN2}	S1−4, M1−4, K1−4, P1−4, TEST1, TEST2, INT, RES (M1−4, P1−4: Input mode)	V_{SS2}−0.3 to 0.3	V
Maximum Output Voltage	V_{OUT1}	TEST3, CUP2, OSCOUT	V_{SS1}−0.3 to 0.3	V
	V_{OUT2}	SEGOUT, COM1−2, CUP1, ALARM, LIGHT, CNT1, CNT2, M1−4, P1−4 (M1−4, P1−4: Output mode)	V_{SS2}−0.3 to 0.3	V
Operating Temperature	Topg		−20 to +65	°C
Storage Temperature	Tstg		−30 to +125	°C

Allowable Operating Conditions at Ta=25±2°C, V_{DD}=0V			min	typ	max	unit
Supply Voltage	V_{SS1}		−3.6		−1.3	V
	V_{SS2}	$V_{SS2}=V_{SS3}$	−3.6		−2.0	V
"H"-Level Input Voltage	V_{IH}	S1–4, M1–4, K1–4, P1–4, INT, RES (M1–4, P1–4: Input mode)	−0.4		0	V
"L"-Level Input Voltage	V_{IL}	" "	V_{SS2}		V_{SS2}+0.4	V
Operation Frequency	fopg	Ta=−20 to 65°C	32		33	kHz

Electrical Characteristics at Ta=25±2°C, V_{DD}=0V			min	typ	max	unit
Input Resistance	R_{IN1A}	V_{SS2}=−2.9V, $V_{IL}=V_{SS2}$+0.4V, "L"-level hold tr., *1, Fig. 4	50		500	kohm
	R_{IN1B}	V_{SS2}=−2.9V, "L"-level pull-in tr., *1, Fig. 4	200		2000	kohm
	R_{IN2A}	V_{SS2}=−2.9V, $V_{IL}=V_{SS2}$+0.4V, input mode, "L"-level hold tr., *2, Fig. 4	50		500	kohm
	R_{IN2B}	V_{SS2}=−2.9V, input mode, "L"-level pull-in tr., *2, Fig. 4	200		2000	kohm
	R_{IN3}	V_{SS2}=−2.9V, TEST1, 2, RES	10		300	kohm
"H"-Level Output Voltage	V_{OH1}	V_{SS2}=−2.9V, I_{OH}=−0.4μA, SEGOUT	−0.2			V
"L"-Level Output Voltage	V_{OL1}	V_{SS2}=−2.9V, I_{OL}=0.4μA, SEGOUT			V_{SS2}+0.2	V
"H"-Level Output Voltage	V_{OH2}	V_{SS2}=−2.9V, I_{OH}=−4μA, COM1–2	−0.2			V
"M"-Level Output Voltage	V_{OM}	V_{SS2}=−2.9V, I_{OH}=−4μA, I_{OL}=4μA, COM1–2	V_{SS2}/2−0.2		V_{SS2}/2+0.2	V
"L"-Level Output Voltage	V_{OL2}	V_{SS2}=−2.9V, I_{OL}=4μA, COM1–2			V_{SS2}+0.2	V
"H"-Level Output Voltage	V_{OH3}	V_{SS2}=−2.4V, I_{OH}=−250μA, ALM, LIGHT, CNT1, CNT2	−0.65			V
"L"-Level Output Voltage	V_{OL3}	V_{SS2}=−2.4V, I_{OL}=250μA, ALM, LIGHT, CNT1, CNT2			V_{SS2}+0.65	V
"H"-Level Output Voltage	V_{OH4}	V_{SS2}=−2.9V, I_{OH}=−40μA, M1–4, P1–4 (M1–4, P1–4: Output mode)	−0.4			V
"L"-Level Output Voltage	V_{OL4}	V_{SS2}=−2.9V, I_{OL}=40μA, M1–4, P1–4 (M1–4, P1–4: Output mode)			V_{SS2}+0.4	V
"H"-Level Output Voltage	V_{OH6}	V_{SS2}=−2.4V, I_{OH}=−10μA, Segment ($^{output}_{port}$) PAD No. 14 to 22, 57 to 64 QIP80 pin No. 3 to 11, 43 to 50	−1	−0.3		V
"L"-Level Output Voltage	V_{OL6}	V_{SS2}=−2.4V, I_{OL}=40μA, Segment ($^{output}_{port}$) PAD No. 14 to 22, 57 to 64 QIP80 pin No. 3 to 11, 43 to 50	V_{SS2}+0.3		V_{SS2}+1	V
"H"-Level Output Voltage	V_{OH7}	V_{SS2}=−2.4V, I_{OH}=6μA, Segment ($^{output}_{port}$) PAD No. 23 to 34, 65 to 77 QIP80 pin No. 12 to 23, 51 to 63	−1	−0.3		V
"L"-Level Output Voltage	V_{OL7}	V_{SS2}=−2.4V, I_{OL}=20μA, Segment ($^{output}_{port}$) PAD No. 23 to 34, 65 to 77 QIP80 pin No. 12 to 23, 51 to 63	V_{SS2}+0.3		V_{SS2}+1	V
"H"-Level Output Voltage	V_{OH8}	V_{SS2}=−2.4V, I_{OH}=−10μA, Segment PAD No. 14 to 22, 57 to 64 QIP80 pin No. 3 to 11, 43 to 50	−1	−0.3		V
Output OFF Leakage Current	I_{OFF}	V_{SS2}=−2.6V, $V_{OUT}=V_{SS2}$			1	μA
Output Voltage (halver)	V_{SS1}	V_{SS2}=−2.9V, C1=C2=0.1μF, fopg=32.768kHz, Fig. 5			−1.35	V
Current Dissipation	I_{DD1}	V_{SS2}=−2.9V, standard watch/clock operation, C1=C2=0.1μF, Co=Cg=20pF, Cl=25kohm, Fig. 5		5.0		μA
Oscillation Start Voltage	V_{stt}	$V_{SS1}=V_{SS2}$, Co=Cg=20pF, Cl=25kohm, Fig. 6	−2.2			V
Oscillation Hold Voltage	V_{HOLD}	$V_{BAK}=V_{SS2}$, Co=Cg=20pF, Cl=25kohm, Fig. 5			−2.0	V
Oscillation Start Time	t_{stt}	$V_{SS1}=V_{SS2}$=−2.9V, Co=Cg=20pF, Cl=25kohm, Fig. 6			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

Operation from Ag Battery [1/2 bias, 1/3 duty]

Absolute Maximum ratings at Ta=25±2°C, V_{DD}=0V

				unit
Maximum Supply Voltage	V_{SS1}		−4.0 to +0.3	V
	V_{SS2}	V_{SS2}=V_{SS3}	−4.0 to +0.3	V
Maximum Input Voltage	V_{IN1}	S1−4, M1−4, K1−4, P1−4, TEST1−3, 10P, OSCIN, INT, RES (M1−4, P1−4: Input mode)	V_{SS1}−0.3 to 0.3	V
Maximum Output Voltage	V_{OUT1}	TEST3, CUP2, OSCOUT, ALARM, LIGHT, CNT1, CNT2, M1−4, P1−4 (M1−4, P1−4: Output mode)	V_{SS1}−0.3 to 0.3	V
	V_{OUT2}	SEGOUT, COM1−3, CUP1	V_{SS2}−0.3 to 0.3	V
Operating Temperature	Topg		−20 to +65	°C
Storage Temperature	Tstg		−30 to +125	°C

Allowable Operating Conditions at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Supply Voltage	V_{SS1}		−1.65		−1.30	V
	V_{SS2}	V_{SS2}=V_{SS3}	−3.3		−2.4	V
"H"-Level Input Voltage	V_{IH}	S1−4, M1−4, K1−4, P1−4, INT, RES (M1−4, P1−4: Input mode)	−0.2		0	V
"L"-Level Input Voltage	V_{IL}	" "	V_{SS1}		V_{SS1}+0.2	V
Operating Frequency	fopg	Ta=−20 to +65°C	32		33	kHz

Electrical Characteristics at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Input Resistance	R_{IN1A}	V_{SS1}=−1.55V, V_{IL}=V_{SS1}+0.2V, "L"-level hold tr., *1, Fig. 1	50		500	kohm
	R_{IN1B}	V_{SS1}=−1.55V, "L"-level pull-in tr., *1, Fig. 1	200		2000	kohm
	R_{IN2A}	V_{SS1}=−1.55V, V_{IL}=V_{SS1}+0.2V, input mode, "L"-level hold tr., *2, Fig. 1	50		500	kohm
	R_{IN2B}	V_{SS1}=−1.55V, Input mode, "L"-level hold tr., *2, Fig. 1	200		2000	kohm
	R_{IN3}	V_{SS1}=−1.55V, TEST1, 2, RES	10		300	kohm
"H"-Level Output Voltage	V_{OH1}	V_{SS1}=−1.55V, I_{OH}=−0.4μA, SEGOUT	−0.2			V
"L"-Level Output Voltage	V_{OL1}	V_{SS1}=−1.55V, I_{OL}=0.4μA, SEGOUT			V_{SS2}+0.2	V
"H"-Level Output Voltage	V_{OH2}	V_{SS1}=−1.55V, I_{OH}=−4μA, COM1−3	−0.2			V
"M"-Level Output Voltage	V_{OM}	V_{SS1}=−1.55V, I_{OH}=−4μA, I_{OL}=4μA, COM1−3	V_{SS1}−0.2		V_{SS1}+0.2	V
"L"-Level Output Voltage	V_{OL2}	V_{SS1}=−1.55V, I_{OL}=4μA, COM1−3			V_{SS2}+0.2	V
"H"-Level Output Voltage	V_{OH3}	V_{SS1}=−1.35V, I_{OH}=−250μA, ALM, LIGHT, CNT1, CNT2	−0.65			V
"L"-Level Output Voltage	V_{OL3}	V_{SS1}=−1.35V, I_{OL}=250μA, ALM, LIGHT, CNT1, CNT2			V_{SS1}+0.65	V
"H"-Level Output Voltage	V_{OH4}	V_{SS1}=−1.55V, I_{OH}=−20μA, M1−4, P1−4 (M1−4, P1−4: Output mode)	−0.2			V
"L"-Level Output Voltage	V_{OL4}	V_{SS1}=−1.55V, I_{OL}=20μA, M1−4, P1−4 (M1−4, P1−4: Output mode)			V_{SS1}+0.2	V
Output Voltage (doubler)	V_{SS2}	V_{SS1}=−1.35V, C1=C2=0.1μF, fopg=32.768kHz, Fig. 2			−2.5	V
Current Dissipation	I_{DD}	V_{SS1}=−1.55V, standard watch/clock operation, C1=C2=0.1μF, Co=Cg=20pF, Cl=25kohm, Fig. 2		2.0		μA
Oscillation Start Voltage	V_{stt}	Co=Cg=20pF, Cl=25kohm, Fig. 3	−1.35			V
Oscillation Hold Voltage	V_{HOLD}	V_{BAK}=V_{SS1}, Co=Cg=20pF, Cl=25kohm, Fig. 2	−1.65		−1.30	V
Oscillation Start Time	t_{stt}	V_{SS1}=−1.35V, Co=Cg=20pF, Cl=25kohm, Fig. 3			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

Operation from LI Battery [1/2 bias, 1/3 duty]

Absolute Maximum Ratings at Ta=25±2°C, V_{DD}=0V

				unit
Maximum Supply Voltage	V_{SS1}	V_{BAK}=V_{SS1} or V_{SS2}	−4.0 to +0.3	V
	V_{SS2}	V_{SS2}=V_{SS3}, V_{BAK}=V_{SS1} or V_{SS2}	−4.0 to +0.3	V
Maximum Input Voltage	V_{IN1}	10P, OSCIN, TEST3	V_{BAK}−0.3 to 0.3	V
	V_{IN2}	S1−4, M1−4, K1−4, P1−4, TEST1, TEST2, INT, RES (M1−4, P1−4: Input mode)	V_{SS2}−0.3 to 0.3	V
Maximum Output Voltage	V_{OUT1}	TEST3, CUP2, OSCOUT	V_{BAK}−0.3 to 0.3	V
	V_{OUT2}	SEGOUT, COM1−3, CUP1, ALARM, LIGHT, CNT1, CNT2, M1−4, P1−4 (M1−4, P1−4: Output mode)	V_{SS2}−0.3 to 0.3	V
Operation Temperature	Topg		−20 to +65	°C
Storage Temperature	Tstg		−30 to +125	°C

Allowable Operating Conditions at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Supply Voltage	V_{BAK}		−3.6		−1.3	V
	V_{SS2}	V_{SS2}=V_{SS3}	−3.6		−2.0	V
"H"-Level Input Voltage	V_{IH}	S1−4, K1−4, M1−4, P1−4, INT RES (M1−4, P1−4: Input mode)	−0.4		0	V
"L"-Level Input Voltage	V_{IL}	" "	V_{SS2}		V_{SS2}+0.4	V
Operating Frequency	fopg	Ta=−20 to +65°C	32		33	kHz

Electrical Characteristics at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Input Resistance	R_{IN1A}	V_{SS2}=−2.9V, V_{IL}=V_{SS2}+0.4V, "L"-level hold tr., *1, Fig. 4	50		500	kohm
	R_{IN1B}	V_{SS2}=−2.9V, "L"-level pull-in tr., *1, Fig. 4	200		2000	kohm
	R_{IN2A}	V_{SS2}=−2.9V, V_{IL}=V_{SS2}+0.4V, input mode, "L"-level hold tr., *2, Fig. 4	50		500	kohm
	R_{IN2B}	V_{SS2}=−2.9V, input mode, "L"-level pull-in tr., *2, Fig. 4	200		2000	kohm
	R_{IN3}	V_{SS2}=−2.9V, TEST1, 2, RES	10		300	kohm
"H"-Level Output Voltage	V_{OH1}	V_{SS2}=−2.9V, I_{OH}=−0.4μA, SEGOUT	−0.2			V
"L"-Level Output Voltage	V_{OL1}	V_{SS2}=−2.9V, I_{OL}=0.4μA, SEGOUT			V_{SS2}+0.2	V
"H"-Level Output Voltage	V_{OH2}	V_{SS2}=−2.9V, I_{OH}=−4μA, COM1−3	−0.2			V
"M"-Level Output Voltage	V_{OM}	V_{SS2}=−2.9V, I_{OH}=−4μA, I_{OL}=4μA, COM1−3	V_{SS2}/2−0.2		V_{SS2}/2+0.2	V
"L"-Level Output Voltage	V_{OL2}	V_{SS2}=−2.9V, I_{OL}=4μA, COM1−3			V_{SS2}+0.2	V
"H"-Level Output Voltage	V_{OH3}	V_{SS2}=−2.4V, I_{OH}=−250μA, ALM, CNT1, CNT2	−0.65			V
"L"-Level Output Voltage	V_{OL3}	V_{SS2}=−2.4V, I_{OL}=250μA, ALM, CNT1, CNT2			V_{SS2}+0.65	V
"H"-Level Output Voltage	V_{OH4}	V_{SS2}=−2.4V, I_{OH}=−150μA, LIGHT	−1.5			V
"L"-Level Output Voltage	V_{OL4}	V_{SS2}=−2.4V, I_{OL}=150μA, LIGHT			V_{SS2}+1.5	V
"H"-Level Output Voltage	V_{OH5}	V_{SS2}=−2.9V, I_{OH}=−40μA, M1−4, P1−4 (M1−4, P1−4: Output mode)	−0.4			V
"L"-Level Output Voltage	V_{OL5}	V_{SS2}=−2.9V, I_{OH}=40μA, M1−4, P1−4 (M1−4, P1−4: Output mode)			V_{SS2}+0.4	V
"H"-Level Output Voltage	V_{OH6}	V_{SS2}=−2.4V, I_{OH}=−10μA, Segment (output port) PAD No. 14 to 22, 57 to 64 QIP80 pin No. 3 to 11, 43 to 50	−1	−0.3		V
"L"-Level Output Voltage	V_{OL6}	V_{SS2}=−2.4V, I_{OL}=40μA, Segment (output port) PAD No. 14 to 22, 57 to 64 QIP80 pin No. 3 to 11, 43 to 50	V_{SS2}+0.3		V_{SS2}+1	V
"H"-Level Output Voltage	V_{OH7}	V_{SS2}=−2.4V, I_{OH}=−5μA, Segment (output port) PAD No. 23 to 34, 65 to 77 QIP80 pin No. 12 to 23, 61 to 63	−1	−0.3		V
"L"-Level Output Voltage	V_{OL7}	V_{SS2}=−2.4V, I_{OL}=20μA, Segment (output port) PAD No. 23 to 34, 65 to 77 QIP80 pin No. 12 to 23, 61 to 63	V_{SS2}+0.3		V_{SS2}+1	V

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			min	typ	max	unit
"H"-Level Output Voltage	V_{OH6}	V_{SS2}=−2.4V, I_{OH}=−10μA, Segment PAD No. 14 to 22, 57 to 64 QIP80 pin No. 3 to 11, 43 to 50	−1	−0.3		V
Output OFF Leakage Current	I_{OFF}	V_{SS2}=−2.6V, V_{OUT}=V_{SS2}			1	μA
Output Voltage (halver)	V_{SS1}	V_{SS2}=−2.9V, C1=C2=0.1μF, fopg=32.768kHz			−1.35	V
Current Dissipation	I_{DD1}	V_{SS2}=−2.9V, standard watch/clock operation, C1=C2=0.1μF, Co=Cg=20pF, Cl=25kohm, Fig. 5		1.0		μA
Oscillation Start Voltage	V_{stt}	V_{SS1}=V_{SS2}, Co=Cg=20pF, Cl=25kohm, Fig. 6	−1.35			V
Oscillation Hold Voltage	V_{HOLD}	V_{BAK}=V_{SS1}=V_{SS2}/2, Co=Cg=20pF, Cl=25kohm, Fig. 5			−2.6	V
Oscillation Start Time	t_{stt}	V_{SS1}=V_{SS2}=−2.9V, Co=Cg=20pF, Cl=25kohm, Fig. 6			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

Operation from EXTV [1/2 bias, 1/3 duty]

Absolute Maximum Ratings at Ta=25±2°C, V_{DD}=0V

				unit
Maximum Supply Voltage	V_{SS1}		−4.0 to +0.3	V
	V_{SS2}	V_{SS2}=V_{SS3}	−4.0 to +0.3	V
Maximum Input Voltage	V_{IN1}	10P, OSCIN, TEST3	V_{SS1}−0.3 to 0.3	V
	V_{IN2}	S1−4, M1−4, K1−4, P1−4, TEST1, TEST2, INT, RES (M1−4, P1−4: Input mode)	V_{SS2}−0.3 to 0.3	V
Maximum Output Voltage	V_{OUT1}	TEST3, CUP2, OSCOUT	V_{SS1}−0.3 to 0.3	V
	V_{OUT2}	SEGOUT, COM1−3, CUP1, ALARM, LIGHT, CNT1, CNT2, M1−4, P1−4 (M1−4, P1−4: Output mode)	V_{SS2}−0.3 to 0.3	V
Operating Temperature	Topg		−20 to 65	°C
Storage Temperature	Tstg		−30 to +125	°C

Allowable Operating Conditions at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Supply Voltage	V_{SS1}		−3.6		−1.3	V
	V_{SS2}	V_{SS2}=V_{SS3}	−3.6		−2.0	V
"H"-Level Input Voltage	V_{IH}	S1−4, M1−4, K1−4, P1−4, INT, RES (M1−4, P1−4: Input mode)	−0.4		0	V
"L"-Level Input Voltage	V_{IL}	" "	V_{SS2}		V_{SS2}+0.4	V
Operating Frequency	fopg	Ta=−20 to +65°C	32		33	kHz

Electrical Characteristics at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Input Resistance	R_{IN1A}	V_{SS2}=−2.9V, V_{IL}=V_{SS2}+0.4V, "L"-level hold tr., *1, Fig. 4	50		500	kohm
	R_{IN1B}	V_{SS2}=−2.9V, "L"-level pull-in tr., *1, Fig. 4	200		2000	kohm
	R_{IN2A}	V_{SS2}=−2.9V, V_{IL}=V_{SS2}+0.4V, input mode, "L"-level hold tr., *1, Fig. 4	50		500	kohm
	R_{IN2B}	V_{SS2}=−2.9V, input mode, "L"-level tr., *1, Fig. 4	200		2000	kohm
	R_{IN3}	V_{SS2}=−2.9V, TEST1, 2, RES	10		300	kohm
"H"-Level Output Voltage	V_{OH1}	V_{SS2}=−2.9V, I_{OH}=−0.4μA, SEGOUT	−0.2			V
"L"-Level Output Voltage	V_{OL1}	V_{SS2}=−2.9V, I_{OL}=0.4μA, SEGOUT			V_{SS2}+0.2	V
"H"-Level Output Voltage	V_{OH2}	V_{SS2}=−2.9V, I_{OH}=−4μA, COM1−3	−0.2			V
"M"-Level Output Voltage	V_{OM}	V_{SS2}=−2.9V, I_{OH}=−4μA, I_{OL}=4μA, COM1−3	V_{SS2}/2−0.2		V_{SS2}/2+0.2	V
"L"-Level Output Voltage	V_{OL2}	V_{SS2}=−2.9V, I_{OL}=4μA, COM1−3			V_{SS2}+0.2	V
"H"-Level Output Voltage	V_{OH3}	V_{SS2}=−2.4V, I_{OH}=−250μA, ALM, LIGHT, CNT1, CNT2	−0.65			V
"L"-Level Output Voltage	V_{OL3}	V_{SS2}=−2.4V, I_{OL}=250μA ALM, LIGHT, CNT1, CNT2			V_{SS2}+0.65	V

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			min	typ	max	unit
"H"-Level Output Voltage	V_{OH4}	V_{SS2}=−2.9V, I_{OH}=−40μA, M1−4, P1−4 (M1−4, P1−4: Output mode)	−0.4			V
"L"-Level Output Voltage	V_{OL4}	V_{SS2}=−2.9V, I_{OL}=40μA, M1−4, P1−4 (M1−4, P1−4: Output mode)			V_{SS2}+0.4	V
"H"-Level Output Voltage	V_{OH6}	V_{SS2}=−2.4V, I_{OH}=−10μA, Segment (output) port PAD No. 14 to 22, 57 to 64 QIP80 pin No. 3 to 11, 43 to 50	−1	−0.3		V
"L"-Level Output Voltage	V_{OL6}	V_{SS2}=−2.4V, I_{OL}=40μA, Segment (output) port PAD No. 14 to 22, 57 to 64 QIP80 pin No. 3 to 11, 43 to 50		V_{SS2}+0.3	V_{SS2}+1	V
"H"-Level Output Voltage	V_{OH7}	V_{SS2}=−2.4V, I_{OH}=−5μA, Segment (output) port PAD No. 23 to 34, 65 to 77 QIP80 pin No. 12 to 23, 61 to 63	−1	−0.3		V
"L"-Level Output Voltage	V_{OL7}	V_{SS2}=−2.4V, I_{OL}=20μA, Segment (output) port PAD No. 23 to 34, 65 to 77 QIP80 pin No. 12 to 23, 61 to 63		V_{SS2}+0.3	V_{SS2}+1	V
"H"-Level Output Voltage	V_{OH6}	V_{SS2}=−2.4V, I_{OH}=−10μA, Segment PAD No. 14 to 22, 57 to 64 QIP80 pin No. 3 to 11, 43 to 50	−1	−0.3		V
Output OFF Leakage Current	I_{OFF}	V_{SS2}=−2.6V, V_{OUT}=V_{SS2}			1	μA
Output Voltage (halver)	V_{SS1}	V_{SS2}=−2.9V, C1=C2=0.1μF, fopg=32.768kHz			−1.35	V
Current Dissipation	I_{DD1}	V_{SS2}=−2.9V, standard watch/clock operation, C1=C2=0.1μF, Co=Cg=20pF, Cl=25kohm, Fig. 5		5.0		μA
Oscillation Start Voltage	V_{stt}	V_{SS1}=V_{SS2}, Co=Cg=20pF, Cl=25kohm, Fig. 6	−2.2			V
Oscillation Hold Voltage	V_{HOLD}	V_{BAK}=V_{SS2}, Co=Cg=20pF, Cl=25kohm, Fig. 6			−2.0	V
Oscillation Start Time	t_{stt}	V_{SS1}=V_{SS2}=−2.9V, Co=Cg=20pF, Cl=25kohm, Fig. 6			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

Operation from Ag Battery [1/3 bias, 1/3 duty]

Absolute Maximum Ratings at Ta=25±2°C, V_{DD}=0V

				unit
Maximum Supply Voltage	V_{SS1}		−4.0 to +0.3	V
	V_{SS2}		−4.0 to +0.3	V
	V_{SS3}		−5.5 to +0.3	V
Maximum Input Voltage	V_{IN1}	S1−4, M1−4, K1−4, P1−4, TEST1−3, 10P, OSCIN, INT, RES (M1−4, P1−4: Input mode)	V_{SS1}−0.3 to 0.3	V
Maximum Output Voltage	V_{OUT1}	TEST3, CUP2, OSCOUT, ALARM, LIGHT, CNT1, CNT2, M1−4, P1−4 (M1−4, P1−4: Output mode)	V_{SS1}−0.3 to 0.3	V
	V_{OUT2}	SEGOUT, COM1, COM2, COM3, CUP1	V_{SS3}−0.3 to 0.3	V
Operating Temperature	Topg		−20 to +65	°C
Storage Temperature	Tstg		−30 to +125	°C

Allowable Operating Conditions at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Supply Voltage	V_{SS1}		−1.65		−1.30	V
	V_{SS2}		−3.3		−2.4	V
	V_{SS3}		−4.95		−3.7	V
"H"-Level Input Voltage	V_{IH}	S1−4, M1−4, K1−4, P1−4, INT, RES (M1−4, P1−4: Input mode)	−0.2		0	V
"L"-Level Input Voltage	V_{IL}	" "	V_{SS1}		V_{SS1}+0.2	V
Operating Frequency	fopg	Ta=−20 to +65°C	32		33	kHz

Electrical Characteristics at Ta=25±2°C, V_{DD}=0V			min	typ	max	unit
Input Resistance	R_{IN1A}	V_{SS1}=−1.55V, V_{IL}=V_{SS1}+0.2V, "L"-level hold tr., *1, Fig. 7	50		500	kohm
	R_{IN1B}	V_{SS1}=−1.55V, "L"-level pull-in tr., *1, Fig. 7	200		2000	kohm
	R_{IN2A}	V_{SS1}=−1.55V, V_{IL}=V_{SS1}+0.2V, input mode, "L"-level hold tr., *2, Fig. 7	50		500	kohm
	R_{IN2B}	V_{SS1}=−1.55V, input mode, "L"-level pull-in tr., *2, Fig. 7	200		2000	kohm
	R_{IN3}	V_{SS1}=−1.55V, TEST1, 2, RES	10		300	kohm
"H"-Level Output Voltage	V_{OH1}	V_{SS1}=−1.55V, I_{OH}=−0.4μA, SEGOUT	−0.2			V
"M1"-Level Output Voltage	V_{OM1-1}	V_{SS1}=−1.55V, I_{OH}=−0.4μA,	V_{SS1}−0.2		V_{SS1}+0.2	V
"M2"-Level Output Voltage	V_{OM2-1}	I_{OL}=0.4μA, SEGOUT	V_{SS2}−0.2		V_{SS2}+0.2	V
"L"-Level Output Voltage	V_{OL1}	V_{SS1}=−1.55V, I_{OL}=−0.4μA, SEGOUT	V_{SS3}−0.2		V_{SS3}+0.2	V
"H"-Level Output Voltage	V_{OH2}	V_{SS1}=−1.55V, I_{OH}=−4μA, COM1, COM2, COM3	−0.2			V
"M1"-Level Output Voltage	V_{OM1-2}	V_{SS1}=−1.55V, I_{OL}=4μA,	V_{SS1}−0.2		V_{SS1}+0.2	V
"M2"-Level Output Voltage	V_{OM2-2}	I_{OH}=−4μA, COM1, COM2, COM3	V_{SS2}−0.2		V_{SS2}+0.2	V
"L"-Level Output Voltage	V_{OL2}	V_{SS1}=−1.55V, I_{OL}=4μA, COM1−3			V_{SS3}+0.2	V
"H"-Level Output Voltage	V_{OH3}	V_{SS1}=−1.35V, I_{OH}=−250μA, ALM, LIGHT, CNT1, CNT2	−0.65			V
"L"-Level Output Voltage	V_{OL3}	V_{SS1}=−1.35V, I_{OL}=250μA, ALM, LIGHT CNT1, CNT2			V_{SS1}+0.65	V
"H"-Level Output Voltage	V_{OH4}	V_{SS1}=−1.55V, I_{OH}=−20μA, M1−4, P1−4 (M1−4, P1−4: Output mode)	−0.2			V
"L"-Level Output Voltage	V_{OL4}	V_{SS1}=−1.55V, I_{OL}=20μA, (M1−4, P1−4: Output mode)			V_{SS1}+0.2	V
Output Voltage	V_{SS2}	V_{SS1}=−1.35V, C1 to C3=0.1μF, fopg=32.768kHz, Fig. 8			−2.5	V
	V_{SS3}				−3.75	V
Current Dissipation	I_{DD1}	V_{SS1}=−1.55V, standard watch/clock operation, C1 to C3=0.1μF, Co=Cg=20pF, CI=25kohm, Fig. 8		3.5		μA
Oscillation Start Voltage	V_{stt}	Co=Cg=20pF, CI=25kohm, Fig. 9	−1.35			V
Oscillation Hold Voltage	V_{HOLD}	V_{BAK}=V_{SS1}, Co=Cg=20pF, CI=25kohm, Fig. 8	−1.65		−1.30	V
Oscillation Start Time	t_{stt}	V_{SS1}=−1.35V, Co=Cg=20pF, CI=25kohm, Fig. 9			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

Operating from Li Battery [1/3 bias, 1/3 duty]

Absolute Maximum Ratings at Ta=25±2°C, V_{DD}=0V				unit
Maximum Supply Voltage	V_{SS1}	V_{BAK}=V_{SS1} or V_{SS2}	−4.0 to +0.3	V
	V_{SS2}	V_{BAK}=V_{SS1} or V_{SS2}	−4.0 to +0.3	V
	V_{SS3}	V_{BAK}=V_{SS1} or V_{SS2}	−5.5 to +0.3	V
Maximum Input Voltage	V_{IN1}	10P, OSCIN, TEST3	V_{BAK}−0.3 to 0.3	V
	V_{IN2}	S1−4, M1−4, K1−4, P1−4, TEST1, TEST2, INT, RES (M1−4, P1−4: Input mode)	V_{SS2}−0.3 to 0.3	V
Maximum Output Voltage	V_{OUT1}	TEST3, OSCOUT	V_{BAK}−0.3 to 0.3	V
	V_{OUT2}	ALARM, LIGHT, CNT1, CNT2, M1−4, P1−4, CUP2 (M1−4, P1−4: Output mode)	V_{SS2}−0.3 to 0.3	V
	V_{OUT3}	SEGOUT 1−64, COM1 to COM3, CUP1	V_{SS3}−0.3 to 0.3	V
Operating Temperature	Topg		−20 to +65	°C
Storage Temperature	Tstg		−30 to +125	°C

Allowable Operating Conditions at Ta=25±2°C, V_{DD}=0V,			min	typ	max	unit
Supply Voltage	V_{BAK}		−3.6		−1.3	V
	V_{SS2}		−3.6		−2.0	V
	V_{SS3}	V_{SS3}≅V_{SS2}+V_{SS1}	−5.0		−3.9	V
"H"-Level Input Voltage	V_{IH}	S1−4, M1−4, K1−4, P1−4, INT, RES (M1−4, P1−4: Input mode)	−0.4		0	V
"L"-Level Input Voltage	V_{IL}	" "	V_{SS2}		V_{SS2}+0.4	V
Operating Frequency	fopg	Ta=−20 to +65°C	32		33	kHz

Electrical Characteristics at Ta=25±2°C, V_{DD}=0V			min	typ	max	unit
Input Resistance	R_{IN1A}	V_{SS2}=−2.9V, V_{IL}=V_{SS2}+0.4V, "L"-level hold tr., *1, Fig. 10	50		500	kohm
	R_{IN1B}	V_{SS2}=−2.9V, "L"-level pull-in tr., *1, Fig. 10	200		2000	kohm
	R_{IN2A}	V_{SS2}=−2.9V, V_{IL}=V_{SS2}+0.4V, input mode, "L"-level hold tr., *2, Fig. 10	50		500	kohm
	R_{IN2B}	V_{SS2}=−2.9V, input mode, "L"-level pull-in tr., *2, Fig. 10	200		2000	kohm
	R_{IN3}	V_{SS2}=−2.9V, TEST1, 2, RES	10		300	kohm
"H"-Level Output Voltage	V_{OH1}	V_{SS2}=−2.9V, I_{OH}=−0.4μA, SEGOUT	−0.2			V
"M1"-Level Output Voltage	$V_{OM1\text{-}1}$	V_{SS2}=−2.9V, I_{OH}=−0.4μA, I_{OL}=0.4μA, SEGOUT	1/2V_{SS2}−0.2		1/2V_{SS2}+0.2	V
"M2"-Level Output Voltage	$V_{OM2\text{-}1}$		V_{SS2}−0.2		V_{SS2}+0.2	V
"L"-Level Output Voltage	V_{OL1}	V_{SS2}=−2.9V, I_{OL}=0.4μA, SEGOUT			V_{SS3}+0.2	V
"H"-Level Output Voltage	V_{OH2}	V_{SS2}=−2.9V, I_{OH}=−4μA, COM1−3	−0.2			V
"M1"-Level Output Voltage	$V_{OM1\text{-}2}$	V_{SS2}=−2.9V, I_{OH}=−4μA, I_{OL}=4μA, COM1, COM2, COM3	1/2V_{SS2}−0.2		1/2V_{SS2}+0.2	V
"M2"-Level Output Voltage	$V_{OM2\text{-}2}$		V_{SS2}−0.2		V_{SS2}+0.2	V
"L"-Level Output Voltage	V_{OL2}	V_{SS2}=−2.9V, I_{OL}=4μA, COM1−3			V_{SS3}+0.2	V
"H"-Level Output Voltage	V_{OH3}	V_{SS2}=−2.4V, I_{OH}=−250μA, ALM, CNT1, CNT2	−0.65			V
"L"-Level Output Voltage	V_{OL3}	V_{SS2}=−2.4V, I_{OL}=250μA, ALM, CNT1, CNT2			V_{SS}+0.65	V
"H"-Level Output Voltage	V_{OH4}	V_{SS2}=−2.4V, I_{OH}=−150μA, LIGHT	−1.5			V
"L"-Level Output Voltage	V_{OL4}	V_{SS2}=−2.4V, I_{OL}=150μA, LIGHT			V_{SS2}+1.5	V
"H"-Level Output Voltage	V_{OH5}	V_{SS2}=−2.9V, I_{OH}=−40μA, M1−4, P1−4 (M1−4, P1−4: Output mode)	−0.4			V
"L"-Level Output Voltage	V_{OL5}	V_{SS2}=−2.9V, I_{OL}=40μA, M1−4, P1−4 (M1−4, P1−4: Output mode)			V_{SS2}+0.4	V
"H"-Level Output Voltage	V_{OH6}	V_{SS2}=−2.4V, I_{OH}=−10μA, Segment (output) port PAD No. 14 to 22, 57 to 64 QIP80 pin No. 3 to 11, 43 to 50	−1	−0.3		V
"L"-Level Output Voltage	V_{OL6}	V_{SS2}=−2.4V, I_{OL}=40μA, Segment (output) port PAD No. 14 to 22, 57 to 64 QIP80 pin No. 3 to 11, 43 to 50	V_{SS2}+0.3		V_{SS2}+1	V
"H"-Level Output Voltage	V_{OH7}	V_{SS2}=−2.4V, I_{OH}=−5μA, Segment (output) port PAD No. 23 to 34, 65 to 77 QIP80 pin No. 12 to 23, 51 to 63	−1	−0.3		V
"L"-Level Output Voltage	V_{OL7}	V_{SS2}=−2.4V, I_{OL}=20μA, Segment (output) port PAD No. 23 to 34, 65 to 77 QIP80 pin No. 12 to 23, 51 to 63	V_{SS2}+0.3		V_{SS2}+1	V
"H"-Level Output Voltage	V_{OH6}	V_{SS2}=−2.4V, I_{OH}=−10μA, Segment PAD No. 14 to 22, 57 to 64 QIP80 pin No. 3 to 11, 43 to 50	−1	−0.3		V
Output OFF Leakage Cuttent	I_{OFF}	V_{SS2}=−2.6V, V_{OUT}=V_{SS2}			1	μA
Output Voltage	V_{SS1}	V_{SS2}=−2.9V, C1 to C4=0.1μF, fopg=32.768kHz, Fig. 11			−1.35	V
	V_{SS3}				−4.1	V
Current Dissipation	I_{DD1}	V_{SS2}=−2.9V, standard watch/clock operation, C1 to C4=0.1μF, Co=Cg=20pF, CI=250kohm, Fig. 11		2.0		μA
Oscillation Start Voltage	V_{stt}	V_{SS1}=V_{SS2}, Co=Cg=20pF, CI=250kohm, Fig. 12	−1.35			V

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			min	typ	max	unit
Oscillation Hold Voltage	V_{HOLD}	$V_{BAK}=V_{SS1}=V_{SS2}/2$, Co=Cg=20pF, Cl=250kohm, Fig. 11			−2.6	V
Oscillation Start Time	t_{stt}	V_{SS2}=−2.9V, $V_{SS1}=V_{SS2}$, Co=Cg=20pF, Cl=25kohm, Fig. 12			10	sec
Oscillation Correction Capacitance	10P	External pin	8	10	12	pF
	20P	OSCOUT	16	20	24	pF

Operation from EXTV [1/3 bias, 1/3 duty]

Absolute Maximum Ratings at Ta=25±2°C, V_{DD}=0V

				unit
Maximum Supply Voltage	V_{SS1}		−4.0 to +0.3	V
	V_{SS2}		−4.0 to +0.3	V
	V_{SS3}		−5.5 to +0.3	V
Maximum Input Voltage	V_{IN1}	10P, OSCIN, TEST3	V_{SS1}−0.3 to 0.3	V
	V_{IN2}	S1–4, M1–4, K1–4, P1–4, TEST1, 2, INT, RES (M1–4, P1–4: Input mode)	V_{SS1}−0.3 to 0.3	V
Maximum Output Voltage	V_{OUT1}	TEST3, OSCOUT	V_{SS1}−0.3 to 0.3	V
	V_{OUT2}	ALRM, LIGHT, CNT1, CNT2, M1–4, P1–4, CUP2 (M1–4, P1–4: Output mode)	V_{SS2}−0.3 to 0.3	V
	V_{OUT3}	SEGOUT1–64, COM1 to COM3, CUP1	V_{SS3}−0.3 to 0.3	V
Operating Temperature	Topg		−20 to +65	°C
Storage Temperature	Tstg		−30 to +125	°C

Allowable Operating Conditions at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Supply Voltage	V_{SS1}		−3.6		−1.3	V
	V_{SS2}		−3.6		−2.0	V
	V_{SS3}	$V_{SS3}=V_{SS2}+V_{SS1}$	−5.0		−3.9	V
"H"-Level Input Voltage	V_{IH}	S1–4, M1–4, K1–4, INT, RES (M1–4, P1–4: Input mode)	−0.4		0	V
"L"-Level Input Voltage	V_{IL}	" "	V_{SS2}		V_{SS2}+0.4	V
Operating Frequency	fopg	Ta=−20 to +65°C	32		33	kHz

Electrical Characteristics at Ta=25±2°C, V_{DD}=0V

			min	typ	max	unit
Input Resistance	R_{IN1A}	V_{SS2}=−2.9V, $V_{IL}=V_{SS2}$+0.4V, "L"-level hold tr., *1, Fig. 10	50		500	kohm
	R_{IN1B}	V_{SS2}=−2.9V, "L"-level pull-in tr., *1, Fig. 10	200		2000	kohm
	R_{IN2A}	V_{SS2}=−2.9V, $V_{IL}=V_{SS2}$+0.4V, input mode, "L"-level hold tr., *2, Fig. 10	50		500	kohm
	R_{IN2B}	V_{SS2}=−2.9V, input mode, "L"-level pull-in tr., *2, Fig. 10	200		2000	kohm
	R_{IN3}	V_{SS2}=−2.9V, TEST1, 2, RES	10		300	kohm
"H"-Level Output Voltage	V_{OH1}	V_{SS2}=−2.9V, I_{OH}=−0.4μA, SEGOUT	−0.2			V
"M1"-Level Output Voltage	V_{OM1-1}	V_{SS2}=−2.9V, I_{OH}=−0.4μA,	1/2V_{SS2}−0.2		1/2V_{SS2}+0.2	V
"M2"-Level Output Voltage	V_{OM2-1}	I_{OL}=0.4μA, SEGOUT	V_{SS2}−0.2		V_{SS2}+0.2	V
"L"-Level Output Voltage	V_{OL1}	V_{SS2}=−2.9V, I_{OL}=0.4μA, SEGOUT			V_{SS3}+0.2	V
"H"-Level Output Voltage	V_{OH2}	V_{SS2}=−2.9V, I_{OH}=−4μA, COM1, COM2, COM3	−0.2			V
"M1"-Level Output Voltage	V_{OM1-2}	V_{SS2}=−2.9V, I_{OH}=−4μA,	1/2V_{SS2}−0.2		1/2V_{SS2}+0.2	V
"M2"-Level Output Voltage	V_{OM2-2}	I_{OL}=4μA, COM1, COM2, COM3	V_{SS2}−0.2		V_{SS2}+0.2	V
"L"-Level Output Voltage	V_{OL2}	V_{SS2}=−2.9V, I_{OL}=4μA, COM1, COM2, COM3			V_{SS2}+0.2	V
"H"-Level Output Voltage	V_{OH3}	V_{SS2}=−2.4V, I_{OH}=−250μA, ALM, LIGHT, CNT1, CNT2	−0.65			V
"L"-Level Output Voltage	V_{OL3}	V_{SS2}=−2.4V, I_{OL}=250μA, ALM, LIGHT, CNT1, CNT2			V_{SS2}+0.65	V
"H"-Level Output Voltage	V_{OH4}	V_{SS2}=−2.9V, I_{OH}=−40μA, M1–4, P1–4 (M1–4, P1–4: Output mode)	−0.4			V
"L"-Level Output Voltage	V_{OL4}	V_{SS2}=−2.9V, I_{OL}=40μA, M1–4, P1–4 (M1–4, P1–4: Output mode)			V_{SS2}+0.4	V

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				min	typ	max	unit
"H"-Level Output Voltage	V_{OH6}	V_{SS2}=–2.4V, I_{OH}=–10μA	Segment PAD No. 14 to 22, 57 to 64 QIP80 pin No. 3 to 11, 43 to 50	–1	–0.3		V
"L"-Level Output Voltage	V_{OL6}	V_{SS2}=–2.4V, I_{OL}=40μA		V_{SS2}+0.3		V_{SS2}+1	V
"H"-Level Output Voltage	V_{OH7}	V_{SS2}=–2.4V, I_{OH}=–5μA	Segment (output port) PAD No. 23 to 34, 65 to 77 QIP80 pin No. 12 to 23, 51 to 63	–1	–0.3		V
"L"-Level Output Voltage	V_{OL7}	V_{SS2}=–2.4V, I_{OL}=20μA		V_{SS2}+0.3		V_{SS2}+1	V
"H"-Level Output Voltage	V_{OH6}	V_{SS2}=–2.4V, I_{OH}=–10μA	Segment PAD No. 14 to 22, 57 to 64 QIP80 pin No. 3 to 11, 43 to 50	–1	–0.3		V
Output OFF Leakage Current	I_{OFF}	V_{SS2}=–2.6V, V_{OUT}=V_{SS2}				1	μA
Output Voltage	V_{SS1}	V_{SS2}=–2.9V, C1 to C4=0.1μF, fopg=32.768kHz, Fig. 11				–1.35	V
	V_{SS3}					4.1	V
Current Dissipation	IIDDI	V_{SS2}=–2.9V, standard watch/clock operation, C1 to C4=0.1μF, Co=Cg=20pF, Cl=250kohm, Fig. 11			5.0		μA
Oscillation Start Voltage	V_{stt}	V_{SS1}=V_{SS2}, Co=Cg=20pF, Cl=25kohm, Fig. 12		–2.2			V
Oscillation Hold Voltge	V_{HOLD}	V_{BAK}=V_{SS2}, Co=Cg=20pF, Cl=25kohm, Fig. 11				–2.0	V
Oscillation Start Time	t_{stt}	V_{SS2}=–2.9V, V_{SS1}=V_{SS2}, Co=Cg=20pF, Cl=25kohm, Fig. 12				10	sec
Oscillation Correction Capacitance	10P	External pin		8	10	12	pF
	20P	OSCOUT		18	20	24	pF

*1 S1· S2· S3· S4· INT· K1· K2· K3· K4

*2 M1· M2· M3· M4· P1· P2· P3· P4

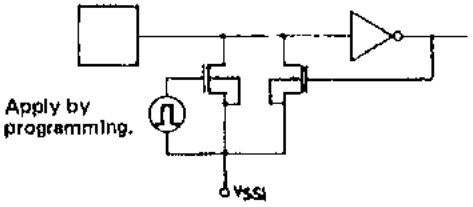

Fig. 1 Input configuration of S1–4, M1–4, K1–4, P1–4, INT

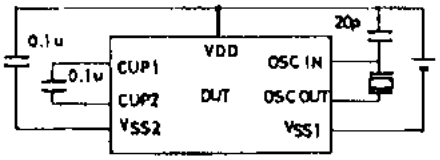

Fig. 2 Output voltage, current dissipation, oscillation hold voltage test circuit

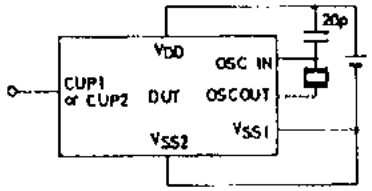

Fig. 3 Oscillation start voltage, oscillation start time, frequency stability test circuit

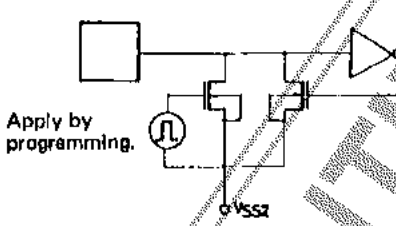

Fig. 4 Input configuration S1–4, M1–4, K1–4, P1–4, INT

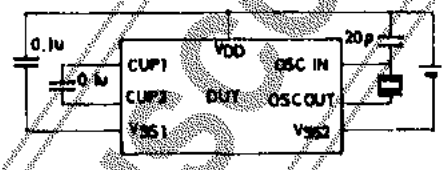

Fig. 5 Output voltage, current dissipation, oscillation hold voltage test circuit

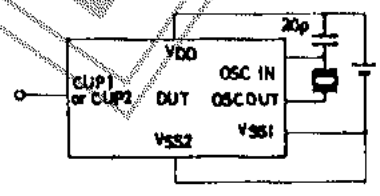

Fig. 6 Oscillation start voltage, oscillation start time, frequency stability test circuit

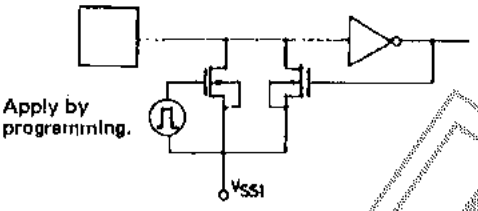

Fig. 7 Input configuration of S1–4, M1–4, K1–4, P1–4, INT

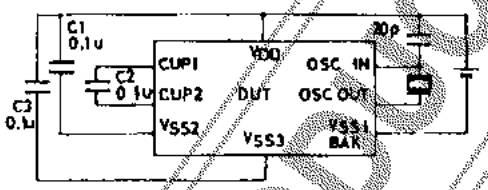

Fig. 8 Output voltage, current dissipation, oscillation hold voltage test circuit

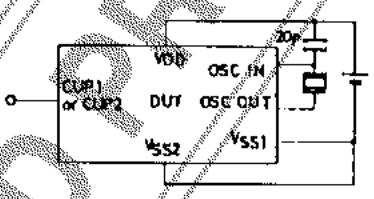

Fig. 9 Oscillation start voltage, oscillation start time, frequency stability test circuit

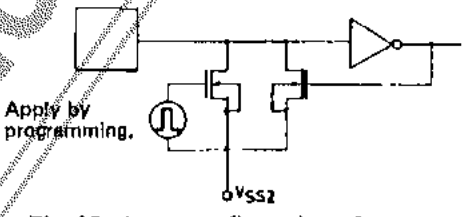

Fig. 10 Input configuration of S1–4, M1–4, K1–4, P1–4, INT

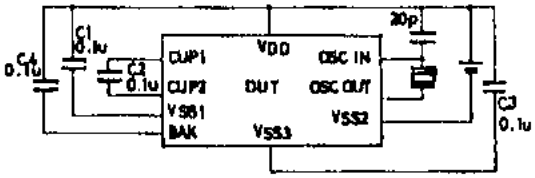

Fig. 11 Output voltage, current dissipation, oscillation hold voltage test circuit

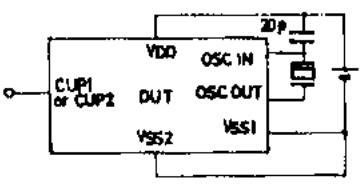

Fig. 12 Oscillation start voltage, oscillation start time, frequency stability test circuit

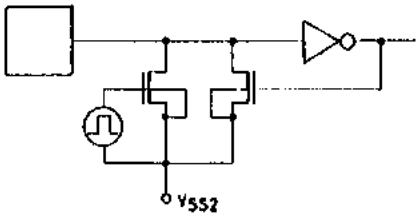

Fig. 13 Input configuration
S1–4, M1–4, K1–4, P1–4, INT

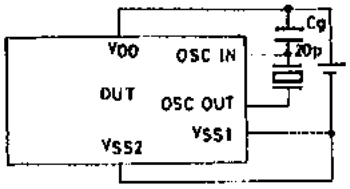

Fig. 14 Output voltage, current dissipation, oscillation hold voltage test circuit

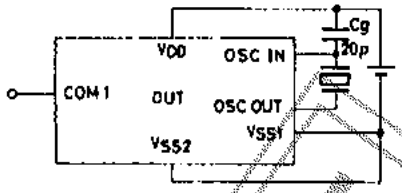

Fig. 15 Oscillation start voltage, oscillation start time, frequency stability test circuit

INSTRUCTION SET OF LC5800

Summary of LC5800 Instructions

Symbol	Description
AC	: Accumulator
ACn	: Accumulator-bit n
CF	: Carry flag
DP	: Data pointer
DPF	: Data pointer flag
SP	: Strobe pointer
PC	: Program counter
(P( ))	: Contents of port ( )
Rx	: Memory of address x
Rxn	: Memory-bit n of address x
IEFn	: Interrupt enable flag n
WRFn	: Working register n
E/S F	: Interrupt/switch select flag
BCF	: Bakup flag
SCFn	: Start condition flag n
PDF	: Pull-down flag

Symbol	
HQF	: Halt request flag
HEFn	: Halt release enable flag
HRFn	: Halt release request flag
CC	: Chrono counter
LSF	: Lap sample flag
LPF	: Lap mode flag
CSTF	: Chrono start flag
CMF	: Chrono mode flag
CDF	: Chrono data decoder flag
TM	: Timer
L	: LCD latch
( )	: Contents
←	: Transfer direction, result
∧	: AND
∨	: OR
∀	: Exclusive OR

Instruction group	Mnemonic		Instruction code D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 / D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Function	Description	Status flag to be affected
Accumulator manipulation instructions, memory manipulation instructions	CLA	Clear AC	0 1 0 1 1 0 1 0 / 0 0 0 0 0 0 0 0	AC ← 0	The AC contents are cleared.	
	RCF	Reset CF	1 1 1 0 1 1 0 0 / 0 0 0 0 0 0 0 1	CF ← 0 ≡RF1-1	The CF contents are cleared.	CF
	SCF	Set CF	1 1 1 0 1 0 0 0 / 0 0 0 0 0 0 0 1	CF ← 1 ≡SF1-1	The CF is set.	CF
	MRW Y, X	Move Rx to Working Register R_Y	0 1 1 0 0 0 Y_2 Y_1 / Y_0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC, R_Y ← (Rx)	The memory (Rx) contents are loaded to the AC and working register (Ry).	
	MWR X, Y	Move Working Register R_Y to R_x	0 1 1 0 0 1 Y_2 Y_1 / Y_0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC, Rx ← (R_Y)	The working register (Ry) contents are loaded to the AC and memory (Rx).	
	SR0 X	Shift Right Rx & MSB=0	0 1 1 0 1 0 0 0 / 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	Rxn, AC_n ← (Rxn+1) / Rx_3, AC_3 ← 0	The memory (Rx) contents are shifted right and 0 is loaded to the MSB. The same contents are loaded to the AC.	
	SR1 X	Shift Right Rx & MSB=1	0 1 1 0 1 0 0 1 / 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	Rxn, AC_n ← (Rxn+1) / Rx_3, AC_3 ← 1	The memory (Rx) contents are shifted right and 1 is loaded to the MSB. The same contents are loaded to the AC.	
	SL0 X	Shift Left Rx & LSB=0	0 1 1 0 1 0 1 0 / 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	Rxn, ACn ← (Rxn-1) / Rx_0, AC_0 ← 0	The memory (Rx) contents are shifted left and 0 is loaded to the LSB. The same contents are loaded to the AC.	
	SL1 X	Shift Left Rx & LSB=1	0 1 1 0 1 0 1 1 / 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	Rxn, ACn ← (Rxn-1) / Rx_0, AC_0 ← 1	The memory (Rx) contents are shifted left and 1 is loaded to the LSB. The same contents are loaded to the AC.	
	RAR X	Rotate Right Rx	0 1 1 0 1 1 0 0 / 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	Rxn, ACn ← (Rxn+1) / Rx_3, AC_3 ← Rx_0	The memory (Rx) contents are rotated right. The same contents are loaded to the AC.	
	RAL X	Rotate Left Rx	0 1 1 0 1 1 1 0 / 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	Rxn, ACn ← (Rxn-1) / Rx_0, AC_0 ← Rx_3	The memory (Rx) contents are rotated left. The same contents are loaded to the AC.	
	MAF X	Move CF & WRF to AC & Rx	0 1 1 1 0 1 0 0 / 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC, Rx ← (CF, WRF)	The CF, WRF contents are loaded to the AC and memory (Rx). (See table below)	
	MRA X	Move Rx to CF & WRF	0 0 0 0 1 1 1 1 / 1 X_6 X_5 X_4 X_3 X_2 X_1 X_0	CF, WRF ← (Rx)	The memory (Rx) contents are loaded to the CF and WRF. Bit has the same correspondence as for MAF X.	
Operation instructions	ADC X	Add AC to Rx with CF	0 1 0 0 0 0 0 0 / 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC ← (Rx)+(AC) +(CF)	The memory (Rx), AC, CF contents are binary-added and the result is loaded to the AC.	CF
	ADC* X	Add AC to Rx with CF	0 1 0 0 0 0 0 1 / 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC, Rx ← (Rx)+(AC) +(CF)	The memory (Rx), AC, CF contents are binary-added and the result is loaded to the AC, Rx.	CF
	SBCX	Subtract AC from Rx with CF	0 1 0 0 0 0 1 0 / 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC, ← (Rx)+$\overline{(AC)}$ +(CF)	The AC, CF contents are binary subtracted from the memory (Rx) contents and the result is placed in the AC.	CF
	SBC* X	Subtract AC from Rx with CF	0 1 0 0 0 0 1 1 / 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC ← (Rx)+$\overline{(AC)}$ +(CF)	The AC, CF contents are binary subtracted from the memory (Rx) contents and the result is placed in the AC, Rx.	CF

AC, Rx bit	Contents
3	CF
2	
1	WRF2
0	WRF1

Instruction group	Mnemonic		Instruction code								Function	Description	Status flag to be affected
			D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8			
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			
Operation instructions	ADD X	Add AC to Rx	0	1	0	0	0	1	0	0	AC ← (Rx)+(AC)	The memory (Rx), AC contents are binary-added and the result is loaded to the AC.	CF
			0	X_6	X_5	X_4	X_3	X_2	X_1	X_0			
	ADD* X	Add AC to Rx	0	1	0	0	0	1	0	1	AC, Rx ← (Rx)+(AC)	The memory (Rx), AC contents are binary-added and the result is loaded to the AC, Rx.	CF
			0	X_6	X_5	X_4	X_3	X_2	X_1	X_0			
	SUB X	Subtract AC	0	1	0	0	0	1	1	0	AC ← (Rx)+$\overline{(AC)}$+1	The AC contents are binary subtracted from the memory (Rx) contents and the result is placed in the AC.	CF
		from Rx	0	X_6	X_5	X_4	X_3	X_2	X_1	X_0			
	SUB* X	Subract AC	0	1	0	0	0	1	1	1	AC, Rx ← (Rx)+$\overline{(AC)}$+1	The AC contents are binary subtracted from the memory (Rx) contents and the result is placed in the AC, Rx.	CF
		from Rx	0	X_6	X_5	X_4	X_3	X_2	X_1	X_0			
	ADN X	Add AC to Rx	0	1	0	0	1	0	0	0	AC ← (Rx)+(AC)	The memory (Rx), AC contents are binary-added and the result is loaded to the AC.	
			0	X_6	X_5	X_4	X_3	X_2	X_1	X_0			
	ADN* X	Add AC to Rx	0	1	0	0	1	0	0	1	AC, Rx ← (Rx)+(AC)	The memory (Rx), AC contents are binary-added and the result is loaded to the AC, Rx.	
			0	X_6	X_5	X_4	X_3	X_2	X_1	X_0			
	AND X	And AC to Rx	0	1	0	0	1	0	1	0	AC ← (Rx)∧(AC)	The memory (Rx) contents and AC contents are ANDed and the result is loaded to the AC.	
			0	X_6	X_5	X_4	X_3	X_2	X_1	X_0			
	AND* X	And AC to Rx	0	1	0	0	1	0	1	1	AC, Rx ← (Rx)∧(AC)	The memory (Rx) contents and AC contents are ANDed and the result is loaded to the AC, Rx.	
			0	X_6	X_5	X_4	X_3	X_2	X_1	X_0			
	EOR X	Exclusive or	0	1	0	0	1	1	0	0	AC ← (Rx)∀(AC)	The memory (Rx), AC contents are exclusive-ORed and the result is loaded to the AC.	
		AC to Rx	0	X_6	X_5	X_4	X_3	X_2	X_1	X_0			
	EOR* X	Exclusive or	0	1	0	0	1	1	0	1	AC, Rx ← (Rx)∀(AC)	The memory (Rx), AC contents are exclusive-ORed and the result is loaded to the AC, Rx.	
		AC to Rx	0	X_6	X_5	X_4	X_3	X_2	X_1	X_0			
	OR X	OR AC to Rx	0	1	0	0	1	1	1	0	AC ← (Rx)∨(AC)	The memory (Rx), AC contents are ORed and the result is loaded to the AC.	
			0	X_6	X_5	X_4	X_3	X_2	X_1	X_0			
	OR* X	OR AC to Rx	0	1	0	0	1	1	1	1	AC, Rx ← (Rx)∨(AC)	The memory (Rx), AC contents are ORed and the result is loaded to the AC, Rx.	
			0	X_6	X_5	X_4	X_3	X_2	X_1	X_0			
	ADCI X, Y	Add Immediate	0	1	0	1	0	0	0	0	AC ← (Rx)+Y+(CF)	The memory (Rx) contents, Y, CF contents are binary-added and the result is loaded to the AC. The relation between absolute address of data memory (Rx) and X is as follows: Absolute address=XH+70H	CF
		data to Rx with CF	Y_3	Y_2	Y_1	Y_0	X_3	X_2	X_1	X_0			
	ADCI* X, Y	Add Immediate	0	1	0	1	0	0	0	1	AC, Rx ← (Rx)+Y+(CF)	The memory (Rx) contents, Y are binary-added and the result is loaded to the AC, Rx.	CF
		data to Rx with CF	Y_3	Y_2	Y_1	Y_0	X_3	X_2	X_1	X_0			
	SBCI X, Y	Subtract Immediate	0	1	0	1	0	0	1	0	AC ← (Rx)+$\overline{Y}$+(CF)	Immediate data Y and the CF contents are binary subtracted from the memory (Rx) contents and the result is placed in the AC.	CF
		data & CF from Rx	Y_3	Y_2	Y_1	Y_0	X_3	X_2	X_1	X_0			
	SBCI* X, Y	Subtract Immediate	0	1	0	1	0	0	1	1	AC, Rx ← (Rx)+$\overline{Y}$+(CF)	Immediate data Y and the CF contents are binary subtracted from the memory (Rx) contents and the result is placed in the AC, Rx.	CF
		data & CF from Rx	Y_3	Y_2	Y_1	Y_0	X_3	X_2	X_1	X_0			
	ADDI X, Y	Add Immediate	0	1	0	1	0	1	0	0	AC ← (Rx)+Y	The memory (Rx) contents and Y are binary-added and the result is loaded to the AC.	CF
		data to Rx	Y_3	Y_2	Y_1	Y_0	X_3	X_2	X_1	X_0			
	ADDI* X, Y	Add Immediate	0	1	0	1	0	1	0	1	AC, Rx ← (Rx)+Y	The memory (Rx) contents and Y are binary-added and the result is loaded to the AC, Rx.	CF
		data to Rx	Y_3	Y_2	Y_1	Y_0	X_3	X_2	X_1	X_0			
	SUBI X, Y	Subtract Immediate	0	1	0	1	0	1	1	0	AC ← (Rx)+$\overline{Y}$+1	Immediate data Y is binary subtracted from the memory (Rx) contents and the result is placed in the AC.	CF
		data from Rx	Y_3	Y_2	Y_1	Y_0	X_3	X_2	X_1	X_0			
	SUBI* X, Y	Subtract Immediate	0	1	0	1	0	1	1	1	AC, Rx ← (Rx)+$\overline{Y}$+1	Immediate data Y is binary subtracted from the memory (Rx) contents and the result is placed in the AC, Rx.	CF
		data from Rx	Y_3	Y_2	Y_1	Y_0	X_3	X_2	X_1	X_0			
	ADNI X, Y	Add Immediate	0	1	0	1	1	0	0	0	AC ← (Rx)+Y	The memory (Rx) contents and Y are binary-added and the result is loaded to the AC.	
		data to Rx	Y_3	Y_2	Y_1	Y_0	X_3	X_2	X_1	X_0			
	ADNI* X, Y	Add Immediate	0	1	0	1	1	0	0	1	AC, Rx ← (Rx)+Y	The memory (Rx) contents and Y are binary-added and the result is loaded to the AC, Rx.	
		data to Rx	Y_3	Y_2	Y_1	Y_0	X_3	X_2	X_1	X_0			

Instruction group	Mnemonic		Instruction code	Function	Description	Status flag to be affected
Operation instructions	ANDI X, Y	And Immediate data to Rx	0 1 0 1 1 0 1 0 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC ← (Rx)∧Y	The memory (Rx) contents and Y are ANDed and the result is loaded to the AC.	
	ANDI* X, Y	And Immediate data to Rx	0 1 0 1 1 0 1 1 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC, Rx ← (Rx)∧Y	The memory (Rx) contents and Y are ANDed and the result is loaded to the AC, Rx.	
	EORI X, Y	Exclusive Or Y to Rx	0 1 0 1 1 1 0 0 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC ← (Rx)∨Y	The memory (Rx) contents and Y are exclusive-ORed and the result is loaded to the AC.	
	EORI* X, Y	Exclusive Or Y to Rx	0 1 0 1 1 1 0 1 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC, Rx ← (Rx)∨Y	The memory (Rx) contents and Y are exclusive-ORed and the result is loaded to the AC, Rx.	
	ORI X, Y	Or Immediate data to Rx	0 1 0 1 1 1 1 0 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC ← (Rx)∨Y	The memory (Rx) contents and Y are ORed and the result is loaded to the AC.	
	ORI* X, Y	Or Immediate data to Rx	0 1 0 1 1 1 1 1 Y_3 Y_2 Y_1 Y_0 X_3 X_2 X_1 X_0	AC, Rx ← (Rx)∨Y	The memory (Rx) contents and Y are ORed and the result is loaded to the AC, Rx.	
Data pointer and flag manipulation instructions	MOPL X	Move DPL to Rx	0 1 1 1 0 1 1 1 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC, Rx ← (DPL)	The DPL contents are loaded to the memory (Rx).	
	MOPH X	Move DPH to Rx	0 1 1 1 0 1 1 0 1 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC, Rx ← (DPH)	The DPH contents are loaded to the AC and memory (Rx).	
	MRDH X	Move Rx to DPH	0 1 1 0 1 0 1 1 1 X_6 X_5 X_4 X_3 X_2 X_1 X_0	DPH, AC ← (Rx)	The memory (Rx) contents are loaded to the AC and DPH. (If the DPF is set with X=00H to 0FH, the memory (Rx) contents are not loaded to the DPH.)	
	MRDL X	Move Rx to DPL	0 1 1 0 1 0 0 1 1 X_6 X_5 X_4 X_3 X_2 X_1 X_0	DPL, AC ← (Rx)	The memory (Rx) contents are loaded to the AC and DPL. (If the DPF is set with X=00H to 0FH, the memory (Rx) contents are not loaded to the DPL.)	
	MRSB X	Move Strove Pointer	0 1 1 0 1 0 1 0 1 X_6 X_5 X_4 X_3 X_2 X_1 X_0	SP, AC ← (Rx)	The memory (Rx) contents are loaded to the AC and SP.	
	SF1 X	Set Flag 1 Group	1 1 1 0 1 0 X_9 X_8 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0		The flag corresponding to the data specified with X9 to X0 is set.	CF DPF
				Data of X9 to X0	X_0=1 | X_1=1 | X_2=1 | X_3=1	
				Instruction to be executed	SCF | SCEX | SCT1 | SFSP	
				Data of X9 to X0	X_4=1 | X_5=1 | X_6=1 | X_7=1	
				Instruction to be executed	SFPD | COMD1 | COMO2 | SDPF	
				X_8=1, X_9=1	Used for test.	
	RF1 X	Reset Flag 1 Group	1 1 1 0 1 1 X_9 X_8 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0		Each flag is reset corresponding to SF1.	CF DPF
	SF2 X	Set Flag 2 Group	1 1 1 1 0 0 X_9 X_8 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0		The flag corresponding to the data specified with X8 to X0 is set.	BCF CMF CDF PDF HQF
				Data of X9 to X0	X_0=1 | X_1=1 | X_2=1 | X_3=1 | X_4=1	
				Instruction to be executed	SCHF1 | SCHF2 | SBAK | LON | LON SLOT	
				Data of X9 to X0	X_5=1 | X_6=1 | X_7=1 | X_8=1 | X_9=1	
				Instruction to be executed	SPDF1 | SPDF2 | SPDF4 | SPDF8 | SCT2	
	RF2 X	Reset Flag 2 Group	1 1 1 1 0 1 X_9 X_8 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0		Each flag is reset corresponding to SF2.	
	SDPF	Set DPF	1 1 1 0 1 0 0 0 1 0 0 0 0 0 0 0	DPF ← 1 ≡SF1 80H	The DPF is set. The memory address is specified with the DP. If the instruction code address is 70H to 7FH, the instruction code address prevails.	DPF
	RDPF	Reset DPF	1 1 1 0 1 1 0 0 1 0 0 0 0 0 0 0	DPF ← 0 ≡RF1 80H	The DPF is reset.	DPF

Instruction group	Mnemonic		Instruction code	Function	Description	Status flag to be affected
Load/store instructions	STA X	Store AC to Rx	0 1 1 1 0 1 1 1 1 X_6 X_5 X_4 X_3 X_2 X_1 X_0	Rx ← (AC)	The AC contents are loaded to the memory (Rx).	
	LDS X, D	Load AC with Data & Store AC to Rx	0 1 1 1 1 D_3 D_2 D_1 D_0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC, Rx ← D	Immediate data D is loaded to the AC and memory (Rx).	
	LDA X	Load AC from Rx	0 1 1 0 1 0 0 0 1 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC ← (Rx)	The memory (Rx) contents are loaded to the AC.	
CPU control instructions	HALT	HALT	1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0		The operation of CPU is stopped. The following 3 conditions cause the halt mode to be released. 1) An interrupt is accepted. 2) The signal change specified by the SSW instruction is applied to port S, K. 3) The halt release condition specified by the SIC instruction is met. When an interrupt is accepted to release the halt mode, the halt mode restores by executing the RTS instruction after completion of interrupt service.	
	SSW X	Set Switch State	1 1 1 0 0 0 0 0 0 0 X_5 X_4 X_3 X_2 X_1 X_0		The data specified by X causes the halt mode to be released. The signal change at port S, K is specified. $X_0 \sim X_5$: X_0=1 S1; X_1=1 S2; X_2=1 S3; X_3=1 S4 Signal change at input port $X_0 \sim X_5$: X_4=1 Fall signal at one of K1 to K4; X_5=1 Rise signal at one of K1 to K4	
	SIC X	Set/Reset Interupt Enable Flag	1 1 1 1 1 0 1 X_8 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	X_0=1	The HEF0 is set so that Interrupt 0 (overflow from the divider) is accepted.	$IEF_{0\sim3}$ $HEF_{0\sim3}$ E/SF The IEF0 to 3 are reset automatically when an interrupt is accepted.
				X_1=1	The IEF2 is set so that Interrupt 2 (overflow from the CC) is accepted.	
				X_2=1	The IEF1 is set so that Interrupt 1 (underflow from the TM) is accepted.	
				X_3=1	The IEF0 is set so that Interrupt 0 (mode shown below) is accepted. 1) Signal change at port S specified by the SSW. 2) Signal change at port K specified by the SSW. 3) Rise signal change at external interrupt pin INT. Refer to the operation for X_8=1 also.	
				X_4=1	The HEF3 is set so that overflow from the divider causes the halt mode to be released.	
				X_5=1	The HEF2 is set so that overflow from the CC causes the halt mode to be released.	
				X_6=1	The HEF1 is set so that underflow from the TM causes the halt mode to be released.	
				X_7=1	The HEF0 is set so that the halt mode is released when the rise signal change is applied to INT. In this case X_8 must be 0.	
				X_8=1	For X_3=1, port S/K is selected at X_8=1 (E/SF set); INT is selected at X_8=0 (E/SF reset). In the case of X_7=1, X_8 must be 1.	
	SIC* X		1 1 1 1 1 1 1 0 0 0 0 0 X_3 X_2 X_1 X_0		Only X0 to X3 of the SIC instruction are significant. X4 to X8 remain unaffected.	

Instruction group	Mnemonic		Instruction code D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 / D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Function	Description	Status flag to be affected
CPU control instructions	MSB X	Move SCF & BCF to AC & Rx	0 1 1 1 0 1 0 1 / 1 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC, Rx ← $SCF_{1\sim3}$ BCF	The SCF1 to 3 and BCF contents are loaded to the AC and memory (Rx).	
				The AC contents and the meaning of bit after execution of this instruction are as follows: Bit 0 ···· BCF: "1" at the backup mode. Bit 1 ···· SCF1: "1" when the halt mode is released by the signal change at port K. Bit 2 ···· SCF2: "1" when the halt mode is released by the SCF4 to 7. Bit 3 ···· SCF3: "1" when the halt mode is released by the signal change at port S.	
	MSC X	Move SCF to AC & Rx	0 1 1 1 0 1 1 0 / 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC, Rx←SCF4~7	The SCF4 to 7 contents are loaded to the AC and memory (Rx).	
				The AC contents and the meaning of bit after execution of this instruction are as follows: Case where the corresponding bit is "1": Bit 0 ···· SCF4: The halt mode is released by overflow from the divider. Bit 1 ···· SCF5: The halt mode is released by overflow from the CC. Bit 2 ···· SCF6: The halt mode is released by underflow the TM. Bit 3 ···· SCF7: The halt mode is released by the signal change at INT.	
				The SIC instruction is used to specify that the INT/port S, KTM, CC, divider should be specified for interrupt service, halt release, or no operation.		
	NOP	No Operation	0 0 0 0 0 0 0 0 / 0 0 0 0 0 0 0 0			
	LON	Light ON	1 1 1 1 0 0 0 0 / 0 0 0 1 1 0 0 0	Set Light & HQF =SF2 18H	The Light Out pin is made active and the halt request flag (HRQ) is set to cause the halt mode to be entered.	HQF
	LOFF	Light OFF	1 1 1 1 0 1 0 0 / 0 0 0 1 1 0 0 0	Reset Light & HQF =RF2 18H	The Light Out pin is made nonactive and the HRQ is reset.	HQF
	SBAK	Set Back-up Mode	1 1 1 1 0 0 0 0 / 0 0 0 0 0 1 0 0	=SF 2 4	V_{SS2} is applied to the logic unit at the LI battery power supply mode. The inverter size of the oscillator is approximately doubled at the Ag, LI battery, EXTV power supply mode.	BCF
	RBAK	Reset Back-up Mode	1 1 1 1 0 1 0 0 / 0 0 0 0 0 1 0 0	=RF 2 4	The backup mode is released.	BCF
Chrono instructions	MCD X	Move Chrono Counter Date to AC & Rx	0 1 1 1 0 1 0 0 / 1 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC, Rx← (CC)	The CC contents are loaded to the AC and memory (Rx).	
	MCF X	Move Chrono Flag to AC & Rx	0 1 1 1 0 1 0 1 / 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	AC, Rx← CMF, CSTF	The contents of each flag are loaded to the AC and memory (Rx).	
				The AC contents after execution of this instruction are as follows: Bit 0 ···· LSF: "1" at the CC overflow mode at LPF=1. Bit 1 ···· LPF: "1" at the lap mode. Bit 2 ···· CSTF: "1" at the chrono start mode. Bit 3 ···· CMF: "1" at the chrono mode.	
	CCC	Clear CC	1 1 1 1 1 1 0 0 / 0 0 1 0 0 0 1 0	CC←0 LSF←0		LSF
	RLP	Reset LPF	1 1 1 1 1 1 0 0 / 0 1 0 0 0 0 0 0	LPF←0 PLC 040H	The lap mode is released.	LPF
	CSP	Chrono Stop	1 1 1 1 1 1 0 0 / 1 0 0 0 0 0 0 0	CSTF←0	1/100 second pulse is inhibited from being applied to the CC.	CSTF

Instruction group	Mnemonic		Instruction code D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 / D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Function	Description	Status flag to be affected
Chrono instructions	CST	Chrono Start	1 1 1 1 1 1 0 1 0 0 0 0 0 0 0 0	≡PLC 100H	1/100 second pulse is applied to the CC.	
	SCEX	Set CC External Input Mode	1 1 1 0 1 0 0 0 0 0 0 0 0 0 1 0	≡SF1_2	The CC input connected to K4 pin, instead of 1/100 pulse. At the initial mode the CC input is connected to 1/100 pulse.	
	RCEX	Reset CC External Input Mode	1 1 1 0 1 1 0 0 0 0 0 0 0 0 1 0	≡RF1_2	The CC input is connected to 1/100 pulse.	
	SCHF X	Set Chrono Flag	1 1 1 1 0 0 0 0 0 0 0 0 0 0 X_1 X_0	CMF ← 1 (at X_0=1) CDF ← 1 (at X_1=1) ≡One of SF2	The CMF and CDF are set. When the CMF is set, the chrono start/stop, tap/lap release mode can be controlled by the signal at port S of the dedicated instruction. When the CDF is set, the data decode is connected to the CC.	CMF CDF At the initial mode the CMF and CDF are reset.
	RCHF X	Reset Chrono Flag	1 1 1 1 0 1 0 0 0 0 0 0 0 0 X_1 X_0	CMF ← 0 (at X_0=1) CDF ← 0 (at X_1=1) ≡One of RF2	The CMF and CDF are reset.	CMF CDF
Input/output instructions	IPP X	Input Port P to AC & Rx	0 1 1 1 0 0 0 1 1 X_6 X_5 X_4 X_3 X_2 X_1 X_0	Rx, AC ← [P(P)]	The input data at input/output port P is loaded to the AC and memory (Rx).	
	IPS X	Input Port S to AC & Rx	0 1 1 1 0 0 0 0 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	Rx, AC ← [P(S)]	The input data at input port S is loaded to the AC and memory (Rx).	
	IPM X	Input Port M to AC & Rx	0 1 1 1 0 0 0 0 1 X_6 X_5 X_4 X_3 X_2 X_1 X_0	Rx, AC ← [P(M)]	The input data at input/output port M is loaded to the AC and memory (Rx).	
	IPK X	Input Port K to AC & Rx	0 1 1 1 0 0 0 1 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	Rx, AC ← [P(K)]	The input data at input port K is loaded to the AC and memory (Rx).	
	OPP X	Output Rx to Port P	0 0 0 0 0 0 0 0 1 X_6 X_5 X_4 X_3 X_2 X_1 X_0	[P(P)] ← Rx	The memory (Rx) contents are loaded to input/output port P.	
	OPM X	Output Rx to Port M	0 0 0 0 1 1 1 1 0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	[P(M)] ← Rx	The memory (Rx) contents are loaded to input/output port M.	
	SCT1	Set CNT OUT 1	1 1 1 0 1 0 0 0 0 0 0 0 0 1 0 0	≡SF1_4	The CNT1 OUT pin is made active (ON).	
	RCT1	Reset CNT OUT 1	1 1 1 0 1 1 0 0 0 0 0 0 0 1 0 0	≡RF1_4	The CNT1 OUT pin is made nonactive (OFF).	
	SCT2	Set CNT OUT 2	1 1 1 1 0 0 1 0 0 0 0 0 0 0 0 0	≡SF2 200H	The CNT2 OUT pin is made active (ON).	
	RCT2	Reset CNT OUT 2	1 1 1 1 0 1 1 0 0 0 0 0 0 0 0 0	≡RF2 200H	The CNT2 OUT pin is made nonactive (OFF).	
	SLGT	Set Light	1 1 1 1 0 0 0 0 0 0 0 1 0 0 0 0	≡SF2 10H	The LIGHT OUT pin is made active (ON). (Refer to the LON instruction.)	
	RLGT	Reset Light	1 1 1 1 0 1 0 0 0 0 0 1 0 0 0 0	≡RF2 10H	The LIGHT OUT pin is made nonactive (OFF). (Refer to the LOFF instruction.)	
	SAS X	Set Alarm Sound	1 1 1 1 1 0 0 X_8 X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	The waveform specified by X_8 to X_0 is delivered at the Alarm Out pin.		

X_7~X_0	X_0=1	X_1=1	X_2=1	X_3=1	X_4=1
Enable Signal	32Hz	16Hz	8Hz	4Hz	2Hz
X_7~X_0	X_5=1	$\overline{X_8}X_7$=1	$\overline{X_8}X_7$=1	$X_8\overline{X_7}$=1	X_8X_7=1
Enable Signal	1Hz	1kHz	2kHz	4kHz	DC

At X_8=1 the signal specified by X_6, X_7 is enabled.

Instruction group	Mnemonic		Instruction code D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 / D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Function	Description	Status flag to be affected
Input/output instructions	RAS	Reset Alarm Sound	1 1 1 1 1 0 0 0 / 0 0 0 0 0 0 0 0	≡SAS 0	The Alarm Out pin is made nonactive (OFF).	
	COMD X	Change to Output Mode	1 1 1 0 1 0 0 0 / 0 X_1 X_0 0 0 0 0 0	≡One of SF1	Input/output port M or P is changed to the output mode. At the initial mode the port is in the input mode. X=1, X=2, X=3 correspond to port M, port P, port M, P respectively.	
	CIMD X	Change to Input Mode	1 1 1 0 1 1 0 0 / 0 X_1 X_0 0 0 0 0 0	≡One of RF1	Input/output port M or P is changed to input port.	
	SPDF X	Set PDF	1 1 1 1 0 0 0 X_3 / X_2 X_1 X_0 0 0 0 0 0	PDF ← 1 ≡One of SF2	The pull-down MOS transistor of the corresponding input port is turned ON.	PDF
				$X_0 \sim X_3$	X_0=1 / X_1=1 / X_2=1 / X_3=1	
				Corresponding port	S / M / K, INT / P	
	RPDF X	Reset PDF	1 1 1 1 0 1 0 X_3 / X2 X_1 X_0 0 0 0 0 0	PDF ← 0 ≡One of RF2		PDF
	SFSP	Set High Frequency Switch Sample Mode	1 1 1 0 1 0 0 0 / 0 0 0 0 1 0 0 0	≡SF1 8	The 7ms chattering eliminator is connected to input port S, K.	
	RFSP	Reset High Frequency Switch Sample Mode	1 1 1 0 1 1 0 0 / 0 0 0 0 1 0 0 0	≡RF1 8	The 31ms chattering eliminator is connected to input port S, K. At the initial mode the RFSP mode is entered.	
	WRT Y, X	Write Rx to LCD Latch (L_Y)	0 0 0 0 Y_4 Y_3 Y_2 Y_1 / Y_0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	Y=00H, 01H, 1EH, 1FH causes a different instruction to occur. For input/output of the data decoder, refer to page 60.	The memory (Rx) contents are loaded to the LCD latch (L_Y) through the data decoder. For DPF=1, X=00H to 6FH, the address of Rx is specified by DP; the address of L_Y is specified by SP.	
	WRB Y, X	Write Rx to LCD Latch (L_Y)	0 0 0 1 Y_4 Y_3 Y_2 Y_1 / Y_0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	Same as above.	Same as WRT X, Y. Output data "a" to "h" corresponding to input data of the data decoder are all 0.	
	WRC Y, X	Write Rx to LCD Latch (L_Y)	0 0 1 0 Y_4 Y_3 Y_2 Y_1 / Y_0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	For input/output of the data decoder, refer to page 60.	Same as WRT X, Y except input/output of the data decoder.	
	WRP Y, X	Write Rx to LCD Latch (L_Y)	0 0 1 1 Y_4 Y_3 Y_2 Y_1 / Y_0 X_6 X_5 X_4 X_3 X_2 X_1 X_0	For input/output of the data decoder, refer to page 60.	Same as WRT X, Y except input/output of the data decoder.	
Jump instructions	JMP X	Jump	1 1 0 0 0 X_{10} X_9 X_8 / X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$PC_{10} \sim PC_0 \leftarrow X_{10} \sim X_0$	The data specified by X_{10} to X_0 is loaded to the PC to produce an unconditional jump.	
	BAB0 X	Branch on AC bit 0 High	1 0 0 0 0 X_{10} X_9 X_8 / X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$PC_{10} \sim PC_0 \leftarrow X_{10} \sim X_0$ if AC_0='1'	If bit 0 of the AC is "1", a jump occurs. If "0", the PC is incremented +1.	
	BAB1 X	Branch on AC bit 1 High	1 0 0 0 1 X_{10} X_9 X_8 / X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$PC_{10} \sim PC_0 \leftarrow X_{10} \sim X_0$ if AC_1='1'	If bit 1 of the AC is "1", a jump occurs. If "0" the PC is incremented +1.	
	BAB2 X	Branch on AC bit 2 High	1 0 0 1 0 X_{10} X_9 X_8 / X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$PC_{10} \sim PC_0 \leftarrow X_{10} \sim X_0$ if AC_2='1'	If bit 2 of the AC is "1", a jump occurs. If "0", the PC is incremented +1.	
	BAB3 X	Branch on AC bit 3 High	1 0 0 1 1 X_{10} X_9 X_8 / X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$PC_{10} \sim PC_0 \leftarrow X_{10} \sim X_0$ if AC_3='1'	If bit 3 of the AC is "1", a jump occurs. If "0", the PC is incremented +1.	
	BANZ X	Branch on AC not Zero	1 0 1 0 0 X_{10} X_9 X_8 / X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$PC_{10} \sim PC_0 \leftarrow X_{10} \sim X_0$ if AC≠0	If the AC is not "0", a jump occurs. If "0", the PC is incremented +1.	
	BAZ X	Branch on AC Zero	1 0 1 1 0 X_{10} X_9 X_8 / X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0	$PC_{10} \sim PC_0 \leftarrow X_{10} \sim X_0$ if AC=0	If the AC is "0", a jump occurs. If not "0", the PC is incremented +1.	

Instruction group	Mnemonic		Instruction code								Function	Description	Status flag to be affected
			D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8			
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			
Jump instructions	BCNH X	Branch on CF not High	1	0	1	0	1	X_{10}	X_9	X_8	PC_{10}~PC_0 ← X_{10}~X_0 if CF=1	If the CF is "0", a jump occurs. If "1" the PC is incremented +1.	
			X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0			
	BCH X	Branch on CF High	1	0	1	1	1	X_{10}	X_9	X_8	PC_{10}~PC_0 ← X_{10}~X_0 if CF=1	If the CF is "1", a jump occurs. If "0", the PC is incremented +1.	
			X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0			
Subroutine instructions	CALL X	Call Subroutine	1	1	0	0	1	X_{10}	X_9	X_8	STACK ← (PC)+1 PC_{10}~PC_0 ← X_{10}~X_0	A subroutine is called.	
			X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0			
	RTS	Return from Subroutine	1	1	0	1	0	0	0	0	PC ← (STACK)	A return from a subroutine occurs.	
			0	0	0	0	0	0	0	0			
	POP	POP the stack	1	1	0	1	1	0	0	0		The stack pointer is popped −1.	
			0	0	0	0	0	0	0	0			
Other instructions	STM X	Set Timer	1	1	1	0	0	1	X_9	X_8	For the relation between X data and time setting, refer to page	The data specified by X_9 to X_0 is loaded to the TM to start the TM.	
			X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0			
	RTM	Reset Timer	1	1	1	1	1	1	0	0	≡PLC 4	The TM stops operating. When using the TM to release the halt mode, this instruction is executed to stop the TM and to reset the halt release request signal. When the timer interrupt is accepted, the TM stops operating automatically.	
			0	0	0	0	0	1	0	0			
	SFPD	Set High Frequency Pre-Divider Over Flow Mode	1	1	1	0	1	0	0	0	≡SF1 10H	Overflow signal from the divider is changed from 2Hz to 4Hz. When watch count is based on the 2Hz/4Hz signal, this instruction must be executed so that no error occurs in watch operation.	
			0	0	0	1	0	0	0	0			
	RFPD	Reset High Frequency Pre-Divider Over Flow Mode	1	1	1	0	1	1	0	0	≡RF1 10H	Overflow signal from the divider is changed from 4Hz to 2Hz. At the initial mode 2Hz is set.	
			0	0	0	1	0	0	0	0			
	PLC X	Pulse Control	1	1	1	1	1	1	0	X_8		The pulse corresponding to the data specified by X_8 to X_0 is generated.	$HRF_{0\sim3}$
			X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0			

X_0~X_8	Mode after execution of instruction
X_0=1	Halt release request flag HRF3 caused by overflow from the divider is reset.
X_1=1	Halt release request flag HRF2 caused by overflow from the CC is reset.
X_2=1	Halt release request flag HRF1 caused by overflow from the TM is reset.
X_3=1	Halt release request flag HRF0 caused by the signal at input port S, K or INT is reset.
X_4=1	The last 5 bits of the divider (15 bits) are reset. When executing this instruction, X_0 must be set to "1".
X_5=1	The CC and LSF are cleared. When executing this instruction, X_1 must be set to "1". Same as the CCC instruction.
X_6=1	Same as the RLP instruction.
X_7=1	Same as the CSP instruction.
X_8=1	Same as the CST instruction.

Note) 4Hz of the SFPD, RFPD instructions is for the chip (LC5800F/6800F) whose cycle time is 244μs.
8Hz is for the chip (LC5800G/6800G) whose cycle time is 122μs.

Input/Output of data decoder at WRT instruction execution mode

Input data	Output data							
	a	b	c	d	e	f	g	h
0	1	1	1	1	1	1	0	0
1	0	1	1	0	0	0	0	0
2	1	1	0	1	1	0	1	0
3	1	1	1	1	0	0	1	0
4	0	1	1	0	0	1	1	0
5	1	0	1	1	0	1	1	0
6	1	0	1	1	1	1	1	0
7	1	1	1	0	0	0	0	0
8	1	1	1	1	1	1	1	0
9	1	1	1	1	0	1	1	0
A/B	1	0	0	1	1	1	1	0
C/D	0	0	0	0	0	0	1	0
E/F	0	0	0	0	0	0	0	0

Input/output of data decoder at WRC instruction execution mode

Input data	Output data							
	a	b	c	d	e	f	g	h
0	0	0	0	0	0	0	0	1
1	0	1	0	0	0	0	0	0
2	0	0	0	1	0	0	0	0
3	0	0	1	0	0	0	0	0
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	0	1	0
6	0	0	0	0	1	0	0	0
7	1	0	0	0	0	0	0	0
8 ~ F	0	0	0	0	0	0	0	0

Input/output of data decoder WRP instruction execution mode

Input data	(Rx0)	(Rx1)	(Rx2)	(Rx3)	(AC0)	(AC1)	(AC2)	(AC3)
Output data	a	b	c	d	e	f	g	h

Data specified by X_9 to X_0 and set time at STM instruction execution mode

Set value										Set time (μs)
X_9	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	
0	0	0	0	0	0	0	0	0	0	244
0	0	0	0	0	0	0	0	0	1	488
0	0	0	0	0	0	0	0	1	0	732
⟆			⟆				⟆			⟆
1	1	1	1	1	1	1	1	0	1	249512
1	1	1	1	1	1	1	1	1	0	249756
1	1	1	1	1	1	1	1	1	1	250000

Note) The set time is for the chip (LC5800F/5899F) whose cycle time is 244μs.
For the chip (LC5800G/5899G) whose cycle time is 122μs, the set time is halved.