

**SANYO**

No.2844B

**LC36256P,PL,PM,PML-10/12/15**

Asynchronous Silicon Gate CMOS LSI

32768 Words × 8 Bits Static RAMs

**General Description**

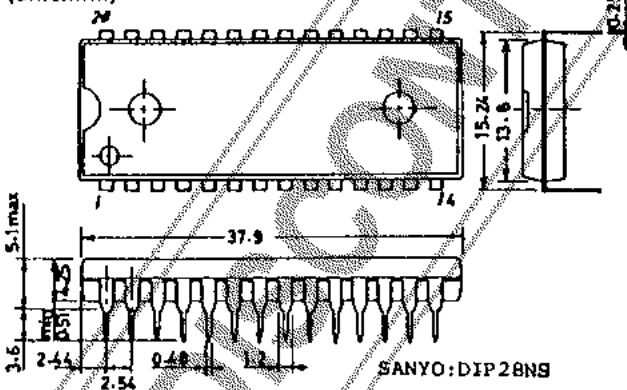
The LC36256P,PL,PM,PML are fully asynchronous silicon gate CMOS static RAMs organized as 32768 words x 8bits. The CMOS-used peripheral permits less current dissipation.

The LC36256P,PL,PM,PML have two control signal inputs:  $\overline{OE}$  for high-speed memory access and chip enable input  $\overline{CE}$  for power-down and device select. Therefore, the LC36256P,PL,PM,PML are especially suited for use in systems which require high speed, low power, battery backup and it is easy to expand the memory capacity.

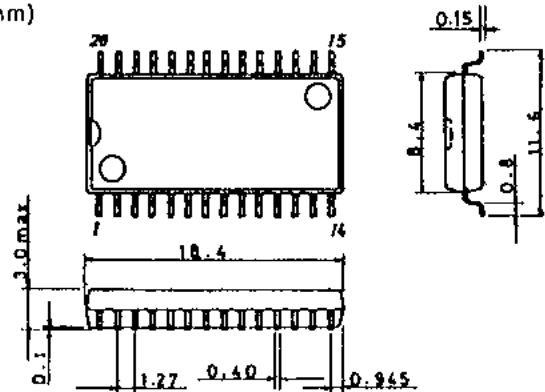
**Features**

- Access time
  - LC36256P,PL,PM,PML-10:100ns(max)
  - LC36256P,PL,PM,PML-12:120ns(max)
  - LC36256P,PL,PM,PML-15:150ns(max)
- Low standby current
  - LC36256PL,PML-10/12/15 :100uA(max)
  - LC36256P,PM-10/12/15 : 1mA(max)
- Single 5V supply:5V±10%
- Data retention supply voltage:2.0 to 5.5V
- No clock required (Fully static memory)
- Directly TTL compatible:All inputs and outputs
- Common data input and output using 3-state outputs
- 28-pin DIP plastic package
- 28-pin SOP (450mit) plastic package

Case Outline 3081-D28NS  
(unit:mm)



Case Outline 3156-SOP28VL  
(unit:mm)



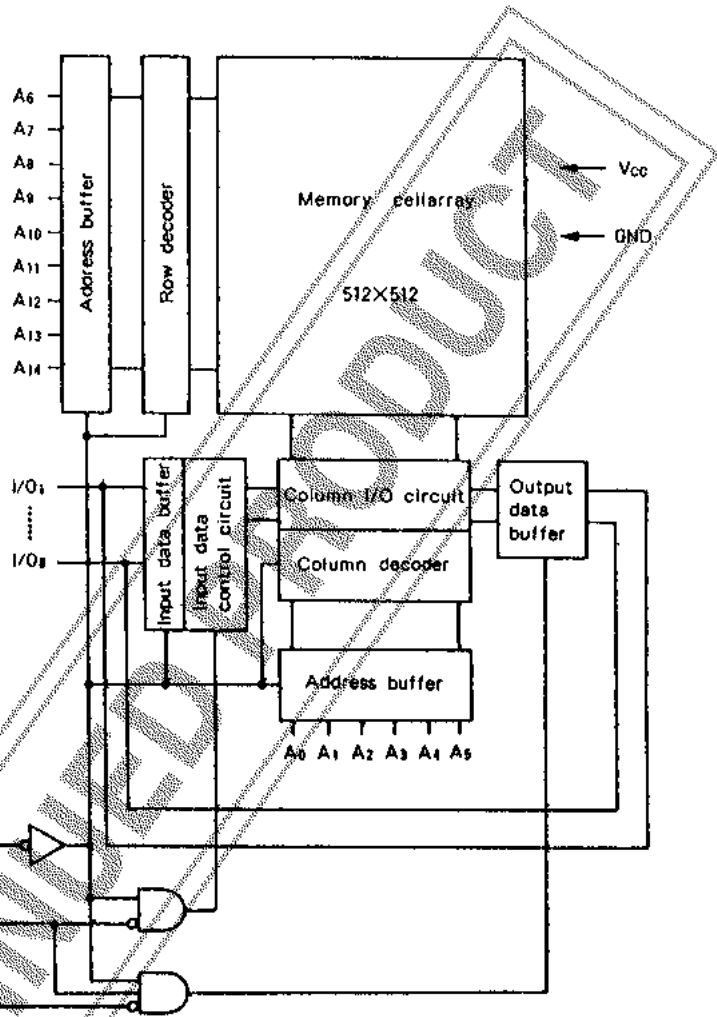
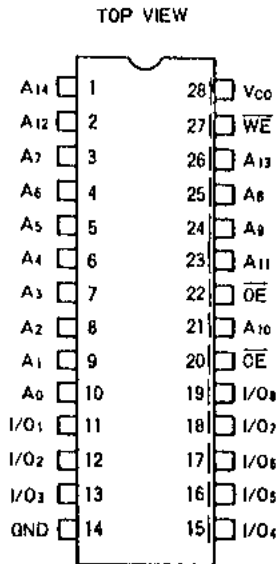
Specifications and information herein are subject to change without notice.

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5182JN/7310TA/9158TA,TS No.2844-1/6

■ Pin Assignment

■ Block Diagram



- A0 to A14 :Address input
- WE :Read/write control input
- OE :Output enable input
- CE :Chip enable input
- I/O<sub>0</sub> to I/O<sub>8</sub> :Data input/output
- Vcc,GND :Power supply pin

■ Functional Table

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Supply current
Read Cycle	L	L	H	Data output	ICCA
Write Cycle	L	X	L	Data Input	ICCA
Output Disable	L	H	H	High impedance	ICCA
Nonselect	H	X	X	High impedance	ICCS

X : H or L

### ■ Absolute Maximum Ratings

Parameter	Symbol	Condition	Limits	unit	
Maximum Supply Voltage	VCC max		+7.0	V	
Input Pin Voltage	V <sub>IN</sub>		-0.5~V <sub>CC</sub> +0.5	V	
I/O Pin Voltage	V <sub>I/O</sub>		-0.5~V <sub>CC</sub> +0.5	V	
Allowable Power Dissipation	Pd max	Ta=+70°C	DIP	1.0	W
			SOP	0.7	
Operating Temperature	Topg		0~+70	°C	
Storage Temperature	Tstg		-55~+125	°C	

### ■ DC Allowable Operating Conditions at Ta=0 to +70°C

Parameter	Symbol	min	typ	max	unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Input 'H'-Level Voltage	V <sub>IH</sub>	2.2		V <sub>CC</sub> +0.3	V
Input 'L'-Level Voltage	V <sub>IL</sub>	-0.3		0.8	V

### ■ DC Electrical Characteristics at Ta=0 to +70°C, Vcc=5V±10%

Parameter	Symbol	Condition	min	typ*	max	unit
Input Leak Current	I <sub>LI</sub>	V <sub>IN</sub> =0~V <sub>CC</sub>	-1.0		1.0	μA
I/O Leak Current	I <sub>LO</sub>	V <sub>CE</sub> =V <sub>IH</sub> or V <sub>OE</sub> =V <sub>IH</sub> or V <sub>WE</sub> =V <sub>IL</sub> , V <sub>I/O</sub> =0~V <sub>CC</sub>	-1.0		1.0	μA
Output 'H'-Level Voltage	V <sub>OH</sub>	I <sub>OH</sub> =-1.0mA	2.4			V
Output 'L'-Level Voltage	V <sub>OL</sub>	I <sub>OL</sub> =2.1mA			0.4	V
Operating Supply Current (DC)	ICCA1	V <sub>CE</sub> ≤0.2V, I <sub>I/O</sub> =0mA, V <sub>IN</sub> ≥0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V			15	mA
	ICCA2	V <sub>CE</sub> =V <sub>IL</sub> , I <sub>I/O</sub> =0mA, V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>			15	mA
Average Operating Supply Current	ICCA3	V <sub>CE</sub> =V <sub>IL</sub> , I <sub>I/O</sub> =0mA, min cycle			70	mA
Standby Supply Current	ICCS1	V <sub>CE</sub> ≥V <sub>CC</sub> -0.2V, V <sub>IN</sub> =0~V <sub>CC</sub>		2	100	μA
			LC36256PL,PML-10/12/15		1	mA
	ICCS2	V <sub>CE</sub> =V <sub>IH</sub> , V <sub>IN</sub> =0~V <sub>CC</sub>			3	mA

\*:Reference value at Vcc=5V, Ta=+25°C

### ■ Input/Output Capacitance at Ta=+25°C, f=1MHz

Parameter	Symbol	Condition	min	typ	max	unit
Input/Output Capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> =0V			10	pF
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V			5	pF

Note)The values shown above are based on sampling inspection.

### ■ AC Electrical Characteristics at Ta=0 to +70°C, Vcc=5V±10%

#### AC Test Conditions

Input pulse voltage level	:0.6V, 2.4V
Input rise/fall time	:5ns
Input/output timing level	:1.5V
Output load	:1TTL gate + C <sub>L</sub> = 100pF (Including jig capacitance)

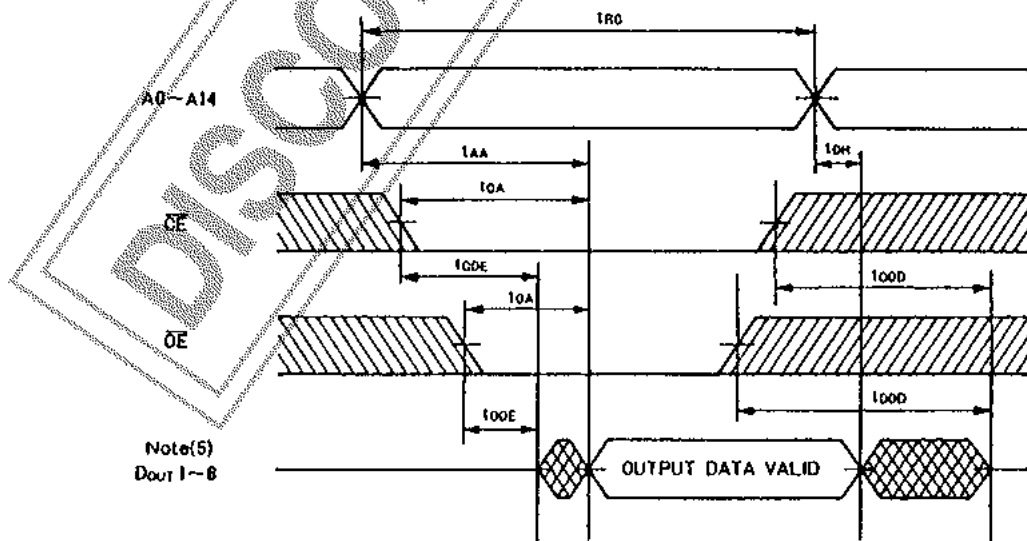
Read Cycle

Parameter	Symbol	LC36256P, PL, PM, PML-10		LC36256P, PL, PM, PML-12		LC36256P, PL, PM, PML-15		unit
		min	max	min	max	min	max	
Read Cycle Time	t <sub>RC</sub>	100		120		150		ns
Address Access time	t <sub>AA</sub>		100		120		150	ns
$\overline{CE}$ Access Time	t <sub>CA</sub>		100		120		150	ns
$\overline{OE}$ Access Time	t <sub>OA</sub>		50		60		70	ns
Output Hold Time	t <sub>OH</sub>	10		10		10		ns
$\overline{CE}$ -Output Enable Time	t <sub>COE</sub>	10		10		10		ns
$\overline{OE}$ -Output Enable Time	t <sub>OOE</sub>	5		5		5		ns
$\overline{CE}$ -Output Disable Time	t <sub>COD</sub>		35		40		50	ns
$\overline{OE}$ -Output Disable Time	t <sub>OOD</sub>		35		40		50	ns

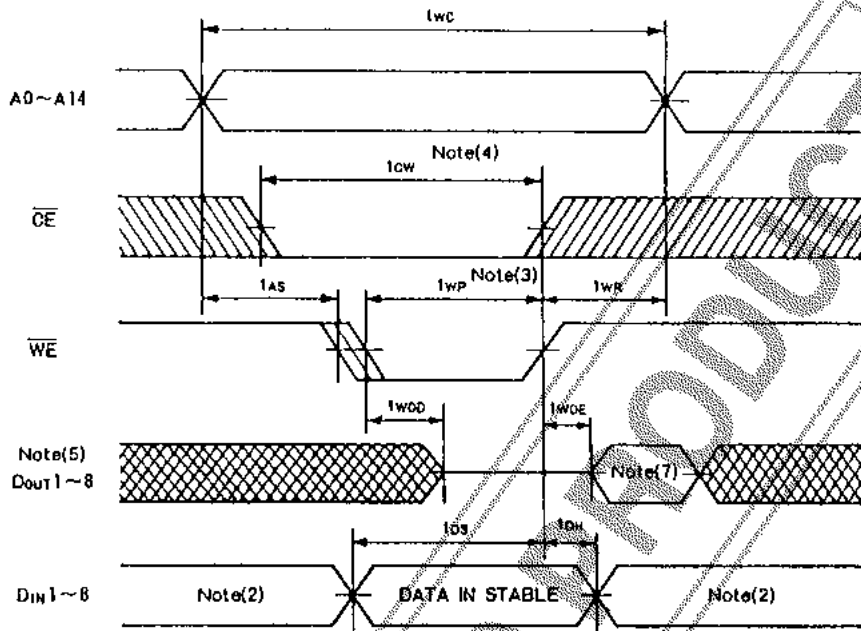
Write Cycle

Parameter	Symbol	LC36256P, PL, PM, PML-10		LC36256P, PL, PM, PML-12		LC36256P, PL, PM, PML-15		unit
		min	max	min	max	min	max	
Write Cycle Time	t <sub>WC</sub>	100		120		150		ns
Address Setup Time	t <sub>AS</sub>	0		0		0		ns
Write Pulse Width	t <sub>WP</sub>	70		80		90		ns
$\overline{CE}$ Setup Time	t <sub>CW</sub>	80		90		100		ns
Write Recovery Time	t <sub>WR</sub>	0		0		0		ns
Data Setup Time	t <sub>DS</sub>	40		50		60		ns
Data Hold Time	t <sub>DH</sub>	0		0		0		ns
$\overline{WE}$ -Output Enable Time	t <sub>WOE</sub>	10		10		10		ns
$\overline{WE}$ -Output Disable time	t <sub>WOD</sub>		35		40		50	ns

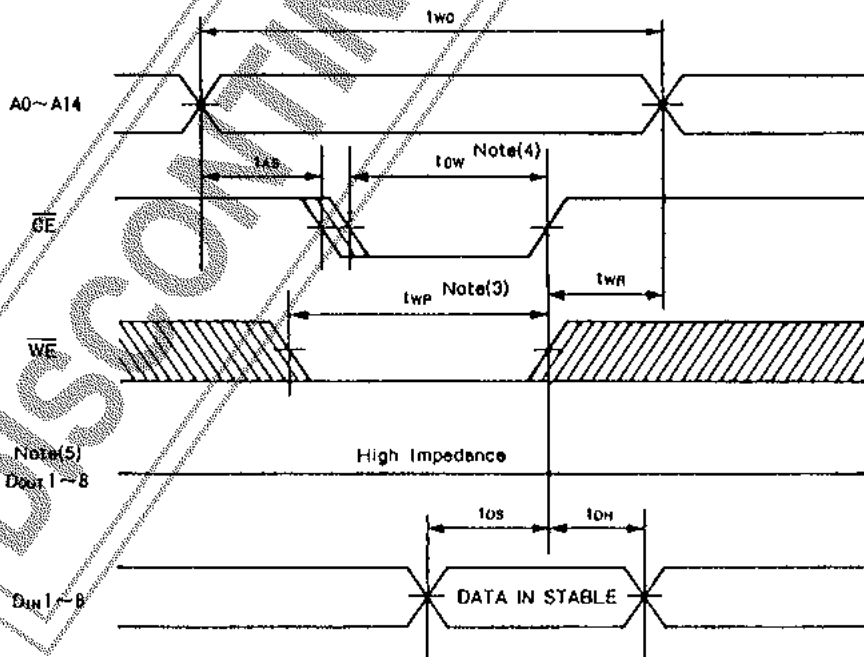
Timing Chart  
[Read Cycle] Note(1)



[Write Cycle 1] ( $\overline{WE}$  Write) Note(6)



[Write Cycle 2] ( $\overline{CE}$  Write) Note(6)



- Note) (1)  $\overline{WE}$  must be high during read cycle.  
 (2) When  $D_{OUT}$  is in the output state, no opposite polarity signal must be applied externally.  
 (3)  $t_{WP}$  occurs during the overlap of a low  $\overline{CE}$  and a low  $\overline{WE}$ .  $t_{WP}$  is measured from  $\overline{WE}$  going low to the earlier of  $\overline{CE}$  going high.  
 (4)  $t_{CW}$  occurs during the overlap of a low  $\overline{CE}$  and A low  $\overline{WE}$ .  $t_{CW}$  is measured form  $\overline{CE}$  going low to the earlier of  $\overline{CE}$  or  $\overline{WE}$  going high.  
 (5)  $D_{OUT}$  is in a high impedance state when  $\overline{OE}$  is high or  $\overline{CE}$  is high or  $\overline{WE}$  is low.  
 (6) When  $\overline{OE}$  is high during write cycle,  $D_{OUT}$  is in a high impedance state.  
 (7)  $D_{OUT}$  has the same polarity as write data of this write cycle.

■ Data Retention Characteristics at  $T_a=0$  to  $+70^\circ\text{C}$

Parameter	Symbol	Condition	min	typ*	max	unit
Data Retention Supply Voltage	VDR	$V_{CE} \geq V_{CC} - 0.2\text{V}$	2.0		5.5	V
Data Retention Supply Current	I <sub>CCDR</sub>	$V_{CC} = 3.0\text{V}$ $V_{CE} \geq V_{CC} - 0.2\text{V}$		1.0	50	$\mu\text{A}$
					500	$\mu\text{A}$
Chip Enable Setup Time	t <sub>CDR</sub>		0			ns
Chip Enable Hold Time	t <sub>R</sub>		t <sub>RC**</sub>			ns

\*Reference value at  $T_a=+25^\circ\text{C}$  \*\*t<sub>RC</sub>=Read Cycle Time

Data Retention Waveform

