Ordering number : EN4327

Asynchronous Silicon Gate CMOS LSI

No. 4327

LC36256ALL, AMLL-70/85/10/12

256 K (32768 words × 8 bits) SRAM

Overview

The LC36256ALL, AMLL-70/85/10/12 are fully asynchronous silicon gate CMOS static RAMs with an 32768 words × 8 bits.

This series has $\overline{CE}$ chip enable pin for device select/nonselect control and an $\overline{OE}$ output enable pin for output control, and features high speed as well as low power dissipation.

Current dissipation is notably reduced during stand-by and data retention. For these reasons, this series is most suited for use in systems requiring high speed, low power consumption and long-term battery backup. Simple memory capacity expansion is also supported.

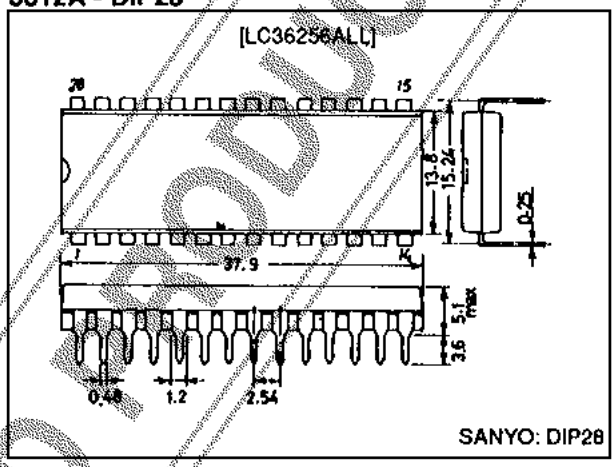
Features

- Access time
  - 70 ns (max.) : LC36256ALL-70, LC36256AMLL-70
  - 85 ns (max.) : LC36256ALL-85, LC36256AMLL-85
  - 100 ns (max.) : LC36256ALL-10, LC36256AMLL-10
  - 120 ns (max.) : LC36256ALL-12, LC36256AMLL-12
- Low current dissipation
  - During standby
    - 0.5 µA (max.) / Ta = 25°C
    - 1 µA (max.) / Ta = 0 to 40°C
    - 5 µA (max.) / Ta = 0 to 70°C
  - During data retention
    - 0.3 µA (max.) / Ta = 25°C
    - 0.6 µA (max.) / Ta = 0 to 40°C
    - 3 µA (max.) / Ta = 0 to 70°C
  - During operation (DC)
    - 10 mA (max.)
- Single 5 V power supply: 5 V ±10%
- Data retention power supply voltage: 2.0 to 5.5 V
- No clock required (Fully static memory)
- All input/output levels are TTL compatible
- Common input/output pins, with three output states
- Packages
  - DIP 28-pin plastic package (600 mil) : LC36256ALL
  - SOP 28-pin plastic package (450 mil) : LC36256AMLL

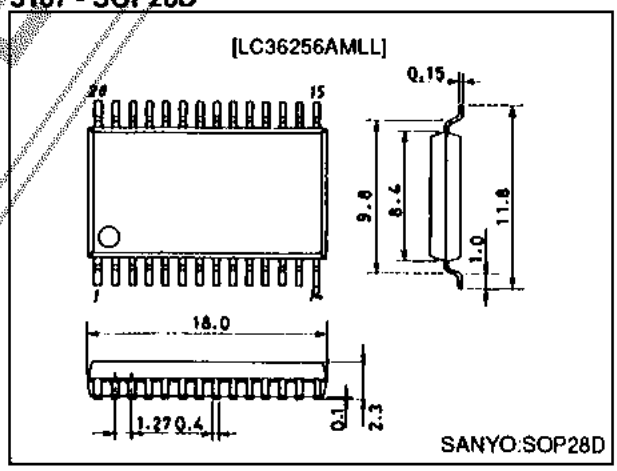
Package Dimensions

unit : mm

3012A - DIP28

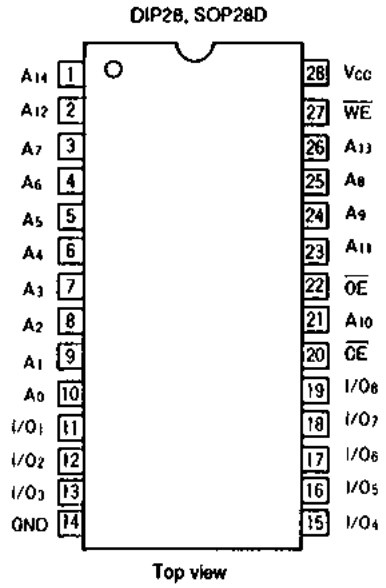


3187 - SOP28D

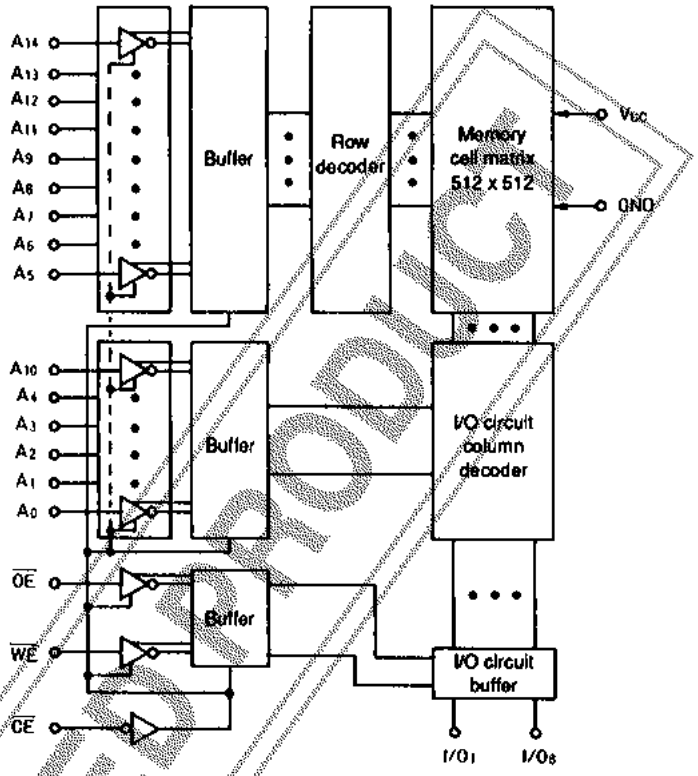


SANYO Electric Co., Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO JAPAN

Pin Assignment



Block Diagram



A0 to A14 : Address input
$\overline{WE}$: Read/write control input
$\overline{OE}$: Output enable input
$\overline{CE}$: Chip enable input
I/O1 to I/O8 : Data input/output
VCC, GND : Power supply pins

Functions

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Supply current
Read cycle	L	L	H	Data output	ICCA
Write cycle	L	X	L	Data input	ICCA
Output disable	L	H	H	High impedance	ICCA
Nonselect	H	X	X	High impedance	ICCS

X : H or L

Specifications

Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		7.0	V
Input pin voltage	V_{IN}		−0.5* to V_{CC}+0.5	V
I/O pin voltage	$V_{I/O}$		−0.5* to V_{CC}+0.5	V
Allowable power dissipation	Pd max	LC36256ALL	1.0	W
		LC36256AMLL	0.7	W
Operating temperature range	Topr		0 to +70	°C
Storage temperature range	Tstg		−55 to +150	°C

* −3.0 V when pulse width is less than 50 ns

DC Recommended Operating Ranges at Ta = 0 to 70°C

Parameter	Symbol	min	typ	max	Unit
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high level voltage	V_{IH}	2.2		V_{CC}+0.3	V
Input low level voltage	V_{IL}	−0.3*		+0.8	V

* −3.0 V when pulse width is less than 50 ns

DC Electrical Characteristics at Ta = 0 to 70°C, V_{CC} = 5 V ±10%

Parameter	Symbol	Conditions			min	typ*	max	Unit
Input leakage current	I_{LI}	V_{IN} = 0 to V_{CC}			−0.5		+0.5	µA
I/O leakage current	I_{LO}	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0 to V_{CC}			−0.5		+0.5	µA
Output high level voltage	V_{OH}	I_{OH} = −1.0mA			2.4			V
Output low level voltage	V_{OL}	I_{OL} = 2.1mA					0.4	V
Operating supply current (DC)	I_{CCA1}	$\overline{CE}$ ≤ 0.2V, V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC}−0.2V				1	5	mA
	I_{CCA2}	$\overline{CE}$ = V_{IL}, $I_{I/O}$=0mA				3	10	mA
Average operating supply current	I_{CCA3}	min cycle Duty = 100% $I_{I/O}$ = 0mA	Access time	70ns		30	50	mA
				85ns		25	50	
				100ns		23	50	
				120ns		20	50	
Standby supply current	I_{CCS1}	$V_{\overline{CE}}$ ≥ V_{CC}-0.2V	LC36256ALL/ AMLL	0 to 70°C			5	µA
				0 to 40°C			1	
				25°C		0.2	0.5	
	I_{CCS2}	$\overline{CE}$ = V_{IH}				0.4	2	mA

* Reference values at V_{CC} = 5 V, Ta = 25°C

Input/Output Capacitance at Ta = 25°C, f = 1 MHz

Parameter	Symbol	Conditions	min	typ	max	Unit
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0V			8	pF
Input capacitance	C_{IN}	V_{IN} = 0V			6	pF

Note: These parameters were obtained through sampling, and not full-lot measurement.

AC Electrical Characteristics at Ta = 0 to 70°C, V_{CC} = 5 V ±10%

AC testing conditions

Input pulse voltage level	:	0.8 V, 2.2 V
Input rise and fall time	:	5 ns
Input - output timing level	:	1.5 V
Output load	:	1 TTL gate + C_L = 100 pF (85 ns/100 ns/120 ns) 1 TTL gate + C_L = 30 pF (70 ns) (including scope and jig capacitance)

Read Cycle

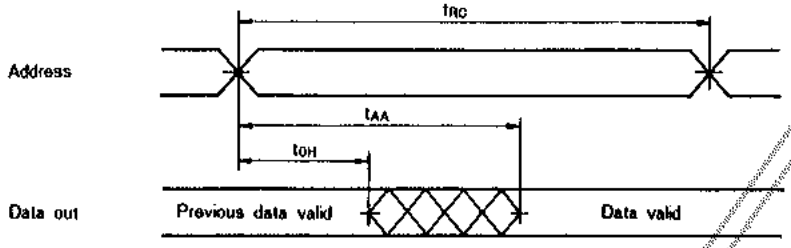
Parameter	Symbol	LC36256ALL-70 LC36256AMLL-70		LC36256ALL-85 LC36256AMLL-85		LC36256ALL-10 LC36256AMLL-10		LC36256ALL-12 LC36256AMLL-12		Unit
		min	max	min	max	min	max	min	max	
Read cycle time	t_{RC}	70		85		100		120		ns
Address access time	t_{AA}		70		85		100		120	ns
$\overline{CE}$ access time	t_{CA}		70		85		100		120	ns
$\overline{OE}$ access time	t_{OA}		35		45		50		60	ns
Output hold time	t_{OH}	20		20		20		20		ns
$\overline{CE}$ output enable time	t_{COE}	10		10		10		10		ns
$\overline{OE}$ output enable time	t_{OOE}	5		5		5		5		ns
$\overline{CE}$ output disable time	t_{COD}	0	30	0	30	0	30	0	30	ns
$\overline{OE}$ output disable time	t_{OOD}	0	30	0	30	0	30	0	30	ns

Write Cycle

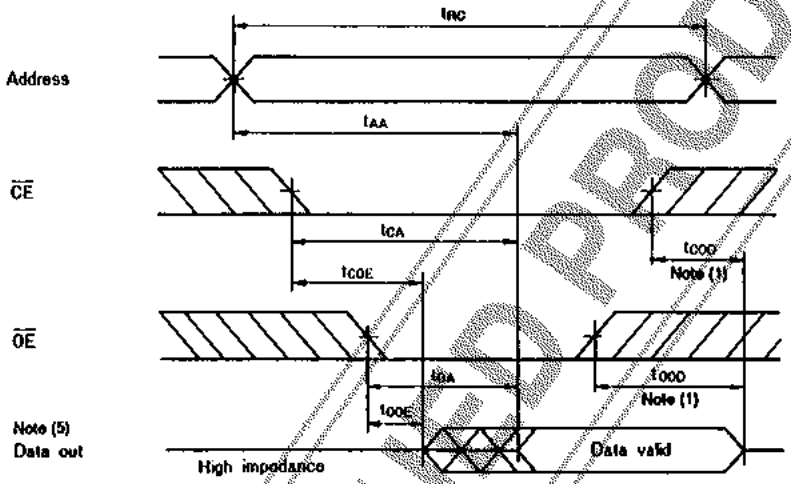
Parameter	Symbol	LC36256ALL-70 LC36256AMLL-70		LC36256ALL-85 LC36256AMLL-85		LC36256ALL-10 LC36256AMLL-10		LC36256ALL-12 LC36256AMLL-12		Unit
		min	max	min	max	min	max	min	max	
Write cycle time	t_{WC}	70		85		100		120		ns
Address valid to end of write	t_{AW}	65		75		80		100		ns
Address setup time	t_{AS}	0		0		0		0		ns
Write pulse width	t_{WP}	50		50		60		70		ns
$\overline{CE}$ setup time	t_{CW}	65		75		80		100		ns
Write recovery time ($\overline{WE}$)	t_{WR}	0		0		0		0		ns
Write recovery time ($\overline{CE}$)	t_{WR1}	0		0		0		0		ns
Data setup time	t_{DS}	30		30		35		40		ns
Data hold time	t_{DH}	0		0		0		0		ns
$\overline{WE}$ output enable time	t_{WOE}	10		10		10		10		ns
$\overline{WE}$ output disable time	t_{WOD}	0	25	0	25	0	25	0	25	ns

Timing Chart

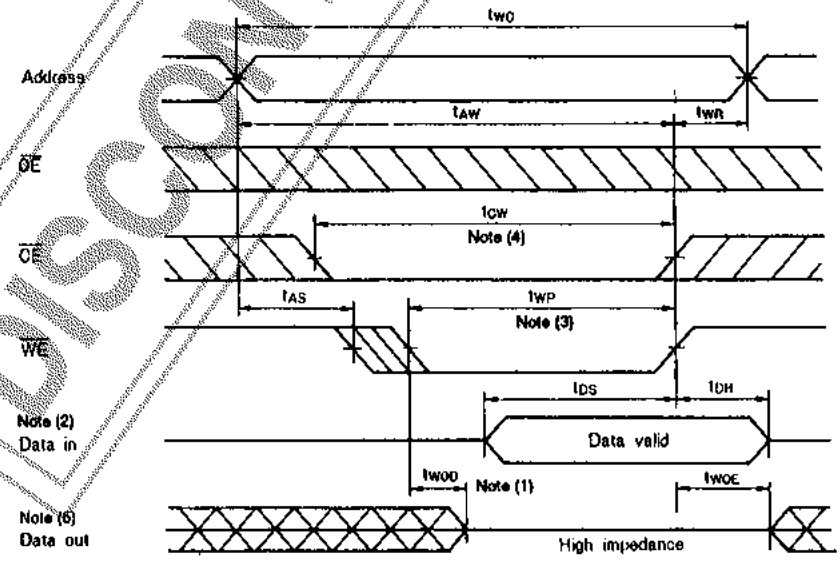
• Read Cycle (1): $\overline{CE}$ = $\overline{OE}$ = VIL, $\overline{WE}$ = VIH



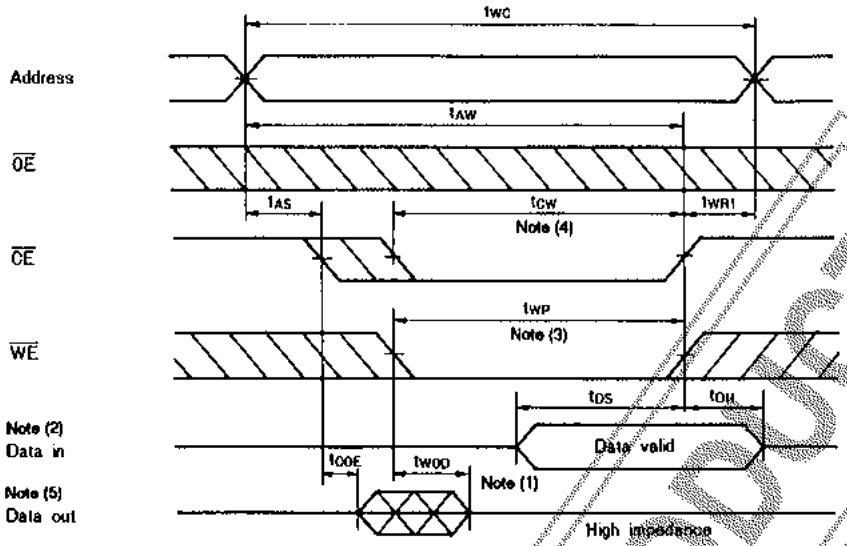
• Read Cycle (2): $\overline{WE}$ = VIH



• Write Cycle (1): $\overline{WE}$ Control Note (6)



• Write Cycle (2): $\overline{CE}$ Control Note (6)



Notes (1) t_{COD}, t_{OOD}, and t_{WOD} are defined as the time at which the outputs becomes the high impedance state and are not referred to output voltage levels.

(2) An external antiphase signal must not be applied when DOUT is in the output state.

(3) t_{WP} is the time interval that $\overline{CE}$ and $\overline{WE}$ are low-level and is defined as the interval from the falling of $\overline{WE}$ to the rising of $\overline{CE}$ or $\overline{WE}$ whichever is earlier.

(4) t_{CW} is the time interval that $\overline{CE}$ and $\overline{WE}$ are low-level and is defined as the time from the falling of $\overline{CE}$ to the rising of $\overline{CE}$ or $\overline{WE}$ whichever is earlier.

(5) DOUT goes to the high-impedance state when either $\overline{OE}$ is high-level, $\overline{CE}$ is high-level, or $\overline{WE}$ is low-level.

(6) When $\overline{OE}$ is high-level during the write cycle, DOUT goes to the high-impedance state.

Data Retention Characteristics at Ta = 0 to 70°C

Parameter	Symbol	Conditions		LC36256ALL/AMLL			Unit
				min	typ*	max	
Data retention supply voltage	V_{DR}	$V_{\overline{CE}} \geq V_{CC}-0.2V$		2.0		5.5	V
Data retention supply current	I_{CCDR1}	V_{CC} = 3.0V, $V_{\overline{CE}} \geq 2.8V$	0 to 70°C			3	µA
			0 to 40°C			0.6	
			25°C		0.1	0.3	
	I_{CCDR2}	V_{CC} = 2.0 to 5.5V, $V_{\overline{CE}} \geq V_{CC}-0.2V$			0.2	5	µA
$\overline{CE}$ setup time	t_{CDR}			0			ns
$\overline{CE}$ hold time	t_R			t_{RC}**			ns

* Reference values at V_{CC} = 5V, Ta = 25°C ** t_{RC} = Read Cycle time

Data Retention Waveform