Ordering number: EN4794B

SANYO

No.4794B

LC3564S, SS, SM, ST-70/85/10

64K (8192words×8 bits)SRAM

Overview

The LC3564S, LC3564SS, LC3564SM, and LC3564ST are asynchronous silicon gate CMOS static RAMs with an 8192-word X 8-bit organization. These SRAMs are full CMOS type SRAMs with a six-transistor memory cell and feature high-speed access, a low operating current, and an ultra-low standby current. Control signal inputs include an $\overline{OE}$ input for high-speed memory access and two chip enable inputs, $\overline{CE1}$ and CE2, for power-down and device selection. Thus these products are optimal for systems that require low power and/or battery backup and they support easy expansion of memory capacities. The ultra-low standby mode current drain allows capacitors to be used for backup and 3V operation makes these devices an excellent choice for use in battery operated portable equipment.

Features

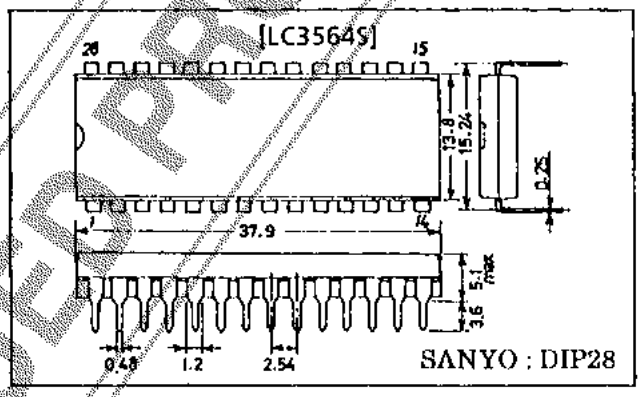
- Supply voltage : 2.7 to 5.5V
  - 5V operation : 5.0V±10%
  - 3V operation : 3.0V±10%
- Address access time (t_{AA})
  - 5V operation
  - LC3564S, SS, SM, ST-70 : 70ns (max.)
  - LC3564S, SS, SM, ST-85 : 85ns (max.)
  - LC3564S, SS, SM, ST-10 : 100ns (max.)
  - 3V operation
  - LC3564S, SS, SM, SS-70 : 200ns (max.)
  - LC3564S, SS, SM, SS-85 : 250ns (max.)
  - LC3564S, SS, SM, SS-10 : 500ns (max.)
- Ultra-low standby current
  - 5V operation : 1.0μA (Ta≦70°C)
  - 3.0μA (Ta≦85°C)
  - 3V operation : 0.8μA (Ta≦70°C)
  - 2.5μA (Ta≦85°C)
- Operating temperature
  - 3V operation : −40°C to +85°C
  - 5V operation : −40°C to +85°C
- Data retention voltage : 2.0 to 5.5V
- All I/O levels
  - 5V operation : TTL compatible
  - 3V operation : V_{CC}−0.2V/0.2V
- Three control inputs ($\overline{OE}$, $\overline{CE1}$, CE2)
- Common input/output pins, three-state outputs
- No clock or timing signals required

- Package :
  - 28-pin DIP (600mil)plastic package : LC3564S
  - 28-pin DIP (300mil)plastic package : LC3564SS
  - 28-pin SOP (450mil)plastic package : LC3564SM
  - 28-pin TSOP (8×13.4mm)plastic package : LC3564ST

Package Dimensions

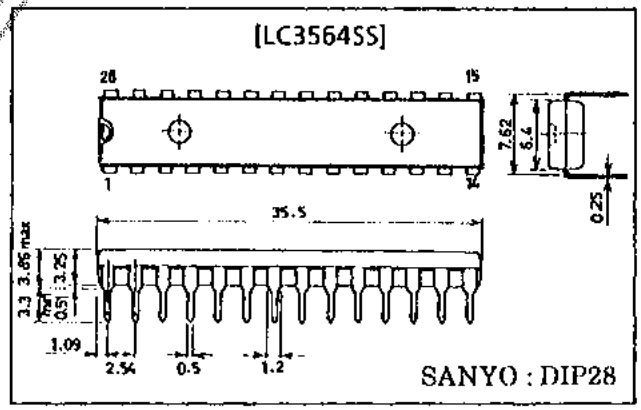
unit : mm

3012A-DIP28



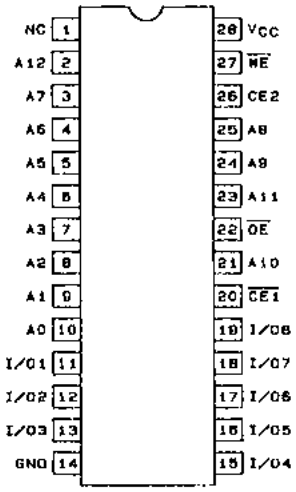
unit : mm

3133-DIP28



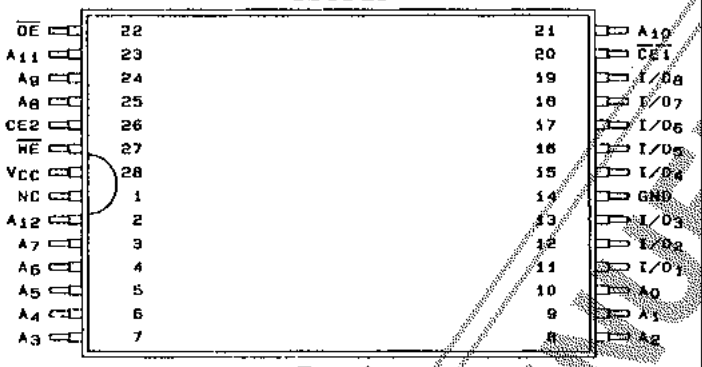
Pin Assignments

DIP28, SOP28



Top view

TSOP28



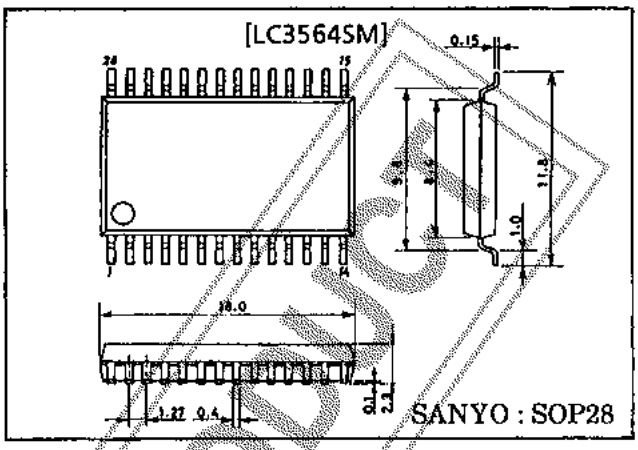
Top view

A0 to A12	Address input
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
$\overline{CE1}$, CE2	Chip enable
I/O_1 to I/O_8	Data input/output
V_{CC}, GND	Power, ground

Package Dimensions

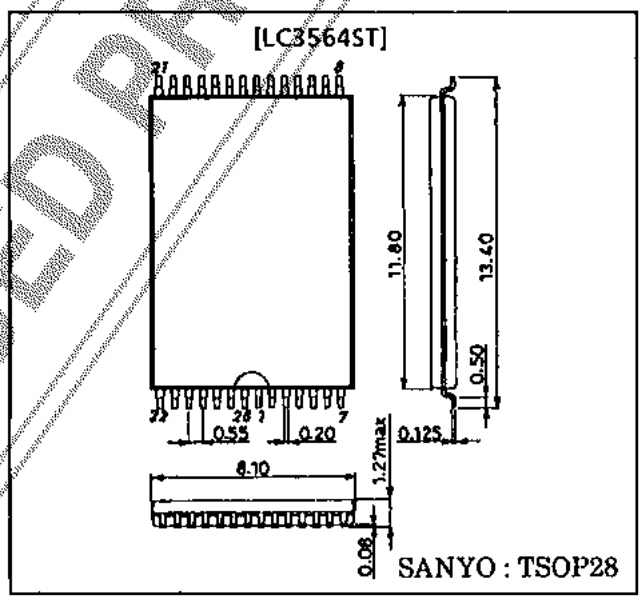
unit : mm

3187-SOP28

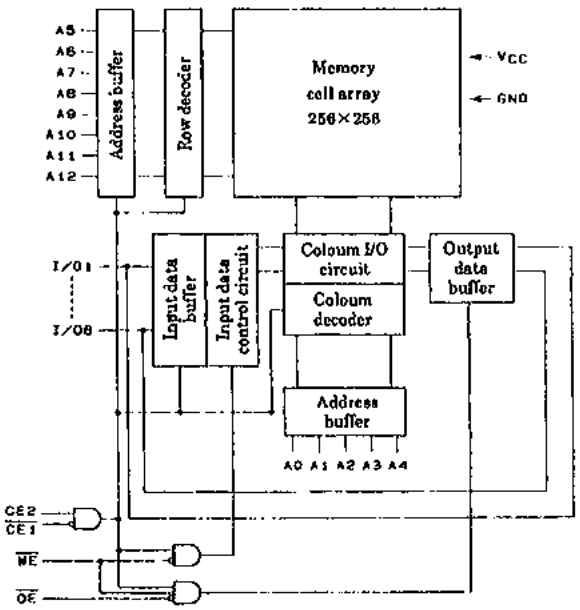


unit : mm

3221-TSOP28



Block Diagram



Pin Functions

Mode	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	I/O	Current
Read Cycle	L	H	L	H	Data output	I_{CCA}
Write Cycle	L	H	×	L	Data input	I_{CCA}
Output Disable	L	H	H	H	High impedance	I_{CCA}
Unselected	H	×	×	×	High impedance	I_{CCS}
	×	L	×	×	High impedance	I_{CCS}

× : Arbitrary H or L

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Max supply voltage	V_{CC} max		7.0	V
Input voltage	V_{IN}		−0.3* to V_{CC} + 0.3	V
I/O voltage	$V_{I/O}$		−0.3 to V_{CC} + 0.3	V
Operating temperature range	Topr		−40 to +85	°C
Storage temperature range	Tstg		−55 to +125	°C

*) The inputs may undershoot to −3.0V (min.) for periods less than 30ns.

I/O Capacitance at Ta = 25°C, f = 1MHz

Parameter	Symbol	Conditions	min	typ	max	Unit
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0V		6	10	pF
Input capacitance	C_I	V_{IN} = 0V		6	10	pF

(Note) This parameter is sampled and not 100% tested.

5V Operation

DC Recommended Operating Ranges at Ta = −40 to +85°C, V_{CC} = 4.5 to 5.5V

Parameter	Symbol	min	typ	max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2		V_{CC} + 0.3	V
	V_{IL}	−0.3*		+0.8	V

*) The inputs may undershoot to −3.0V (min.) for periods less than 30ns.

DC Electrical Characteristics at Ta = −40 to +85°C, V_{CC} = 4.5 to 5.5V

Parameter		Symbol	Conditions			min	typ*	max	Unit
Input leakage current		I_{LI}	V_{IN} = 0 to V_{CC}			−1.0		+1.0	μA
I/O leakage current		I_{LO}	$V_{\overline{CE1}} = V_{IH}$ or $V_{CE2} = V_{IL}$ or $V_{\overline{OE}} = V_{IH}$ or $V_{\overline{WE}} = V_{IL}$, $V_{I/O}$ = 0 to V_{CC}			−1.0		+1.0	μA
Output high level voltage		V_{OH}	I_{OH} = −1.0mA			2.4			V
Output low level voltage		V_{OL}	I_{OL} = 2.0mA					0.4	V
Operating current	V_{CC}−0.2V/ 0.2V input	I_{CCA1}	$V_{\overline{CE1}} \leqq 0.2V$, $V_{CE2} \geqq V_{CC}-0.2V$, $I_{I/O}$ = 0mA, $V_{IN} \leqq 0.2V$ or $V_{IN} \geqq V_{CC}-0.2V$		Ta≦70°C		0.01	1.0	μA
					Ta≦85°C			3.0	
		I_{CCA4}	$V_{\overline{CE1}} \leqq 0.2V$, $V_{CE2} \geqq V_{CC}-0.2V$, $I_{I/O}$ = 0mA, DUTY 100%	min cycle	LC3564S, SS, SM, ST-70			35	mA
					LC3564S, SS, SM, ST-85			35	
					LC3564S, SS, SM, ST-10			30	
				1μs cycle			4		mA
	TTL input	I_{CCA2}	$V_{\overline{CE1}} = V_{IL}$, $V_{CE2} = V_{IH}$, $I_{I/O}$ = 0mA, $V_{IN} = V_{IH}$ or V_{IL}					7	mA
		I_{CCA3}	$V_{\overline{CE1}} = V_{IL}$, $V_{CE2} = V_{IH}$, $I_{I/O}$ = 0mA, DUTY 100%	min cycle	LC3564S, SS, SM, SS-70			40	mA
					LC3564S, SS, SM, SS-85			40	
					LC3564S, SS, SM, SS-10			35	
				1μs cycle			7		mA
Standby current	V_{CC}−0.2V/ 0.2V input	I_{CCS1}	$V_{CE2} \leqq 0.2V$ or $V_{\overline{CE1}} \geqq V_{CC}-0.2V$ $V_{CE2} \geqq V_{CC}-0.2V$		Ta≦70°C		0.01	1.0	μA
					Ta≦85°C			3.0	
	TTL input	I_{CCS2}	$V_{CE2} = V_{IL}$ or $V_{\overline{CE1}} = V_{IH}$, V_{IN} = 0 to V_{CC}					2.0	mA

*) Reference value at V_{CC} = 5V, Ta = 25°C

AC Electrical Characteristics at Ta = −40 to +85°C, V_{CC} = 4.5 to 5.5V

AC test conditions

Input pulse levels		: V_{IH} = 2.4V, V_{IL} = 0.6V
Input rise and fall time		: 5ns
Input and output timing reference levels		: 1.5V
Output load	LC3564S, SS, SM, ST-70	: 30pF + 1TTL gate (including jig capacitance)
	LC3564S, SS, SM, ST-85/10	: 100pF + 1TTL gate (including jig capacitance)

Read Cycle

Parameter	Symbol	LC3564S, SS, SM, ST						Unit
		−70		−85		−10		
		min	max	min	max	min	max	
Read cycle time	t_{RC}	70		85		100		ns
Address access time	t_{AA}		70		85		100	ns
$\overline{CE1}$ access time	t_{CA1}		70		85		100	ns
CE2 access time	t_{CA2}		70		85		100	ns
$\overline{OE}$ access time	t_{OA}		35		45		50	ns
Output hold time	t_{OH}	10		10		10		ns
$\overline{CE1}$ − output enable time	t_{COE1}	10		10		10		ns
CE2 − output enable time	t_{COE2}	10		10		10		ns
$\overline{OE}$ − output enable time	t_{OOE}	5		5		5		ns
$\overline{CE1}$ − output disable time	t_{COD1}		30		35		35	ns
CE2 − output disable time	t_{COD2}		30		35		35	ns
$\overline{OE}$ − output disable time	t_{OOD}		25		25		25	ns

Write Cycle

Parameter	Symbol	LC3564S, SS, SM, ST						Unit
		−70		−85		−10		
		min	max	min	max	min	max	
Write cycle time	t_{WC}	70		85		100		ns
Address setup time	t_{AS}	0		0		0		ns
Write pulse width	t_{WP}	50		55		55		ns
$\overline{CE1}$ setup time	t_{CW1}	60		65		65		ns
CE2 setup time	t_{CW2}	60		65		65		ns
Write recovery time	t_{WR}	0		0		0		ns
$\overline{CE1}$ write recovery time	t_{WR1}	0		0		0		ns
CE2 write recovery time	t_{WR2}	0		0		0		ns
Data setup time	t_{DS}	35		40		40		ns
Data hold time	t_{DH}	0		0		0		ns
$\overline{CE1}$ data hold time	t_{DH1}	0		0		0		ns
CE2 data hold time	t_{DH2}	0		0		0		ns
$\overline{WE}$ − output enable time	t_{WOE}	5		5		5		ns
$\overline{WE}$ − output disable time	t_{WOD}		30		35		35	ns

3V Operation

DC Recommended Operating Ranges at Ta = −40 to +85°C, V_{CC} = 2.7 to 3.3V

Parameter	Symbol	min	typ	max	Unit
Supply voltage	V_{CC}	2.7	3.0	3.3	V
Input voltage	V_{IH}	V_{CC}−0.2		V_{CC}	V
	V_{IL}	0		0.2	V

DC Electrical Characteristics at Ta = −40 to +85°C, V_{CC} = 2.7 to 3.3V

Parameter		Symbol	Conditions			min	typ*	max	Unit
Input leakage current		I_{LI}	V_{IN} = 0 to V_{CC}			−1.0		+1.0	μA
I/O leakage current		I_{LO}	$V_{\overline{CE1}} = V_{IH}$ or $V_{CE2} = V_{IL}$ or $V_{\overline{OE}} = V_{IH}$ or $V_{\overline{WE}} = V_{IL}$, $V_{I/O}$ = 0 to V_{CC}			−1.0		+1.0	μA
Output high level voltage		V_{OH}	I_{OH} = −0.5mA			V_{CC}−0.2V			V
Output low level voltage		V_{OL}	I_{OL} = 1.0mA					0.2	V
Operating current	V_{CC}−0.2V/0.2V input	I_{CCA1}	$V_{\overline{CE1}} \geqq V_{IL}$, $V_{CE2} \geqq V_{IH}$, $I_{I/O}$ = 0mA, $V_{IN} \leqq V_{IL}$, $V_{IN} \geqq V_{IH}$		Ta≦70°C		0.01	0.8	μA
					Ta≦85°C			2.5	
		I_{CCA4}	$V_{\overline{CE1}} \leqq V_{IL}$, $V_{CE2} \geqq V_{IH}$, $I_{I/O}$ = 0mA, DUTY = 100%	min cycle	LC3564S, SS, SM, ST-70			20	mA
					LC3564S, SS, SM, ST-85			20	
					LC3564S, SS, SM, ST-10			10	
				1μs cycle			3		mA
Standby current	V_{CC}−0.2V/0.2V input	I_{CCS1}	$V_{CE2} \leqq V_{IL}$ or $V_{\overline{CE1}} \geqq V_{IH}$ or $V_{CE2} \geqq V_{IH}$		Ta≦70°C		0.01	0.8	μA
					Ta≦85°C			2.5	

*) Reference value at V_{CC} = 3V, Ta = 25°C

AC Electrical Characteristics at Ta = −40 to +85°C, V_{CC} = 2.7 to 3.3V

AC test conditions

Input pulse levels		: $V_{IH} = V_{CC} - 0.2V$, $V_{IL} = 0.2V$
Input rise and fall time		: 10ns
Input and output timing reference levels		: 1.5V
Output load	LC3564S, SS, SM, ST-70	: 30pF (including scope and jig)
	LC3564S, SS, SM, ST-85/10	: 100pF (including scope and jig)

Read Cycle

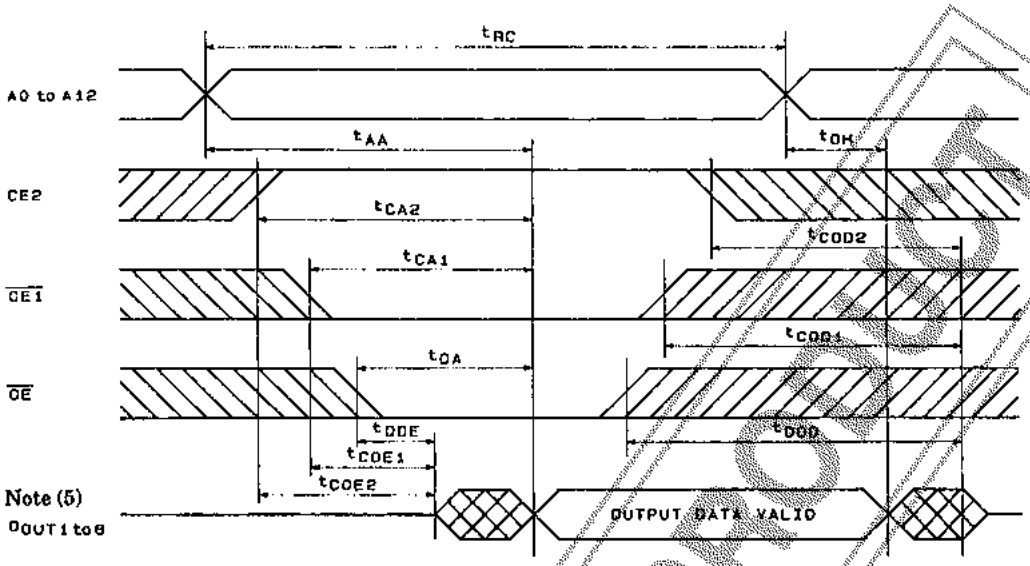
Parameter	Symbol	LC3564S, SS, SM, ST						Unit
		−70		−85		−10		
		min	max	min	max	min	max	
Read cycle time	t_{RC}	200		250		500		ns
Address access time	t_{AA}		200		250		500	ns
$\overline{CE1}$ access time	t_{CA1}		200		250		500	ns
CE2 access time	t_{CA2}		200		250		500	ns
$\overline{OE}$ access time	t_{OA}		100		130		250	ns
Output hold time	t_{OH}	20		20		20		ns
$\overline{CE1}$ − output enable time	t_{COE1}	20		20		20		ns
CE2 − output enable time	t_{COE2}	20		20		20		ns
$\overline{OE}$ − output enable time	t_{OOE}	10		10		10		ns
$\overline{CE1}$ − output disable time	t_{COD1}		60		80		120	ns
CE2 − output disable time	t_{COD2}		60		80		120	ns
$\overline{OE}$ − output disable time	t_{OOD}		50		70		100	ns

Write Cycle

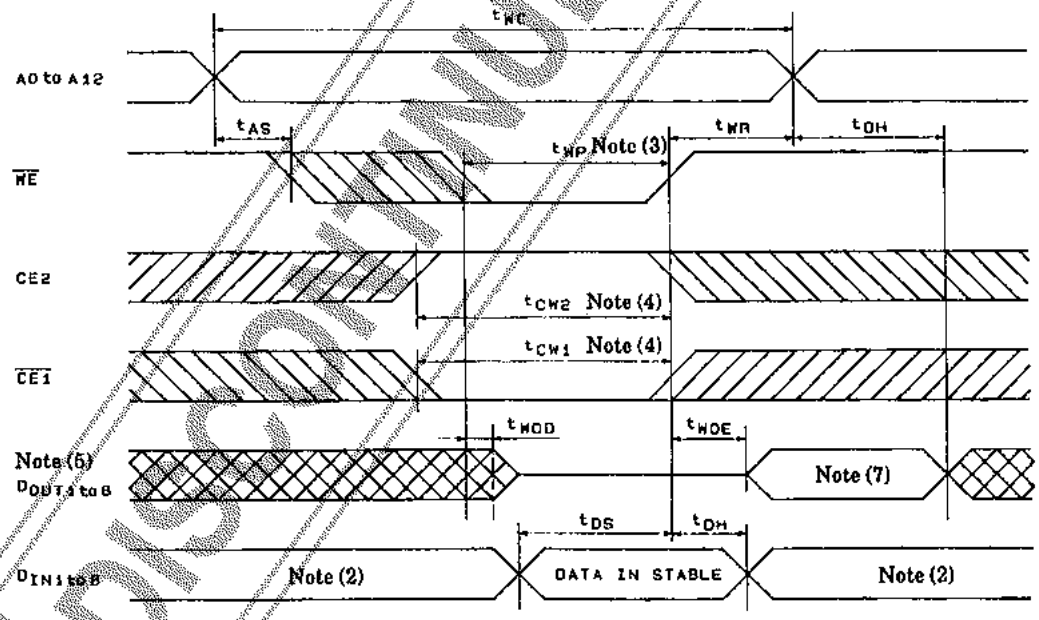
Parameter	Symbol	LC3564S, SS, SM, ST						Unit
		−70		−85		−10		
		min	max	min	max	min	max	
Write cycle time	t_{WC}	200		250		500		ns
Address setup time	t_{AS}	0		0		0		ns
Write pulse width	t_{WP}	140		160		200		ns
$\overline{CE1}$ setup time	t_{CW1}	150		180		250		ns
CE2 setup time	t_{CW2}	150		180		250		ns
Write recovery time	t_{WR}	0		0		0		ns
$\overline{CE1}$ write recovery time	t_{WR1}	0		0		0		ns
CE2 write recovery time	t_{WR2}	0		0		0		ns
Data setup time	t_{DS}	130		150		180		ns
Data hold time	t_{DH}	0		0		0		ns
$\overline{CE1}$ data hold time	t_{DH1}	0		0		0		ns
CE2 data hold time	t_{DH2}	0		0		0		ns
$\overline{WE}$ − output enable time	t_{WOE}	10		10		10		ns
$\overline{WE}$ − output disable time	t_{WOD}		60		80		120	ns

Timing Waveform

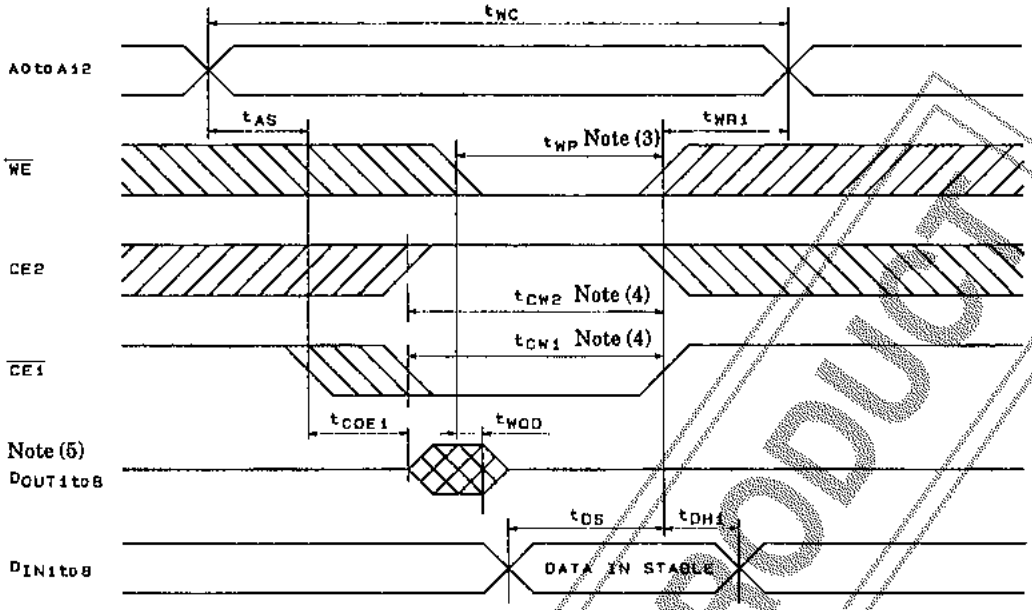
Read Cycle Note (1)



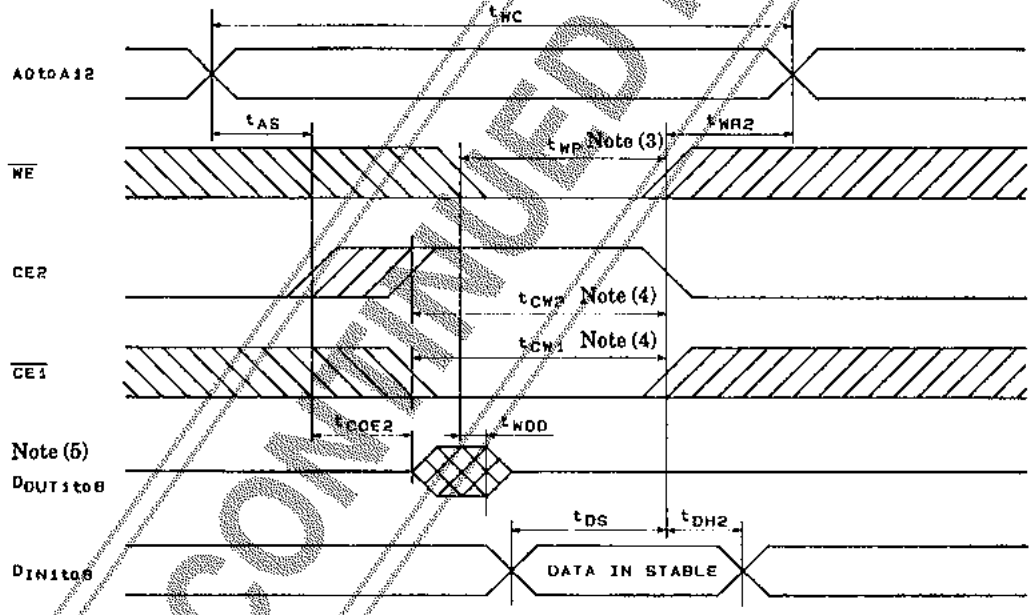
Write Cycle 1 ($\overline{WE}$ Write) Note (6)



Write Cycle 2 ($\overline{CE1}$ Write) Note (6)



Write Cycle 3 (CE2 Write) Note (6)



Notes : (1) In Read Cycle, $\overline{WE}$ should be high.

(2) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.

(3) A write occurs during the overlap of a low $\overline{CE1}$, a high CE2 and a low $\overline{WE}$.
A write begins at the latest transition among $\overline{CE1}$ going low, CE2 going high and $\overline{WE}$ going low.
A write ends at the earliest transition among $\overline{CE1}$ going high, CE2 going low and $\overline{WE}$ going high.
t_{WP} is measured from the beginning of write to the end of write.

(4) t_{CW1}, t_{CW2} are measured from the later of $\overline{CE1}$ going low or CE2 going high to the end of write.

(5) If one of these conditions ($\overline{OE}$ is high, $\overline{CE1}$ is high, CE2 is low, $\overline{WE}$ is low) at least is satisfied, D_{OUT} goes to high impedance state.

(6) In Write Cycle, $\overline{OE} = V_{IH}$ or V_{IL}.

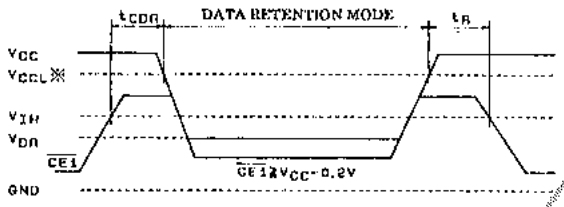
(7) D_{OUT} is in the same phase of written data of this cycle.

Data Retention Characteristics at Ta = −40 to +85°C

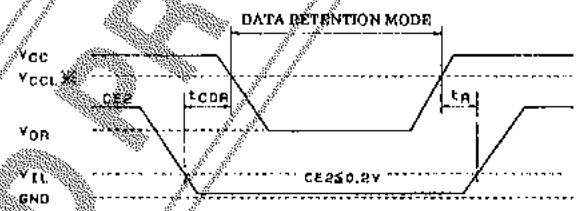
Parameter	Symbol	Conditions		min	typ	max	Unit
Date retention supply voltage	V_{DR}	$V_{CE2} \leqq 0.2V$, or $V_{\overline{CE1}} \geqq V_{CC}-0.2V$ $V_{CE2} \geqq V_{CC}-0.2V$		2.0		5.5	V
Data retention current	I_{CCDR}	V_{CC} = 3V, $V_{CE2} \leqq 0.2V$, or $V_{\overline{CE1}} \geqq V_{CC}-0.2V$ $V_{CE2} \geqq V_{CC}-0.2V$	Ta≦70°C			0.8	μA
			Ta≦85°C			2.5	
Chip enable setup time	t_{CDR}			0			ns
Chip enable hold time	t_R			t_{RC}*			ns

*) t_{RC} = Read Cycle Time

Data Retention Waveform (1) ($\overline{CE1}$ CONTROL)



Data Retention Waveform (2) (CE2 CONTROL)



*)V_{CCL} — 5V operation : 4.5V
3V operation : 2.7V