Ordering number: EN 1437E

SANYO No.1437E

LC3100

C MOS LSI

128K-BIT CMOS MASK ROM

The LC3100 is a 128k-bit CMOS mask ROM that contains an interface connectable direct to the speech synthesizer LSI LC8100. With one piece of this mask ROM, approximately 100 seconds of speech synthesis can be attained. A selection of 8-bit, 4-bit, or single-bit output data is allowed by means of external control. This mask ROM is also suited for use in applications other than speech synthesis.

Features

• ROM capacity	128k bits
• Access time	6.9μsec typ (for operation at 800kHz typ.) 26.0μsec typ (for operation at 200kHz typ.)
• Cycle time	8.1μsec typ (for operation at 800kHz typ.) 30.6μsec typ (for operation at 200kHz typ.)
• Function	(1) Contains an interface to the LC8100 (speech synthesizer LSI). (2) Possible to select the bit length of output data. 8-bit data 4-bit data Single-bit data
• Low power dissipation	CMOS
• Current dissipation	2mA max. (at operating mode) 1μA max. (at nonoperating mode)
• Single +5V power supply	+4.5 to 6.5 V (supply voltage range)
• Package	DIP24, QIP64A, QIP64B, MFP28

Specifications and information herein are subject to change without notice.

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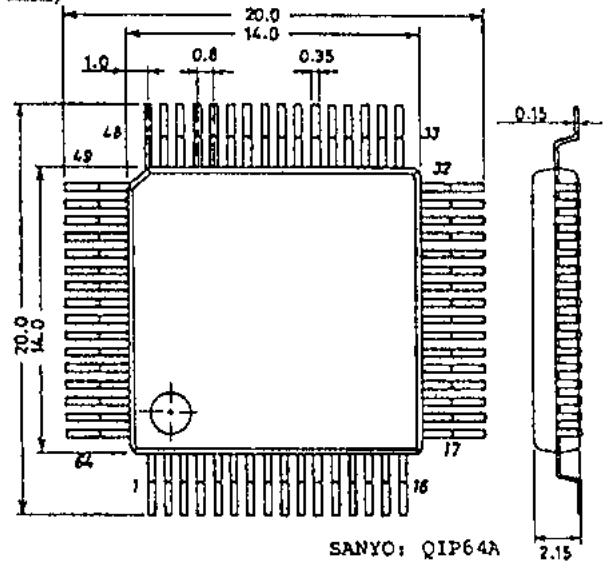
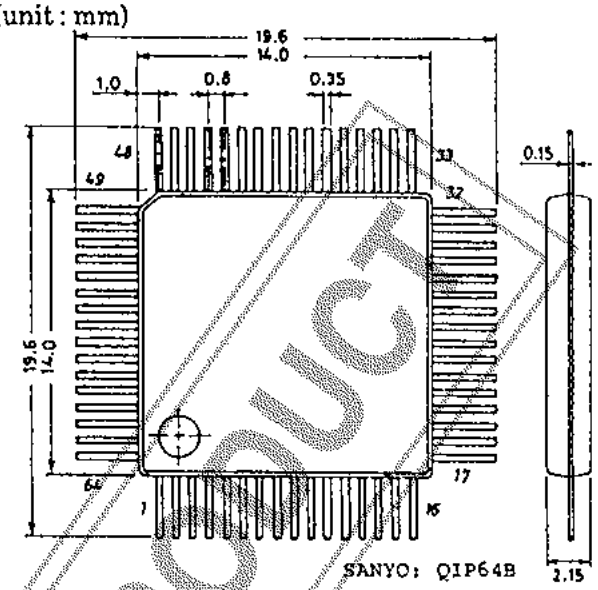
Package Dimensions 3057

(unit : mm)



Package Dimensions 3026B

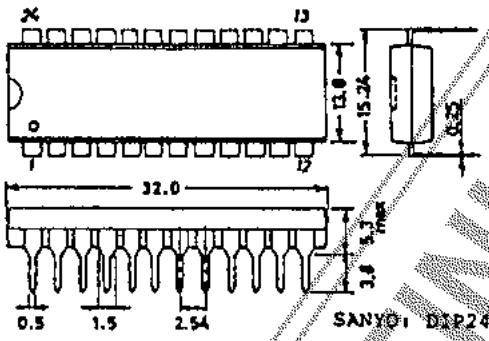
(unit : mm)



Note) When mounting the QIP and MFP package on the board, do not dip it in solder.

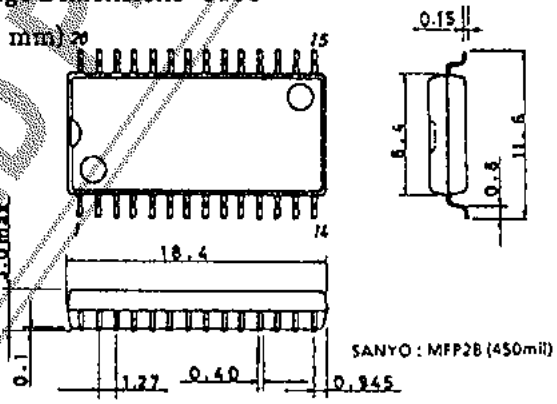
Package Dimensions 3011A

(unit : mm)

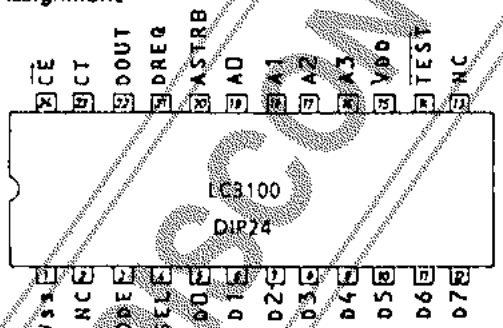


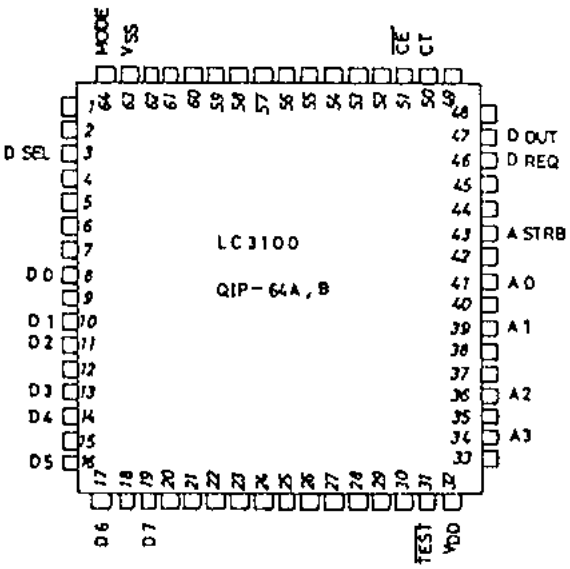
Package Dimensions 3158

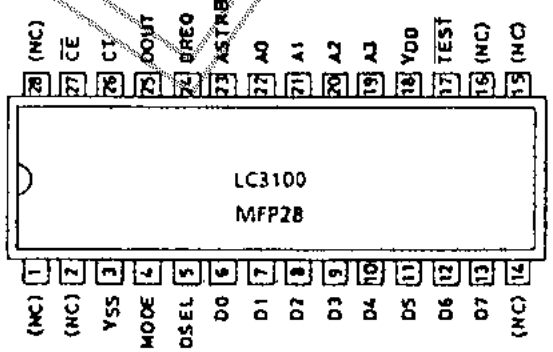
(unit : mm)



Pin Assignment

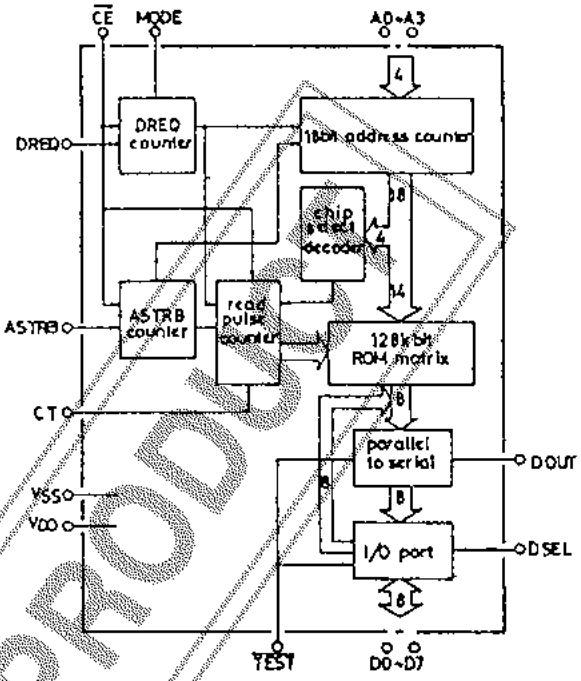






Equivalent Circuit Block Diagram

A0 to A3:	18-bit address setting pins
ASTRB:	A0 to A3 strobe pin
DREQ:	ROM data request pin
DOUT:	ROM data serial output pin
CT:	Basic operation clock input pin
D0 to D7:	8-bit input/output pins
MODE:	DREQ pin input pulse count control pin
DSEL:	Output bit length select pin
$\overline{CE}$:	Power-down control pin
$\overline{TEST}$:	Test pin
V_{DD},V_{SS}:	Power supply pin



Description of Operation of Internal Block

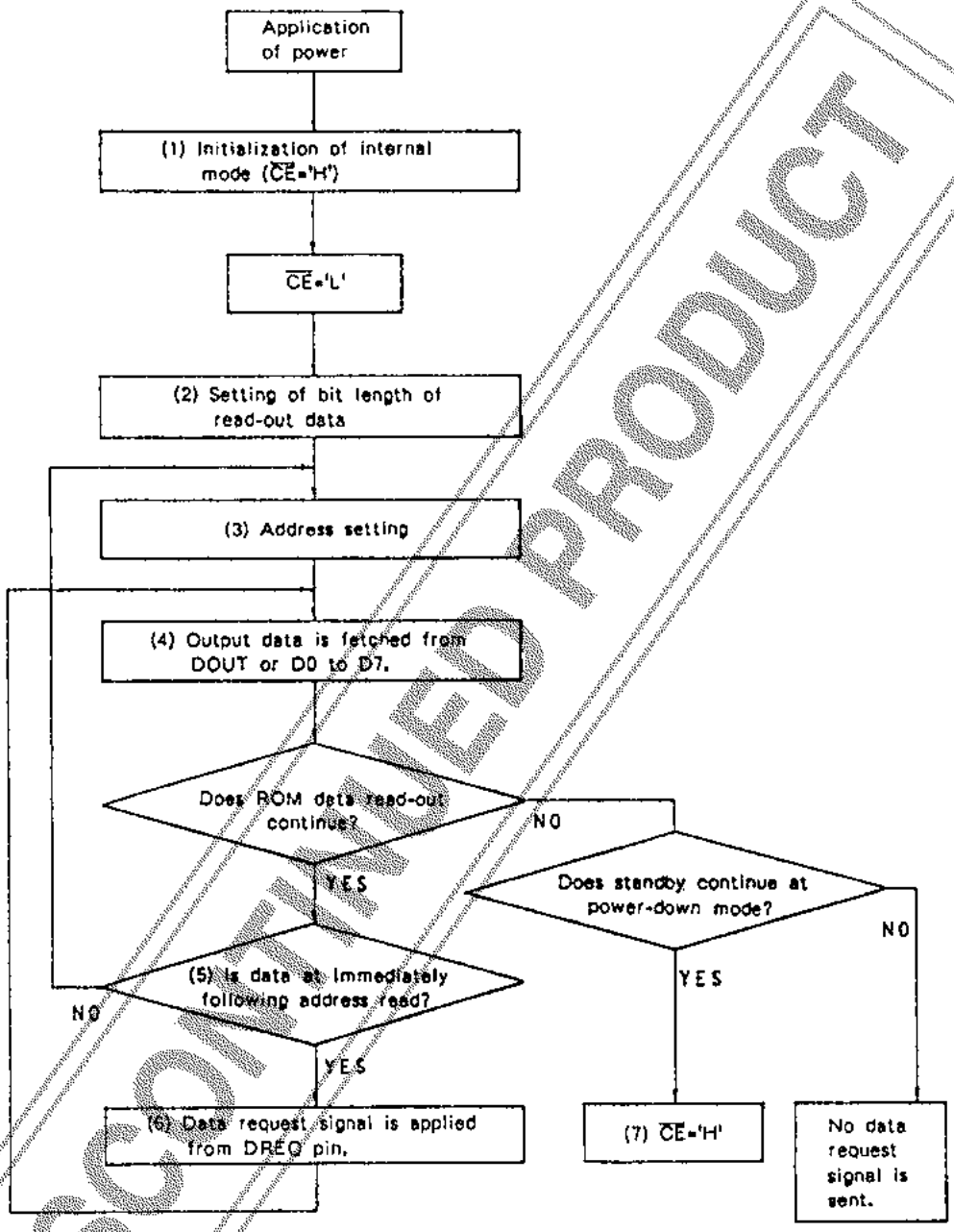
- ASTRB COUNTER: Block which internally sets address information applied in 5 steps from A0 to A3 pins.
- 18-bit ADDRESS COUNTER: Address counter organized with 18 bits.
- READ PULSE COUNTER: Block which generates signal to operate address decoder, data selector.
- CHIP SELECT DECODER: Makes chip select signal with 2^{14} to 2^{17} bits of 18-bit address.
- 128k-bit ROM MATRIX: ROM matrix cell organized with 128k bits.
- PARALLEL TO SERIAL: Shift register which serially outputs 8-bit parallel data to DOUT pin.
- I/O PORT: Selects input/output at D0 to D7 pins.

Pin Description

Pin No. QIP64	Pin No. DIP28	Pin Name	Input/Output	Function
43	20	ASTRB	Input	Pin for inputting strobe signal which causes data A0 to A3 to be latched at address setting mode.
46	21	DREQ	Input	ROM data request signal input pin.
47	22	DOUT	Output	Pin for outputting ROM data serially. When used in conjunction with the LC8100, this pin is connected to DIN pin of the LC8100.
50	23	CT	Input	Pin for inputting basic operation clock of ROM system. When used in conjunction with the LC8100, this pin is connected to CT pin of the LC8100.
51	24	$\overline{CE}$	Input	Pin for controlling initialization of LSI system immediately after application of power and internal operation stop (power-down). For performing synthesization or ROM data read-out, set $\overline{CE}$ to 'L'.
63	1	VSS	—	Connected to 0V of power supply.
32	15	VDD	—	Connected to +side of power supply.
64	3	MODE	Input	Pin for controlling number of input pulses at DREQ pin. When ROM data read-out is performed serially in bit units, set MODE to 'L'. When ROM data read-out is performed in units of 8 bits or 4 bits, set MODE to 'H'.
3	4	DSEL	Input	Used when ROM data read-out is performed in units of 4 bits. When DSEL is set to 'H', 2 to 2 bits are output to D0 to D3 pins.
8	5	D0	Input/output	Pins for outputting ROM data in units of 8 bits and inputting data in units of 8 bits.
10	6	D1		
11	7	D2		
13	8	D3		
14	9	D4		
16	10	D5		
17	11	D6		
19	12	D7		
31	14	$\overline{TEST}$	Input	LSI test pin. Open or connected to VDD.
34	16	A3	Input	Pins for setting 18-bit address. At address setting mode, address information is input by 4 bits from high-order bit downward in 5 steps.
36	17	A2		
39	18	A1		
41	19	A0		

ROM Data Read-out Procedure

The following flowchart shows the outline of read-out procedure. (1) to (7) give a more detailed description.



(1) Initialization of internal mode

There are 4 counter blocks (ASTRB counter, 18-bit ADDRESS counter, READ PULSE counter, DREQ counter) inside the LC3100. Since initialization is required immediately after application of power, apply one 'H' level pulse to $\overline{CE}$ pin. When $\overline{CE}$ is set to 'L' level, the power-down mode is released (refer to (6)) and it is possible to start read-out any time.

(2) Setting of bit length of read-out data

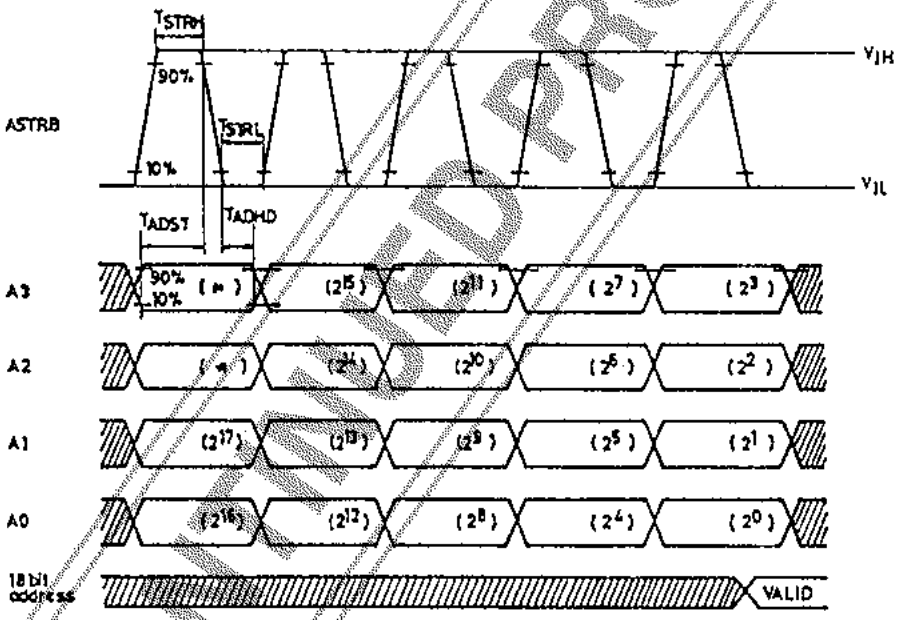
For the bit length of ROM data output, a selection of 3 lengths is allowed: 8 bits, 4 bits, and a single bit. For controlling this selection, MODE, DSEL pins are used. The following Table shows 3 types of pin setting.

DSEL \ MODE	L	H
L	Single-bit length (speech synthesis)	8-bit or 4-bit length or 4-bit length (Note)
H		4-bit length (Note)

(Note) When DSEL is set to 'L', 2^0 to 2^3 bits are output at D0 to D3 pins.
When DSEL is set to 'H', 2^4 to 2^7 bits are output at D0 to D3 pins.

(3) Address setting

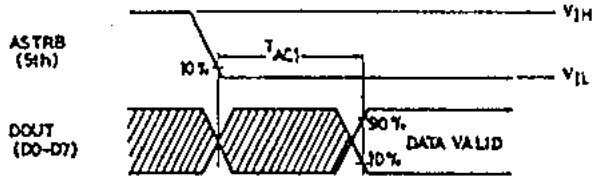
Apply 5 successive pulses to ASTRB pin. Synchronously with these pulses apply 18-bit address information to A0 to A3 pins from high-order bit downward by 4 bits in 5 steps. At this address setting mode DREQ pin must be set to 'L' level. Shown below is the timing.



(Note) - "*"=don't care.
- "2n"=Binary number at the nth bit to be set in address counter.
- For the numeric values of TSTRH, TSTRL, TADST, TADHS, refer to Electrical Characteristics.

Start of read-out of set address data

Read-out of ROM data starts at the falling of the 5th ASTRB pulse or the first (MODE='H') or the 8th (MODE='L') DREQ pulse, and when access time TAC1 has elapsed 2^0 bit is output at DOUT pin and 2^0 to 2^7 data are output at D0 to D7 pins. (Refer to the following Timing Chart.)
Note) For the numeric value of TAC1, refer to Electrical Characteristics.

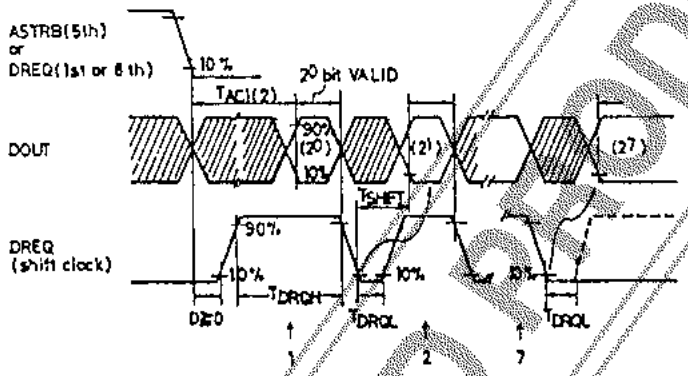


(4) Fetching of output data

As shown above, whenever access time T_{AC1} has elapsed, data can be fetched from output ports DOUT or D0 to D7 pins. (Pin setting as shown in Table in (2) is required.)

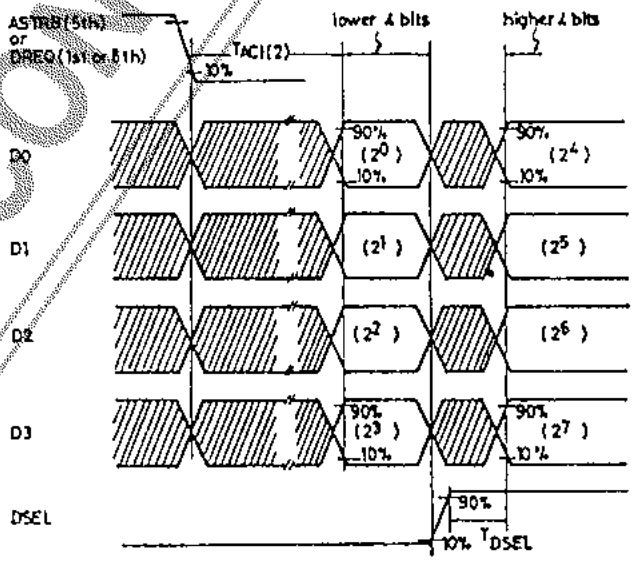
Counting one byte in bit units from DOUT pin

Count a single bit (2^n bit) from DOUT pin. To count the following single bit (2^{n+1} bit), apply a shift clock to DREQ pin. Shown below is Timing Chart.
For the numeric values of T_{AC1}, T_{DROH}, T_{DROL}, T_{SHFT}, refer to Electrical Characteristics.



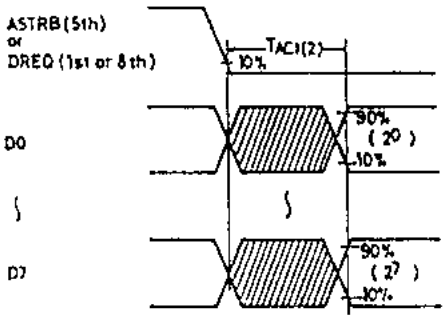
Counting one byte in units of 4 bits from D0 to D3 pins

In accordance with Table and (Note) in (2), one byte is fetched from D0 to D3 pins by 4 bits in 2 steps. Shown below is Timing Chart.



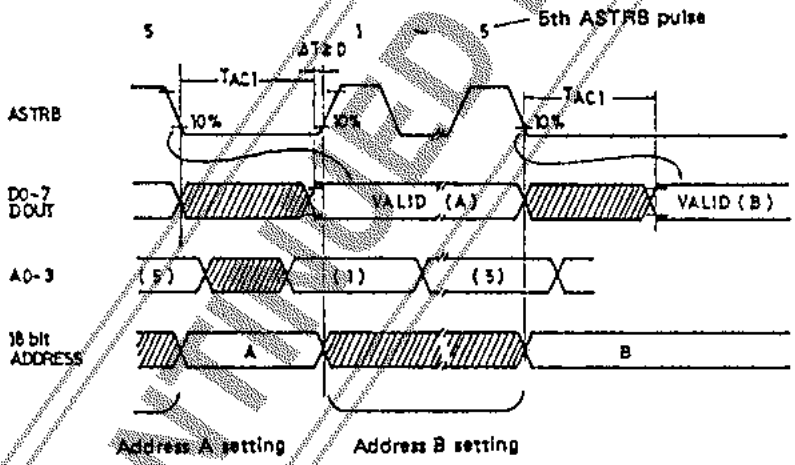
Counting one byte in units of 8 bits from D0 to D7 pins

Eight bits are fetched from D0 to D7 pins. Shown below is Timing Chart.

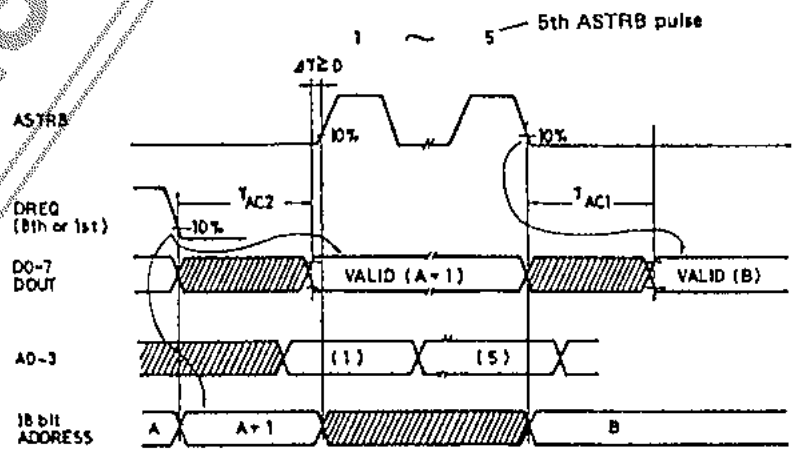


(5) Setting address again and counting data

(1) Timing for application of ASTRB pulse when address A is set and read out and then address B is set and read out.



(2) Timing for application of ASTRB pulse when data is read out by application of DREQ signal (refer to (6) below) and then address B is set and read out.

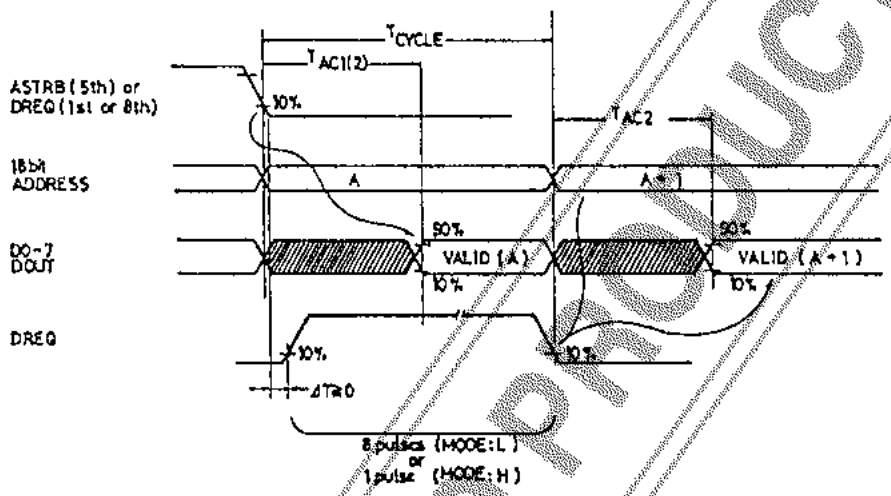


(6) Request of ROM data at the following address

When the signal shown below is applied to the LSI, the LSI begins to read out data at the address immediately following the address at which preceding data is read out.

Falling of 8th DREQ pulse (MODE='L')
Falling of 1st DREQ pulse (MODE='H')

Shown below is Timing Chart.



Note) Apply ROM data request signal after TCYCLE or more has elapsed.
For the numeric value of TCYCLE, refer to Electrical Characteristics.

(7) Power-down mode

When the input at $\overline{CE}$ pin is set to 'H' level, the LC3100 enters power-down mode (each block inside the LSI stops its operation, with no unnecessary current dissipated.). At this mode, the LSI system becomes as follows and current dissipation is reduced.

(1) Input at input ports (ASTRB, DREQ, A0 to A3) is inhibited.
(It should be noted that if input is floating, current dissipation increases.)
(2) Both address decoder and data selector in 128k-bit ROM matrix stop their internal operation.
(3) Output at 3-state output pins DOUT, D0 to D7 is floating or fixed. (The user can select either of the two. Refer to "User mask".) When $\overline{CE}$ is set to 'H', in addition to reduction in current dissipation as mentioned above, 4 internal counters (ASTRB COUNTER, 18-BIT ADDRESS COUNTER, READ PULSE COUNTER, DREQ COUNTER) are initialized in readiness for read-out after power-down mode release ($\overline{CE}$='L').

User mask

(1) CHIP SELECT DECODER

User mask option which makes LSI chip select signal (select, nonselect) with 2^{14} to 2^{17} bits of 18-bit addresses. Shown below is the output modes including $\overline{CE}$ pin conditions.

	$\overline{CE}$='L'	$\overline{CE}$='H' (Power-down)
Chip select	Data is output from DOUT, D0 to D7 pins.	Data immediately before $\overline{CE}$='H' occurs is held and output. (Note)
Chip nonselect	Output at DOUT, D0 to D7 pins is brought to high impedance state.	Output at DOUT, D0 to D7 pins is brought to high impedance state.

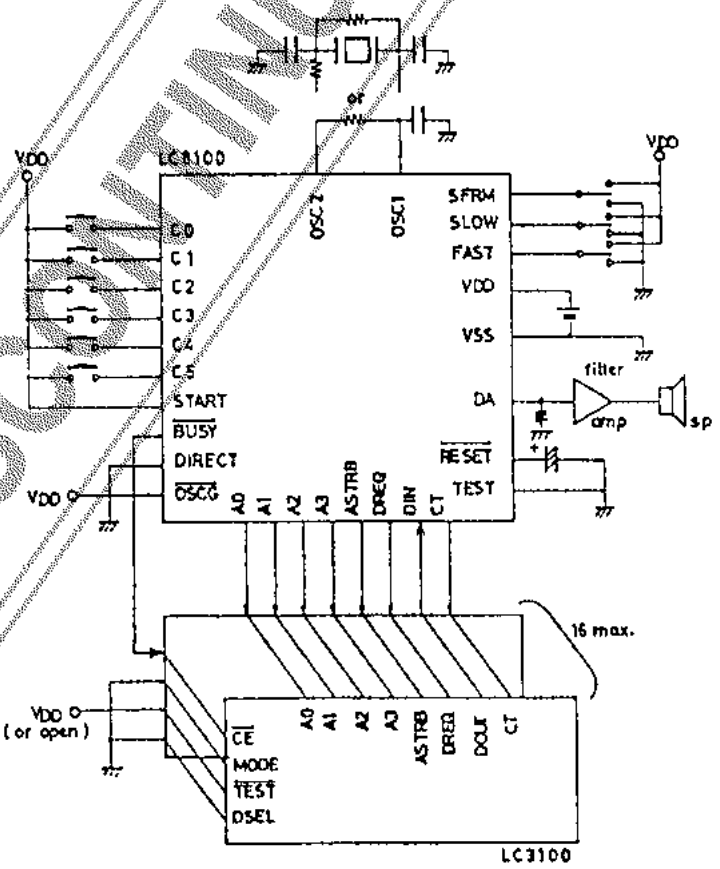
Note) In this case, the LSI only, having CHIP SELECT DECODER whose 2^{14} to 2^{17} bits are all 0, outputs data and all others are brought to high impedance state.

(2) SW mask

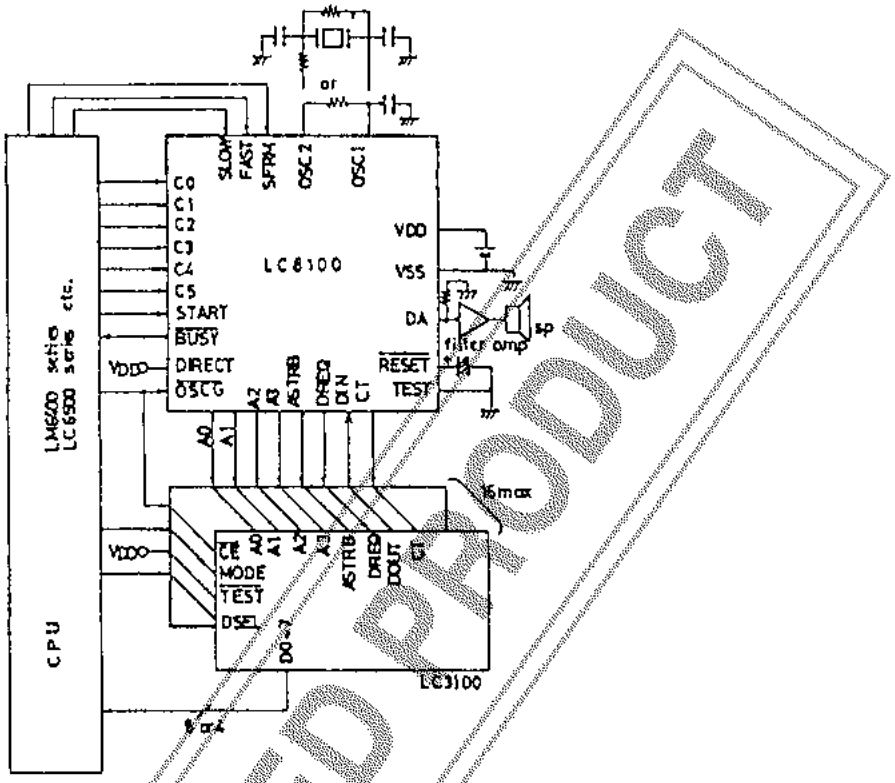
SW mask controls output at DOUT, D0 to D7 output pins in the following two ways at power-down mode. The user can select either of the two beforehand.

(i) Output at DOUT, D0 to D7 pins is brought to high impedance state.
(ii) Data immediately before power-down mode is held and output. (LSI only which has CHIP-SELECT DECODER whose 2^{14} to 2^{17} bits are all 0)

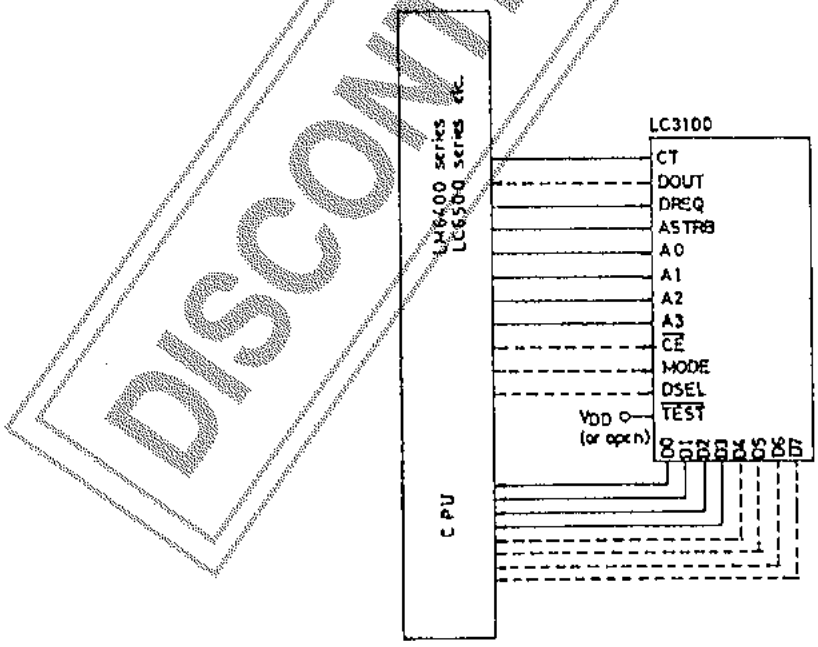
Sample Application Circuit (1) One word to one key correspondence



Sample Application Circuit (2) CPU control: Editing and synthesis with CPU



Sample Application Circuit (3) CPU control: Application other than speech synthesis



Note) Connect signals shown with dotted lines as required.

Absolute Maximum Ratings at Ta=25 °C, V_{SS}=0V

				unit
Maximum Supply Voltage	V_{DD} max	V_{DD} pin	-3.0 to +7.0	V
Input Voltage	V_{IN}	All input pins	-0.3 to V_{DD}+0.3	V
Output Voltag	V_{OUT}	All output pins	-0.3 to V_{DD}+0.3	V
Output Current	I_O	All output pins, per pin	-2.0 to +2.0	mA
Allowable Power Dissipation	Pd max	Ta=-30 to +70 °C	200	mW
Operating Temperature	Topg		-30 to +70	°C
Storage Temperature	Tstg		-55 to +125	°C

Allowable Operating Conditions at Ta=-30 to +70 °C, V_{DD}=4.5 to 6.5V, V_{SS}=0V

			min	typ	max	unit
Supply Voltage	V_{DD}	V_{DD} pin	4.5	5.0	6.5	V
Input 'H'-Level Voltage	V_{IH}	All input pins other than D0 to D7	0.7V_{DD}			V
Input 'L'-Level Voltage	V_{IL}	All input pins other than D0 to D7			0.3V_{DD}	V
Operating Clock Frequency	f_{CT}	Fig. 1, Ta=-30 to +60 °C	150	800	960	kHz
Operating Clock 'H'-Level Pulse Width	$t_{wøH}$	Fig. 1	0.3			µs
Operating Clock 'L'-Level Pulse Width	$t_{wøL}$	Fig. 1	0.47			µs

Electrical Characteristics at Ta=-30 to +70 °C, V_{DD}=4.5 to 6.5V, V_{SS}=0V

			min	typ	max	unit
Input 'H'-Level Current	I_{IH}	V_{IN}=V_{DD}			1.0	µA
Input 'L'-Level Current	I_{IL}	V_{IN}=V_{SS}	-1.0			µA
Output 'H'-Level Voltage	V_{OH}	I_{OH}=-0.3mA	V_{DD}-0.6			V
Output 'L'-Level Voltage	V_{OL}	I_{OL}=0.3mA			0.6	V
Output OFF Leak Current	I_{OFF1}	V_O=V_{DD}, D0 to D7, D_{OUT} pin			1.0	µA
	I_{OFF2}	V_O=V_{SS}, D0 to D7, D_{OUT} pin	-1.0			µA
Input Pin Capacitance	C_I			5	10	pF
Pull-up Resistance	Rup	TEST pin	20		1000	kΩ
Current Dissipation	$I_{DD(1)}$	At operating mode, f_{CT}=960kHz, Fig. 2			2.0	mA
	$I_{DD(2)}$	At nonoperating mode, Ta=-30 to +50 °C, Fig. 2			1.0	µA

AC Characteristics at Ta=-30 to +70 °C, V_{DD}=4.5 to 6.5V, V_{SS}=0V, R_L=200kΩ, Cp=50pF

			min	typ	max	unit
Address Setup Time	T_{ADST}	Fig. 3	0.3			µs
Address Hold Time	T_{ADHD}	Fig. 3	0.3			µs
ASTRB 'H'-Level Pulse Width	T_{STRH}		0.3			µs
ASTRB 'L'-Level Pulse Width	T_{STRL}		0.3			µs
DREQ 'H'-Level Pulse Width	T_{DRQH}		0.3			µs
DREQ 'L'-Level Pulse Width	T_{DRQL}		0.3			µs
ASTRB Pulse Duration	T_{ASTRB}	Fig. 3	1.5			µs
DREQ Pulse Duration	T_{DREQ}	Fig. 4	1.5			µs
ROM Data Access Time (1)	T_{AC1}	f_{CT}=200kHz typ.,Fig.5,Note 1	26.0			µs
ROM Data Access Time (2)	T_{AC2}	f_{CT}=200kHz typ.,Fig.5,Note 1	26.0			µs
DREQ TO DOUT Delay Time	T_{SHFT}	Fig. 6	0.6			µs
DSEL TO D0-3 Delay Time	T_{DSEL}	Fig. 7	0.3			µs
Cycle Time	T_{CYCLE}	f_{CT}=200kHz typ.,Fig.8,Note 1	30.6			µs

Fig. 1 Input Waveform at CT Pin

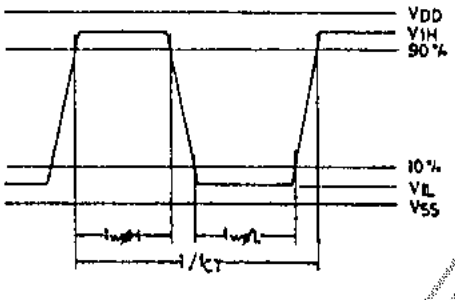


Fig. 2

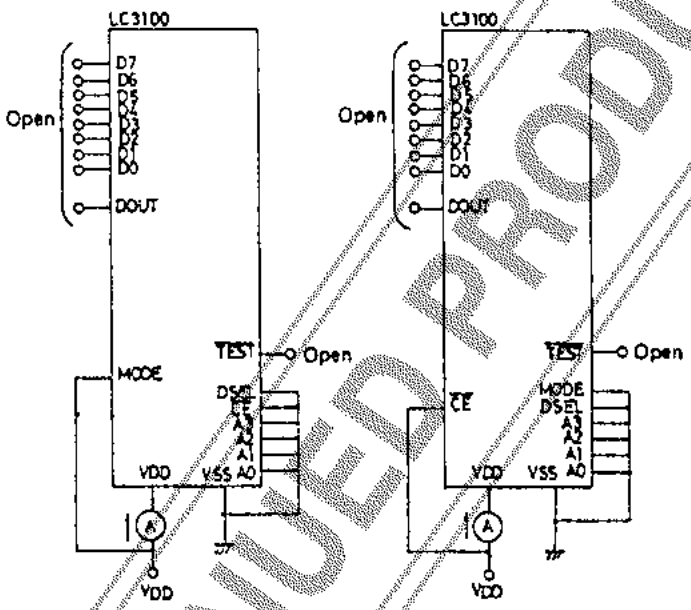


Fig. 3

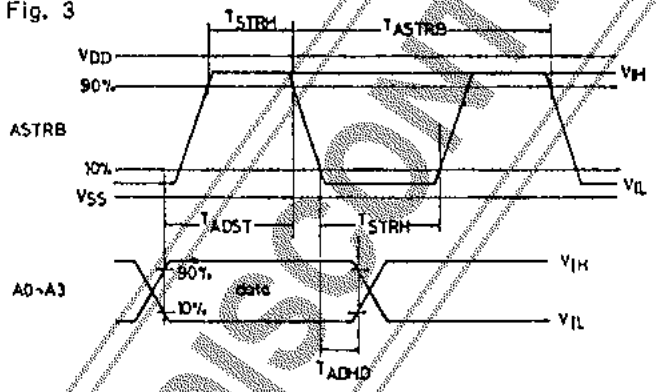


Fig. 4

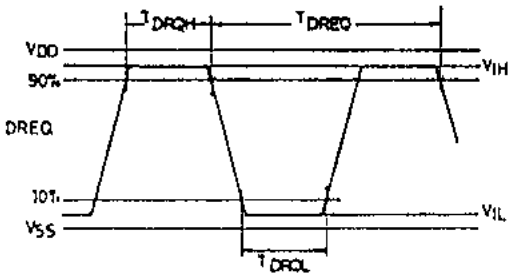


Fig. 5

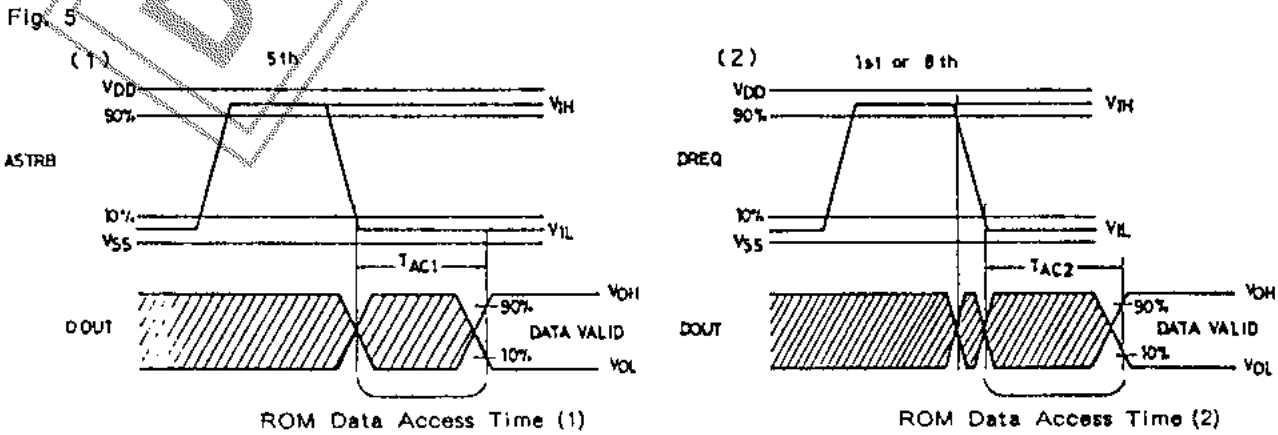


Fig. 6

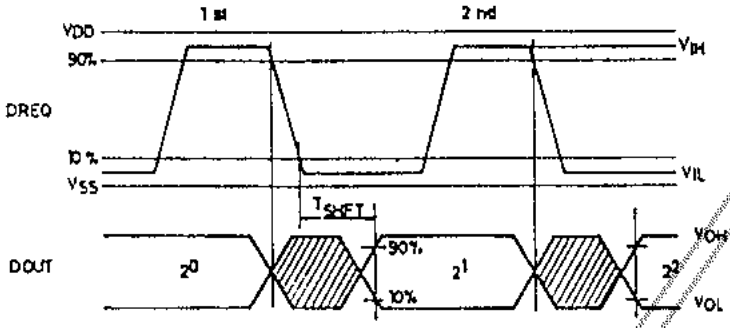


Fig. 7

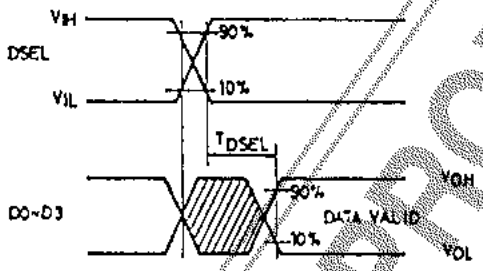
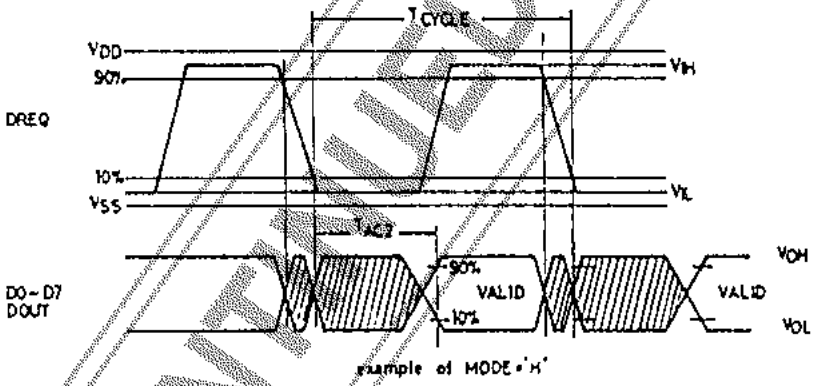


Fig. 8



Note 7 Use the following formulas to calculate T_{AC} max, Tcycle max for a given f_{CT}.

$$T_{AC}\ max = \frac{5000}{f_{CT}(kHz)} + 0.6\mu s \qquad Tcycle\ max = \frac{6000}{f_{CT}(kHz)} + 0.6\mu s$$