DATA SHEET

TDA9151B
Programmable deflection controller

Preliminary specification
Supersedes data of June 1993
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Philips Semiconductors

PHILIPS

Programmable deflection controller TDA9151B

FEATURES

General

- 6.75, 13.5 and 27 MHz clock frequency
- Few external components
- Synchronous logic
- I²C-bus controlled
- Easy interfacing
- Low power
- ESD protection
- Flash detection with restart
- Two-level sandcastle pulse.

Vertical deflection

- 16-bit precision vertical scan
- Self adaptive or programmable fixed slope mode
- DC coupled deflection to prevent picture bounce
- Programmable fixed compression to 75%
- Programmable vertical expansion in the fixed slope mode
- S-correction can be preset
- S-correction setting independent of the field frequency
- Differential output for high DC stability
- Current source outputs for high EMC immunity
- Programmable de-interlace phase.

East-West correction

- DC coupled EW correction to prevent picture bounce
- 2nd and 4th order geometry correction can be preset
- Trapezium correction
- Geometry correction settings are independent of field frequency
- Self adaptive Bult generator prevents ringing of the horizontal deflection
- Current source output for high EMC immunity.

Horizontal deflection

- Phase 2 loop with low jitter
- Internal loop filter
- Dual slicer horizontal flyback input
- Soft start by I²C-bus
- Over voltage protection/detection with selection and status bit.

EHT correction

- Input selection between aquadag or EHT bleeder
- Internal filter.

GENERAL DESCRIPTION

The TDA9151B is a programmable deflection controller contained in a 20-pin DIP package and constructed using BIMOS technology. This high performance synchronization and DC deflection processor has been especially designed for use in both digital and analog based TV receivers and monitors, and serves horizontal and vertical deflection functions for all TV standards. The TDA9151B uses a line-locked clock at 6.75, 13.5 or 27 MHz, depending on the line frequency and application, and requires only a few external components. The device can be programmed in a self-adaptive mode or in a programmable fixed slope mode. Selection of these modes and a large number of other functions is fully programmable via the I²C-bus.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9151B	20	DIP	plastic	SOT146-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.2	8.0	8.8	V
I_{CC}	supply current	f_{clk} = 6.75 MHz	–	27	–	mA
P_{tot}	total power dissipation		–	220	–	mW
T_{amb}	operating ambient temperature		−25	–	+70	°C
Inputs						
V_{14}	line-locked clock (LLC) logic level		–	TTL	–	
V_{13}	horizontal sync (H_A) logic level		–	TTL	–	
V_{12}	vertical sync (V_A) logic level		–	TTL	–	
V_5	line-locked clock select (LLCS) logic level	note 1	–	CMOS 5 V	–	
V_{18}	serial clock (SCL) logic level		–	CMOS 5 V	–	
V_{17}	serial data input (SDA) logic level		–	CMOS 5 V	–	
V_1	horizontal flyback (HFB) phase slicing level	FBL = logic 0	–	3.9	–	V
		FBL = logic 1	–	1.3	–	V
V_1	horizontal flyback (HFB) blanking slicing level		–	100	–	mV
V_3	over voltage protection (PROT) level		–	3.9	–	V
V_9	EHT flash detection level		–	1.5	–	V
Outputs						
V_{20}	horizontal output (HOUT) voltage (open drain)	I_{20} = 10 mA	–	–	0.5	V
I_{11}–$I_{10(M)}$	vertical differential ($VOUT_{A, B}$) output current (peak value)	vertical amplitude = 100%; I_8 = −120 µA; note 2	440	475	510	µA
$V_{10,11}$	vertical output voltage		0	–	3.9	V
$I_{6(M)}$	EW (EWOUT) total output current (peak value)	I_8 = −120 µA	–	–	930	µA
V_6	EW (EWOUT) output voltage		1.0	–	5.5	V
SANDCASTLE OUTPUT LEVELS (DSC)						
V_2	base voltage level		–	0.5	–	V
V_2	horizontal and vertical blanking voltage level		–	2.5	–	V
V_2	video clamping voltage level		–	4.5	–	V
HORIZONTAL OFF-CENTRE SHIFT (OFCS)						
V_{19}	output voltage	I_{19} = 2 mA	0	–	V_{CC}	V

Notes

1. Hard wired to ground or V_{CC} is highly recommended.
2. DAC values: vertical amplitude = 31; EHT = 0; SHIFT = 3; SCOR = 0.

BLOCK DIAGRAM

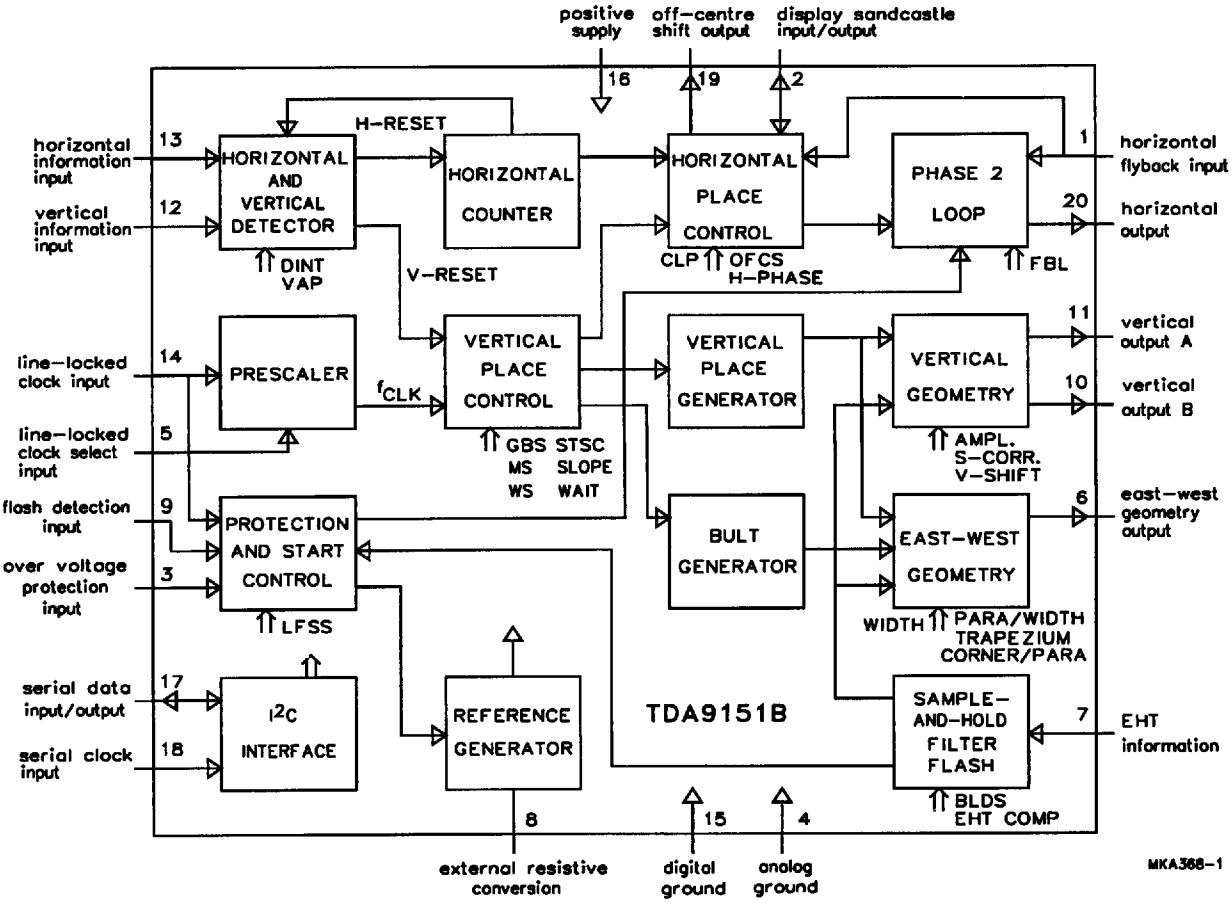


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
HFB	1	horizontal flyback input
DSC	2	display sandcastle input/output
PROT	3	over voltage protection input
AGND	4	analog ground
LLCS	5	line-locked clock selection input
EWOUT	6	east-west geometry output
EHT	7	EHT compensation
R_{CONV}	8	external resistive conversion
FLASH	9	flash detection input
$VOUT_B$	10	vertical output B
$VOUT_A$	11	vertical output A
V_A	12	vertical information input
H_A	13	horizontal information input
LLC	14	line-locked clock input
DGND	15	digital ground
V_{CC}	16	supply input (+8 V)
SDA	17	serial data input/output
SCL	18	serial clock input
OFCS	19	off-centre shift output
HOUT	20	horizontal output

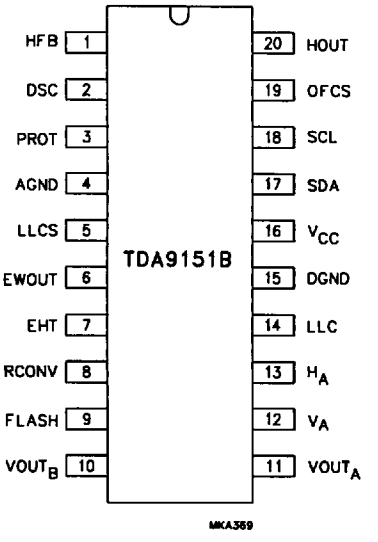


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Input signals (pins 12, 13, 14, 17 and 18)

The TDA9151B requires three signals for minimum operation (apart from the supply). These signals are the line-locked clock (LLC) and the two I²C-bus signals (SDA and SCL). Without the LLC the device will not operate because the internal synchronous logic uses the LLC as the system clock.

I²C-bus transmissions are required to enable the device to perform its required tasks. Once started the IC will use the H_A and/or V_A inputs for synchronization. If the LLC is not present the outputs will be switched off and all operations discarded (if the LLC is not present the line drive will be inhibited within 2 µs, the EW output current will drop to zero and the vertical output current will drop to 20% of the adjusted value within 100 µs). The SDA and SCL inputs meet the I²C-bus specification, the other three inputs are TTL compatible.

The LLC frequency can be divided-by-two internally by connecting LLCS (pin 5) to ground thereby enabling the prescaler.

The LLC timing is given in the Chapter "Characteristics".

I²C-bus commands

Slave address: **8C HEX = 1000110X BIN**

READ MODE

The format of the status byte is: PON PROT 0 0 0 0 0 0

Where:

PON is the status bit for power-on reset (POR) and after power failure:

- Logic 1:
  - after the first POR and after power failure; also set to 1 after a severe voltage dip that may have disturbed the various settings
  - POR 1 to 0 transition, V_{CC} = 6.25 V (typ.)
  - POR 0 to 1 transition, V_{CC} = 5.75 V (typ.)
- Logic 0:
  - after a successful read of the status byte.

PROT is the over voltage detection for the scaled EHT input:

- Logic 1:
  - if the scaled EHT rises above the reference value of 3.9 V
- Logic 0:
  - after a successful read of the status byte and EHT <3.9 V.

Remark: a read action is considered successful when an End Of Data signal has been detected (i.e. no master acknowledge).

Table 1 Write mode with auto increment; subaddress and data byte format.

FUNCTION	SUBADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Vertical amplitude	00	X[1]	X	A5	A4	A3	A2	A1	A0
Vertical S-correction	01	X	X	A5	A4	A3	A2	A1	A0
Vertical start scan	02	X	X	A5	A4	A3	A2	A1	A0
Vertical off-centre shift	03	X	note 2	note 2	note 2	X	A2	A1	A0
EW trapezium correction	03	X	A6	A5	A4	X	note 2	note 2	note 2
EW width/width ratio	04	X	X	A5	A4	A3	A2	A1	A0
EW parabola/width ratio	05	X	X	A5	A4	A3	A2	A1	A0
EW corner/parabola ratio	06	X	X	A5	A4	A3	A2	A1	A0
EHT compensation	07	X	X	A5	A4	A3	A2	A1	A0
Horizontal phase	08	X	X	A5	A4	A3	A2	A1	A0
Horizontal off-centre shift	09	X	X	A5	A4	A3	A2	A1	A0
Clamp shift	0A	X	X	X	X	X	A2	A1	A0
Control 1	0B	MS	WS	FBL	VAP	BLDS	LFSS	DINT	GBS
Vertical slope MSB	0C	A7	A6	A5	A4	A3	A2	A1	A0
Vertical slope LSB	0D	A7	A6	A5	A4	A3	A2	A1	A0
Vertical wait	0E	A7	A6	A5	A4	A3	A2	A1	A0
Control 2	0F	X	X	X	VPR	CPR	DIP	PRD	CSU

Notes

1. X = don't care.
2. Data bit used in another function.

Table 2 Control bits.

CONTROL BIT	LOGIC	FUNCTION
LFSS	0	Line stop: EW output current becomes zero and the vertical output current is reduced to 20% of the adjusted value. LFSS becomes logic 0 after a HIGH on PON.
	1	Line start enabled: the soft start mechanism is now activated.
DINT	0	De-interlace on: the V_A pulse is sampled at a position selected with control bit DIP.
	1	De-interlace off: the V_A pulse is sampled with the system clock and the detected rising edge is used as vertical reset.
BLDS	0	Aquadag selected.
	1	Bleeder selected.
GBS	0	Becomes logic 0 after power-on.
	1	Guard band 48/12 lines.
VAP	0	Positive V_A edge detection.
	1	Negative V_A edge detection.
FBL	0	Horizontal flyback slicing level = 3.9 V.
	1	Horizontal flyback slicing level = 1.3 V.
WS	0	No wait state.
	1	Programmable wait state (only in constant slope mode; MS = logic 1).
MS	0	Adaptive mode with guardband amplitude control.
	1	Constant slope mode (programmable).
CSU	0	No clamping suppression, standard mode of operation.
	1	Clamping suppression in wait, stop and protection modes (used in systems with e.g. TDA4680/81).
PRD	0	No defeat of HOUT, the over voltage information is only written in the PROT status bit.
	1	HOUT is defeated and status bit PROT is set when over voltage is detected.
DIP	0	V_A is sampled 42 clock pulses after the leading edge of H_A.
	1	V_A is sampled 258 clock pulses after the leading edge of H_A.
CPR	0	Nominal amplitude.
	1	Compression to 75% of adjusted amplitude, used for display of 16 : 9 standard pictures on 4 : 3 displays.
VPR	0	Nominal amplitude (100%) during wait, stop and clipping.
	1	Amplitude reduced to 20% during wait, stop and clipping.

Table 3 Explanation of control bits shown in Table 2.

CONTROL BITS	DESCRIPTION
LFSS	line frame start/stop
DINT	de-interlace
BLDS	bleeder mode selection
GBS	guard band selection
VAP	polarity of V_A edge detection
FBL	flyback slicing level
WS	wait state on/off
MS	mode select
CSU	clamping suppression mode
PRD	protection/detection mode
DIP	de-interlace phase
CPR	compression on/off
VPR	vertical power reduction mode

Table 4 Clock frequency control bit (pin 5; note 1).

CONTROL BIT	LOGIC	FUNCTION
LLCS	0	prescaler on: the internal clock frequency $f_{clk} = \frac{1}{2}f_{LLC}$
	1	prescaler off (default by internal pull-up resistor): the internal clock frequency $f_{clk} = f_{LLC}$

Note

1. Switching of the prescaler is only allowed when LFSS is LOW. It is highly recommended to hard wire LLCS to ground or V_{CC}. Active switching may damage the output power transistor due to the changing HOUT pulse. This may cause very high currents and large flyback pulses. The permitted combinations of LLC and the prescaler are shown in Table 5.

Table 5 Line duration with prescaler.

LLC (MHz)	ON (μs)	OFF (μs)
6.75	note 1	64
13.5	64	32
27	32	note 1

Note

1. Combination not allowed.

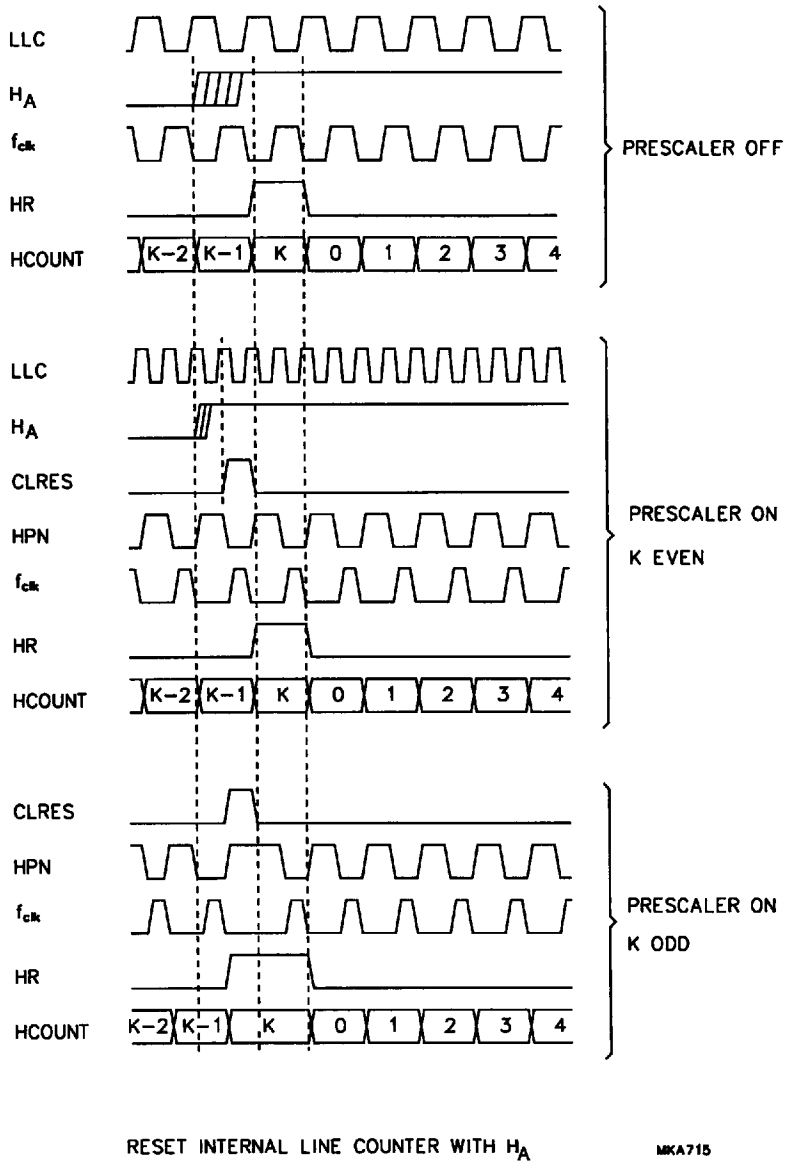


Fig.3 Timing relations between LLC, H_A and line counter.

Horizontal part (pins 1, 2, 13, 19 and 20

SYNCHRONIZATION PULSE

The H_A input (pin 13) is a TTL-compatible CMOS input. Pulses on this input have to fulfil the timing requirements as illustrated in Fig.6. For correct detection the minimum pulse width for both the HIGH and LOW periods is 2 internal clock periods.

FLYBACK INPUT PULSE

The HFB input (pin 1) is a CMOS input. The delay of the centre of the flyback pulse to the leading edge of the H_A pulse can be set via the I²C-bus with the horizontal phase byte (subaddress 08), as illustrated in Fig.7.
The resolution is 6-bit.

OUTPUT PULSE

The HOUT pulse (pin 20) is an open-drain NMOS output. The duty factor for this output is typically $^{52}/_{48}$ (conducting/non-conducting) during normal operation. A soft start causes the duty factor to increase linearly from 5 to 52% over a minimum period of 2000 lines in 2000 steps.

OFF-CENTRE SHIFT

The OFCS output (pin 19) is a push-pull CMOS output which is driven by a pulse-width modulated DAC.

By using a suitable interface, the output signal can be used for off-centre shift correction in the horizontal output stage. This correction is required for HDTV tubes with a 16 × 9 aspect ratio and is useful for high performance flat square tubes to obtain the required horizontal linearity. For applications where off-centre correction is not required, the output can be used as an auxiliary DAC. The OFCS signal is phase-locked with the line frequency. The off-centre shift can be set via the I²C-bus, subaddress 09, with a 6-bit resolution as illustrated in Fig.8.

SANDCASTLE

The DSC input/output (pin 2) acts as a sandcastle generating output and a guard sensing input. As an output it provides 2 levels (apart from the base level), one for the horizontal and vertical blanking and the other for the video clamping. As an input it acts as a current sensor during the vertical blanking interval for guard detection.

CLAMPING PULSE

The clamping pulse width is 21 internal clock periods. The shift, with respect to H_A can be varied from 35 to 49 clock periods in 7 steps via the I²C-bus, clamp shift byte subaddress 0A, as illustrated in Fig.9. It is possible to suppress the clamping pulse during wait, stop and protection modes with control bit CSU. This will avoid unwanted reset of the TDA4680/81 (only used in those circuits).

HORIZONTAL BLANKING

The start of the horizontal blanking pulse is minimum 38 and maximum 41 clock periods before the centre of the flyback pulse, depending on the f_{clk}/f_H ratio K in accordance with 41 – (432 – K).

Stop of the horizontal blanking pulse is determined by the trailing edge of the HFB pulse at the horizontal blanking slicing level crossing as illustrated in Fig.10.

VERTICAL BLANKING

The vertical blanking pulse starts two internal clock pulses after the rising edge of the V_A pulse. During this interval a small guard pulse, generated during flyback by the vertical power output stage, must be inserted. Stop vertical blanking is effected at the end of the blanking interval only when the guard pulse is present (see Section "Vertical guard").

The start scan setting determines the end of vertical blanking with a 6-bit resolution in steps of one line via the I²C-bus subaddress 02 (see Figs 11, 12 and 13).

VERTICAL GUARD

In the vertical blanking interval a small unblanking pulse is inserted. This pulse must be filled-in by a blanking pulse or guard pulse from the vertical power output stage which was generated during the flyback period. In this condition the sandcastle output acts as guard detection input and requires a minimum 800 µA input current. This current is sensed during the unblanking period. Vertical blanking is only stopped at the end of the blanking interval when the inserted pulse is present. In this way the picture tube is protected against damage in the event of missing or malfunctioning vertical deflection (see Figs 11, 12 and 13).

Vertical part (pins 6, 8, 10, 11 and 12)

SYNCHRONIZATION PULSE

The V_A input (pin 12) is a TTL-compatible CMOS input. Pulses at this input have to fulfil the timing requirements as illustrated in Fig.6. For correct detection the minimum pulse width for both the HIGH and LOW period is 2 internal clock periods. For further requirements on minimum pulse width see also Section "De-interlace".

VERTICAL PLACE GENERATOR

An overview of the various modes of operation of the vertical place generator is illustrated in Fig.13.

With control bit CPR a compress to 75% of the adjusted values is possible in all modes of operation. This control bit is used to display 16 : 9 standard pictures on 4 : 3 displays. No new adjustment of other corrections, such as corner and S-correction, is required.

With control bit VPR a reduction of the current during clipping, wait and stop modes to 20% of the nominal value can be selected, which will reduce the dissipation in the vertical drive circuits.

Vertical place generator in adaptive mode (MS = logic 0)

The vertical start-scan data (subaddress 02) determines the vertical placement in the total range of 64 × 432 clock periods in 63 steps. The maximum number of synchronized lines per scan is 910 with an equivalent field frequency of 17.2 or 34.4 Hz for f_H = 15625 or 31250 Hz respectively.

The minimum number of synchronized lines per scan is 200 with an equivalent field frequency of 78 or 156 Hz for f_H = 15 625 or 31250 Hz respectively.

If the V_A pulse is not present, the number of lines per scan will increase to 910.2. If the LLC is not present the vertical blanking will start within 2 μs.

Amplitude control is automatic, with a settling time of 1 to 2 new fields and an accuracy of either 16/12 or 48/12 lines depending on the value of the GBS bit.

Differences in the number of lines per field, as can occur in TXT or in multi-head VTR, will not affect the amplitude setting providing the differences are less than the value selected with GBS. This is called amplitude control guardband. The difference sequence and the difference sequence length are not important.

Vertical place generator in constant slope mode (MS = logic 1)

In this mode the slope can be programmed directly with a two byte value on subaddress 0C (MSB) and 0D (LSB). When the actual number of lines is greater than the programmed number of lines, the circuit will enter the stop state in which the differential vertical output current remains 100% or drops to 20% (programmable with control bit VPR). The programmed value for the slope is the required number of lines multiplied by 72. The programming limits are; minimum 200 × 72 and maximum 910 × 72.

A vertical expansion is obtained with a combination of slope data and a programmable wait status, at subaddress 0E. The wait status is selected with control bit MS and can only be activated in the constant slope mode. The wait state is an 8-bit value, programmable from 0 to 255. The actual wait state is one line longer than the programmed value. If blanking is applied during stop and wait status the differential output current will be the same with VPR selected value (20 or 100%).

DE-INTERLACE

With de-interlace on (DINT = logic 0), the V_A pulse is sampled with LLC at a position supplied by control bit DIP (de-interlace phase).

When DIP = logic 0 sampling takes place 42 clock pulses after the leading edge of H_A ($T = T_{line} \times 42/432$).

When DIP = logic 1 sampling takes place 258 clock pulses after the leading edge of H_A ($T = T_{line} \times 258/432$).

The distance between the two selectable sampling points is ($T_{line} \times (258 - 42)/432$) which is exactly half a line, thus de-interlace is possible in two directions.

The duration of the V_A pulse must, therefore, be sufficient to enable the H_A pulse to caught, in this event an active time of minimum of half a line (see Fig.14 which has an integration time of $T_{line} \times 1/4$ for the V_A pulse).

With de-interlace off, the V_A pulse is sampled with the system clock. The leading edge is detected and used as the vertical reset. Selection of the positive or negative leading edge is achieved by the control bit VAP.

VERTICAL GEOMETRY PROCESSING

The vertical geometry processing is DC-coupled and therefore independent of field frequency. The external resistive conversion (R_{CONV}) at pin 8 sets the reference current for both the vertical and EW geometry processing. A useful range is 100 to 150 μA, the recommended value is 120 μA.

VERTICAL OUTPUTS

The vertical outputs $VOUT_A$ and $VOUT_B$ on pins 10 and 11 together form a differential current output. The vertical amplitude can be varied over the range 80 to 120% in 63 steps via the I²C-bus (subaddress 00). Vertical S-correction is also applied to these outputs and can be set from 0 to 16% by subaddress 01 with a 6-bit resolution.

The vertical off-centre shift (OFCS) shifts the vertical deflection current zero crossing with respect to the EW parabola bottom. The control range is −1.5 to +1.5% ($\pm 1/8 \times I_8$) in 7 steps set by the least significant nibble at subaddress 03.

EW GEOMETRY PROCESSING

The EW geometry processing is DC coupled and therefore independent of field frequency. R_{CONV} sets the reference current for both the vertical and EW geometry processing.

The EW output is an ESD-protected single-ended current output.

The EW width/width ratio can be set from 100 to 80% in 63 steps via subaddress 04 and the EW parabola/width ratio from 0 to 20% via subaddress 05. The EW corner/EW parabola ratio has a control range of −40 to 0% in 63 steps via subaddress 06.

The EW trapezium correction can be set from −1.5 to +1.5% in 7 steps via the most significant nibble at subaddress 03.

BULT GENERATOR

The Bult generator makes the EW waveform continuous (see Fig.21).

Protection input (pin 3)

The protection input (PROT) is a CMOS input.

The input voltage must be EHT scaled and has the following characteristics:

Two modes of protection are available with the aid of control bit PRD.

- With PRD = logic 1 the protection mode is selected, HOUT will be defeated and the PROT bit in the status word is set if the input voltage is above 3.9 V. Thus the deflection stops and EW output current is zero, while the vertical output current is reduced to 20% of the adjusted value. A new start of the circuit is I²C-bus controlled with the user software.
- With PRD = logic 0 the detection mode is selected, HOUT will not be defeated and the over voltage information is only written in the PROT status bit and can be read by the I²C-bus.

All further actions, such as a write of the LFSS bit, are achieved by the I²C-bus. They depend on the configuration used and are defined by user software.

Flash detection/protection input (pin 9)

The FLASH input is a CMOS input with an internal pull-up current of approximately 8 μA.

When a negative-going edge crosses the 0.75 V level a restart will be executed with a soft start of approximately 2000 lines, such as in the soft-start mode. When the function is not used pin 9 can be connected to ground, V_{CC} or left open-circuit, the internal pull-up current source will prevent any problems. However a hard wired connection to V_{CC} or ground is recommended when the function is not used.

EHT compensation (pin 7)

The EHT input is a CMOS input.

The EHT compensation input permits scan amplitude modulation should the EHT supply not be perfect. For correct tracking of the vertical and horizontal deflection the gain of the EW output stage, provided by the ratio $R_{CONV\text{-}EW}/R_{CONV}$, must be $1/16 V_{scan} \times V_{ref}$ (see Fig.15).

The input for EHT compensation can be derived from an EHT bleeder or from the picture tubes aquadag (subaddress 0B, bit BLDS).

EHT compensation can be set via subaddress 07 in 63 steps allowing a scan modulation range from −10 to +9.7%.

INTERNAL CIRCUITRY

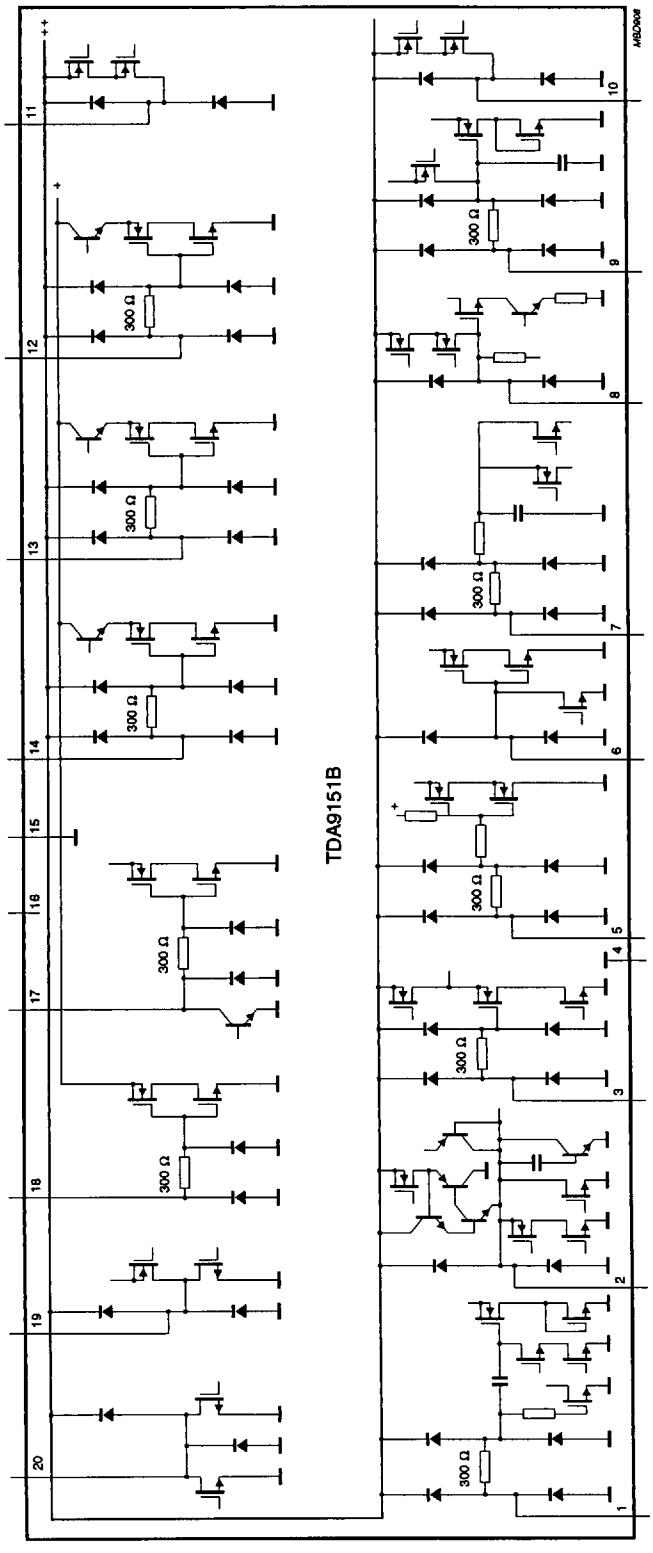


Fig.4 Internal circuitry.

APPLICATION INFORMATION

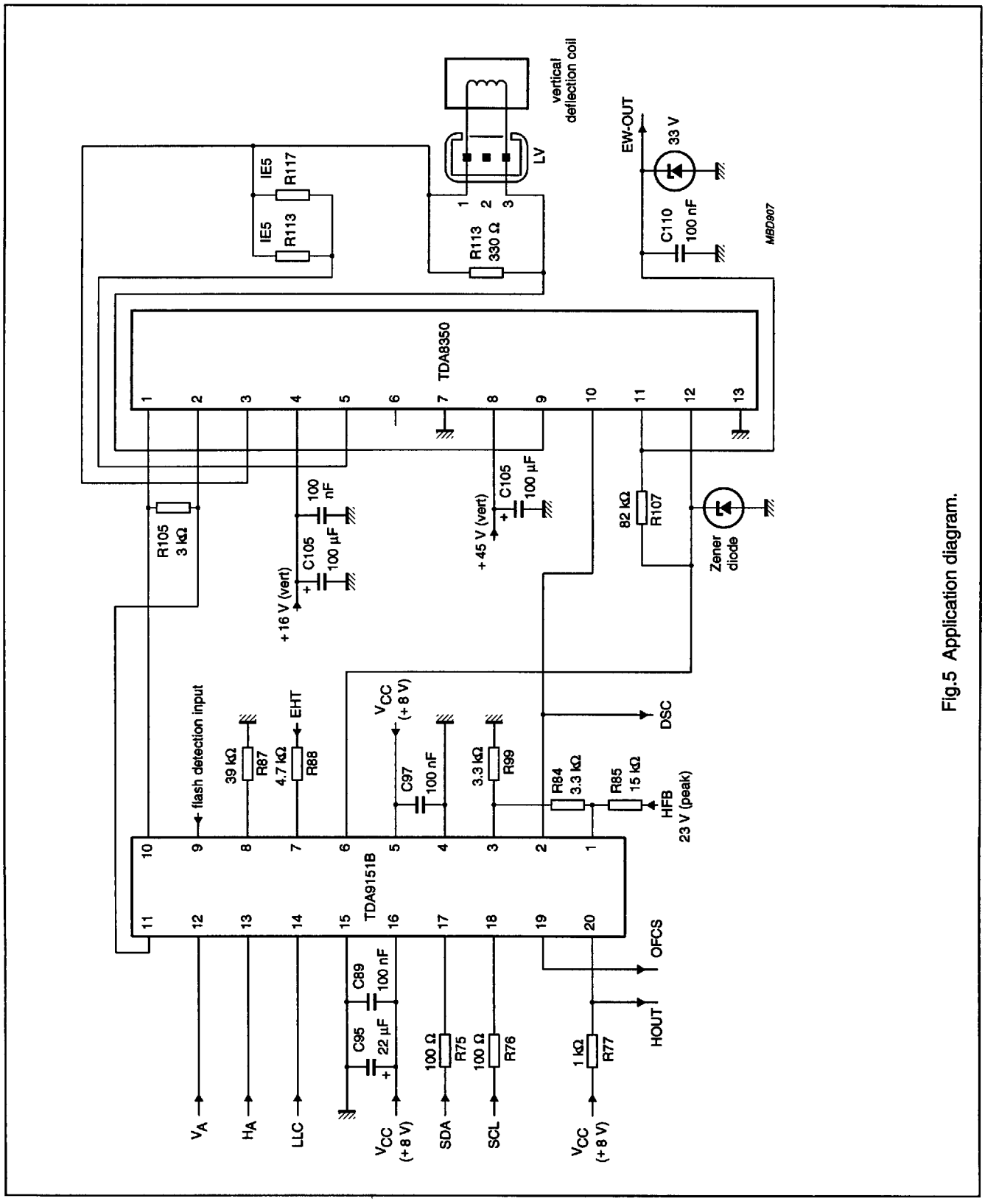


Fig.5 Application diagram.

TIMING DIAGRAMS

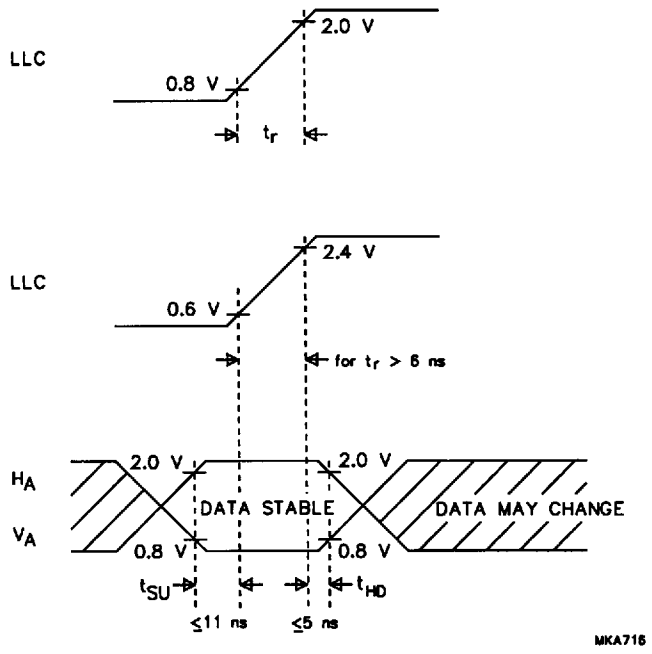


Fig.6 Timing requirements for LLC, H_A and V_A.

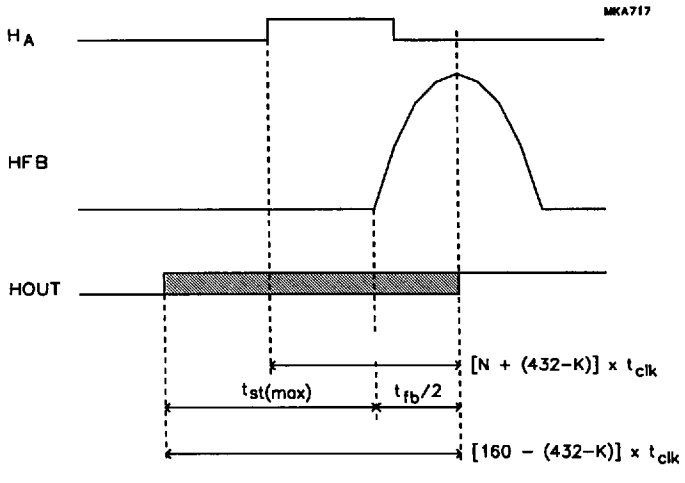


Fig.7 Horizontal phase and HOUT control range.

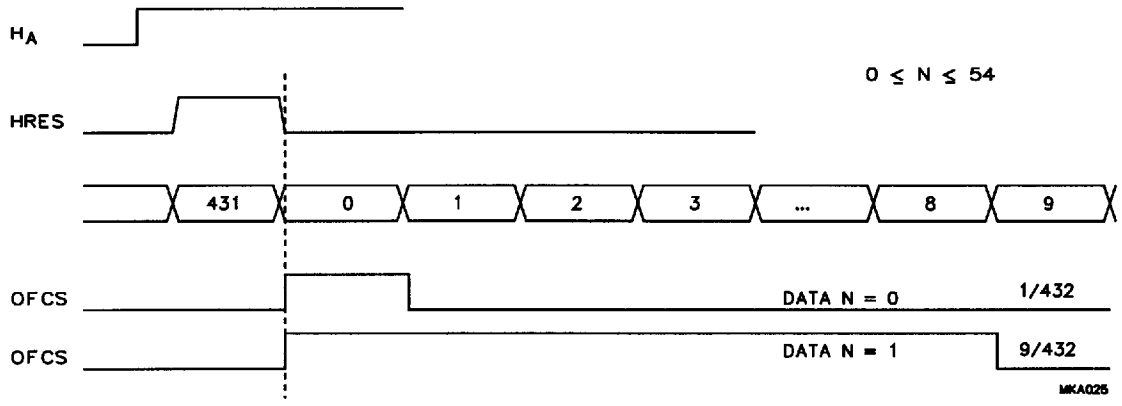


Fig.8 OFCS duty factor.

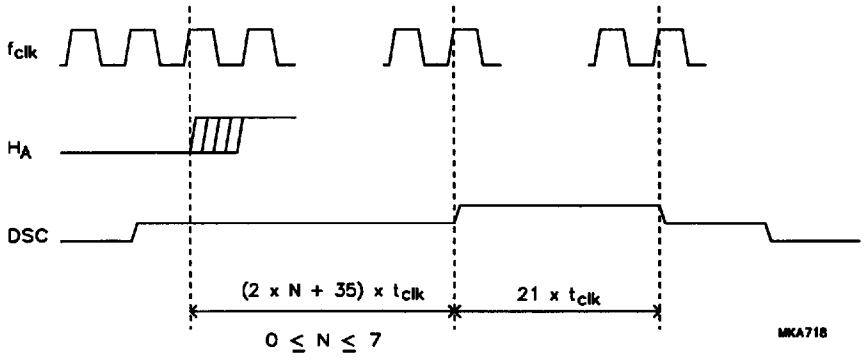


Fig.9 DSC clamping pulse.

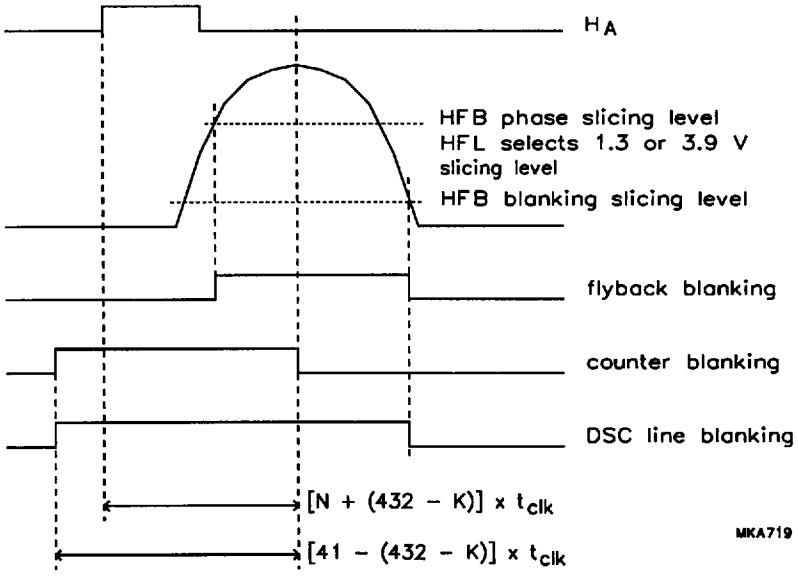


Fig.10 DSC line blanking.

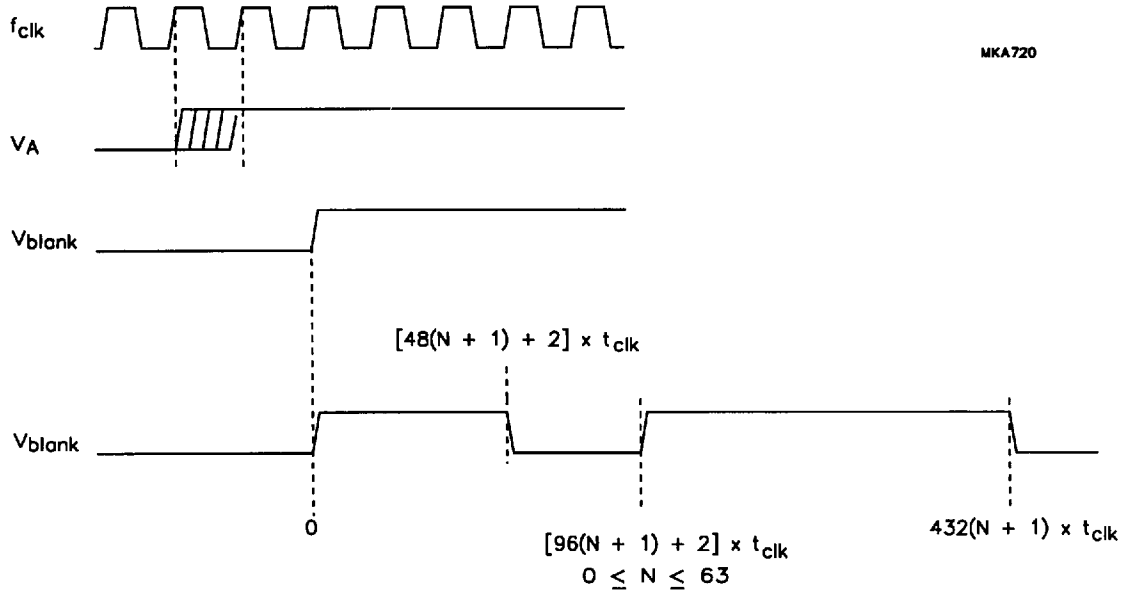
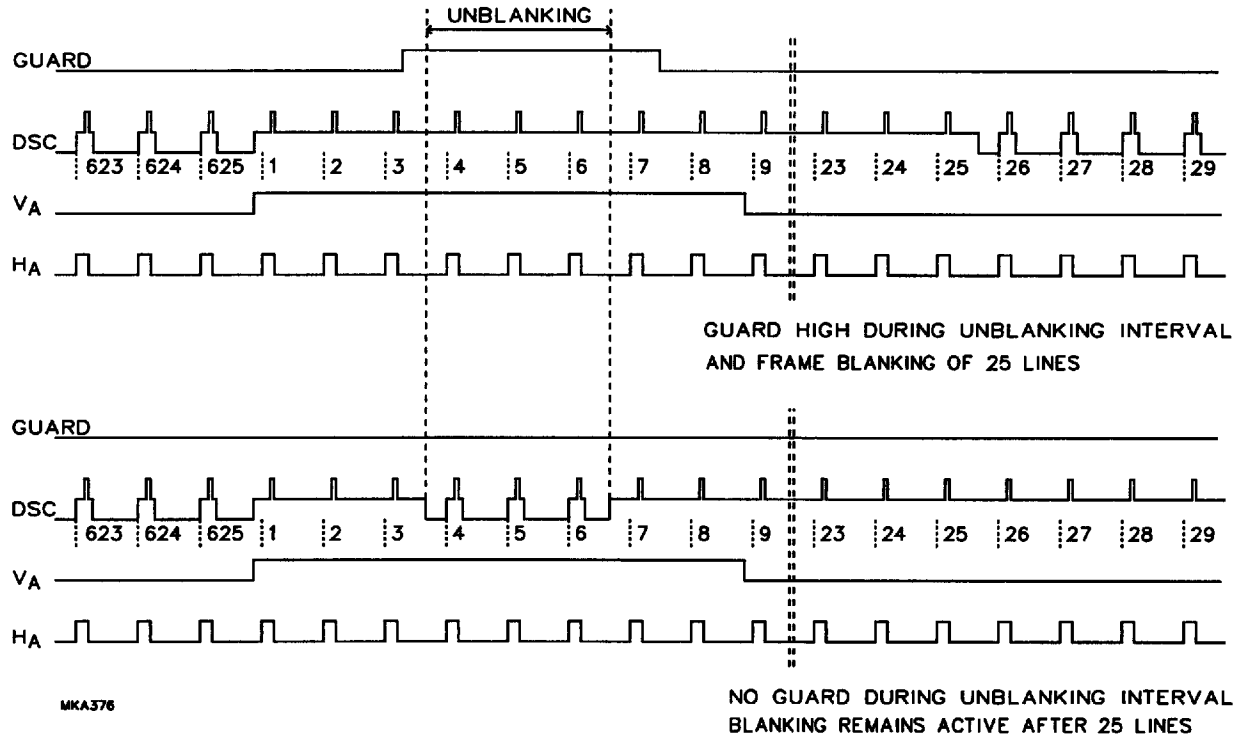


Fig.11 DCS vertical blanking with unblanking.



Vertical blanking LOW period: during scan, during unblanking.
Vertical blanking HIGH period (2.5 V): during STSC, stop and wait.
Vertical blanking continuously HIGH: POR = logic 1, LFSS = logic 0, no guard detected.

Fig.12 DSC with guard interval; start scan = 24.

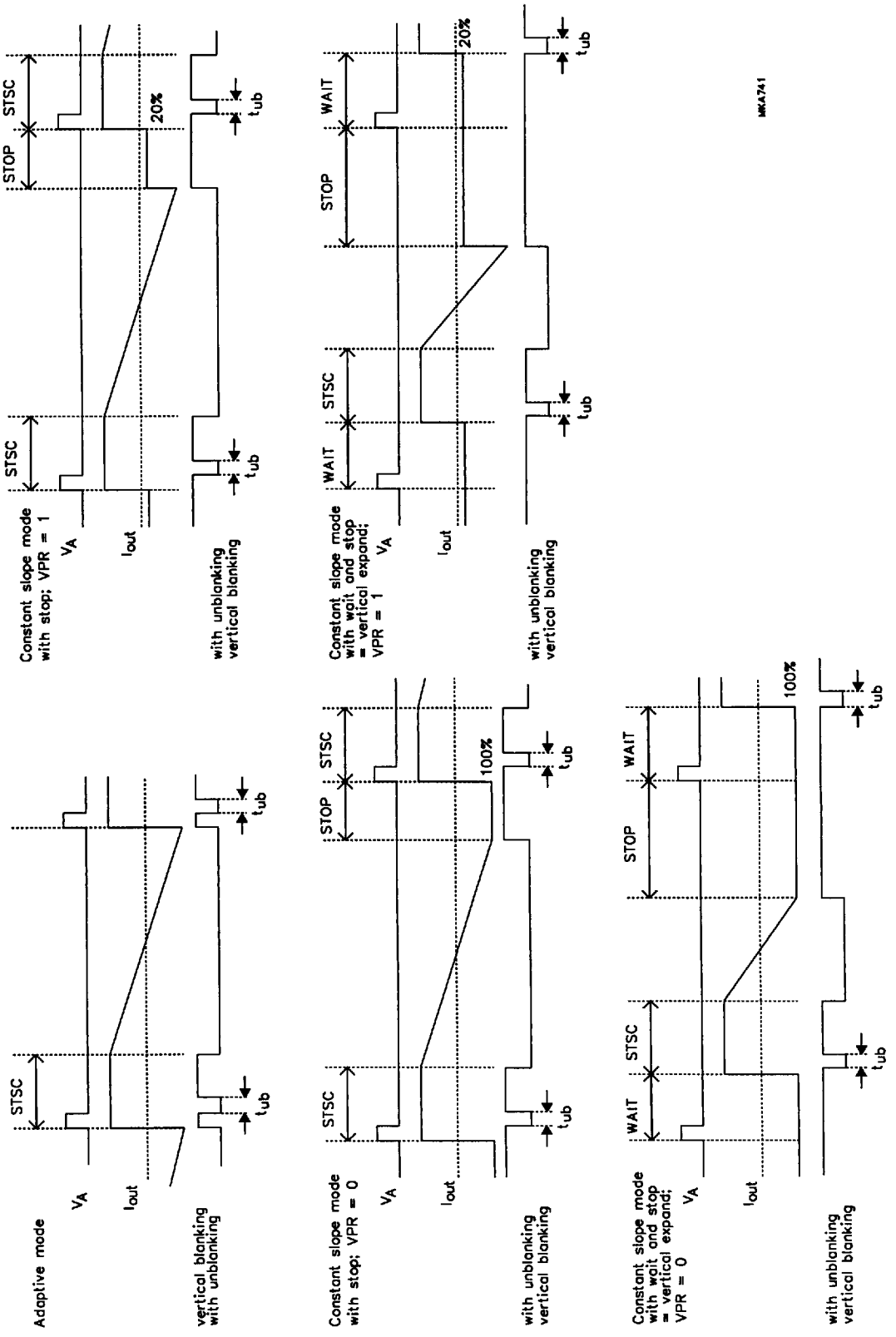
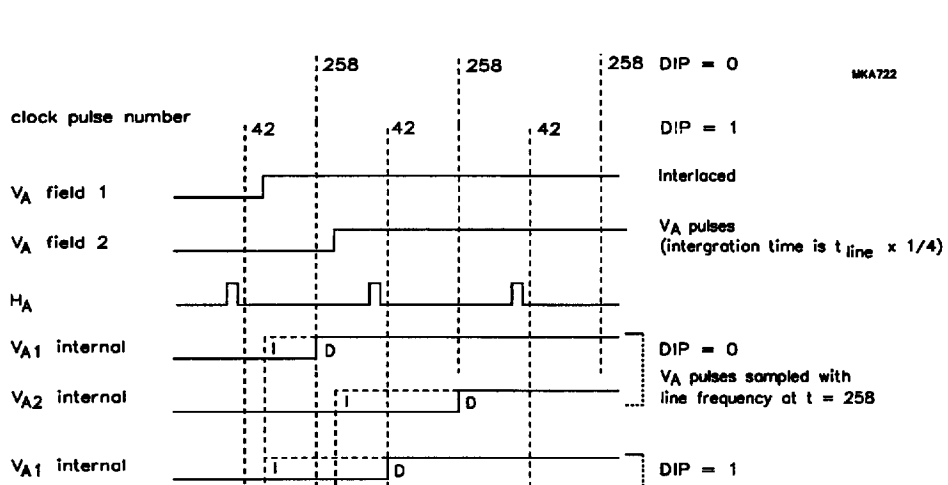


Fig.13 Vertical deflection operating modes.



I = start V_A for DINT = logic 1.
D = start V_A for DINT = logic 0.

Fig.14 De-interlace timing.

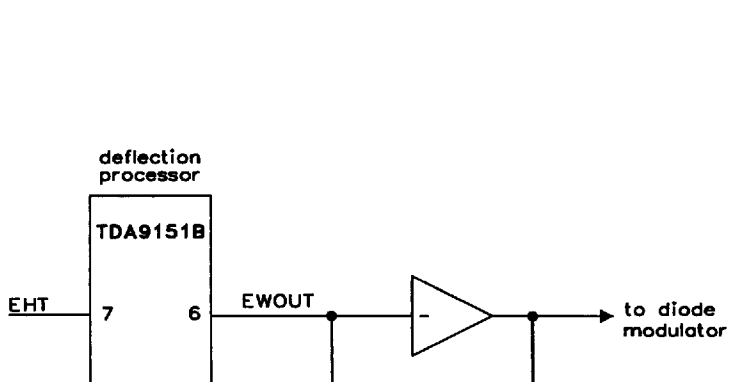


Fig.15 Explanation of $R_{CONV-EW}/R_{CONV}$ ratio.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	−0.5	8.8	V
I_{CC}	supply current	−10	+50	mA
P_{tot}	total power dissipation	−	500	mW
T_{stg}	storage temperature	−65	+150	°C
T_{amb}	operating ambient temperature	−25	+70	°C
V_{supply}	voltage supplied to pins 1 to 3, 5 to 14 and 17 to 20	−0.5	V_{CC} + 0.5	V
$I_{I/O}$	current in or out of any pin except pins 4, 15 and 16	−20	+20	mA
V_{ESD}	electrostatic handling for all pins (note 1)	−	±2000	V

Note

1. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	70	K/W

CHARACTERISTICS

V_{CC} = 8 V; T_{amb} = 25 °C; DGND = AGND = 0 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	supply voltage		7.2	8.0	8.8	V
I_{CC}	supply current	note 1; f_{clk} = 6.75 MHz	–	27	–	mA
P_{tot}	total power dissipation		–	220	–	mW
V_{por}	power-on reset	POR 1-to-0 transition	–	6.25	7.0	V
		POR 0-to-1 transition	5.0	5.75	–	V
SDA and SCL (pins 17 and 18)						
V_{17}	SDA input voltage		0	–	5.5	V
V_{IL}	LOW level input voltage (pin 17)		–	–	1.5	V
V_{IH}	HIGH level input voltage (pin 17)		3.5	–	–	V
I_{IL}	LOW level input current (pin 17)	$V_{17} = V_{SSD}$	–	–	–10	µA
I_{IH}	HIGH level input current (pin 17)	$V_{17} = V_{CC}$	–	–	10	µA
V_{OL}	LOW level output voltage (pin 17)	I_{IL} = 3 mA	–	–	0.4	V
V_{18}	SCL input voltage		0	–	5.5	V
V_{IL}	LOW level input voltage (pin 18)		–	–	1.5	V
V_{IH}	HIGH level input voltage (pin 18)		3.5	–	–	V
I_{IL}	LOW level input current (pin 18)	$V_{18} = V_{SSD}$	–	–	–10	µA
I_{IH}	HIGH level input current (pin 18)	$V_{18} = V_{CC}$	–	–	10	µA
Line-locked clock and line-locked clock select (pins 14 and 5)						
V_{IL}	LOW level input voltage (pin 14)		–	–	0.8	V
V_{IH}	HIGH level input voltage (pin 14)		2.0	–	–	V
I_{14}	input current	V_{14} = <5.5 V	–10	–	+10	µA
t_r	rise time		0	–	$\frac{1}{2}t_{LLC}$	
t_f	fall time		0	–	$\frac{1}{2}t_{LLC}$	
δ_0	duty factor	LLCS = logic 0; at 1.4 V; note 2	40	50	60	%
δ_1	duty factor	LLCS = logic 1; at 1.4 V; note 2	25	50	75	%
TIMING (PRESCALER ON; $f_{clk} = \frac{1}{2}f_{LLC}$ WHERE f_{clk} = INTERNAL CLOCK)						
f_{LLC}	line-locked clock frequency		12.4	–	29.2	MHz
K	line-locked clock frequency ratio between f_{LLC} and f_H	H locked	856	864	865	
		H unlocked	–	866	–	
	line-locked clock frequency ratio between f_{clk} and f_H	H locked	428	432	432.5	
		H unlocked	–	433	–	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TIMING (PRESCALER OFF; $f_{clk} = f_{LLC}$ WHERE f_{clk} = INTERNAL CLOCK)						
f_{LLC}	line-locked clock frequency		6.2	–	15.5	MHz
K	line-locked clock frequency ratio between f_{LLC} and f_H	H locked	428	432	432	
		H unlocked	–	433	–	
	line-locked clock frequency ratio between f_{clk} and f_H	H locked	428	432	432	
		H unlocked	–	433	–	
V_5	LLCS input voltage		0	–	8.8	V
V_{IL}	LOW level input voltage (pin 5)		–	–	1.5	V
V_{IH}	HIGH level input voltage (pin 5)		3.5	–	–	V
I_{IL}	LOW level input current (pin 5)	$V_5 = V_{SSD}$	–	–	–150	µA
I_{IH}	HIGH level input current (pin 5)	$V_5 = V_{CC}$	–	–	100	µA
Horizontal part						
INPUT SIGNALS						
H_A (pin 13)						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	–	V
I_{13}	input current	$V_{13} = 5.5$ V	–10	–	+10	µA
t_r	rise time		0	–	$\frac{1}{2}t_{LLC}$	ns
t_f	fall time		0	–	$\frac{1}{2}t_{LLC}$	ns
t_{WH}	pulse width HIGH		$2 \times t_{clk}$	–	–	
t_{WL}	pulse width LOW		$2 \times t_{clk}$	–	–	
HFB (pin 1)						
V_{PSL}	phase slicing level;	FBL = logic 0	3.7	3.9	4.1	V
		FBL = logic 1	1.1	1.3	1.5	V
V_{blank}	blanking slicing level		0	0.1	0.2	V
I_1	input current		–10	–	+10	µA
Horizontal phase (delay centre flyback pulse to leading edge of H_A; where N = horizontal phase data)						
CR	control range		0	$N \times t_{clk}$	$N + (432 - K) \times t_{clk}$	
	number of steps		–	63	–	
OUTPUT SIGNALS						
HOUT (pin 20)						
V_{20}	output voltage	$I_{20} = 0$	0	–	V_{CC}	V
V_{OL}	LOW level output voltage	$I_{20} = 10$ mA	–	–	0.5	V
I_{20}	input current	output off	–10	–	+10	µA
δ	duty factor	normal operation	51	52	53	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Soft start (duty factor controlled line drive)						
t_W	initial pulse width soft start		–	–	5	%
CR	control range		5	–	53	%
t_{ss}	soft start time		1500	–	3000	lines
Switch-off time to the centre of the flyback pulse						
CR	control range	note 3	0	–	160 – (432 – K) × t_{clk}	
Φ	control sensitivity (loop gain)		400	1000	–	µs/µs
k	correction factor	note 4	–	0.5	–	
σ	sigma value of phase jitter	note 5	–	750	–	ps
PSRR	power supply rejection ratio		–	–	10	ns/V
Horizontal off-centre shift (pin 19; N = off-centre shift data)						
V_{19}	output voltage		0	–	V_{CC}	V
V_{OL}	LOW level output voltage	I_{19} = 2 mA	–	–	0.5	V
V_{OH}	HIGH level output voltage	I_{19} = –2 mA	V_{CC} – 0.5	–	–	V
$\delta_{(max)}$	maximum duty factor	N <54	1/K	(8N+1)/K	425/K	%
δ	duty factor	N ≥54	–	1	–	%
	number of steps		–	54	–	
SANDCASTLE (PIN 2)						
DSC output voltage						
V_{clamp}	video clamping voltage		4.0	4.5	5.0	V
V_{blank}	horizontal and vertical blanking voltage level		2.0	2.5	3.0	V
V_{base}	base voltage level		0	0.5	1.0	V
I_2	output current	guard not detected	–1.0	–	+0.35	mA
		guard detected	0.8	–	2.5	mA
t_r	rise time		–	60	–	ns
t_f	fall time		–	60	–	ns
Clamping pulse (N = clamp pulse shift data)						
t_W	clamping pulse width		–	21 × t_{clk}	–	
t_{clamp}	clamp pulse shift w.r.t H_A		35	(2N + 35) × t_{clk}	49	
	number of steps		–	7	–	
t_{start}	start of horizontal blanking before middle of flyback pulse		38	41 – (432 – K) × t_{clk}	41	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vertical blanking width (N = vertical start-scan data)						
CR	control range		$1 \times 432t_{clk}$	$(N + 1) \times 432t_{clk}$	$64 \times 432t_{clk}$	
		K = 432	1	–	64	lines
	number of steps		–	63	–	
Guard detection (N = vertical start-scan data)						
t_{start}	start interval w.r.t V_A	no wait	$\{48(N+1) +2\} \times t_{clk}$	–	–	
t_{stop}	stop interval w.r.t V_A	no wait	$\{96(N+1) +2\} \times t_{clk}$	–	–	
Vertical section						
INPUT SIGNALS (PIN 12; V_A)						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	–	V
I_{12}	input current	V_{12} <5.5 V	–10	–	+10	µA
t_r	rise time		0	–	$\frac{1}{2}t_{LLC}$	ns
t_f	fall time		0	–	$\frac{1}{2}t_{LLC}$	ns
t_{WH}	pulse width HIGH		$2 \times t_{clk}$	–	–	
t_{WL}	pulse width LOW		$2 \times t_{clk}$	–	–	
t_{WH}	pulse width HIGH	de-interlace mode	$0.5 \times t_{line}$	–	–	
t_{WL}	pulse width LOW	de-interlace mode	$0.5 \times t_{line}$	–	–	
Vertical place generator in adaptive mode (N = vertical start-scan data)						
CR	control range		$1 \times 432t_{clk}$	$(N + 1) \times 432t_{clk}$	$64 \times 432t_{clk}$	
		K = 432	1	–	64	lines
	number of steps		–	63	–	
L_{max}	maximum number of synchronized lines per scan		–	910	–	lines/ scan
f_{eq}	equivalent field frequency at 910 lines/scan	f_H = 15625 Hz	–	17.2	–	Hz
		f_H = 31250 Hz	–	34.4	–	Hz
L_{min}	minimum number of synchronized lines per scan		–	200	–	lines/ scan
f_{eq}	equivalent field frequency at 200 lines/scan	f_H = 15625 Hz	–	78	–	Hz
		f_H = 31250 Hz	–	156	–	Hz
CA	amplitude control		–	automatic	–	
CA_g	amplitude control guardband	GBS = logic 0	–	16/12	–	lines
		GBS = logic 1	–	48/12	–	lines
	settling time		1	1.5	2	new fields

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vertical place generator in constant slope mode (N = vertical wait data)						
CR	control range		$1 \times 432t_{clk}$	$(N + 1) \times 432t_{clk}$	$64 \times 432t_{clk}$	
		K = 432	1	–	64	lines
	number of steps		–	255	–	
	programmable slope		200	–	910	lines/scan
	programmable slope data (number of lines × 72)	2-byte instruction;	200 × 72	–	910 × 72	lines
Vertical geometry processing						
$\Delta I_{(M)}$	vertical differential output current between $VOUT_A$ and $VOUT_B$ (peak value)	V_A = 100%; note 6; I_8 = −120 µA	440	475	510	µA
D/ΔT	drift over temperature range		–	–	10^{-4}	K^{-1}
	amplitude error due to S-correction setting		–	–	2	%
$\frac{1}{2}(I_{10}+I_{11})$	vertical output signal bias current	I_8 = −120 µA	275	325	375	µA
I_{os}	vertical output offset current	note 7	–	–	1	%
OS/ΔT	offset over temperature range		–	–	10^{-4}	K^{-1}
V_{10}	vertical output voltage (pin 10)		0	–	3.9	V
V_{11}	vertical output voltage (pin 11)		0	–	3.9	V
CMRR	common mode rejection ratio		–	–	1	%/V
LE	linearity error	adjacent blocks; note 8	–	–	2.0	%
		non-adjacent blocks; note 8	–	–	3.0	%
Vertical amplitude (N = vertical amplitude data)						
CR	control range	note 9	81	–	119	%
	number of steps		–	63	–	
Vertical S-correction (N = S-correction data)						
CR	control range	note 9	0	–	15	%
	number of steps		–	63	–	
Vertical shift						
CR	control range		$-\frac{1}{8}I_8$	–	$+\frac{1}{8}I_8$	µA
	number of steps		–	7	–	
EW output (pin 6)						
V_6	output voltage	note 10	1.0	–	5.5	V
I_6	output current	I_8 = −120 µA; note 11	15	–	930	µA
RR	output ripple rejection		–	0.15	1	%/V
D/ΔT	output drift over temperature range		–	–	5.10^{-4}	K^{-1}

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EW WIDTH/WIDTH RATIO						
CR	control range	note 9	100	–	81	%
$I_{eq(typ)}$	typical equivalent output current	V_6 = 3 V	15	–	440	µA
	number of steps		–	63	–	
EW PARABOLA/WIDTH RATIO						
CR	control range	note 9	1	–	19	%
$I_{eq(typ)}$	typical equivalent output current	width = 100%	10	–	430	µA
		width = 80%	10	–	345	µA
	number of steps		–	63	–	
EW CORNER/EW PARABOLA RATIO						
CR	control range	notes 9 and 12	40	–	0	%
$I_{eq(typ)}$	typical equivalent output current	width = 100%	0	–	200	µA
		width = 80%	0	–	160	µA
	number of steps		–	63	–	
EW TRAPEZIUM CORRECTION						
	EW trapezium/width ratio	note 9	–1.5	–	+1.5	%
	number of steps		–	7	–	
EHT input (pin 7)						
V_{ref}	reference voltage	BLDS = logic 1	–	3.9	–	V
		BLDS = logic 0	–	V_{CC}	–	V
V_I	input voltage w.r.t V_{ref}	BLDS = logic 1	–20	0	+20	%
V_I	input voltage w.r.t V_{CC}	BLDS = logic 0	0	–	$-2V_{ref}$	V
m_{scan}	scan modulation		–10	0	+9.7	%
m_{GC}	modulation gain control		0	–	1	
	number of steps		–	63	–	
I_I	input current		–100	–	+100	nA
R_{CONV} input (pin 8)						
V_O	output voltage	I_8 = –120 µA	3.7	3.9	4.1	V
I_8	current range		–100	–120	–150	µA
PROT input (pin 3)						
V_I	input voltage		0	–	V_{CC}	V
V_3	voltage detection level		3.7	3.9	4.1	V
I_I	input current		–10	–	+10	µA
FLASH detection input (pin 9)						
V_I	input voltage		0	–	V_{CC}	V
V_9	voltage detection level	falling edge	0.5	0.75	1.0	V
H	detection level hysteresis		0.3	0.5	0.8	V
I_9	detection pull-up current		–4	–8	–16	µA

Notes to the characteristics

1. For all other frequencies the expected supply current will be as shown in Table 6 (f_{clk} is the internal clock frequency, f_{LLC} is the internal clock frequency applied to pin 14).
2. When the prescaler is on, one in two LLC HIGH periods is omitted.
3. For 16 kHz operation the minimum value of the control range is 5.7 µs. With $\frac{1}{2}t_{FB}$ = 5.7 µs the minimum storage time is 0 and the maximum is 18 µs.

   For 32 kHz operation the minimum value of the control range is 0 µs. With $\frac{1}{2}t_{FB}$ = 2.85 µs the minimum storage time is 0 and the maximum is 9 µs.
4. The k factor is defined as the amount of correction of a phase step. Thus with k = 0.5 a 50% correction of the error takes place each line. The resulting step response now becomes k^n, with n the line number after the step.
5. The sigma value (σ) of the jitter with respect to LLC (H_A) at f_H = 32 kHz and a storage time of 5 µs.

   Measurement of σ is carried out during 200 lines in the active scan, the resulting peak-to-peak value is approximately 6σ. The visible jitter on the screen will be higher than the peak-to-peak jitter, depending on the deflection stage.
6. DAC values: vertical amplitude = 31; EHT = 0; SHIFT = 3; SCOR = 0.
7. Value is a percentage of $I_{10} - I_{11}$.
8. The linearity error is measured without S-correction and based on the same measurement principle as used for the screen. Measuring method: divide the output signal $I_{10} - I_{11}$ into 22 equal parts, ranging from 1 to 22 inclusive. Measure the value of two succeeding parts called one block starting with part 2 and 3 (block 1) and ending with part 20 and 21 (block 10). Thus part 1 and 22 are unused.

   Linearity error for adjacent blocks = $\frac{a_k - a_{(k+1)}}{a_{avg}}$

   Linearity error for non-adjacent blocks = $\frac{a_{max} - a_{min}}{a_{avg}}$

   Where a = amplitude, a_k = amplitude block k and a_{avg} = average amplitude.
9. Minimum available range.
10. Selection of test mode.

    When the EW output is pulled above V_{CC} – 0.5 V a special test mode is entered in which the prescaler and the clock detector are disabled.
11. DAC values: vertical amplitude = 31; EHT = 0.
12. The value of –40% (typically 46%) corresponds with data 3F (hexadecimal) and implies maximum 4th order compensation.

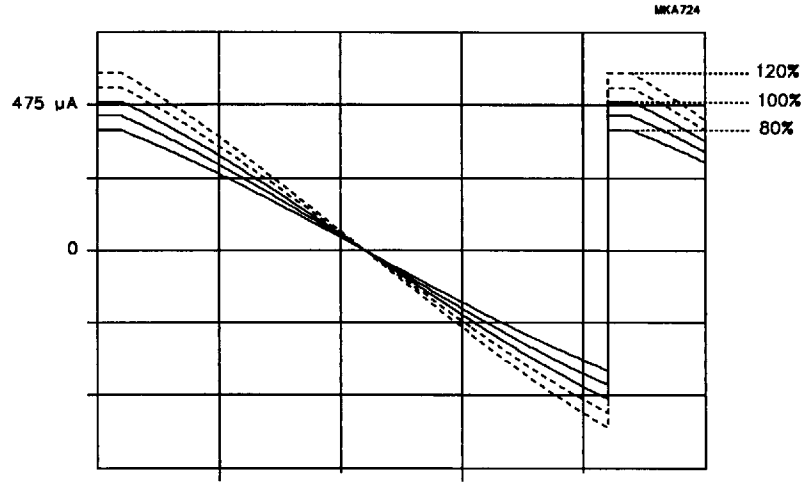
Table 6 Supply current with prescaler on/off.

LLC (MHz)	ON (mA)	OFF (mA)
6.75	note 1	27
13.5	27	38
27	42	note 1

Note

1. Combination not allowed.

TEST AND APPLICATION INFORMATION



$I_{11} - I_{10}$.

Fig.16 Control range amplitude.

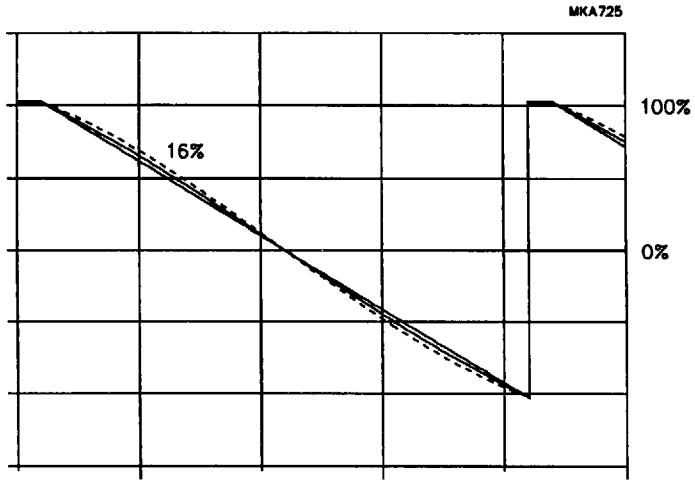


Fig.17 Control range S-correction.

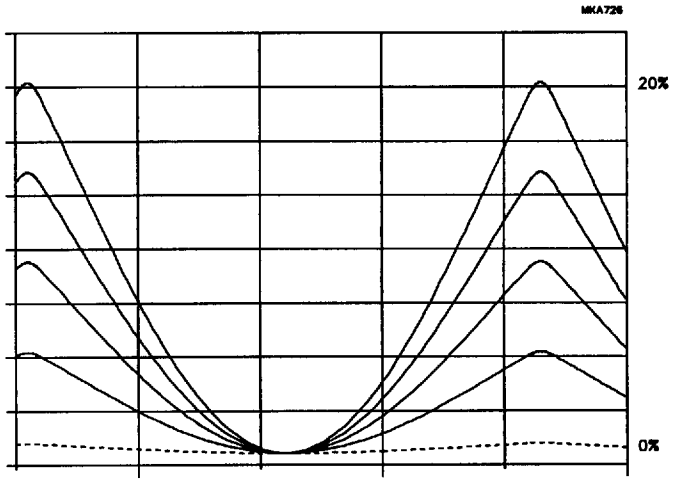


Fig.18 Control range EW parabola/width ratio.

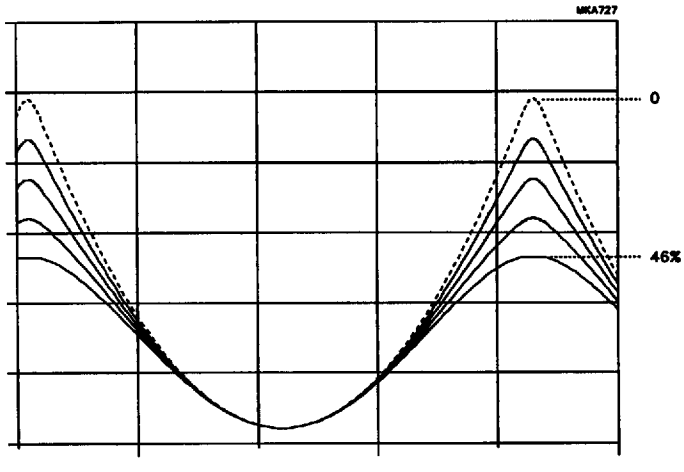


Fig.19 Control range EW corner/EW parabola ratio.

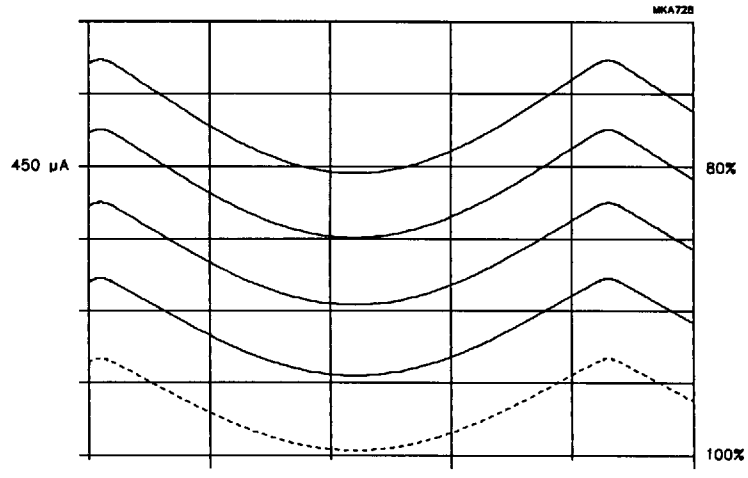


Fig.20 Control range EW width.

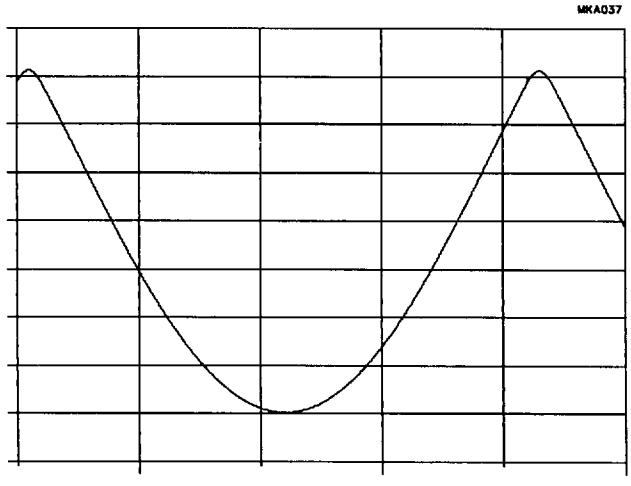
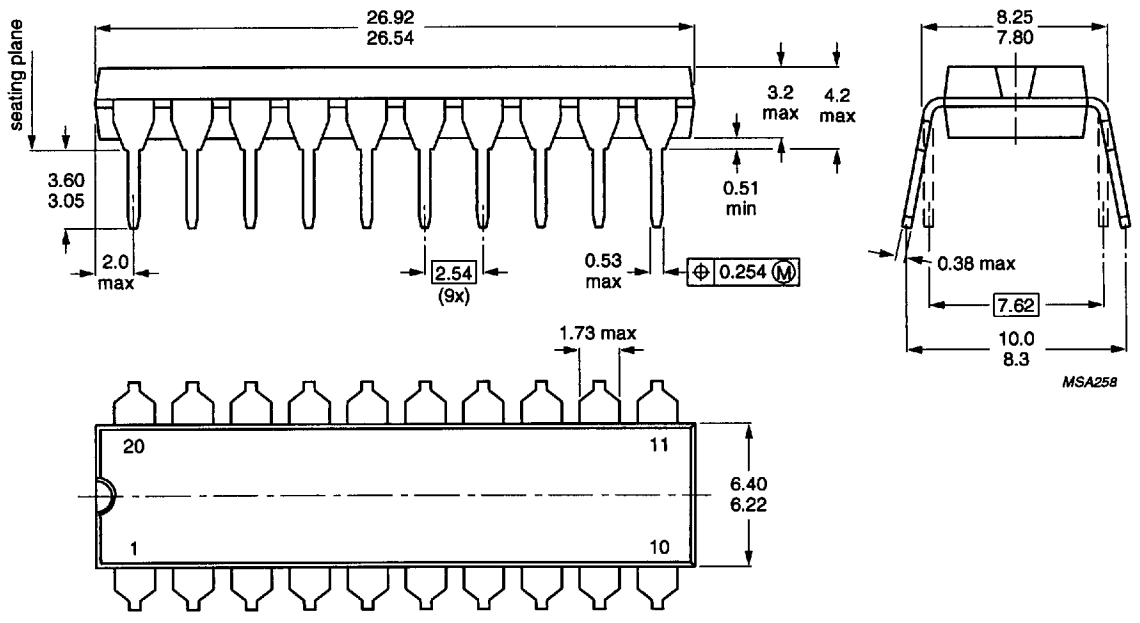


Fig.21 The BULT makes the EW waveform continuous.

PACKAGE OUTLINE



Dimensions in mm.

Fig.22 Plastic dual in-line package; 20 leads (300 mil); DIP20, SOT146-1.

SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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PURCHASE OF PHILIPS I²C COMPONENTS

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