DATA SHEET

TDA8793

8-bit, low-power, 3 V, 100 Msps Analog-to-Digital Converter (ADC)

Preliminary specification
Supersedes data of 1998 May 14
File under Integrated Circuits, IC02

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Philips
Semiconductors

PHILIPS

8-bit, low-power, 3 V, 100 Msps Analog-to-Digital Converter (ADC)

TDA8793

FEATURES

- 8-bit low-power ADC (170 mW typical)
- 2.7 to 3.6 V operation
- Sampling rate up to 100 Msps
- Track-and-hold circuit
- CMOS/TTL compatible digital inputs and outputs
- Internal references
- Adjustable full scale range possibility with external reference
- Power-down mode; 5 mW.

GENERAL DESCRIPTION

The TDA8793 is an 8-bit low-power Analog-to-Digital Converter (ADC) which includes a track-and-hold circuit and internal references. The device converts an analog input signal, up to 100 MHz, into 8-bit binary codes at a maximum sample rate of 100 Msps. All digital inputs and output are TTL/CMOS compatible. A sine wave clock input signal can also by used.

The Power-down mode enables the device power consumption to be reduced to 5 mW.

APPLICATIONS

- Radio communications
- Digital data storage read channels
- Medical imaging
- Digital instrumentation.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		2.7	3.0	3.6	V
V_{CCD}	digital supply voltage		2.7	3.0	3.6	V
V_{CCO}	output stages supply voltage		2.7	3.0	3.6	V
I_{CCA}	analog supply current	operating	32	40	48	mA
		standby	0	5	100	μA
I_{CCD}	digital supply current	operating	13	16	22	mA
		standby	0	0.65	1.1	mA
I_{CCO}	output stages supply current		–	0.1	–	mA
INL	integral non-linearity	ramp input; f_{CLK} = 2 MHz; $V_{CCA} = V_{CCD}$ = 3 V	–	±0.8	tbf	LSB
DNL	differential non-linearity	ramp input; f_{CLK} = 2 MHz; $V_{CCA} = V_{CCD}$ = 3 V	–	±0.25	tbf	LSB
$f_{CLK(max)}$	maximum clock input frequency		100	–	–	MHz
P_{tot}	total power dissipation	V_{CC} = 3 V	–	170	–	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8793HL	LQFP32	plastic low profile quad flat package; 32 leads; body 5 × 5 × 1.4 mm	SOT401-1

BLOCK DIAGRAM

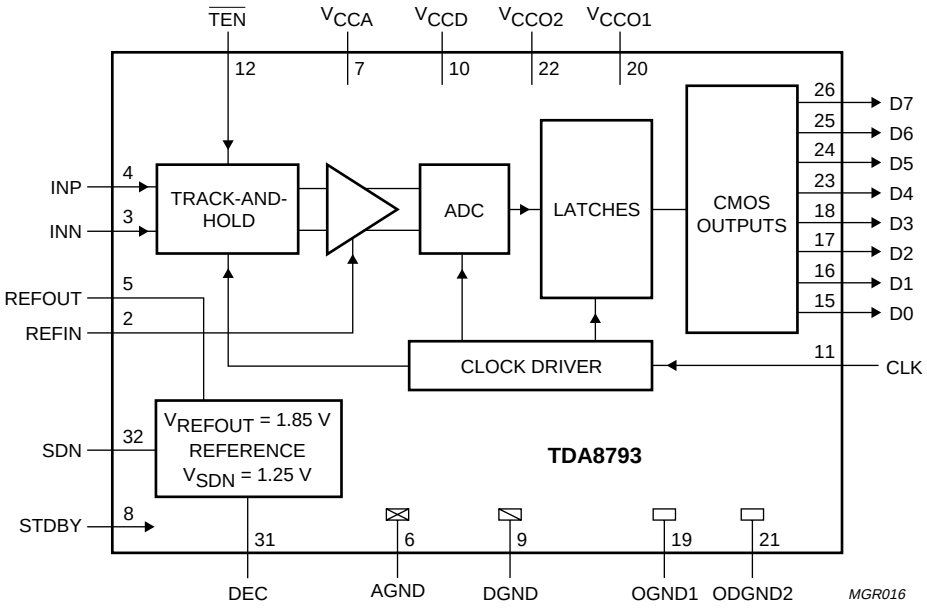


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
REFIN	2	reference input for ADC
INN	3	negative input
INP	4	positive input
REFOUT	5	reference for AC coupling
AGND	6	analog ground
V_{CCA}	7	analog supply voltage
STDBY	8	standby mode input
DGND	9	digital ground
V_{CCD}	10	digital supply voltage
CLK	11	clock input
$\overline{TEN}$	12	track enable input (active LOW)
n.c.	13	not connected
n.c.	14	not connected
D0	15	data output bit 0 (LSB)
D1	16	data output bit 1
D2	17	data output bit 2
D3	18	data output bit 3
OGND1	19	output ground 1
V_{CCO1}	20	output supply voltage 1
OGND2	21	output ground 2
V_{CCO2}	22	output supply voltage 2
D4	23	data output bit 4
D5	24	data output bit 5
D6	25	data output bit 6
D7	26	data output bit 7 (MSB)
n.c	27	not connected
n.c	28	not connected
n.c	29	not connected
n.c	30	not connected
DEC	31	decoupling
SDN	32	stabilized decoupling node

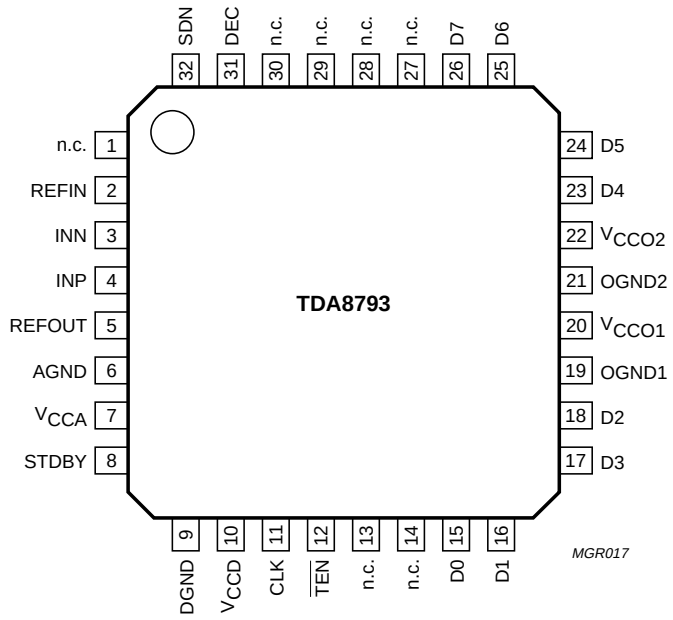


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage		–0.3	+7.0	V
V_{CCD}	digital supply voltage		–0.3	+7.0	V
V_{CCO}	output stages supply voltage		–0.3	+7.0	V
ΔV_{CC}	supply voltage differences between				
	V_{CCA} and V_{CCD}		–1.0	+1.0	V
	V_{CCO} and V_{CCD}		–1.0	+1.0	V
	V_{CCA} and V_{CCO}		–1.0	+1.0	V
$V_{INP, INN}$	input voltage range	referenced to AGND	–0.3	+7.0	V
I_O	output current		–	10	mA
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		0	70	°C
T_j	junction temperature		–	–	°C

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	94	K/W

CHARACTERISTICS

V_{CCA} = V_7 to V_6 = 2.7 to 3.6 V; V_{CCD} = V_{10} to V_9 = 2.7 to 3.6 V; V_{CCO} = V_{20} (or V_{22}) to V_{19} (or V_{21}) = 2.7 to 3.6 V; AGND to DGND and OGND shorted together; V_{CCA} to V_{CCD} = −0.15 to +0.15 V; V_{CCD} to V_{CCO} = −0.15 to +0.15 V; V_{CCA} to V_{CCO} = −0.15 to +0.15 V; T_{amb} = 0 to 70 °C; typical values measured at V_{CCA} = V_{CCD} = V_{CCO} = 3.0 V and T_{amb} = 25 °C; single-ended input; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		2.7	3.0	3.6	V
V_{CCD}	digital supply voltage		2.7	3.0	3.6	V
V_{CCO}	output stages supply voltage		2.7	3.0	3.6	V
I_{CCA}	analog supply current		32	40	48	mA
I_{CCD}	digital supply current		13	16	22	mA
I_{CCO}	output stages supply current	f_i = ramp input	–	0.1	tbf	mA
		f_i = 20 MHz	–	4	tbf	mA
Internal reference (pin SDN); note 1						
V_{ref}	reference voltage		1.21	1.25	1.29	V
V_{reg}	line regulation voltage	2.7 < V_{CCA} < 3.6 V	–	0.4	3	mV
TC	temperature coefficient		–	18	–	ppm/K
I_L	load current		–1	–	–	mA
Internal reference (pin REFOUT)						
$V_{o(ref)}$	reference voltage		1.76	1.82	1.88	V
$V_{o(reg)}$	line regulation voltage	2.7 < V_{CCA} < 3.6 V	–	1.5	4	mV
TC	temperature coefficient		–	18	–	ppm/K
I_L	load current		–1	–	–	mA
Adjustable full scale input (pin REFIN); see Figs 3, 4**,** and 7						
I_{ref}	input current	V_{REFIN} = 1.25 V	–	–0.87	–	mA
Clock input (pin CLK); note 2						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2	–	V_{CCD}	V
I_{IL}	LOW-level input current	V_{CLK} = 0	–2	–	+2	µA
I_{IH}	HIGH-level input current	V_{CLK} = V_{CCD}	–	–	5	µA
t_r	clock rise time		0.75	–	tbf	ns
t_f	clock fall time		0.75	–	tbf	ns
Z_i	input impedance	f_{CLK} = 100 MHz	–	32	–	kΩ
C_i	input capacitance	f_{CLK} = 100 MHz	–	2	–	pF
Standby input (pin STDBY); see Table 1						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2	–	V_{CCD}	V
I_{IL}	LOW-level input current	V_{STDBY} = 0	–5	–	–	µA
I_{IH}	HIGH-level input current	V_{STDBY} = V_{CCD}	–	–	5	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Track enable input (pin $\overline{TEN}$); see Table 2						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2	–	V_{CCD}	V
I_{IL}	LOW-level input current	V_{TEN} = 0	–5	–	–	µA
I_{IH}	HIGH-level input current	$V_{TEN} = V_{CCD}$	–	–	5	µA
Inputs (pins INP and INN); analog input voltage referenced to AGND; V_{REFIN} = 1.27 V; see Table 3						
$V_{i(p-p)}$	input voltage range (peak-to-peak value)	$V_i = V_{INP} – V_{INN}$; T_{amb} = 25 °C	0.90	0.97	1.040	V
ΔT_{CI}	input voltage range drift		–	0.5	–	mV/K
$V_{i(os)}$	input offset voltage	output code = 127	–25	–	+25	mV
Z_i	input impedance	f_{INP} = 50 MHz	–	90	–	kΩ
C_i	input capacitance	f_{INP} = 50 MHz	–	2	–	pF
I_{IL}	LOW-level input current	$V_{INP} = V_{REFOUT}$ + 0.5	–1	–	–	µA
		$V_{INP} = V_{REFOUT}$ – 0.5	–1	–	–	µA
I_{IH}	HIGH-level input current	$V_{INP} = V_{REFOUT}$ + 0.5	–	–	40	µA
		$V_{INP} = V_{REFOUT}$ – 0.5	–	–	40	µA
Adjustable full scale range; V_{REFIN} = 1.2 to 1.35 V; see Fig.3						
$V_{I(p-p)}$	input voltage range (peak-to-peak value)	$V_i = V_{INP} – V_{INN}$; T_{amb} = 25 °C	–	1	–	V
Voltage controlled regulator input pin V_{REFIN} (referenced to AGND); note 3						
$V_{i(ref)}$	reference voltage		tbf	1.25	tbf	V
$I_{i(ref)}$	input current on pin V_{REFIN}		–	tbf	1.1	mA
Outputs; ADC data outputs						
V_{OL}	LOW-level output voltage	I_O = 1 mA	–	–	0.5	V
V_{OH}	HIGH-level output voltage	I_O = –0.4 mA	V_{CCO} – 0.5	–	V_{CCO}	V
C_L	output load capacitance		–	–	10	pF
δv/δt	slew rate	10% to 90%; C_L = 10 pF	–	1.2	–	V/ns
Switching characteristics; note 2; see Table 1						
$f_{CLK(min)}$	minimum clock frequency	track = LOW	–	–	6	MHz
$f_{CLK(max)}$	maximum clock frequency		100	–	–	MHz
$t_{W(CLKH)}$	clock pulse width HIGH		4	–	–	ns
$t_{W(CLKL)}$	clock pulse width LOW		4	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog signal processing; note 3; see Figs 4, 5, 6 and 7						
INL	integral non-linearity	ramp input; f_{CLK} = 2 MHz; $V_{CCA} = V_{CCD}$ = 3 V	–	±0.8	tbf	LSB
DNL	differential non-linearity	ramp input; f_{CLK} = 2 MHz; $V_{CCA} = V_{CCD}$ = 3 V	–	±0.25	tbf	LSB
S/N	signal-to-noise ratio (full scale)	without harmonics; f_{CLK} = 100 MHz				
		f_i = 20 MHz	42	45	–	dB
		f_i = 50 MHz	–	45	–	dB
$B_{W(-3dB)}$	–3 dB analog bandwidth		–	350	–	MHz
THD	total harmonics distortion	f_i = 20 MHz	–	–56	–	dB
		f_i = 50 MHz	–	–52	–	dB
$H_{fund(FS)}$	full scale fundamental harmonics	f_{CLK} = 100 MHz				
		f_i = 20 MHz	–	–	0	dB
		f_i = 50 MHz	–	–	0	dB
$H_{D2(FS)}$	second harmonic distortion (full scale) all components included	differential inputs; f_{CLK} = 100 MHz				
		f_i = 20 MHz	–	66	–	dB
		f_i = 50 MHz	–	57	–	dB
		single-ended input; f_{CLK} = 100 MHz				
		f_i = 20 MHz	–	66	–	dB
		f_i = 50 MHz	–	55	–	dB
$H_{D3(FS)}$	third harmonic distortion (full scale) all components included	differential inputs; f_{CLK} = 100 MHz				
		f_i = 20 MHz	–	64	–	dB
		f_i = 50 MHz	–	61	–	dB
		single-ended input; f_{CLK} = 100 MHz				
		f_i = 20 MHz	–	64	–	dB
		f_i = 50 MHz	–	59	–	dB
SFDR	spurious free dynamic range	f_{CLK} = 100 MHz				dB
		f_i = 20 MHz	–	57	–	dB
		f_i = 50 MHz	–	54	–	dB
EB	effective bits	f_{CLK} = 100 MHz; note 4				bits
		f_i = 20 MHz	7.0	7.4	–	bits
		f_i = 50 MHz	–	7.2	–	bits
Data timing; f_{CLK} = 100 MHz; C_L = 10 pF; see Fig.8						
t_{ds}	sampling delay		–	–	1.5	ns
t_h	output hold time		3	–	–	ns
t_d	output delay time		–	5	8	ns

Notes

1. It is possible to use the reference output voltage (pin SDN) to drive other analog circuits under the limits indicated.
2. In addition to a good layout of the digital and analog grounds, it is recommended that the rise and fall times of the clock must be not less than 0.75 ns.
3. It is possible with an external reference voltage connected to REFIN pin to adjust the ADC input range. The input range variation will be fixed.
4. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8 k acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half of the clock frequency (nyquist frequency). Conversion to signal-to-noise ratio: SINAD = 6.02 × EB + 1.76 dB.

Table 1 Standby selection

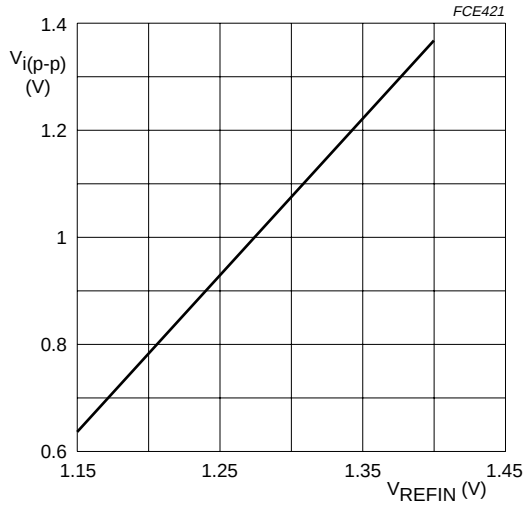
PIN STDBY	D0 TO D7	$I_{CCA} + I_{CCD}$
LOW	inactive	56 mA
HIGH	active; output logic state LOW	0.7 mA

Table 2 Track-and-hold selection

PIN $\overline{TEN}$	TRACK-AND-HOLD
LOW	active
HIGH	inactive; tracking mode

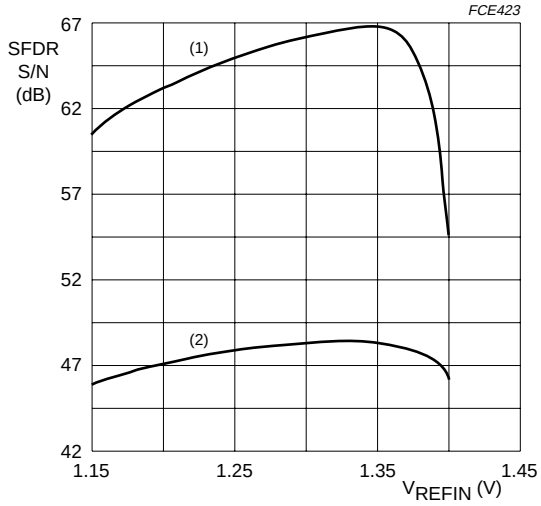
Table 3 Output coding and input voltage (typical values; referenced to AGND); V_{REFIN} = 1.27 V

STEP	V_{INP} (V)	V_{INN} (V)	BINARY OUTPUT BITS							
			D7	D6	D5	D4	D3	D2	D1	D0
Underflow	<1.6	>2.1	0	0	0	0	0	0	0	0
0	1.6	2.1	0	0	0	0	0	0	0	0
1	...	...	0	0	0	0	0	0	0	1
...	...	...	...	...	...	...	...	...	...	...
127	1.85	1.85	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...
254	...	...	1	1	1	1	1	1	1	0
255	2.1	1.6	1	1	1	1	1	1	1	1
Overflow	>2.1	<1.6	1	1	1	1	1	1	1	1



Typical values measured at $V_{CCA} = V_{CCD} = V_{CCO} = 3.0$ V, $f_{CLK} = 100$ MHz, $T_{amb} = 25$ °C and single-ended input.

Fig.3 ADC input voltage as a function of V_{REFIN} reference input voltage.

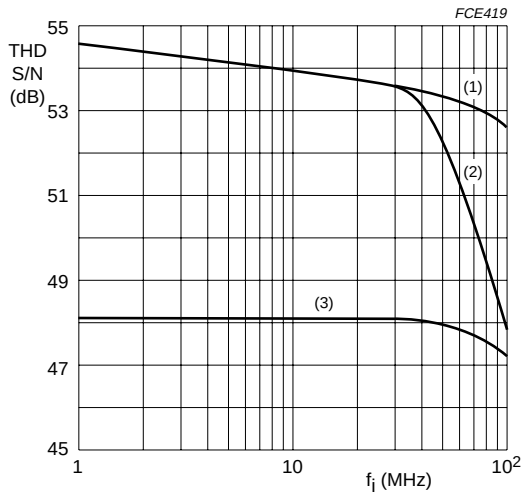


(1) SFDR

(2) S/N

Typical values measured at $V_{CCA} = V_{CCD} = V_{CCO} = 3.0$ V, $f_{CLK} = 100$ MHz, $T_{amb} = 25$ °C and single-ended input.

Fig.4 Noise and spurious free dynamic range as a function of V_{REFIN} reference input voltage.



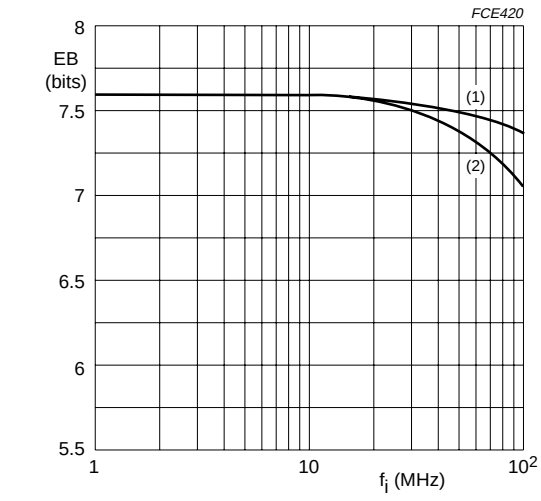
(1) THD for differential inputs

(2) THD for single-ended input

(3) S/N

Typical values measured at $V_{CCA} = V_{CCD} = V_{CCO} = 3.0$ V, $f_{CLK} = 100$ MHz and $T_{amb} = 25$ °C.

Fig.5 Noise and distortion as a function of input frequency.

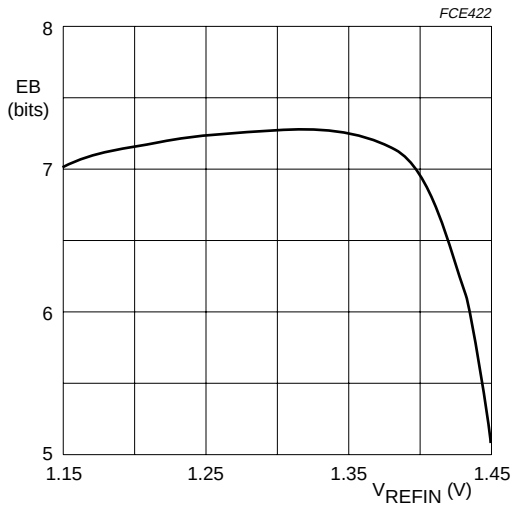


(1) Differential inputs

(2) Single-ended input

Typical values measured at $V_{CCA} = V_{CCD} = V_{CCO} = 3.0$ V, $f_{CLK} = 100$ MHz and $T_{amb} = 25$ °C.

Fig.6 Effective bits as a function of input frequency.



Typical values measured at $V_{CCA} = V_{CCD} = V_{CCO} = 3.0$ V, $f_{CLK} = 100$ MHz, $T_{amb} = 25$ °C and single-ended input.

Fig.7 Effective bits as a function of V_{REFIN} reference input voltage.

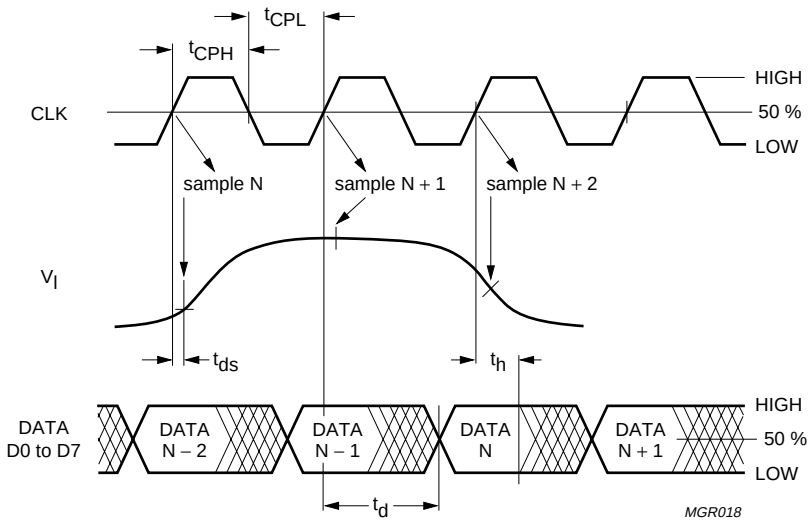


Fig.8 Timing diagram.

APPLICATION INFORMATION

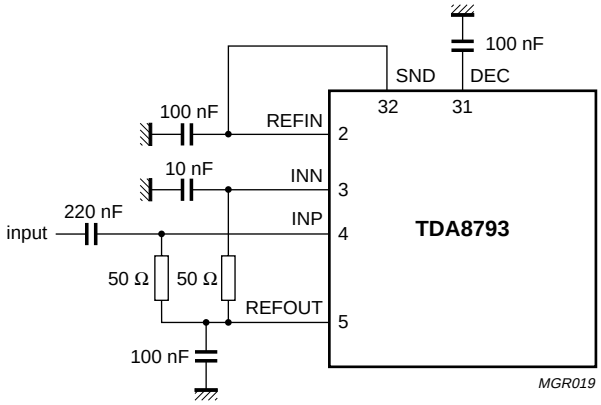


Fig.9 Application diagram for single-ended input mode with internal reference.

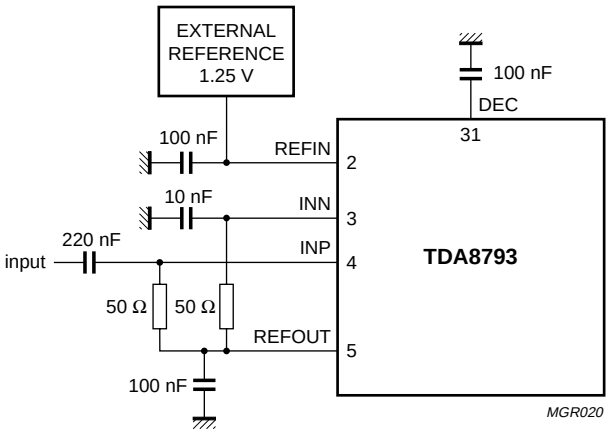


Fig.10 Application diagram for single-ended input mode with external reference.

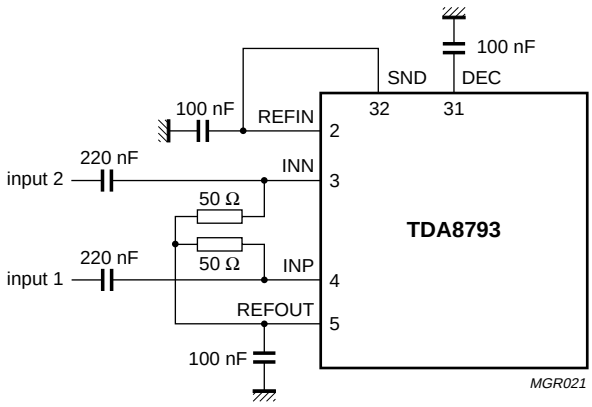


Fig.11 Application diagram for differential input mode with internal reference.

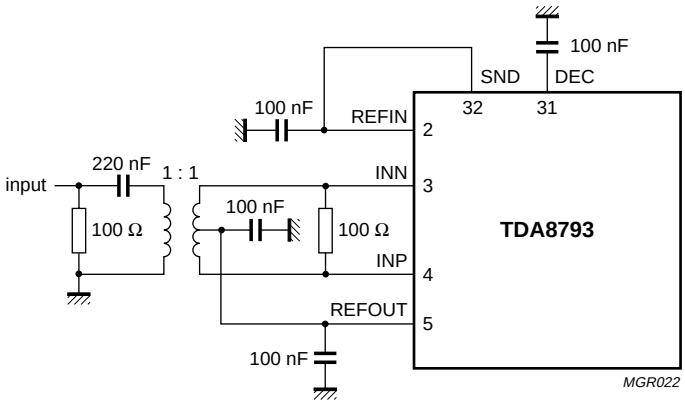
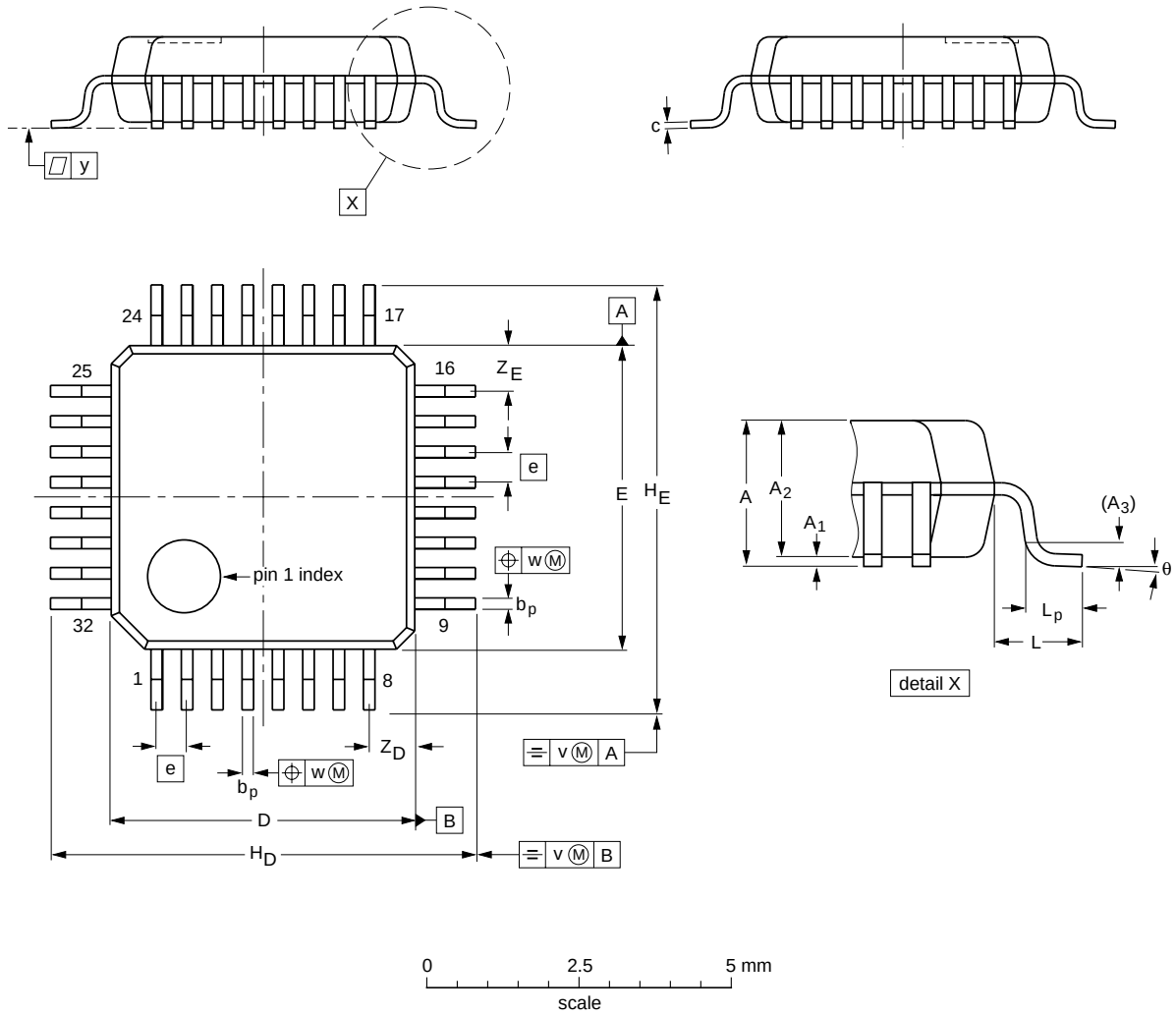


Fig.12 Application diagram for differential input mode using a transformer.

PACKAGE OUTLINE

LQFP32: plastic low profile quad flat package; 32 leads; body 5 x 5 x 1.4 mm **SOT401-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.15 0.05	1.5 1.3	0.25	0.27 0.17	0.18 0.12	5.1 4.9	5.1 4.9	0.5	7.15 6.85	7.15 6.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT401-1						~~95-12-19~~ 97-08-04

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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