DATA SHEET

TDA8765
10-bit high-speed Analog-to-Digital Converter (ADC)

Preliminary specification
Supersedes data of 1998 May 08
File under Integrated Circuits, IC02

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Philips Semiconductors

PHILIPS

10-bit high-speed Analog-to-Digital Converter (ADC)

TDA8765

FEATURES

- 10-bit resolution
- Sampling rate up to 55 MHz
- –3 dB bandwidth of 200 MHz
- 5 V power supplies
- Binary or twos-complement CMOS outputs
- In-range CMOS-compatible output
- TLL- CMOS-compatible static digital inputs
- 3 to 5 V CMOS-compatible digital outputs
- Differential clock input; Positive Emitter Coupled Logic (PECL) compatible
- Power dissipation 325 mW (typical)
- Low analog input capacitance (typical 2 pF), no buffer amplifier required
- Integrated sample-and-hold amplifier
- Differential analog input
- External amplitude range control
- Voltage controlled regulator included.

APPLICATIONS

- High-speed analog-to-digital conversion for
  - Video signal digitizing
  - High Definition TV (HDTV)
  - Imaging (camera scanner)
  - Medical imaging
  - Telecommunication
  - Base-station receiver.

GENERAL DESCRIPTION

The TDA8765 is a bipolar 10-bit Analog-to-Digital Converter (ADC) optimized for telecommunications and professional imaging. It converts the analog input signal into 10-bit binary coded digital words at a maximum sampling rate of 55 MHz. All static digital inputs (SH, $\overline{CE}$ and OTC) are TTL and CMOS compatible and all outputs are CMOS compatible. A sine wave clock input signal can also be used.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output supply voltage		3.0	3.3	5.25	V
I_{CCA}	analog supply current		–	33	tbf	mA
I_{CCD}	digital supply current		–	30	tbf	mA
I_{CCO}	output supply current	f_{CLK} = 4 MHz; f_i = 400 kHz	–	3.2	tbf	mA
INL	integral non-linearity	f_{CLK} = 4 MHz; f_i = 400 kHz	–	±0.5	±1.75	LSB
DNL	differential non-linearity	f_{CLK} = 4 MHz; f_i = 400 kHz	–	±0.3	±0.5	LSB
$f_{CLK(max)}$	maximum clock frequency					
	TDA8765H/4		40	–	–	MHz
	TDA8765H/5		55	–	–	MHz
P_{tot}	total power dissipation		–	325	tbf	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			SAMPLING FREQUENCY (MHz)
	NAME	DESCRIPTION	VERSION	
TDA8765H/4	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2	40
TDA8765H/5	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2	55

BLOCK DIAGRAM

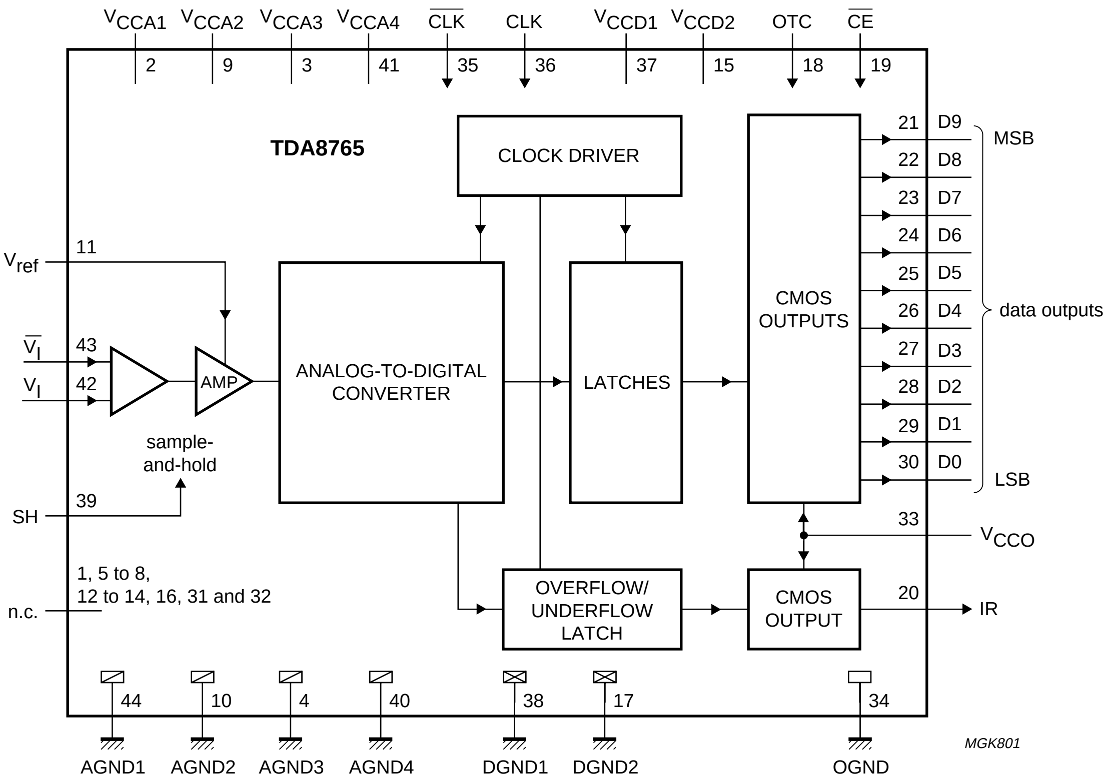


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
V_{CCA1}	2	analog supply voltage 1 (+5 V)
V_{CCA3}	3	analog supply voltage 3 (+5 V)
AGND3	4	analog ground 3
n.c.	5	not connected
n.c.	6	not connected
n.c.	7	not connected
n.c.	8	not connected
V_{CCA2}	9	analog supply voltage 2 (+5 V)
AGND2	10	analog ground 2
V_{ref}	11	reference voltage input
n.c.	12	not connected
n.c.	13	not connected
n.c.	14	not connected
V_{CCD2}	15	digital supply voltage 2 (+5 V)
n.c.	16	not connected
DGND2	17	digital ground 2
OTC	18	control input twos complement output; active HIGH
$\overline{CE}$	19	chip enable input (CMOS level; active LOW)
IR	20	in-range output
D9	21	data output; bit 9 (MSB)
D8	22	data output; bit 8
D7	23	data output; bit 7
D6	24	data output; bit 6
D5	25	data output; bit 5
D4	26	data output; bit 4
D3	27	data output; bit 3
D2	28	data output; bit 2
D1	29	data output; bit 1
D0	30	data output; bit 0 (LSB)
n.c.	31	not connected
n.c.	32	not connected
V_{CCO}	33	output supply voltage (3 to 5.25 V)
OGND	34	output ground
$\overline{CLK}$	35	complementary clock input; active LOW
CLK	36	clock input
V_{CCD1}	37	digital supply voltage 1 (+5 V)
DGND1	38	digital ground 1
SH	39	sample-and-hold enable input (CMOS level; active HIGH)
AGND4	40	analog ground 4
V_{CCA4}	41	analog supply voltage 4 (+5 V)
V_I	42	positive analog input voltage
$\overline{V}_I$	43	negative analog input voltage
AGND1	44	analog ground 1

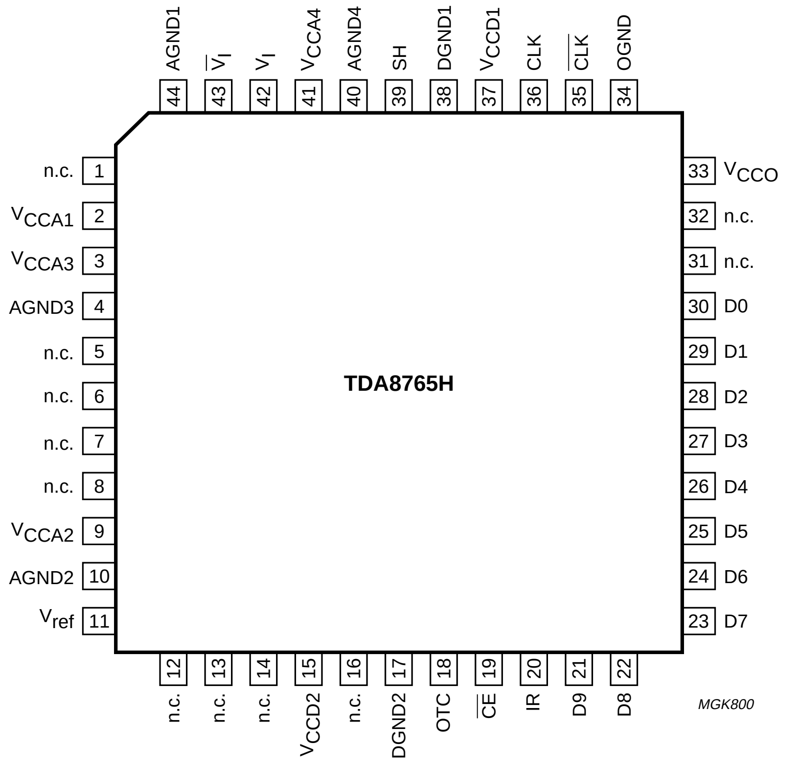


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	note 1	–0.3	+7.0	V
V_{CCD}	digital supply voltage	note 1	–0.3	+7.0	V
V_{CCO}	output supply voltage	note 1	–0.3	+7.0	V
ΔV_{CC}	supply voltage difference				
	$V_{CCA} - V_{CCD}$		–1.0	+1.0	V
	$V_{CCD} - V_{CCO}$		–1.0	+4.0	V
	$V_{CCA} - V_{CCO}$		–1.0	+4.0	V
V_I	input voltage at pins 42 and 43	referenced to AGND	0.3	V_{CCA}	V
$V_{i(p-p)}$	input voltage at pins 35 and 36 for differential clock drive (peak-to-peak value)		–	V_{CCD}	V
I_O	output current		–	10	mA
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		0	+85	°C
T_j	junction temperature		–	150	°C

Note

1. The supply voltages V_{CCA}, V_{CCD} and V_{CCO} may have any value between –0.3 and +7.0 V provided that the supply voltage differences ΔV_{CC} are respected.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	75	K/W

CHARACTERISTICS

V_{CCA} = V_2 to V_{44}, V_9 to V_{10}, V_3 to V_4 and V_{41} to V_{40} = 4.75 to 5.25 V; V_{CCD} = V_{37} to V_{38} and V_{15} to V_{17} = 4.75 to 5.25 V; V_{CCO} = V_{33} to V_{34} = 3.0 to 5.25 V; AGND and DGND shorted together; T_{amb} = 0 to 85 °C; typical values measured at V_{CCA} = V_{CCD} = 5 V and V_{CCO} = 3.3 V, T_{amb} = 25 °C, $V_{I(p-p)} - \overline{V}_{I(p-p)}$ = 2.0 V and C_L = 10 pF; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output supply voltage		3.0	3.3	5.25	V
I_{CCA}	analog supply current		–	33	45	mA
I_{CCD}	digital supply current		–	30	37	mA
I_{CCO}	output supply current	f_{CLK} = 4 MHz; f_i = 400 kHz	–	3.2	tbf	mA
		f_{CLK} = 40 MHz; f_i = 4.43 MHz	–	11	tbf	mA
Inputs						
CLK AND $\overline{CLK}$ (REFERENCED TO DGND)						
V_{IL}	LOW-level input voltage	V_{CCD} = 5 V; note 1	3.19	–	3.52	V
V_{IH}	HIGH-level input voltage	V_{CCD} = 5 V; note 1	3.83	–	4.12	V
I_{IL}	LOW-level input current	V_{CLK} or $V_{\overline{CLK}}$ = 3.19 V	–10	–	–	µA
I_{IH}	HIGH-level input current	V_{CLK} or $V_{\overline{CLK}}$ = 3.83 V	–	–	10	µA
Z_i	input impedance	f_{CLK} = 40 MHz	2	–	–	kΩ
C_i	input capacitance	f_{CLK} = 40 MHz	–	–	2	pF
$\Delta V_{CLK(p-p)}$	differential AC input voltage for switching ($V_{CLK} - V_{\overline{CLK}}$; peak-to-peak value)	DC voltage level = 2.5 V	0.5	–	2.0	V
OTC, SH AND $\overline{CE}$ (REFERENCED TO DGND); see Tables 2 and 3						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW-level input current	V_{IL} = 0.8 V	–20	–	–	µA
I_{IH}	HIGH-level input current	V_{IH} = 2.0 V	–	–	20	µA
V_I AND $\overline{V}_I$ (REFERENCED TO AGND; see Table 1); V_{REF} = V_{CCA} – 1.825 V						
I_{IL}	LOW-level input current		–	10	–	µA
I_{IH}	HIGH-level input current		–	10	–	µA
R_i	input resistance	f_i = 4.43 MHz	100	–	–	kΩ
C_i	input capacitance	f_i = 4.43 MHz	–	–	2	pF
$V_{I(CM)}$	common mode input voltage	$V_I = \overline{V}_I$; output code 511				
		V_{CCA} = 5 V	tbf	3.6	tbf	V
		V_{CCA} = 4.75 V	tbf	3.35	tbf	V
		V_{CCA} = 5.25 V	tbf	3.85	tbf	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage controlled regulator input V_{ref} (referenced to AGND); note 2						
V_{ref}	full-scale fixed voltage	V_{CCA} = 5 V	–	3.175	–	V
$V_{I(p-p)} - \overline{V}_{I(p-p)}$	input voltage amplitude (peak-to-peak value)	$V_{ref} = V_{CCA}$ – 1.825 V	–	2.0	–	V
I_{ref}	input current at V_{ref}		–	0.5	10	μA
Outputs (referenced to OGND)						
DIGITAL OUTPUTS D11 TO D0 AND IR (REFERENCED TO OGND)						
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	0	–	0.5	V
V_{OH}	HIGH-level output voltage	I_{OH} = –0.4 mA	V_{CCO} – 0.5	–	V_{CCO}	V
I_o	output current in 3-state	output level between 0.5 V and V_{CCO}	–20	–	+20	μA
Switching characteristics						
CLOCK FREQUENCY f_{CLK}; see Fig.5						
$f_{CLK(min)}$	minimum clock frequency	SH = HIGH	–	–	1	MHz
		SH = LOW	–	–	1	kHz
$f_{CLK(max)}$	maximum clock frequency					
	TDA8765H/4		40	–	–	MHz
	TDA8765H/5		55	–	–	MHz
t_{CLKH}	clock pulse width HIGH		8.5	–	–	ns
t_{CLKL}	clock pulse width LOW		8.5	–	–	ns
Analog signal processing; 50% clock duty factor; $V_I - \overline{V}_I$ = 2.0 V; $V_{ref} = V_{CCA}$– 1.825 V; see Table 1						
LINEARITY						
INL	integral non-linearity	f_{CLK} = 4 MHz; f_i = 400 kHz	–	±0.5	±1.75	LSB
DNL	differential non-linearity	f_{CLK} = 4 MHz; f_i = 400 kHz; no missing code	–	±0.3	±0.5	LSB
E_{offset}	offset error	$V_{CCA} = V_{CCD} = V_{CCO}$ = 5 V; T_{amb} = 25 °C; $V_I = \overline{V}_I$; output code = 511	tbf	–11	tbf	mV
E_G	gain error amplitude; spread from device to device	$V_{CCA} = V_{CCD} = V_{CCO}$ = 5 V; T_{amb} = 25 °C; $V_{I(p-p)} - \overline{V}_{I(p-p)}$ = 2.0 V	–5	–	+5	%FS
BANDWIDTH (f_{CLK} = 55 MHz); note 3						
B	analog bandwidth	–3 dB; full-scale input	tbf	200	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
HARMONICS (f_{CLK} = 40 MHz)						
$H_{fund(FS)}$	fundamental harmonics (full scale)	f_i = 4.43 MHz	–	–	0	dB
$H_{tot(FS)}$	harmonics (full scale); all components	f_i = 4.43 MHz				
	second harmonic		–	–75	–	dB
	third harmonic		–	–70	–	dB
THD	total harmonic distortion	f_i = 4.43 MHz; note 4	–	–66	–	dB
THERMAL NOISE						
$N_{th(rms)}$	thermal noise (RMS value)	grounded input; f_{CLK} = 40 MHz	–	0.2	tbf	LSB
SPURIOUS FREE DYNAMIC RANGE						
DR_{sf}	spurious free dynamic range	f_i = 4.43 MHz	tbf	71	–	dB
		f_i = 10 MHz	tbf	68	–	dB
		f_i = 20 MHz	tbf	67	–	dB
SIGNAL-TO-NOISE RATIO; note 5						
S/N	signal-to-noise ratio	without harmonics; f_{CLK} = 40 MHz; f_i = 4.43 MHz	–	59	–	dB
EFFECTIVE NUMBER OF BITS; see Figs 3 and 4 and note 5						
N_{bit}	effective number of bits TDA8765H/4 (f_{CLK} = 40 MHz)	f_i = 4.43 MHz	9.0	9.6	–	bits
		f_i = 10 MHz	–	9.6	–	bits
		f_i = 15 MHz	–	9.5	–	bits
	effective number of bits TDA8765H/5 (f_{CLK} = 55 MHz)	f_i = 4.43 MHz	–	9.6	–	bits
		f_i = 10 MHz	–	9.4	–	bits
		f_i = 15 MHz	–	9.3	–	bits
		f_i = 20 MHz	–	9.1	–	bits
INTERMODULATION; note 6						
TTIR	two-tone intermodulation rejection	f_{CLK} = 40 MHz	tbf	66	–	dB
d_3	third-order intermodulation distortion	f_{CLK} = 40 MHz	tbf	67	–	dB
BIT ERROR RATE						
BER	bit error rate	f_{CLK} = 40 MHz; f_i = 4.43 MHz; V_I = ±16 LSB at code 511	–	10^{-15}	tbf	times/ sample

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (C_L = 10 pF); see Fig.5 and note 7						
$t_{d(s)}$	sampling delay time		–	–	2	ns
t_h	output hold time		4	–	–	ns
t_d	output delay time	V_{CCO} = 5.25 V	–	10	15	ns
		V_{CCO} = 3.0 V	–	13	18	ns
3-state output delay times; see Fig.6						
t_{dZH}	enable HIGH		–	14	18	ns
t_{dZL}	enable LOW		–	16	20	ns
t_{dHZ}	disable HIGH		–	16	20	ns
t_{dLZ}	disable LOW		–	14	18	ns

Notes

1. The circuit has two clock inputs: CLK and $\overline{CLK}$. There are four modes of operation:
   a) PECL mode 1 (DC level varies equal to DC level of V_{CCD}): CLK and $\overline{CLK}$ inputs are at differential PECL levels.
   b) PECL mode 2 (DC level varies equal to DC level of V_{CCD}): CLK input is at PECL level and sampling is taken on the falling edge of the clock input signal. A DC level of 3.65 V has to be applied on $\overline{CLK}$ decoupled to GND via a 100 nF capacitor.
   c) PECL mode 3 (DC level varies equal to DC level of V_{CCD}): $\overline{CLK}$ input is at PECL level and sampling is taken on the rising edge of the clock input signal. A DC level of 3.65 V has to be applied on CLK decoupled to GND via a 100 nF capacitor.
   d) AC driving mode 4: when driving the CLK input directly and with any AC signal of minimum 0.5 V (p-p) and with a DC level of 2.5 V, the sampling takes place at the falling edge of the clock signal.
   When driving the $\overline{CLK}$ input with the same signal, sampling takes place at the rising edge of the clock signal. It is recommended to decouple the $\overline{CLK}$ or CLK input to DGND via a 100 nF capacitor.
2. It is possible with an external reference connected to pin V_{ref} to adjust the ADC input range. This voltage has to be referenced to V_{CCA}. For V_{CCA} – 1.825 V, the differential input voltage amplitude is 2 V (p-p).
3. The –3 dB analog bandwidth is determined by the 3 dB reduction in the reconstructed output, the input being a full-scale sine wave.
4. THD (total harmonic distortion) is obtained with the addition of the first five harmonics:

$$THD = 20\log\frac{F}{\sqrt{(2nd)^2 + (3rd)^2 + (4th)^2 + (5th)^2 + (6th)^2}}$$

   where F is the fundamental harmonic referenced at 0 dB for a full-scale sine wave input.
5. Effective number of bits are obtained via a Fast Fourier Transform (FFT). The calculation takes into account all harmonics and noise up to half of the clock frequency (Nyquist frequency). Conversion to SNR:
   $SNR = N_{bit} \times 6.02 + 1.76$ dB.
6. Intermodulation measured relative to either tone with analog input frequencies of 4.43 and 4.53 MHz. The two input signals have the same amplitude and the total amplitude of both signals provides full-scale to the converter (–6 dB below full scale for each input signal).
   d_3 is the ratio of the RMS-value of either input tone to the RMS-value of the worst case third order intermodulation product.
7. Output data acquisition: the output data is available after the maximum delay of t_d.

Table 1 Output coding with differential inputs (typical values to AGND); $V_{i(p-p)} - \overline{V}_{i(p-p)}$ = 2.0 V; $V_{ref} = V_{CCA}$ – 1.825 V

CODE	$V_{i(p-p)}$	$\overline{V}_{i(p-p)}$	IR	BINARY OUTPUTS	TWOS COMPLEMENT OUTPUTS
				D9 TO D0	D9 TO D0
Underflow	<3.1	>4.1	0	0 0 0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0 0 0
0	3.1	4.1	1	0 0 0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0 0 0
1	–	–	1	0 0 0 0 0 0 0 0 0 1	1 0 0 0 0 0 0 0 0 1
↓	–	–	↓	↓	↓
511	3.6	3.6	1	0 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1
↓	–	–	↓	↓	↓
1022	–	–	1	1 1 1 1 1 1 1 1 1 0	0 1 1 1 1 1 1 1 1 0
1023	4.1	3.1	1	1 1 1 1 1 1 1 1 1 1	0 1 1 1 1 1 1 1 1 1
Overflow	>4.1	<3.1	0	1 1 1 1 1 1 1 1 1 1	0 1 1 1 1 1 1 1 1 1

Table 2 Mode selection

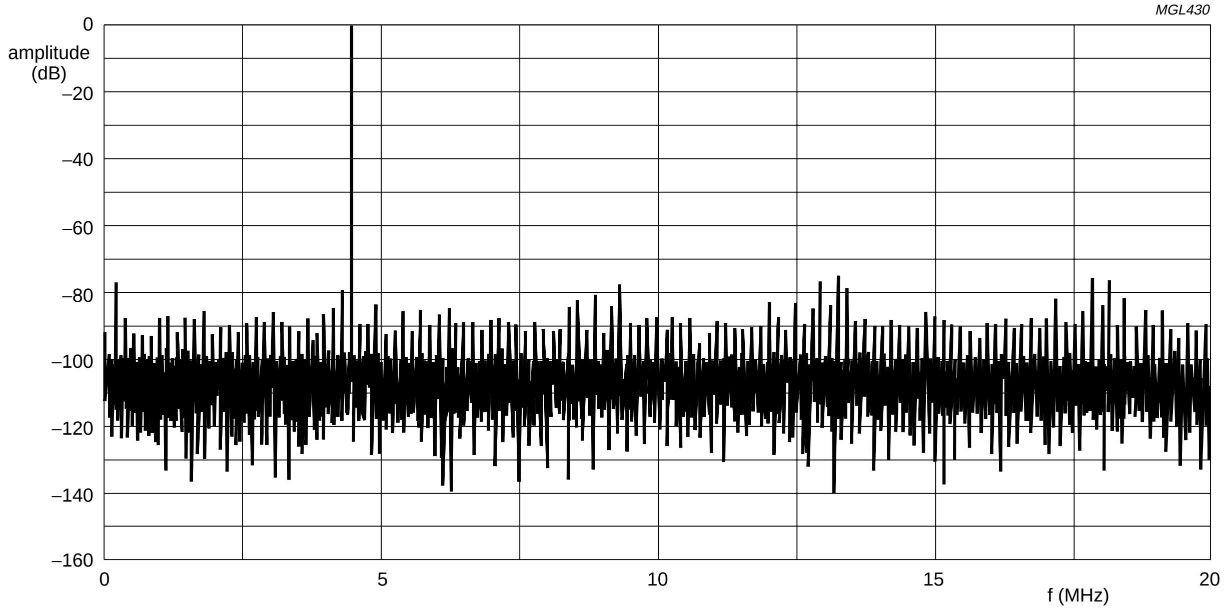
OTC	$\overline{CE}$	D0 TO D9 AND IR
0	0	binary; active
1	0	twos complement; active
X[1]	1	high impedance

Note

1. X = don’t care.

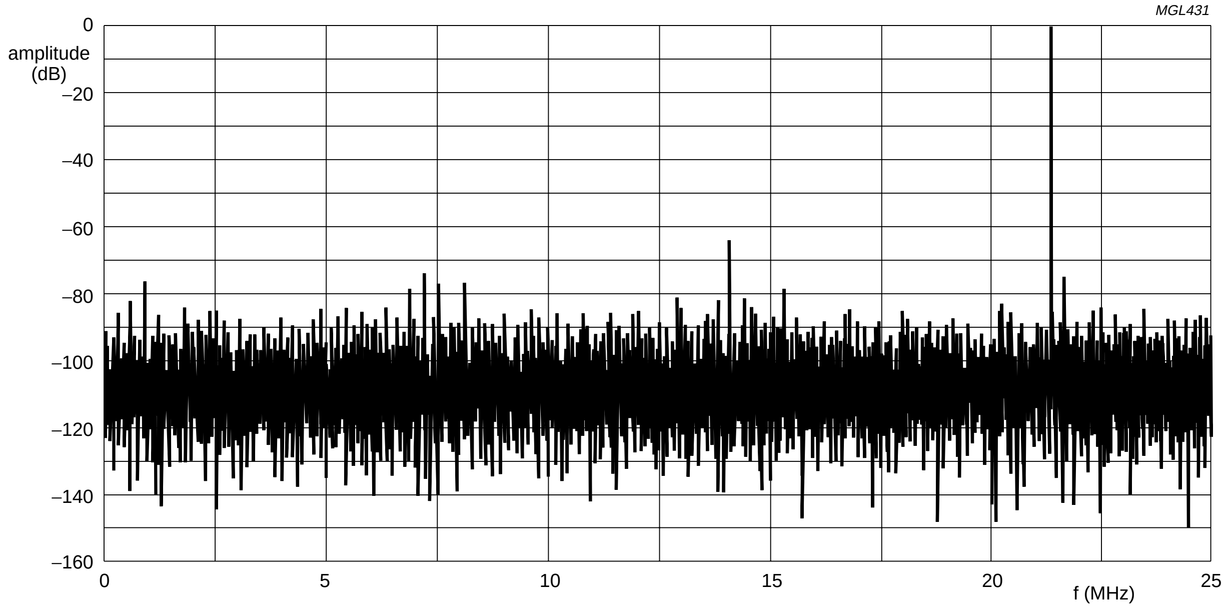
Table 3 Sample-and-hold selection

SH	SAMPLE-AND-HOLD
1	active
0	inactive; tracking mode



Effective bits: 9.68; THD = −70.8 dB.
Harmonic levels (dB): 2nd = −80.3; 3rd = −74.5; 4th = −87.7; 5th = −76.4; 6th = −78.6.

Fig.3 Typical fast Fourier transform (f_{CLK} = 40 MHz; f_i = 4.43 MHz).



Effective bits: 9.12; THD = −62.5 dB.
Harmonic levels (dB): 2nd = −73.0; 3rd = −63.4; 4th = −80.9; 5th = −78.1; 6th = −74.4.

Fig.4 Typical fast Fourier transform (f_{CLK} = 50 MHz; f_i = 21.4 MHz).

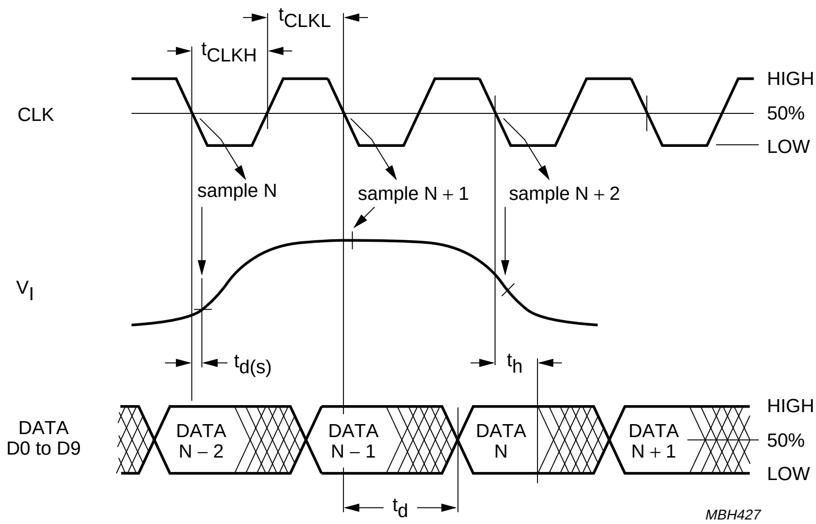
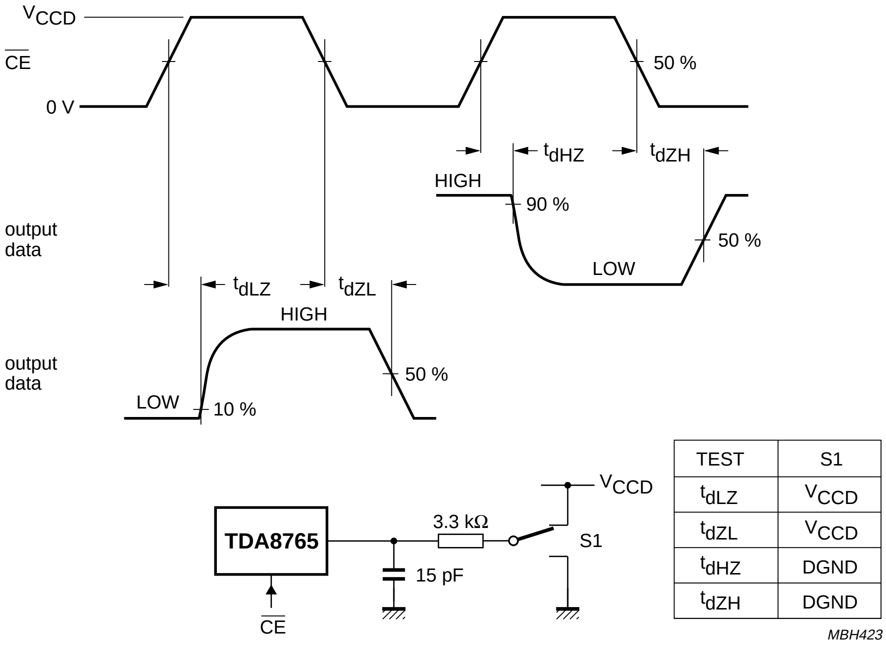


Fig.5 Timing diagram.

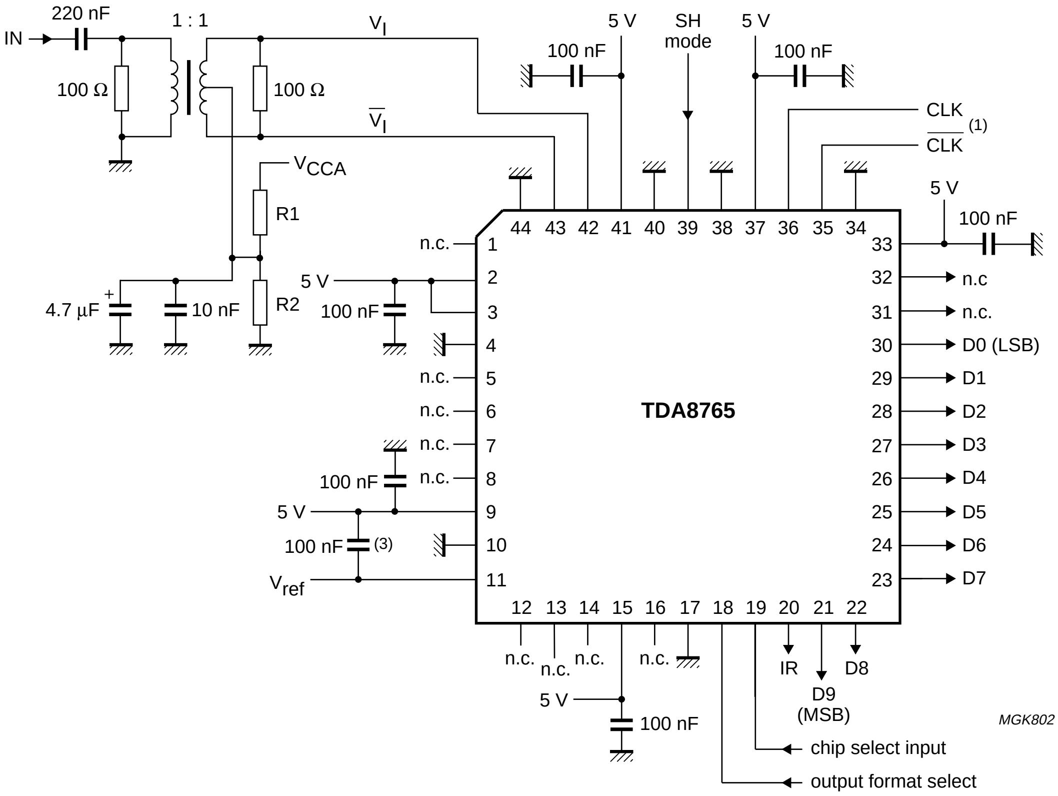


TEST	S1
t_{dLZ}	V_{CCD}
t_{dZL}	V_{CCD}
t_{dHZ}	DGND
t_{dZH}	DGND

$f_{\overline{CE}}$ = 100 kHz.

Fig.6 Timing diagram and test conditions of 3-state output delay time.

APPLICATION INFORMATION



The analog, digital and output supplies should be separated and decoupled.

(1) Single-ended clock signals can be applied if required.

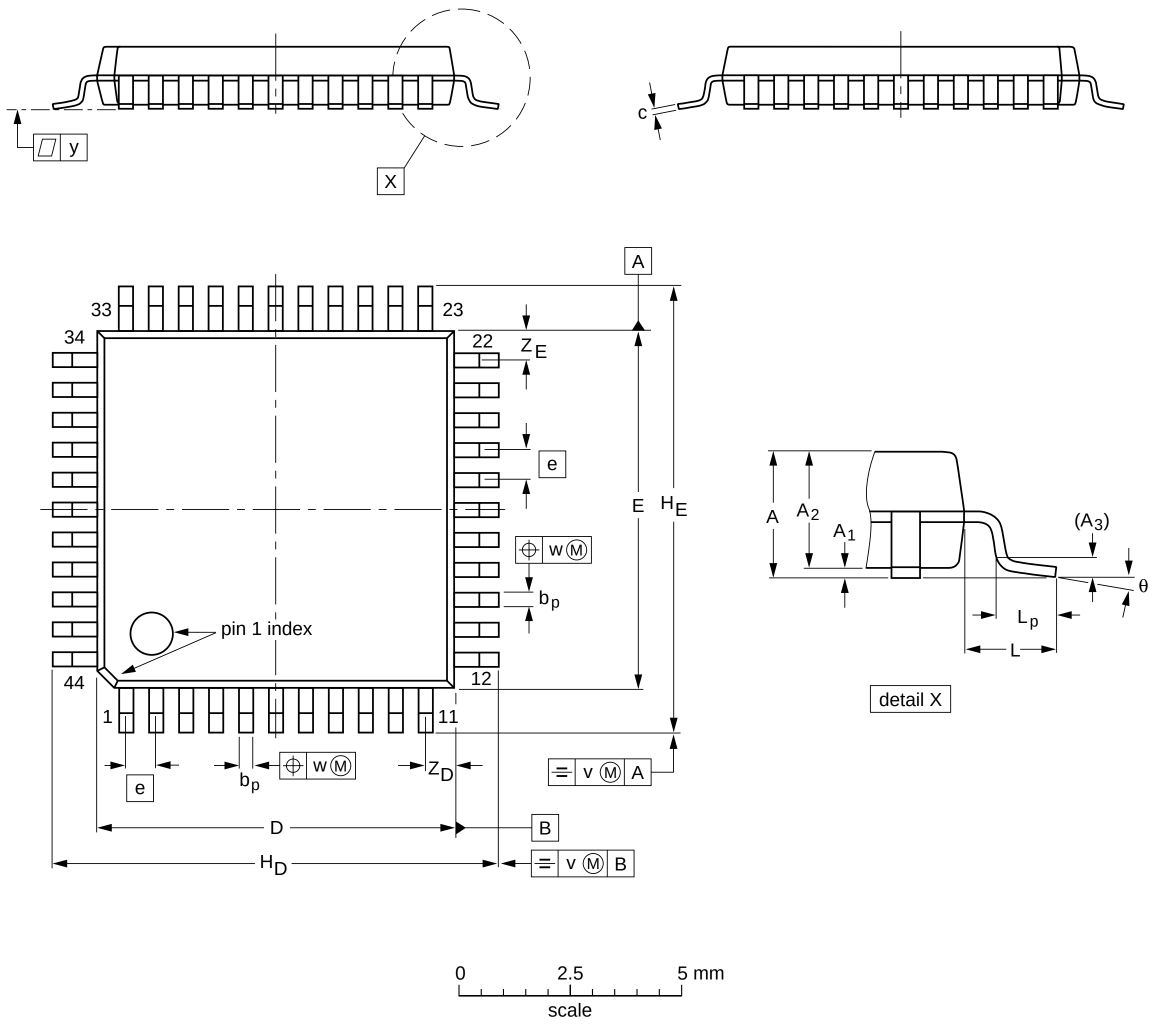
(2) R1 and R2 must be determined in order to obtain a middle voltage of 3.6 V; see common mode input voltage. In addition, the minimum current into these resistors should be about 1 mA in order to ensure a sufficient analog input stability.

(3) V_{ref} must be decoupled to V_{CCA}.

Fig.7 Application diagram.

PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_D	H_E	L	L_p	v	w	y	Z_D(1)	Z_E(1)	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~95-02-04~~ 97-08-01

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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