SMALL SIGNAL COMBINATION IC FOR COLOUR TV

GENERAL DESCRIPTION

The TDA8305A is a TV sub-system circuit, for colour television receivers with the following features.

Features

- Vision IF amplifier with synchronous demodulator
- Automatic gain control (AGC) detector suitable for negative modulation
- AGC tuner
- Automatic frequency control (AFC) circuit with sample-and-hold
- Video preamplifier
- Sound IF amplifier and demodulator
- DC volume control or separate supply for starting the horizontal oscillator
- Audio preamplifier
- Horizontal synchronization circuit with two control loops
- Vertical synchronization (divider system) and sawtooth generation with automatic amplitude adjustment for 50 and 60 Hz
- Transmitter identification (mute)
- Generation of sandcastle pulse

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pin 7)	V_{7-6}	9.5	12	13.2	V
Supply current (pin 7)	I_7	75	125	165	mA
Start current (pin 11)	I_{11}	–	6.5	9.0	mA
Video					
IF sensitivity at 38.9 MHz (RMS value)		25	40	65	μV
IF gain control range	G_{8-9}	–	74	–	dB
Signal-to-noise ratio at 10 mV input signal	S/N	50	57	–	dB
AFC output voltage swing (peak-to-peak value)	$V_{18-6(p-p)}$	10.5	–	11.5	V
Sound					
AF output signal (RMS value)	$V_{12-6(rms)}$	400	600	800	mV
AM suppression at V_I = 50 mV	AMS	53	58	–	dB
Total harmonic distortion	THD	–	0.5	2	%

PACKAGE OUTLINE

28-lead DIL; plastic (with internal heat spreader) (SOT117)

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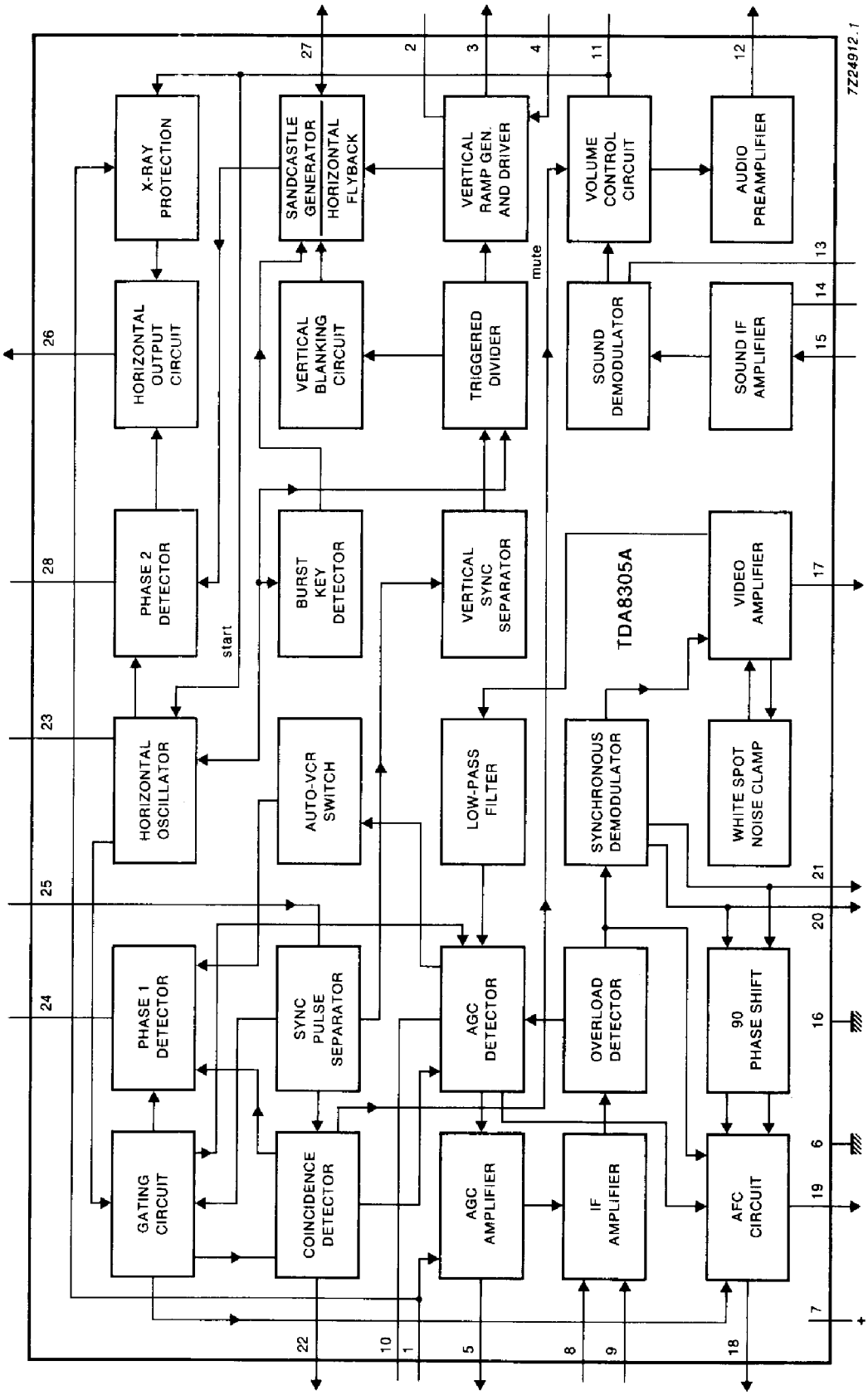

Fig.1 Block diagram.

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QUICK REFERENCE DATA (continued)

parameter	symbol	min.	typ.	max.	unit
Sync pulse input amplitude	V_{25}	200	750	–	mV
Flyback input current	I_{27}	0.1	–	2	mA
Sandcastle output					
during burst key	V_{27}	8	–	–	V
during horizontal blanking	V_{27}	4	4.5	5	V
during vertical blanking	V_{27}	2.1	2.5	2.9	V
Coincidence detector voltage					
in synchronized condition	V_{22}	–	9.5	–	V
in no signal condition	V_{22}	–	1.5	–	V
Vertical feedback input					
DC voltage	V_{22}	2.9	3.3	3.7	V
AC voltage (peak-to-peak value)	$V_{22(p-p)}$	–	1.2	–	V

DEVELOPMENT DATA

PINNING

1. AGC take-over/X-ray protection
2. Vertical ramp generator
3. Vertical drive
4. Vertical feedback
5. Tuner AGC
6. Ground
7. Main supply voltage
8. Vision IF input
9. Vision IF input
10. IF AGC
11. Volume control/start horizontal oscillator
12. Audio output
13. Sound demodulator
14. Sound IF decoupling
15. Sound IF input
16. Ground (for some critical parts)
17. Video output
18. AFC output
19. AFC S/H, AFC switch
20. Vision demodulator tuned circuit
21. Vision demodulator tuned circuit
22. Coincidence detector
23. Horizontal oscillator
24. First phase detector
25. Sync separator
26. Horizontal drive
27. Sandcastle output/horizontal flyback input
28. Second phase detector

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FUNCTIONAL DESCRIPTION

Vision IF amplifier, demodulator and video amplifier

The IF amplifier of the TDA8305A has three AC-coupled stages, each stage having a control range that exceeds 20 dB. AC-coupling means that the DC-feedback circuitry of the amplifier (present in the TDA4505) can be omitted, resulting in a saving of one pin. An additional advantage is the symmetry of the amplifier which results in a less critical application.

In the TDA8305A the regenerated carrier signal is limited by a logarithmic limiter circuit before it is passed on to a passive synchronous demodulator. The limiter has a very low differential phase shift which results in good differential gain and phase figures.

The TDA8305A's video amplifier has a higher bandwidth and better linearity compared with that of the TDA4505. A noise clamp is included in the video amplifier that limits the interference pulses to a level just below the top sync. This circuit is more effective than the noise inverter used in the TDA4505 and results in an improved picture stability, with respect to interference.

AFC circuit

In the TDA4505 and TDA8305A, the reference signal for the AFC circuit is obtained from the demodulator tuned circuit which means only one tuned circuit and adjustment are needed. The disadvantage with this method is that the frequency spectrum fed to the detector is determined by the SAW filter characteristic. This spectrum is asymmetrical with respect to the picture carrier so that the AFC output voltage is dependent on the video signal. This was the main problem found with the TDA4505's AFC circuit.

To remove this problem the TDA8305A is equipped with a sample-and-hold circuit which samples during the sync level of the signal. This means that only the carrier signal is available to the AFC and it will not be affected by the video information. The additional pin required for this circuit is provided by the pin that became available when the DC feedback circuit was removed from the IF amplifier (see previous section).

Weak input signals will cause the drive signal of the AFC to contain a lot of noise. This noise signal has an asymmetrical frequency spectrum that causes an offset in the AFC output voltage, this offset can be reduced by applying a notch to the demodulator circuit. The sample-and-hold circuit is followed by a high output impedance amplifier, therefore the AFC's control steepness is dependent on the load impedance.

AGC circuit

The TDA8305A's AGC detector differs from that of the TDA4505 in that it doesn't need the charge resistor but has an internal current source. Also the circuitry between the detector capacitor and the control stages has been changed to improve the signal-to-noise ratio of the video output signal (no dips in the S/N ratio depending on the input signal amplitude). The point of tuner take-over is preset by the voltage level at pin 1.

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Sound circuit and horizontal oscillator starting function

The input to the sound IF amplifier is by means of a bandpass filter coupling from the video output (pin 17). The sound is demodulated and passed via a volume control stage to the audio output amplifier. Volume control is obtained by connecting a potentiometer (10 kΩ) between pin 11 and ground, or by supplying pin 11 with a variable voltage. Sound output is suppressed by an internal mute signal when no TV signal is identified.

Improvement of sound quality was one of the main reasons for redesigning the TDA4505. To obtain a better idea of the performance of the various circuits of the TDA4505 the following measurements were carried out:

- Weak signal performance when a TBA120 is driven with an intercarrier signal obtained from the vision IF circuit of the TDA4505 (the sound IF of the latter was not used)
- The same measurement for the sound IF circuit of the TDA4505 driven from another TDA4505 (again without using the sound IF circuit)
- The same measurement as in the first case but with the sound IF of the TDA4505 connected normally

From the results of these measurements it was established that the sound problem was caused by an interaction between vision IF and sound circuits. The improved sound quality of the TDA8305A as compared to the TDA4505 was achieved by:

- A very symmetrical vision-IF amplifier which is less sensitive to radiation from the sound IF amplifier
- A change to the internal ground and supply connections of the IC to reduce coupling between both circuits

DEVELOPMENT DATA

DC volume control/Horizontal oscillator start

Horizontal oscillator; the operation depending on the application. During switch-on if no current is supplied to pin 11 this pin will act as a volume control. When a current of 9.0 mA is supplied to pin 11 the volume control is set to a fixed output signal and the device will generate drive pulses for the horizontal deflection. The main supply can then be derived from the horizontal deflection circuit.

Horizontal synchronization

The video input signal (positive video) is connected to pin 25. The horizontal synchronization has two control loops that generate a sandcastle pulse. Using the oscillator sawtooth facilitates accurate timing of the burst key pulse. Therefore, the phase of this sawtooth must have a fixed relationship to the sync pulse, which is achieved by use of the second control loop.

The TDA8305A's horizontal synchronization circuit differs from that of the TDA4505 in that:

- The horizontal oscillator's retrace occurs during the horizontal retrace and not during the scan period. This means that with weak input signals no interference will be visible on the screen. It also prevents video crosstalk from disturbing the picture phase
- The reference signal for the horizontal phase detector is nearer to being symmetrical and is independent of the supply voltage and temperature. As a consequence the frequency shift of the horizontal oscillator during noise is reduced
- The current ratio of the phase detector for strong and weak signals is increased to obtain better behaviour during both VCR-playback and weak signal reception. The switching level is independent of supply voltage and temperature.

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FUNCTIONAL DESCRIPTION (continued)

Horizontal phase detector

The circuit has the following operating conditions.

(a) Strong input signal, synchronized or non-synchronized.
(The strong/weak signal condition is obtained from the AGC circuit; the in-sync/out-of-sync from the coincidence detector). In this condition the time constant is optimum for VCR-playback i.e. fast time constant during the vertical retrace (to be able to correct VCR head-errors) and such, that during scan, fluctuations of the sync are corrected. The phase detector is not gated.

(b) Weak signal - synchronized
In this condition the time constant is increased compared to condition (a). Also the phase detector is gated when the oscillator is synchronized. This ensures a stable display which is not disturbed by noise in the video signal.

(c) Weak signal - non-synchronized.
In this condition the time constant during scan and vertical retrace are the same as during scan in condition (a).

Vertical synchronization

The TDA8305A's vertical circuit differs from that of the TDA4505 in that it has:

- Improved interlacing - the timing of the internal pulses is now close to a 50/50 ratio. This timing is independent of supply voltage and temperature
- The temperature drift of the vertical amplitude has been reduced
- Reduction of noise in the vertical output signal so that modulation of the line distance will no longer be visible on large screen sets.
- When out-of-sync is detected by the horizontal circuit the divider is switched to 625 lines. This results in a stable amplitude when no input signal is available. In the TDA4505 the divider remains in the wide window during this condition which means interference may affect stability.

Vertical sync pulse

The vertical sync pulse integrator will not be disturbed when the vertical sync pulses have a width of 10 μs with a separation of 22 μs. These types of vertical sync pulses are sometimes generated by video tapes with anti-copy guard.

Vertical divider system

The TDA8305A embodies a synchronized divider system for generating the vertical sawtooth at pin 2. The divider system has an internal frequency doubling circuit, which allows the horizontal oscillator to operate at its normal line frequency. One line period equals 2 clock pulses.
Use of the divider system avoids the requirement for vertical frequency adjustment. The divider has a discriminator window for automatic switching from 60 Hz to 50 Hz mode. When the trigger pulse comes before line 576 the 60 Hz mode is selected, otherwise the 50 Hz mode is selected.
The divider system operates with 2 different divider reset windows for maximum interference/ disturbance protection.
The windows are activated via an up/down counter.
The counter increases its counter value by 1 each time the separated vertical sync pulse is within the search window. When not within the search window this value is decreased by 1.
The operating modes of the divider system are as follows:

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Mode A

Large (search) window (divider ratio between 488 and 722)

This mode is valid for the following conditions:

- Divider is looking for a new transmitter
- Divider ratio found - not within the narrow window limits
- Up/down counter value of the divider system operating in the narrow window mode drops below count 10

Mode B

Narrow window (divider ratio between 522 to 528, 60 Hz; or 622 to 628, 50 Hz)

The divider system switches over to this mode when the up/down counter has reached its maximum value of 15 approved vertical sync pulses. When the divider operates in this mode and a vertical sync pulse is missing within the window, the divider is reset at the end of the window and the counter value is decreased by 1. At a counter value below 10 the divider system switches over to the large window mode.
The divider system also generates an anti-topflutter pulse which inhibits the phase 1 detector during the vertical sync pulse. The pulse width is dependent on the divider mode. In Mode A the start is generated by reset of the divider.
In Mode B the anti-topflutter pulse starts at the beginning of the first equalizing pulse.
The anti-topflutter pulse ends at count 10 for the 50 Hz mode and count 12 for the 60 Hz mode.
The vertical blanking pulse is also generated via the divider system. The start is by reset of the divider while the blanking pulse width is 34 (17 lines) for the 60 Hz mode and at count 42 (21 lines) for the 50 Hz mode.
The vertical blanking pulse at the sandcastle output (pin 27) is generated by adding the anti-topflutter pulse to the blanking pulse. Thus the vertical blanking pulse starts at the beginning of the first equalizing pulse when the divider operates in Mode B. The length of the vertical blanking in this condition is 21 lines in the 60 Hz mode and 25 lines in the 50 Hz mode.

DEVELOPMENT DATA

Application when external video signals require synchronization

The input to the sync separator is externally available via pin 25. For normal application the video output signal at pin 17 is AC coupled to this input as shown in Fig.11. It is possible to interrupt this connection and drive the sync separator from other sources such as:

- A teletext decoder in serial mode
- An external video signal via a peritelevision connector

When a teletext decoder is applied the IF amplifier and synchronization circuit are operating in the same phase which means that various connections between the two sections (i.e. AGC gating) can remain active. When external signals are applied to the sync separator the connections between the two parts must be interrupted. This can be achieved by connecting pin 22 to ground, which results in the following conditions:

- AGC detector is not gated
- AFC circuit is active
- Mute circuit not active - sound channel remains switched on
- Phase detector 1 has an optimal time constant for external video sources and is not gated.

X-ray protection

By forcing pin 1 below 1 V the horizontal output changes to a high resistance. The protection can be released by switching off the mains.

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 7)	$V_P = V_{7-6}$	–	13.2	V
Total power dissipation	P_{tot}	–	2.3	W
Operating ambient temperature range	T_{amb}	−25	+65	°C
Storage temperature range	T_{stg}	−25	+150	°C

CHARACTERISTICS

$V_P = V_{7-6}$ = 12 V; T_{amb} = 25 °C; carrier 38.9 MHz, negative modulation; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage range (pin 7)		V_{7-6}	9.5	12	13.2	V
Supply current (pin 7)	at no input	I_7	75	125	165	mA
Start current (pin 11)	note 1	I_{11}	–	6.5	9.0	mA
Start voltage horizontal oscillator		V_{11}	9.5	–	–	V
Start protection level	I_{11} = 12 mA	V_{11}	–	–	16.5	V
Vision IF amplifier (pins 8 and 9)						
Input sensitivity at 38.9 MHz (RMS value)	note 2	V_{8-9}	25	40	60	μV
Input sensitivity at 45.75 MHz (RMS value)	notes 2, 27	V_{8-9}	25	40	60	μV
Differential input resistance	note 3	R_{8-9}	–	1300	–	Ω
Differential input capacitance	note 3	C_{8-9}	–	5	–	pF
Gain control range		G_{8-9}	–	77	–	dB
Maximum input signal		V_{8-9}	100	170	–	mV
Output signal expansion for 48 dB variation of input signal	note 4	ΔV_{17}	–	1	–	dB
Video amplifier	note 5					
Zero signal output level	note 6	V_{17}	–	5.4	–	V
Top sync level		V_{17}	2.3	2.5	2.7	V
Video output signal amplitude	note 7	V_{17}	2.3	2.65	3.0	V
White-spot threshold level			–	5.7	–	V
White-spot insertion level			–	3.8	–	V
Video output impedance		–	–	25	–	Ω
Internal bias current of output transistor (NPN emitter follower)		$I_{17(int)}$	1.4	1.8	–	mA

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parameter	conditions	symbol	min.	typ.	max.	unit
Maximum source current		I_{17}	10	–	–	mA
Bandwidth of demodulated output signal		B	5	7	–	MHz
Differential gain	note 8	G_{17}	–	4	8	%
Differential phase	note 8	φ	–	2	5	deg.
Video non-linearity	note 9	NL	–	2	5	%
Intermodulation	note 10					
f = 1.1 MHz (blue)			50	60	–	dB
f = 1.1 MHz (yellow)			50	60	–	dB
f = 3.3 MHz (blue)			55	65	–	dB
f = 3.3 MHz (yellow)			55	65	–	dB
Signal-to-noise ratio	note 11					
V_i = 10 mV		S/N	50	57	–	dB
end of gain control range		S/N	50	62	–	dB
Residual carrier signal		V_{17}	–	2	10	mV
Residual 2nd harmonic of carrier signal		V_{17}	–	2	10	mV
Tuner AGC						
Minimum starting point tuner take-over (RMS value)		$V_{8\text{-}9(rms)}$	–	–	0.2	mV
Maximum starting point tuner take-over (RMS value)		$V_{8\text{-}9(rms)}$	100	150	–	mV
Maximum tuner AGC output swing	V_5 = 3 V	$I_{5(max)}$	4	–	–	mA
Output saturation voltage	I_5 = 2 mA	$V_{5(sat)}$	–	–	300	mV
Leakage current (pin 5)		I_L	–	–	1	μA
Input signal variation complete tuner control		ΔV_i	0.5	2	4	dB
Minimum voltage tuner take-over		V_1	–	–	1	V
Voltage to switch on the X-ray protection	horizontal output high resistance	V_1	–	–	0.8	V
AFC circuit						
AFC sample-and-hold/switch						
AFC switch-off current		I_{19}	0.1	–	–	mA
Output current	V_{19} = 0 V	I_{19}	–	0.1	0.3	mA
Leakage current at pin 19		I_{LO}	–	–	2	μA

DEVELOPMENT DATA

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CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
AFC circuit (continued)						
AFC output						
AFC output voltage swing	notes 18, 19	V_{18}	10.5	–	11.5	V
Available output current		I_{18}	0.2	–	–	mA
Control steepness			–	100	–	mV /kHz
AFC output voltage with AFC off		V_{18}	5.5	6	6.5	V
AFC output resistance		R_{18}	–	40	–	kΩ
Measured with an input signal amplitude = 150 μV (RMS value)						
Output voltage swing	note 27	V_{18}	–	11	–	V
Control steepness	note 27		–	80	–	mV /kHz
Output voltage shift with respect to V_i = 10 mV (RMS value)	note 27		–	−2	–	V
Sound circuit	note 12					
Input limiting voltage	$V_{o(max)}$ = −3 dB	V_{15}	–	400	800	μV
Input resistance		R_{15}	–	2.6	–	kΩ
Input capacitance		C_{15}	–	6	–	pF
AM suppression	note 13	AMS	53	58	–	dB
AF output signal (RMS value)	note 14	$V_{12(rms)}$	400	600	800	mV
AF output signal when pin 11 is used as a starting pin or connected to V_P (RMS value)	Δf = 50 kHz	$V_{12(rms)}$	500	900	1500	mV
AF output impedance		Z_{12}	–	25	100	Ω
Total harmonic distortion	note 15	THD	–	0.5	2	%
Ripple rejection	volume control 20 dB; f_k = 100 Hz	RR	–	35	–	dB
Output voltage when muted		V_{12}	–	2.5	–	V
Output level shift due to muting	volume control −20 dB	V_{12}	–	–	0.5	V
Signal-to-noise ratio	note 16	S/N	–	47	–	dB
Voltage with pin 11 disconnected		V_{11}	–	6.0	–	V
Current with pin 11 short circuited to ground		I_{11}	–	1	–	mA

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parameter	conditions	symbol	min.	typ.	max.	unit
Temperature dependance of the output signal amplitude	T_{amb} = 20 °C to 65 °C; −30 dB volume control and voltage of pin 11 fixed; note 27	V_{12}	–	2.5	–	dB
Volume control	note 17; see Fig.8					
External control resistor	note 17	R_{11}	–	4.7	–	kΩ
Suppression output signal during mute condition		OSS	60	66	–	dB
Horizontal synchronization circuit	see Fig.9					
Sync separator						
Required sync pulse amplitude	note 20	V_{25}	200	750	–	mV
Input current pin 25	$V_{25} > 5$ V	I_{25}	–	8	–	μA
	$V_{25} = 0$ V	I_{25}	–	−10	–	mA
First control loop						
Holding range PLL		$\pm\Delta f$	–	1500	2000	Hz
Catching range PLL		$\pm\Delta f$	600	1500	–	Hz
Control sensitivity to oscillator	note 21			see Fig.10		
IF input signal at which the time constant is switched (RMS value)	strong to weak	V_{8-9}	–	2.2	–	mV
Second control loop						
Control sensitivity	note 22	$\Delta t_d/\Delta t_o$	–	100	–	–
Control range		t_d	–	25	–	μs
Controlled edge				positive		
Phase adjustment (via second control loop)						
Control sensitivity			–	25	–	μA/μs
Maximum allowed phase shift		α	–	±2	–	μs
Horizontal oscillator (pin 23)						
Free running frequency	R = 34.3 kΩ; C = 2.7 nF	f_{fr}	–	15625	–	Hz
Spread with fixed external components		Δf	–	–	4	%
Frequency variation	ΔV_P = 9.5 to 13.2 V	Δf_{fr}	–	–	2	%
Frequency variation with temperature	note 27	TC	–	−1.6	–	Hz/°C

DEVELOPMENT DATA

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CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Horizontal oscillator (pin 23) (continued)						
Maximum frequency deviation at start of horizontal output		Δf_{fr}	–	–	10	%
Frequency variation when only noise is received	note 27	Δf_{fr}	–	–	500	Hz
Horizontal output						
Output limiting voltage		V_{26}	–	–	16.5	V
Output voltage LOW	I_{sink} = 10 mA	V_{26}	–	0.2	0.5	V
Maximum sink current		I_{26}	10	–	–	mA
Duty cycle output signal			–	46	–	%
Rise time of output pulse		t_r	–	260	–	ns
Fall time of output pulse		t_f	–	100	–	ns
Flyback input and sandcastle output	note 23					
Input current required during flyback pulse		I_{27}	0.1	–	2	mA
Output voltage:						
during burst key pulse		V_{27}	8	–	–	V
during horizontal blanking		V_{27}	4	4.4	5	V
during vertical blanking		V_{27}	2.1	2.5	2.9	V
Pulse width:						
burst key pulse	60 Hz	t_W	2.9	3.3	3.7	µs
burst key pulse	50 Hz	t_W	3.2	3.6	4.0	µs
horizontal blanking pulse			flyback pulse width			
Vertical blanking pulse:						
50 Hz divider in search window			–	21	–	lines
60 Hz divider in search window			–	17	–	lines
50 Hz divider in narrow window			–	25	–	lines
60 Hz divider in narrow window			–	21	–	lines
Delay between start of sync pulse at the video output and the burst key pulse						
trailing edge	60 Hz		–	–	9.3	µs
rising edge			4.7	5.4	6.1	µs

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parameter	conditions	symbol	min.	typ.	max.	unit
Coincidence detector						
Voltage for:						
synchronized condition		V_{22}	–	9.8	–	V
no signal condition		V_{22}	–	1.5	–	V
Switching level to switch the phase detector from fast to slow		V_{22}	6.2	6.7	7.2	V
Hysteresis slow to fast		V_{22}	–	0.6	–	V
Switching level to activate the mute function (transmitter identification)		V_{22}	2.5	2.8	3.1	V
Hysteresis mute function		V_{22}	–	2	–	V
Delay time of mute release after transmitter insertion					300	μs
Allowable load on pin 22					10	μA
External video mode		V_{22}	–	–	0.7	V
Current at pin 22	V_{22} = 0 V	I_{22}	–	–	0.8	mA
Vertical circuit	note 25					
Vertical ramp generator						
Input current during scan		I_2	–	–	2	μA
Discharge current during retrace		I_2	–	0.8	–	mA
Sawtooth amplitude (peak-to-peak value)		$V_{2(p-p)}$	–	1.9	–	V
Interlace timing of the internal pulses			30	32	34	μs
Vertical output						
Available output current	V_3 = 4 V	I_3	–	–	3	mA
Maximum output voltage	I_3 = 0.1 mA	V_3	4.4	5	–	V
Vertical feedback input						
Input voltage						
DC component		V_4	2.9	3.3	3.7	V
AC component (peak-to-peak value)		$V_{4(p-p)}$	–	1	–	V
Input current		I_4	–	–	12	μA
Internal precorrection to sawtooth		Δt_p	–	3	–	%
Deviation amplitude	50/60 Hz		–	–	2	%
Temperature dependence of the amplitude	T_{amb} = 20 °C to 65 °C		–	–	2	%

DEVELOPMENT DATA

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CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Vertical circuit (continued)						
Vertical guard	note 26					
Active switching level at a deviation with respect to the DC feedback level:	V_{27} = 2.5 V					
guard level LOW		ΔV_4	–	2.1	–	V
guard level HIGH		ΔV_4	–	2	–	V

Notes to the characteristics

1. Pin 11 has a double function. When during switch-on a current of 9.0 mA is supplied to this pin, it is used to start the horizontal oscillator.
   The main supply can then be obtained from the horizontal deflection stage. When no current is supplied to this pin it can be used as a volume control.
2. On set AGC.
3. The input impedance has been chosen such that a SAW-filter can be applied.
4. Measured with 0 dB = 450 μV.
5. Measured at 10 mV (RMS value) top sync input signal.
6. So-called projected zero point; i.e. with switched demodulator.
7. White 10% of the top sync amplitude.
8. Measured according to the test line illustrated by Fig.2:
   - The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level.
   - The differential phase is defined as the difference in degrees between the largest and smallest phase angle. The differential gain and phase are measured with a DSB signal.
9. This figure is valid for the complete video signal amplitude (peak white-to-black); see Fig.3. The non-linearity is expressed as a percentage of the maximum deviation of a luminance step from the mean step, with respect to the mean step.
10. The test set-up and input conditions are illustrated by Fig.4. The figures are measured at an input signal of 10 mV (RMS value).
11. Measured with a source impedance of 75 Ω.

$$\text{Signal-to-noise ratio} = 20 \log \frac{V_{\text{out black-to-white}}}{V_{n(\text{rms})} \text{ at } B = 5 \text{ MHz}}$$

12. The sound circuit is measured (unless otherwise specified) with an input signal of V_{15} of 50 mV (RMS value), a carrier frequency of 5.5 MHz at a Δf of 27.5 kHz and an AF frequency of 1 kHz. The QL of the demodulator tuned circuit is 16 and the volume control is connected to the supply. The reference circuit must be tuned in such a way that the output is symmetrical clipping at maximum volume.
13. The test set-up is illustrated by Fig.6. The AM rejection curve (typical) is illustrated by Fig.7.
14. The output signal is measured at aΔf = 7.5 kHz and maximum volume control.
15. The demodulator tuned circuit must be tuned at minimum distortion.
16. Weighted noise, measured according to; CCIR 468.
17. See also note 1. The volume can be controlled by using a potentiometer connected to ground (value 10 kΩ) or by means of a variable direct voltage. In the latter case the relatively low input impedance (pin 11) must be taken into account.

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18. The AFC control voltage is obtained by multiplying the IF output signal (which is also used to drive the synchronous demodulator) with a reference carrier. This reference carrier is obtained from the demodulator tuned circuit via a 90 degree phase shift network. The IF output signal has an asymmetrical frequency spectrum with respect to the carrier frequency. To avoid problems due to this asymmetrical signal the AFC circuit is followed by a sample-and-hold circuit which samples during the sync level. As a result the AFC output voltage contains no video information. The specified control steepness is without using an external load resistor. The control steepness decreases when the AFC output is loaded with two resistors between the voltage supply and ground.
19. At very weak input signals the drive signal for the AFC circuit will have a high noise content. This noise input has an asymmetrical frequency spectrum which will cause an offset of the AFC output voltage. To avoid problems due to this effect a notch filter can be built in to the demodulator tuned circuit. The characteristics given for weak input signals are measured without a notch circuit, with a SAW filter connected in front of the IC (input signal such that the input signal of the IC is 150 μV (RMS value).
20. The minimum value is obtained with a 1.8 kΩ series resistor connected between pin 17 and pin 25. The slicing level can be varied by changing the value of this resistor (a higher resistance results in a larger value of the minimum sync pulse amplitude). The slicing level is independent of the video information.
21. Frequency control is obtained by supplying a correction current to the oscillator RC-network. This is achieved via a resistor connected between the phase 1 detector output and the oscillator network. The oscillator can be adjusted to the correct frequency by:

    - short-circuit the sync separator bias network (pin 25) to the voltage supply.

    To avoid the necessity of a VCR switch, the time constant of the phase detector at strong input signals is sufficiently short to obtain a stable picture during VCR playback. During the vertical retrace period the time constant is even shorter so that VCR head errors are compensated for at the beginning of the scan. During weak signal conditions (information derived from the AGC circuit) the time constant is increased to obtain a good noise immunity.
22. This figure is valid for an external load impedance of 82 kΩ connected between pin 28 and the shift adjustment potentiometer.
23. The horizontal flyback input and the sandcastle output have been combined on pin 27. The flyback pulse is clamped to a level of 4.5 V. The minimum current to drive the second control loop is 0.1 mA.
24. The functions in-sync/out-of-sync and transmitter identification have been combined on pin 22. The capacitor is charged during the sync pulse and discharged during the time difference between gating and sync pulse.
25. The vertical scan is synchronized by means of a divider system, therefore no adjustment is required for the ramp generator. The divider detects whether the incoming signal has a vertical frequency of 50 or 60 Hz and corrects the vertical amplitude.
26. To avoid screenburn due to a collapse of the vertical deflection, a continuous blanking level is inserted into the sandcastle pulse when the feedback voltage of the vertical deflection is not within the specified limits.
27. These figures are based on sampled tests.

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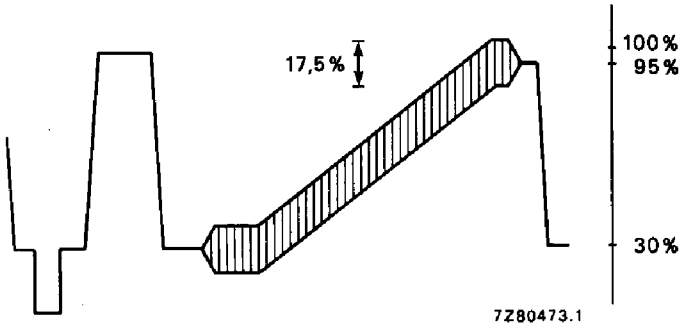

Fig.2 Video output signal.

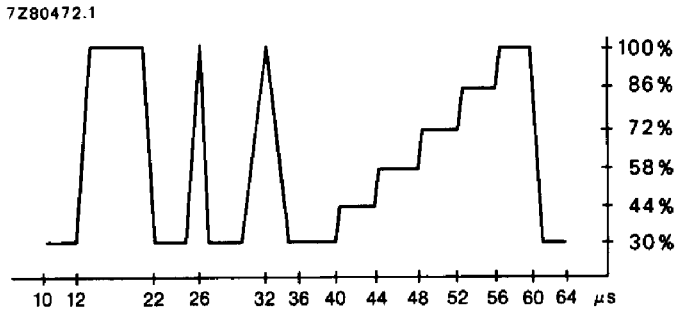

Fig.3 European Broadcasting Union (EBU) test signal waveform (line 330).

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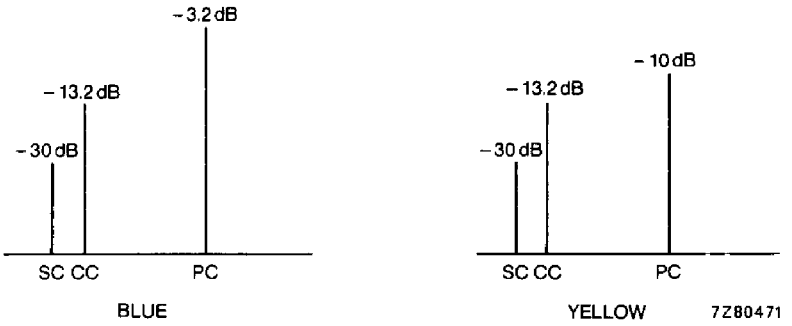
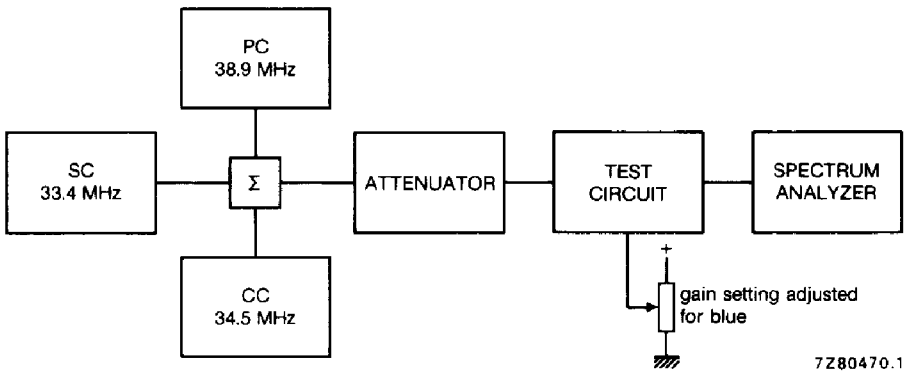


Where

SC = sound carrier
CC = chrominance carrier
PC = picture carrier
All values are with respect to the top sync level



Where

Value at 1.1 MHz: $20 \log \frac{V_o \text{ at } 4.4 \text{ MHz}}{V_o \text{ at } 1.1 \text{ MHz}} + 3.6 \text{ dB}$

Value at 3.3 MHz: $20 \log \frac{V_o \text{ at } 4.4 \text{ MHz}}{V_o \text{ at } 3.3 \text{ MHz}}$

Fig.4 Test set-up intermodulation.

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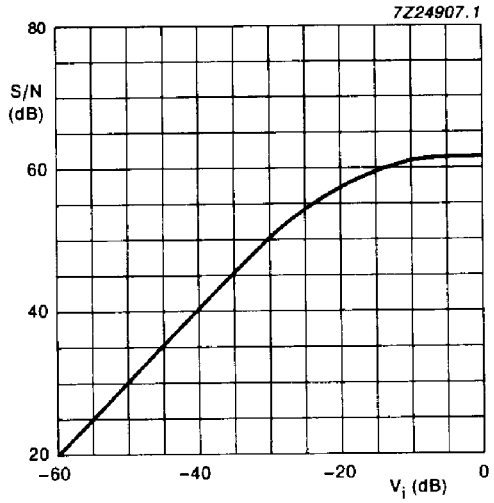

Fig.5 Signal-to-noise ratio as a function of input voltage; 0 dB = 100 mV.

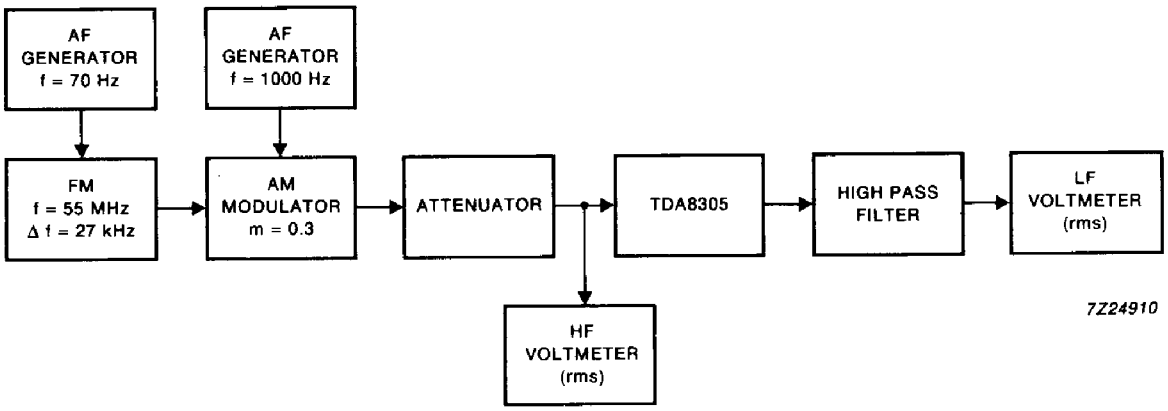

Fig.6 Test set-up AM suppression.

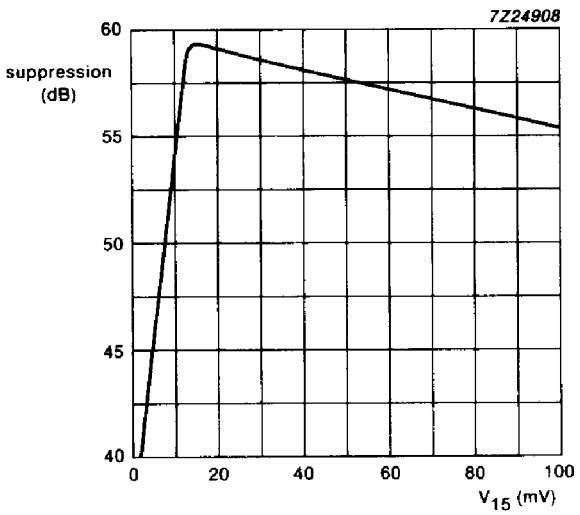

Fig.7 AM suppression.

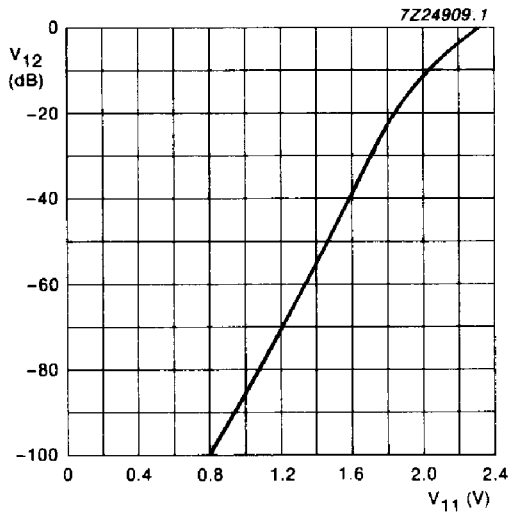

Fig.8 Volume control characteristics.

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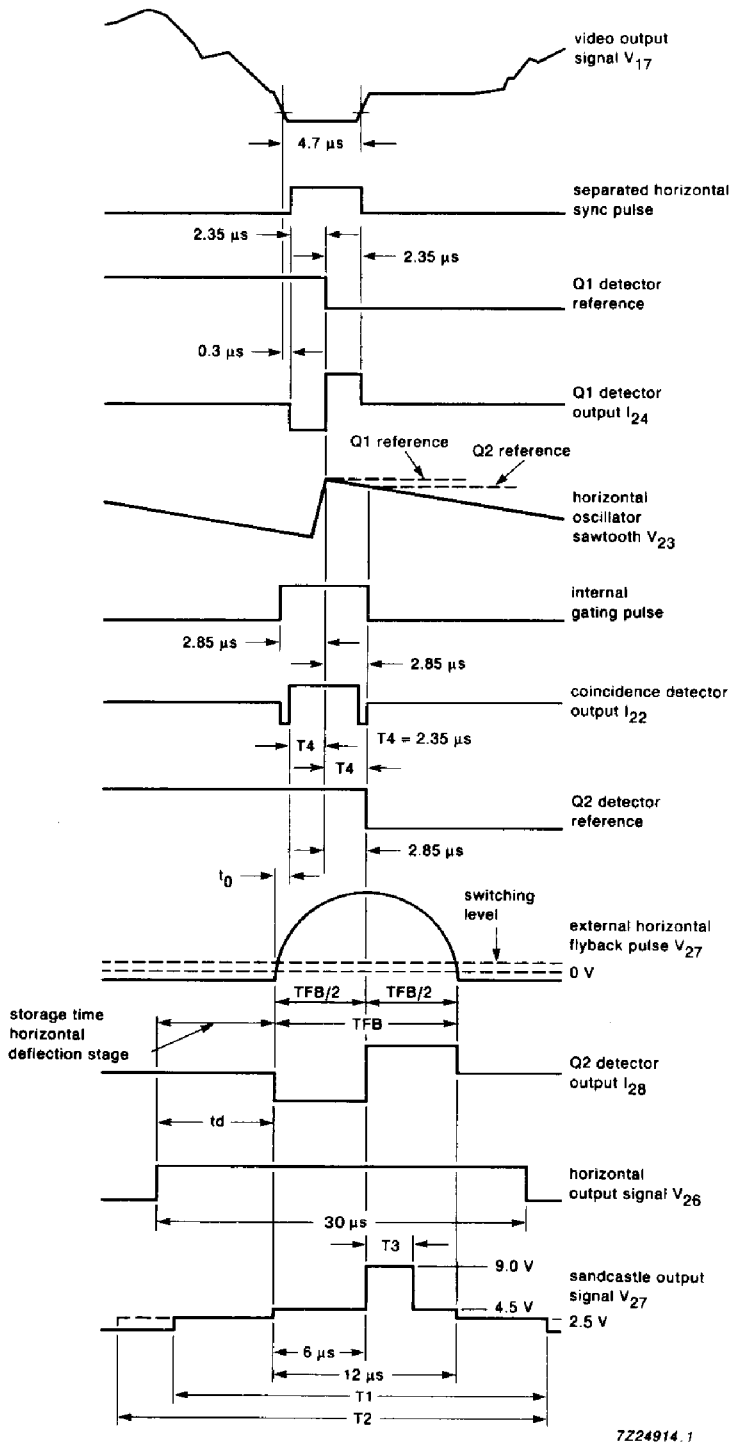
DEVELOPMENT DATA



	50 Hz	60 Hz
T1 – search window –	42P	34P
T2 – narrow window –	50P	42P
T3	3.6 µs	3.3 µs

$$P = \frac{1}{2F_H}$$

Fig.9 Timing diagram.

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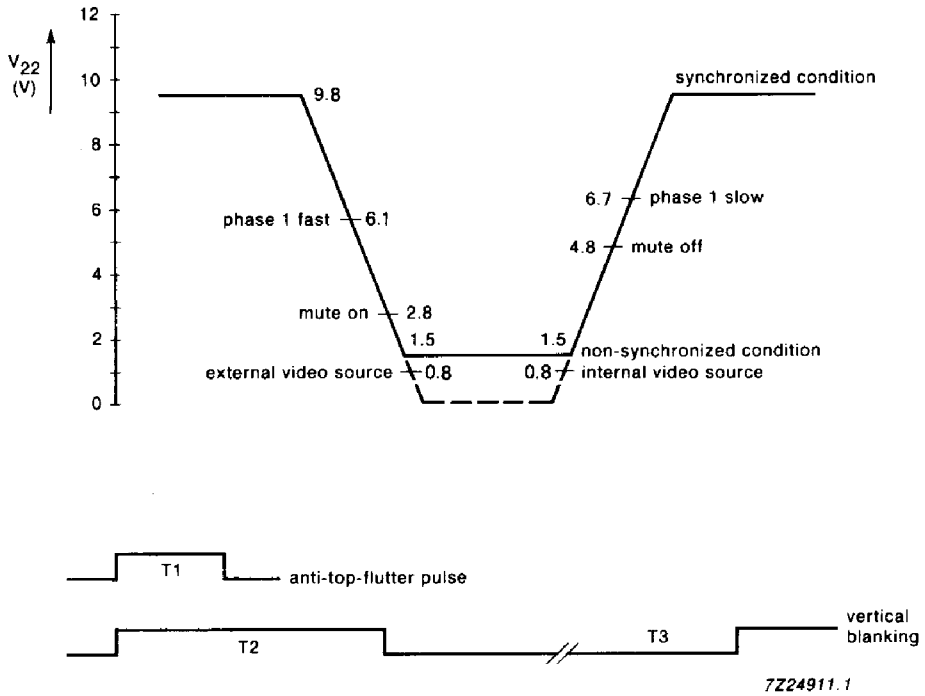

condition	control sensitivity horizontal oscillator		vertical sync separation pulse after
	T2 – T1	T3 = scan	
$V_{22} > 6.7$ V strong signal weak signal	11.3 kHz/μs 1.3 kHz/μs	7.6 kHz/μs 1.3 kHz/μs	16 μs 16 μs
$1 < V_{22} < 5.7$ V strong signal weak signal	11.3 kHz/μs 11.3 kHz/μs	7.6 kHz/μs 7.6 kHz/μs	16 μs 16 μs
$V_{22} < 0.7$ V	11.3 kHz/μs	7.6 kHz/μs	16 μs

Fig.10 Switching levels coincidence detector.

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APPLICATION INFORMATION

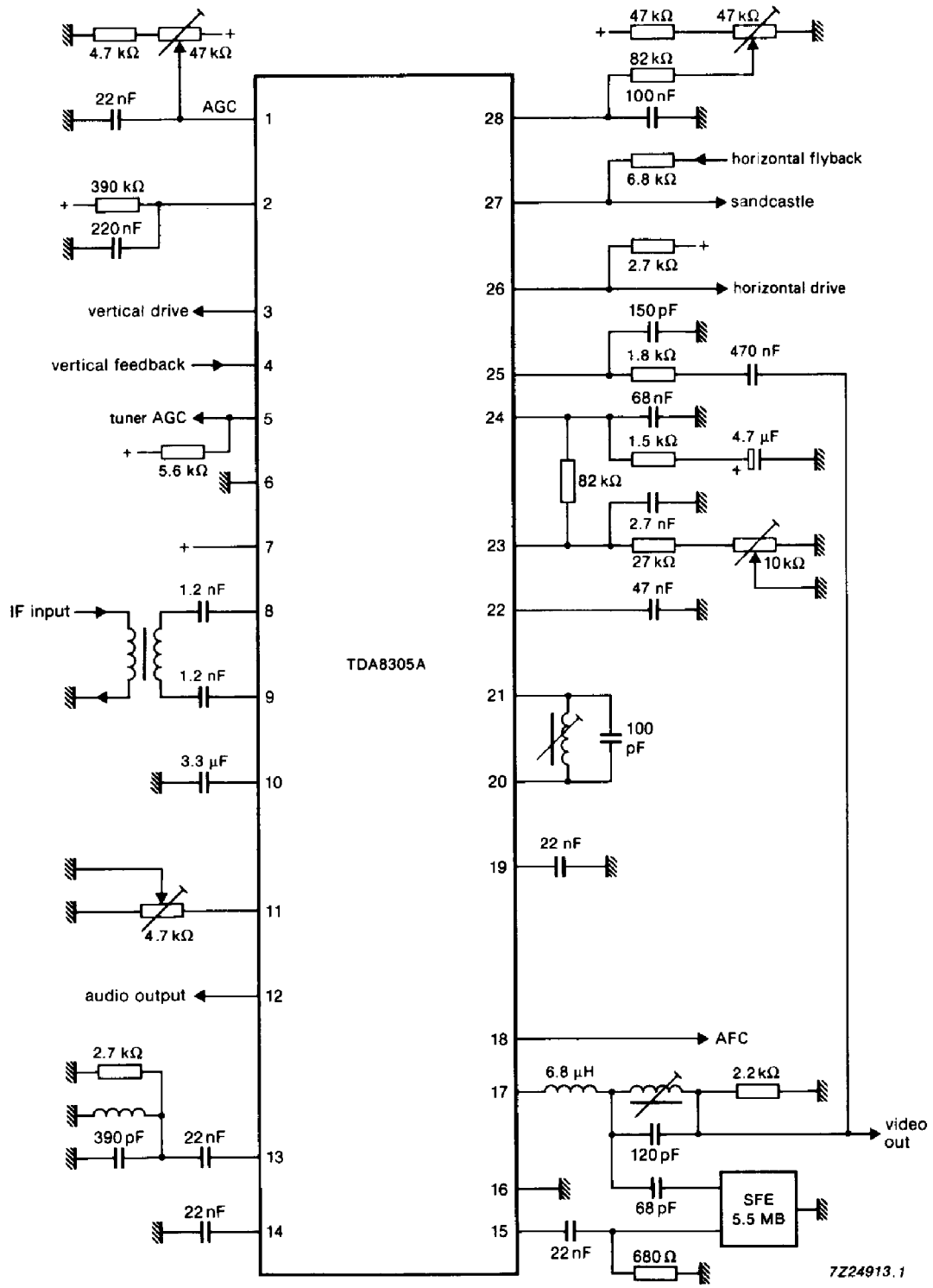

Fig.11 Application diagram.

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